MF1492-01

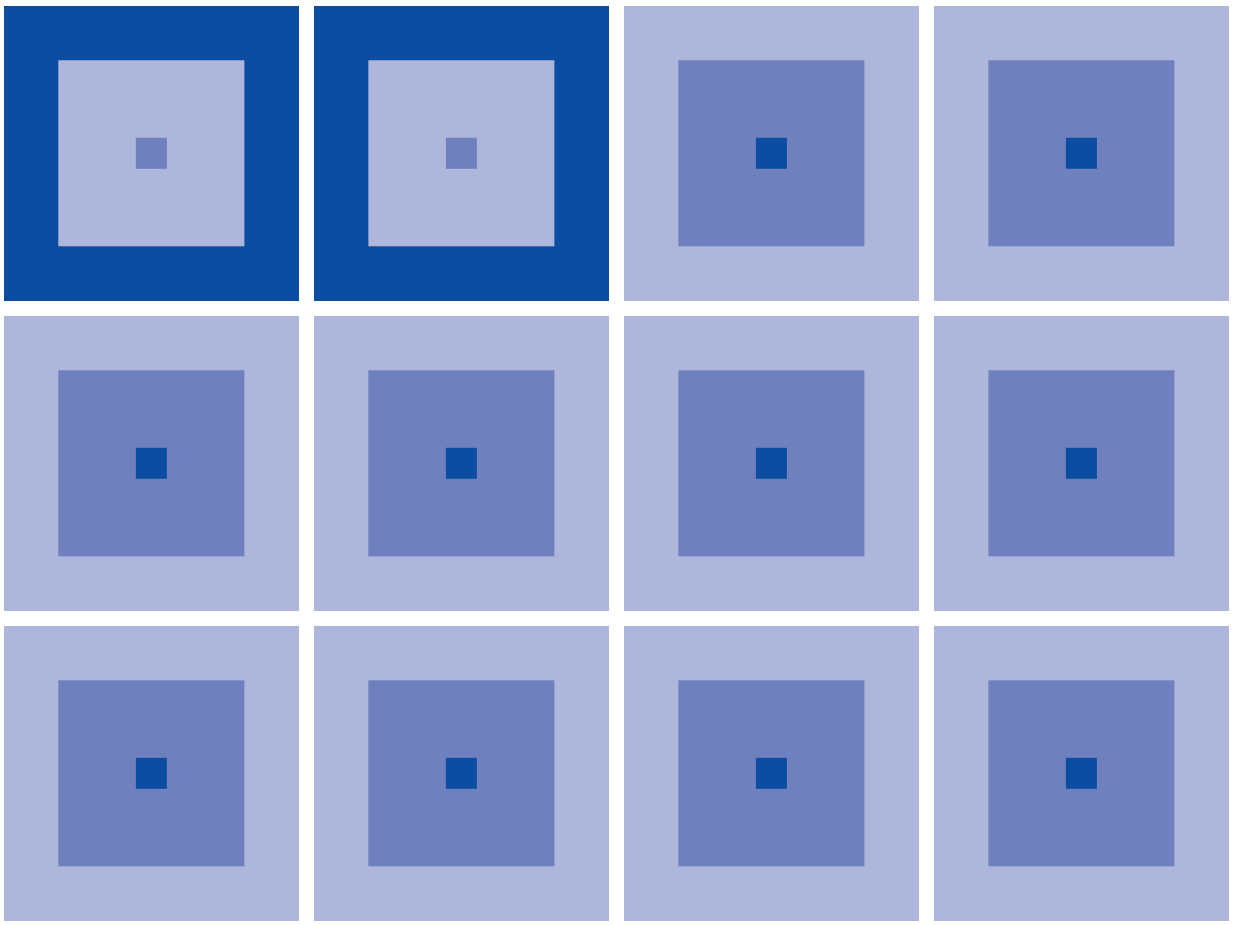
EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

S1C63406

Technical Manual

S1C63406 Technical Hardware



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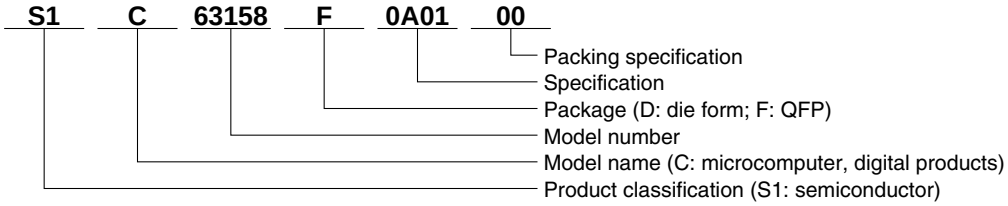
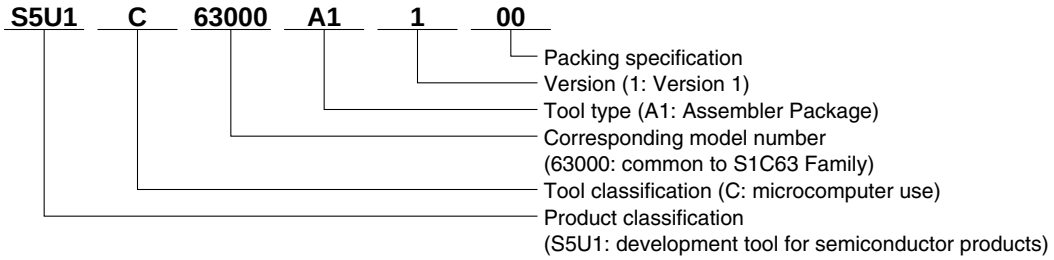
New configuration of product number

Starting April 1, 2001, the product number has been changed as listed below. Please use the new product number when you place an order. For further information, please contact Epson sales representative.

Devices



Development tools



CONTENTS

CHAPTER 1 OUTLINE

The S1C63406 is a microcomputer which has a high-performance 4-bit CPU S1C63000 as the core CPU, code ROM (6,144 words × 13 bits), RAM (1,024 words × 4 bits), data ROM (3,072 words × 4 bits), serial interface, watchdog timer, programmable timer, time base counters (2 systems) and a dot-matrix LCD driver that can drive a maximum 60 segments × 9 commons. Furthermore, the built-in reset circuit (with power-on reset function) can detect the power supply voltage to reset the S1C63406 when the power is turned on or an instantaneous power interruption occurs. The S1C63406 features high speed operation with a low operating voltage (1.3 V to 3.6 V) and low current consumption, this makes it suitable for applications working with batteries, such as portable MD and CD player systems.

1.1 Features

OSC1 oscillation circuit	32.768 kHz (Typ.) crystal or 60 kHz (Typ.) CR oscillation circuit (*1)
OSC3 oscillation circuit	4 MHz (Typ.) crystal, 3.58 MHz (Typ.) ceramic or 2 MHz (Typ.) CR oscillation circuit (*1)
Instruction set	Basic instruction: 47 types (411 instructions with all) Addressing mode: 8 types
Instruction execution time	During operation at 32.768 kHz: 61 µsec 122 µsec 183 µsec During operation at 60 kHz: 33 µsec 67 µsec 100 µsec During operation at 2 MHz: 1 µsec 2 µsec 3 µsec During operation at 3.58 MHz: 0.56 µsec 1.12 µsec 1.68 µsec During operation at 4 MHz: 0.5 µsec 1 µsec 1.5 µsec
ROM capacity	Code ROM: 6,144 words × 13 bits Data ROM: 3,072 words × 4 bits
RAM capacity	Data memory: 1,024 words × 4 bits Display memory: 540 bits (120 words × 4 bits + 60 × 1 bit)
Input port	4 bits (Pull-up resistors may be supplemented *1)
Output port	4 bits (It is possible to switch the 2 bits to special outputs *2)
I/O port	4 bits with Schmitt trigger input (Built-in pull-up resistors may be disabled *2 It is possible to switch to serial I/F inputs/outputs *2)
Serial interface	1 port (8-bit clock synchronous or asynchronous system *2)
LCD driver	60 segments × 8 or 9 commons (*2)
Time base counter	2 systems (Clock timer, stopwatch timer)
Programmable timer	8 bits × 2 ch. or 16 bits × 1 ch., with event counter function
Watchdog timer	Built-in
Supply voltage detection (SVD) circuit	16 values, programmable (1.30 V to 2.80 V)
Reset circuit	Built-in (1.8 V, 1.6 V or 1.4 V *1), with power-on reset function
External interrupt	Input port interrupt: 4 systems
Internal interrupt	Clock timer interrupt: 4 systems Stopwatch timer interrupt: 2 systems Programmable timer interrupt: 2 systems Serial interface interrupt: 3 systems
Power supply voltage	1.3 V to 3.6 V (Min. 1.4 V when 700 kHz (Max.) OSC3 CR oscillator is used) (Min. 1.6 V when 2.2 MHz (Max.) OSC3 CR oscillator is used) (Min. 1.8 V when 4.2 MHz (Max.) OSC3 oscillator is used)
Operating temperature range	-40°C to 85°C
Current consumption	Low-power operation (*3): During SLEEP 1.2 µA (Typ.) During HALT (32 kHz cryctal oscillation) 3.6 V (LCD OFF) 1.3 µA (Typ.) 3.6 V (LCD ON, V_{C1} standard) 3.0 µA (Typ.) 3.6 V (LCD ON, V_{C2} standard) 2.5 µA (Typ.)

During operation (32 kHz cryctal oscillation)
3.6 V (LCD OFF) 3.0 µA (Typ.)
During HALT (60 kHz CR oscillation)
3.6 V (LCD OFF) 3.5 µA (Typ.)
3.6 V (LCD ON, V_{C1} standard) 6.2 µA (Typ.)
3.6 V (LCD ON, V_{C2} standard) 4.6 µA (Typ.)
During operation (60 kHz CR oscillation)
3.6 V (LCD OFF) 7.0 µA (Typ.)
High-speed operation:
During operation (500 kHz CR oscillation)
3.6 V (LCD OFF) 130 µA (Typ.)
During operation (1 MHz CR oscillation)
3.6 V (LCD OFF) 260 µA (Typ.)
During operation (2 MHz CR oscillation)
3.6 V (LCD OFF) 520 µA (Typ.)
During operation (3.58 MHz ceramic oscillation)
3.6 V (LCD OFF) 670 µA (Typ.)
During operation (4 MHz crystal oscillation)
3.6 V (LCD OFF) 780 µA (Typ.)

Package ..... TQFP15-128pin (plastic) or chip

*1: Can be selected with mask option *2: Can be selected with software
*3: Current consumption when the reset circuit option is not selected (Reset circuit current will be added when the reset circuit option is selected.)

1.2 Block Diagram

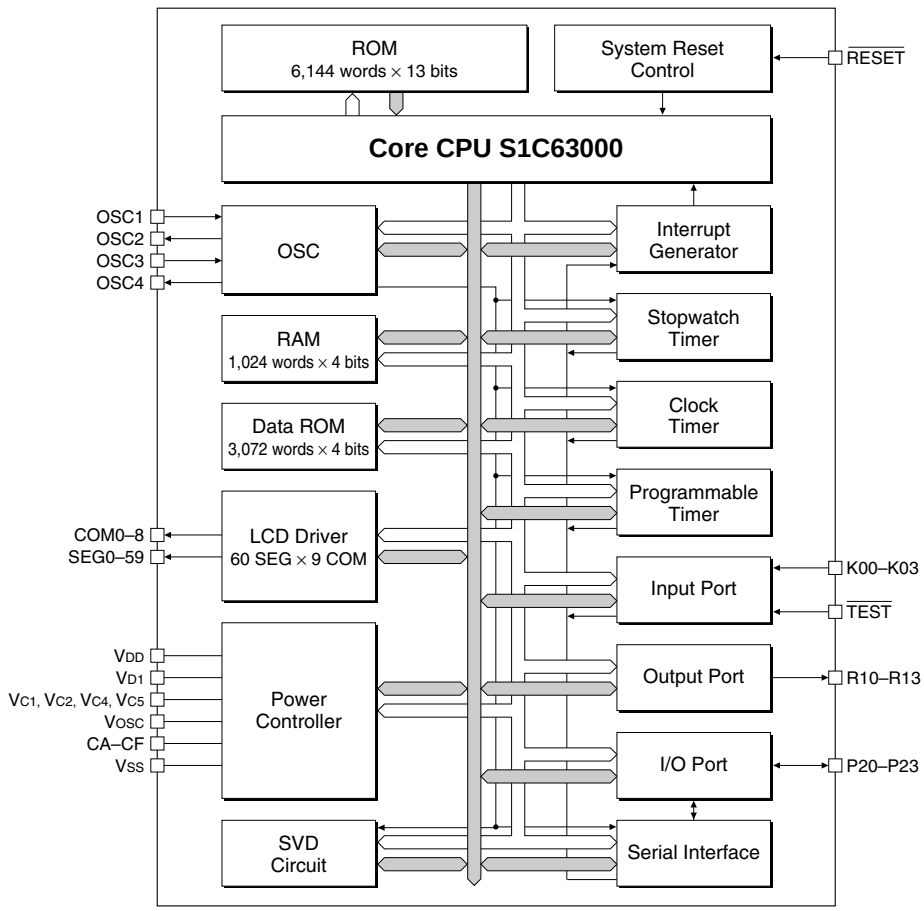
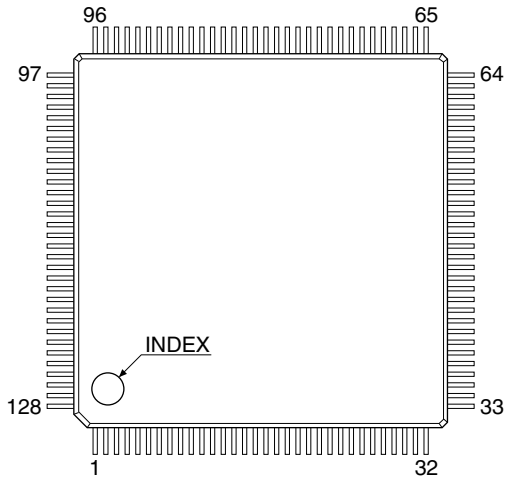


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

TQFP15-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	N.C.	33	CF	65	N.C.	97	SEG15
2	SEG41	34	V_{C5}	66	N.C.	98	SEG16
3	SEG42	35	V_{C4}	67	N.C.	99	SEG17
4	SEG43	36	V_{C2}	68	N.C.	100	SEG18
5	SEG44	37	V_{C1}	69	COM0	101	SEG19
6	SEG45	38	K00	70	COM1	102	SEG20
7	SEG46	39	K01	71	COM2	103	SEG21
8	SEG47	40	K02	72	COM3	104	SEG22
9	SEG48	41	N.C.	73	COM4	105	SEG23
10	SEG49	42	N.C.	74	N.C.	106	N.C.
11	N.C.	43	K03	75	N.C.	107	N.C.
12	N.C.	44	R10	76	N.C.	108	N.C.
13	N.C.	45	R11	77	COM5	109	N.C.
14	SEG50	46	R12	78	COM6	110	SEG24
15	SEG51	47	R13	79	COM7	111	SEG25
16	SEG52	48	P20	80	SEG0	112	SEG26
17	SEG53	49	P21	81	SEG1	113	SEG27
18	SEG54	50	P22	82	SEG2	114	SEG28
19	N.C.	51	P23	83	SEG3	115	SEG29
20	N.C.	52	N.C.	84	N.C.	116	SEG30
21	N.C.	53	N.C.	85	N.C.	117	SEG31
22	SEG55	54	N.C.	86	SEG4	118	SEG32
23	SEG56	55	V_{DD}	87	SEG5	119	N.C.
24	SEG57	56	V_{D1}	88	SEG6	120	N.C.
25	SEG58	57	OSC4	89	SEG7	121	SEG33
26	SEG59	58	OSC3	90	SEG8	122	SEG34
27	COM8	59	V_{OSC}	91	SEG9	123	SEG35
28	CA	60	OSC2	92	SEG10	124	SEG36
29	CB	61	OSC1	93	SEG11	125	SEG37
30	CC	62	V_{SS}	94	SEG12	126	SEG38
31	CD	63	$\overline{\text{RESET}}$	95	SEG13	127	SEG39
32	CE	64	$\overline{\text{TEST}}$	96	SEG14	128	SEG40

N.C. : No Connection

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	In/Out	Function
V_{DD}	55	–	Power (+) supply pin
V_{SS}	62	–	Power (–) supply pin
V_{D1}	56	–	Internal logic system regulated voltage output pin
V_{OSC}	59	–	Oscillation system regulated voltage output pin
V_{C1}, V_{C2}, V_{C4}, V_{C5}	37, 36, 35, 34	–	LCD system power supply pins (1/4 bias)
CA–CF	28–33	–	LCD system boosting/reducing capacitor connecting pins
OSC1	61	I	Crystal or CR oscillation input pin (selected by mask option)
OSC2	60	O	Crystal or CR oscillation output pin (selected by mask option)
OSC3	58	I	Crystal, ceramic or CR oscillation input pin (selected by mask option)
OSC4	57	O	Crystal, ceramic or CR oscillation output pin (selected by mask option)
K00–K02	38–40	I	Input port pins
K03	43	I	Input port pin or EVIN signal input pin (selected by software)
R10, R11	44, 45	O	Output port pins
R12	46	O	Output port pin or TOUT signal output pin (selected by software)
R13	47	O	Output port pin or FOUT signal output pin (selected by software)
P20	48	I/O	I/O port pins or serial I/F data input pin (selected by software)
P21	49	I/O	I/O port pins or serial I/F data output pin (selected by software)
P22	50	I/O	I/O port pins or serial I/F clock input/output pin (selected by software)
P23	51	I/O	I/O port pins or serial I/F ready signal output pin (selected by software)
COM0–COM8	69–73, 77–79, 27	O	LCD common output pin
SEG0–SEG59	80–83, 86–105, 110–118, 121–128, 2–10, 14–18, 22–26	O	LCD segment output pin
$\overline{\text{RESET}}$	63	I	Initial reset input pin
$\overline{\text{TEST}}$	64	I	Testing input pin

1.5 Mask Option

Mask options shown below are provided for the S1C63406. Several hardware specifications are prepared in each mask option, and one of them can be selected according to the application. The function option generator winfog, that has been prepared as the development software tool of S1C63406, is used for this selection. Mask pattern of the IC is finally generated based on the data created by the winfog. Refer to the "S5U1C63000A Manual" for the winfog.

<Mask Option List>

The following is the option list for the S1C63406.
Multiple selections are available in each option item as indicated in the option list. Using "4 Peripheral Circuits and Operation" as reference, select the spcifications that meet the target system and check the appropriate box. Be sure to record the spcifications for unused functions too, according to the instructions provied.

1. OSC1 SYSTEM CLOCK

☐ 1. Crystal (32.768 kHz)
☐ 2. CR (60 kHz)

2. OSC3 SYSTEM CLOCK

☐ 1. CR
☐ 2. Ceramic (3.58 MHz)
☐ 3. Crystal (4 MHz)

3. RESET CIRCUIT

☐ 1. Use (1.8 V)
☐ 2. Use (1.6 V)
☐ 3. Use (1.4 V)
☐ 4. Not Use

4. MULTIPLE KEY ENTRY RESET COMBINATION

☐ 1. Not Use
☐ 2. Use (K00, K01, K02, K03)
☐ 3. Use (K00, K01, K02)
☐ 4. Use (K00, K01)

5. MULTIPLE KEY ENTRY RESET TIME AUTHORIZE

☐ 1. Not Use
☐ 2. Use

6. INPUT PORT PULL UP RESISTOR

- K00 ☐ 1. With Resistor ☐ 2. Gate Direct
- K01 ☐ 1. With Resistor ☐ 2. Gate Direct
- K02 ☐ 1. With Resistor ☐ 2. Gate Direct
- K03 ☐ 1. With Resistor ☐ 2. Gate Direct

7. OUTPUT PORT OUTPUT SPECIFICATION

- R10 ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R11 ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R12 ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- R13 ☐ 1. Complementary ☐ 2. Nch-OpenDrain

8. I/O PORT OUTPUT SPECIFICATION

- P20 ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P21 ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P22 ☐ 1. Complementary ☐ 2. Nch-OpenDrain
- P23 ☐ 1. Complementary ☐ 2. Nch-OpenDrain

<Outline of Mask Option>

(1) OSC1 oscillation circuit

Crystal or CR oscillation can be selected as the OSC1 oscillation circuit.
Refer to Section 4.3.2, "OSC1 oscillation circuit", for details.

(2) OSC3 oscillation circuit

Crystal, ceramic or CR oscillation can be selected as the OSC3 oscillation circuit.
Refer to Section 4.3.3, "OSC3 oscillation circuit", for details.

(3) Internal reset circuit

This mask option selects whether the internal reset circuit is used or not. Select a minimum supply voltage according to the oscillation frequency when this circuit is used.
Refer to Section 2.2.3, "Internal reset circuit", for details.

(4) External reset by simultaneous LOW input to the I/O port (K00–K03)

This function resets the IC when several keys are pressed simultaneously. The mask option is used to select whether this function is used or not. Further when the function is used, a combination of the input terminals (K00–K03), which are connected to the keys to be pressed simultaneously, can be selected. Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(5) Time authorize circuit for the simultaneous LOW input reset function

When using the external reset function (shown in 4 above), using the time authorize circuit or not can be selected by mask option. The reset function works only when the input time of simultaneous LOW is more than the rule time if the time authorize circuit is being used.
Refer to Section 2.2.2, "Simultaneous low input to terminals K00–K03", for details.

(6) Input port pull-up resistor

The mask option is used to select whether the pull-up resistor is supplemented to the input ports or not. It is possible to select for each bit of the input ports.
Refer to Section 4.4.2, "Mask option", for details.

(7) Output specification of the output port

Either complementary output or N-channel open drain output can be selected as the output specification for the output ports. The selection is done in 1-bit units.
Refer to Section 4.5.2, "Mask option", for details.

(8) Output specification of the I/O ports

For the output specification when the I/O ports are in the output mode, either complementary output or N-channel open drain output can be selected in 1-bit units.
Refer to Section 4.6.2, "Mask option", for details.

CHAPTER 2 POWER SUPPLY AND INITIAL RESET

2.1 Power Supply

The S1C63406 operating power voltage is as follows:

Table 2.1.1 Operating power voltage

OSC1 clock	OSC3 clock	Operating power voltage
Max. 80 kHz (crystal or CR)	Not use	1.3 V–3.6 V
	Max. 700 kHz (CR)	1.4 V–3.6 V
	Max. 2.2 MHz (CR)	1.6 V–3.6 V
	Max. 4.2 MHz (crystal, ceramic or CR)	1.8 V–3.6 V

(When V_{C1} standard is selected)

The S1C63406 operates by applying a single power supply within the above range between V_{DD} and V_{SS}. The S1C63406 itself generates the voltage necessary for all the internal circuits by the built-in power supply circuits shown in Table 2.1.2.

Table 2.1.2 Power supply circuits

Circuit	Power supply circuit	Output voltage
OSC1 oscillation circuit	Oscillation system voltage regulator	V_{OSC}
OSC3 oscillation and internal circuits	Internal logic system voltage regulator	V_{D1}
LCD driver	LCD system voltage circuit	V_{C1}, V_{C2}, V_{C4}, V_{C5}

Note: • Do not drive external loads with the output voltage from the internal power supply circuits.

• See Chapter 7, "Electrical Characteristics", for voltage values and drive capability.

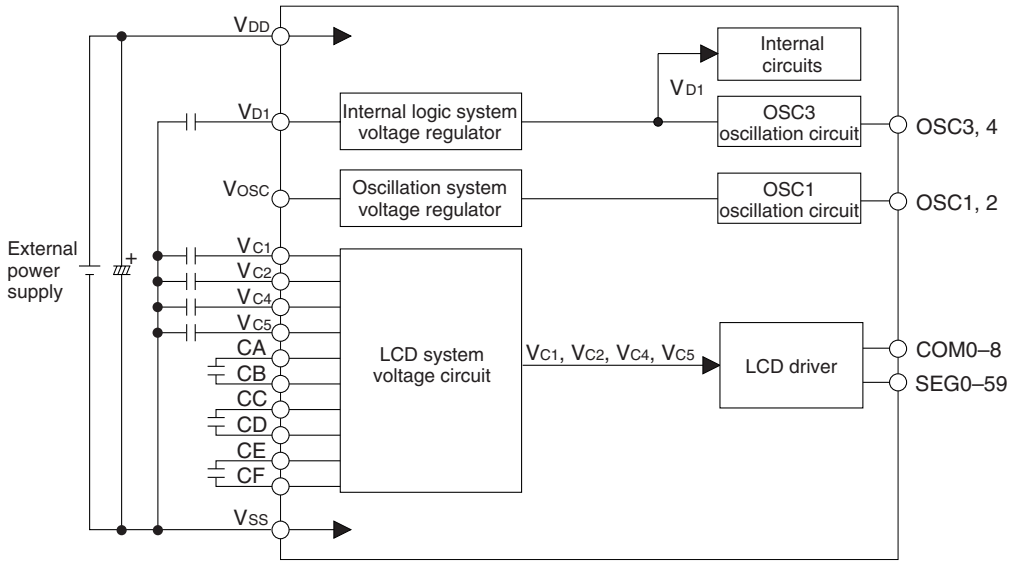


Fig. 2.1.1 Configuration of power supply

2.1.1 Voltage <V_{D1}> for internal circuits

V_{D1} is the voltage for the OSC3 oscillation circuit and the internal logic circuits, and is generated by the internal logic system voltage regulator.
The S1C63406 is designed with twin clock specification; it has two types of oscillation circuits OSC1 and OSC3 built-in. Use OSC1 clock for normal operation, and switch it to OSC3 by the software when high-speed operation is necessary. When switching the clock, the operating voltage V_{D1} must be switched by the software to stabilize the operation of the oscillation circuit and internal circuits.
The internal logic system voltage regulator can output the following four types of V_{D1} voltage. It should be set at the value according to the oscillation circuit and oscillation frequency by the software.

V_{D1} = 1.1 V for low-power operation (when OSC3 oscillation is OFF)
V_{D1} = 1.3 V for high-speed operation (when Max. 700 kHz OSC3 CR oscillation is ON)
V_{D1} = 1.5 V for high-speed operation (when Max. 2.2 MHz OSC3 CR oscillation is ON)
V_{D1} = 1.7 V for high-speed operation (when Max. 4.2 MHz OSC3 crystal/ceramic/CR oscillation is ON)

Refer to Section 4.3, "Oscillation Circuit", for the V_{D1} switching procedure.

2.1.2 Voltage <V_{OSC}> for OSC1 oscillation circuit

V_{OSC} is the voltage for the OSC1 oscillation circuit and is generated by the oscillation system voltage regulator for stabilizing the oscillation.

2.1.3 Voltage <V_{C1}, V_{C2}, V_{C4}, V_{C5}> for LCD driving

V_{C1}, V_{C2}, V_{C4} and V_{C5} are the LCD drive voltages generated by the LCD system voltage circuit. These four output voltages can only be supplied to the externally expanded LCD driver.
The LCD system voltage circuit generates V_{C1} or V_{C2} with the voltage regulator built-in, and generates three other voltages by boosting or reducing the voltage of V_{C1} or V_{C2}. Table 2.1.3.1 shows the V_{C1}, V_{C2}, V_{C4} and V_{C5} voltage values and boost / reduce status.

Table 2.1.3.1 LCD drive voltage when generated internally

LCD drive voltage	V_{DD} = 1.3–3.6 V	V_{DD} = 2.5–3.6 V
V_{C1} (0.975–1.2 V)	V_{C1} (standard)	1/2 × V_{C2}
V_{C2} (1.950–2.4 V)	2 × V_{C1}	V_{C2} (standard)
V_{C4} (2.925–3.6 V)	3 × V_{C1}	3/2 × V_{C2}
V_{C5} (3.900–4.8 V)	4 × V_{C1}	2 × V_{C2}

Note: The LCD drive voltage can be adjusted by the software (see Section 4.7.5). Values in the above table are typical values.

Either the V_{C1} or V_{C2} used for the standard is selected according to the supply voltage by the software. The V_{C2} standard improves the display quality and reduces current consumption, however, the power supply voltage V_{DD} must be 2.5 V or more.
Refer to Section 4.7, "LCD Driver", for control of the LCD drive voltage.

2.2 Initial Reset

To initialize the S1C63406 circuits, initial reset must be executed. There are two ways of doing this.

(1) External initial reset by the $\overline{\text{RESET}}$ terminal
(2) External initial reset by simultaneous low input to terminals K00–K03 (mask option)
(3) Internal initial reset by the reset circuit (mask option)

When the power is turned on, be sure to initialize using the reset function. Figure 2.2.1 shows the configuration of the initial reset circuit.

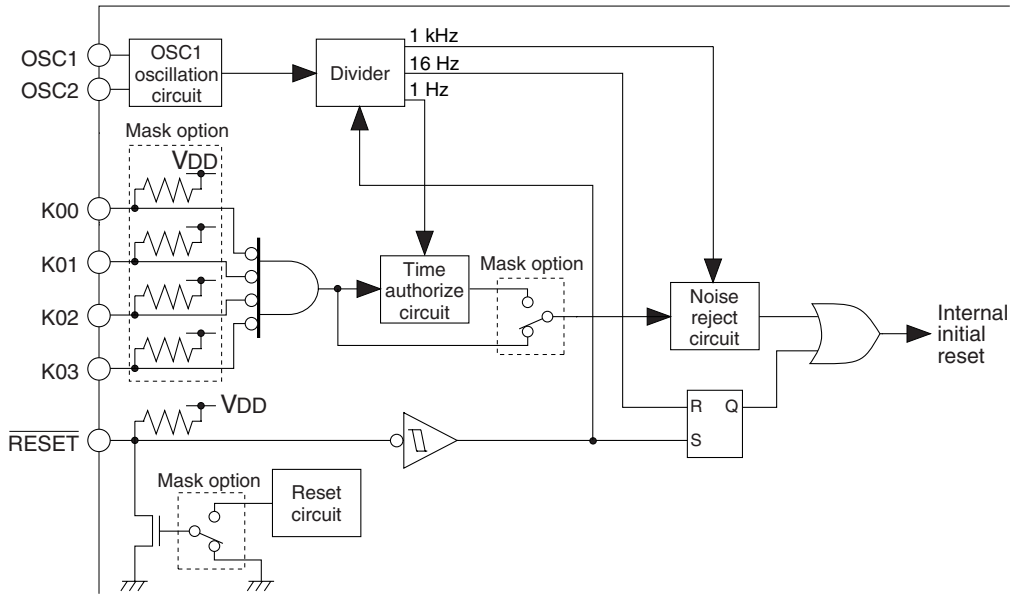


Fig. 2.2.1 Configuration of initial reset circuit

2.2.1 Reset terminal ($\overline{\text{RESET}}$)

Initial reset can be executed externally by setting the reset terminal to a low level (V_{SS}). After that the initial reset is released by setting the reset terminal to a high level (V_{DD}) and the CPU starts operation. The reset input signal is maintained by the RS latch and becomes the internal initial reset signal. The RS latch is designed to be released by a 16 Hz signal (high) that is divided by the OSC1 clock. Therefore in normal operation, a maximum of 32 msec (when f_{OSC1} = 32.768 kHz) is needed until the internal initial reset is released after the reset terminal goes to high level. Be sure to maintain a reset input of 0.1 msec or more.
However, when turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 2.2.1.1.

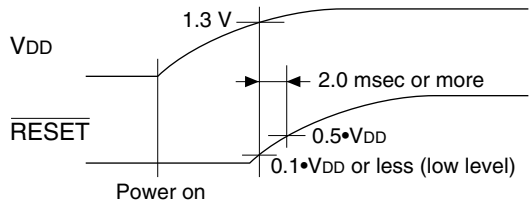


Fig. 2.2.1.1 Initial reset at power on

The reset terminal should be set to 0.1 • V_{DD} or less (low level) until the supply voltage becomes 1.3 V or more.
After that, a level of 0.5 • V_{DD} or less should be maintained more than 2.0 msec.

2.2.2 Simultaneous low input to terminals K00–K03

Another way of executing initial reset externally is to input a low signal simultaneously to the input ports (K00–K03) selected with the mask option.
Since this initial reset passes through the noise reject circuit, maintain the specified input terminals at low level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) during normal operation.
The noise reject circuit does not operate immediately after turning the power on until the oscillation circuit starts oscillating. Therefore, maintain the specified input terminals at low level for at least 1.5 msec (when the oscillation frequency f_{OSC1} is 32.768 kHz) after oscillation starts.
Table 2.2.2.1 shows the combinations of input ports (K00–K03) that can be selected with the mask option.

Table 2.2.2.1 Combinations of input ports

1	Not use
2	K00∗K01∗K02∗K03
3	K00∗K01∗K02
4	K00∗K01

When, for instance, mask option 2 (K00∗K01∗K02∗K03) is selected, initial reset is executed when the signals input to the four ports K00–K03 are all low at the same time. When 3 or 4 is selected, the initial reset is done when a key entry including a combination of selected ports is made.

Further, the time authorize circuit can be selected with the mask option. The time authorize circuit checks the input time of the simultaneous low input and performs initial reset if that time is the defined time (1 to 2 sec) or more.
If using this function, make sure that the specified port terminals do not go low at the same time during ordinary operation.

2.2.3 Internal reset circuit

The S1C63406 has a built-in reset circuit that can be configured by mask option. This reset circuit provides a system reset function when the power is instantaneously interrupted or drops as well as a power-on reset function that is useful when the power is turned on.

Table 2.2.3.1 Reset circuit options

1	Use 1.8 V
2	Use 1.6 V
3	Use 1.4 V
4	Not use

When "Use" is selected by mask option, the reset circuit outputs an initial reset signal to the CPU after turning the power on until the voltage level on the V_{DD} terminal reaches the reset-release level. It also outputs an initial reset signal when the power downs below the reset level.

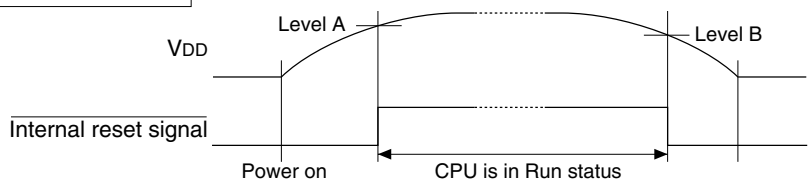


Fig. 2.2.3.1 Internal reset timing

A voltage level (1.8, 1.6 or 1.4 V) must be selected according to the minimum operating voltage (see Table 2.1.1) when this circuit is used. This selection presets the reset-release level (Level A) and reset level (Level B) to the reset circuit. There is a 40 mV (Typ.) of hysteresis between Levels A and B. See Chapter 7, "Electrical Characteristics", for the preset levels.
Note that the power-on reset circuit increases current consumption. In particular, current consumption in reset status will be greatly increased. See Chapter 7, "Electrical Characteristics", for details.

When the "Not Use" option is selected, this circuit does not output an internal initial reset signal at power on and down.

Note: When using the reset circuit, be sure to connect a capacitor to the reset terminal in order to operate it properly. In this case, to avoid a large current flow in the circuit, do not fix the reset terminal at high level.

2.2.4 Internal register at initial resetting

Initial reset initializes the CPU as shown in Table 2.2.4.1.

The registers and flags which are not initialized by initial reset should be initialized in the program if necessary.
In particular, the stack pointers SP1 and SP2 must be set as a pair because all the interrupts including NMI are masked after initial reset until both the SP1 and SP2 stack pointers are set with software.

When data is written to the EXT register, the E flag is set and the following instruction will be executed in the extended addressing mode. If an instruction which does not permit extended operation is used as the following instruction, the operation is not guaranteed. Therefore, do not write data to the EXT register for initialization only.
Refer to the "S1C63000 Core CPU Manual" for extended addressing and usable instructions.

Table 2.2.4.1 Initial values

CPU core			
Name	Symbol	Number of bits	Setting value
Data register A	A	4	Undefined
Data register B	B	4	Undefined
Extension register EXT	EXT	8	Undefined
Index register X	X	16	Undefined
Index register Y	Y	16	Undefined
Program counter	PC	16	0110H
Stack pointer SP1	SP1	8	Undefined
Stack pointer SP2	SP2	8	Undefined
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined
Interrupt flag	I	1	0
Extension flag	E	1	0
Queue register	Q	16	Undefined

Peripheral circuits		
Name	Number of bits	Setting value
RAM	4	Undefined
Display memory	4	Undefined
Other pheripheral circuits	–	*

* See Section 4.1, "Memory Map".

2.2.5 Terminal settings at initial resetting

The output port (R) terminals and I/O port (P) terminals are shared with special output terminals and input/output terminals of the serial interface. These functions are selected by the software. At initial reset, these terminals are set to the general purpose output port terminals and I/O port terminals. Set them according to the system in the initial routine. In addition, take care of the initial status of output terminals when designing a system.
Table 2.2.5.1 shows the list of the shared terminal settings.

Table 2.2.5.1 List of shared terminal settings

Terminal name	Terminal status at initial reset	Special output		Serial I/F		
		TOUT	FOUT	Master	Slave	Async.
R10	R10 (High level output)					
R11	R11 (High level output)					
R12	R12 (High level output)	TOUT				
R13	R13 (High level output)		FOUT			
P20	P20 (Input mode & Pulled-up)			SIN(I)	SIN(I)	SIN(I)
P21	P21 (Input mode & Pulled-up)			SOUT(O)	SOUT(O)	SOUT(O)
P22	P22 (Input mode & Pulled-up)			$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)	
P23	P23 (Input & Pulled-up)				$\overline{\text{SRDY}}$(O)	

For setting procedure of the functions, see explanations for each of the peripheral circuits.

2.3 Test Terminal ($\overline{\text{TEST}}$)

This is the terminal used for the factory inspection of the IC. During normal operation, connect the $\overline{\text{TEST}}$ terminal to V_{DD}.

CHAPTER 3 CPU, ROM, RAM

3.1 CPU

The S1C63406 has a 4-bit core CPU S1C63000 built-in as its CPU part.
Refer to the "S1C63000 Core CPU Manual" for the S1C63000.
The S1C63406 supports the SLEEP function.

3.2 Code ROM

The built-in code ROM is a mask ROM for loading programs, and has a capacity of 6,144 steps × 13 bits. The core CPU can linearly access the program space up to step FFFFH from step 0000H, however, the program area of the S1C63406 is step 0000H to step 17FFH. The program start address after initial reset is assigned to step 0110H. The non-maskable interrupt (NMI) vector and hardware interrupt vectors are allocated to step 0100H and steps 0102H–010AH, respectively.

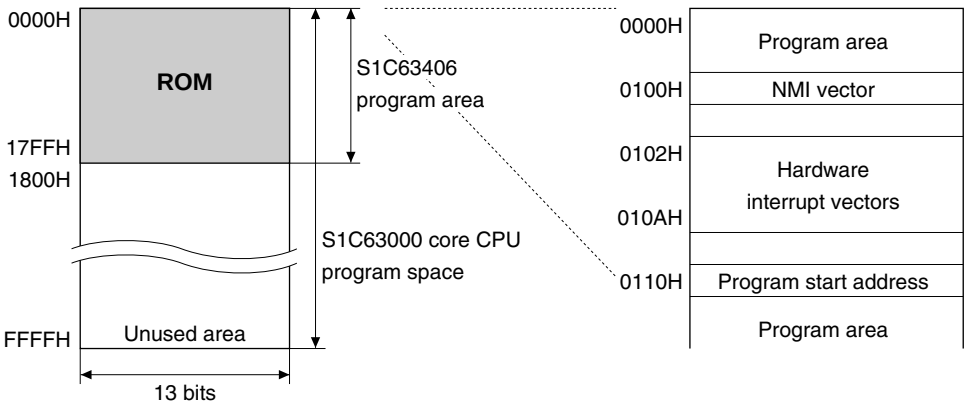


Fig. 3.2.1 Configuration of code ROM

3.3 RAM

The RAM is a data memory for storing various kinds of data, and has a capacity of 1,024 words × 4 bits. The RAM area is assigned to addresses 0000H to 03FFH on the data memory map. Addresses 0100H to 01FFH are 4-bit / 16-bit data accessible areas and in other areas it is only possible to access 4-bit data. When programming, keep the following points in mind.

(1) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(2) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit / 16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit / 16-bit accessible range in the S1C63406 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

(3) Subroutine calls use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1). Interrupts use 4 words (for PC evacuation) in the stack area for 16-bit data (SP1) and 1 word (for F register evacuation) in the stack area for 4-bit data.

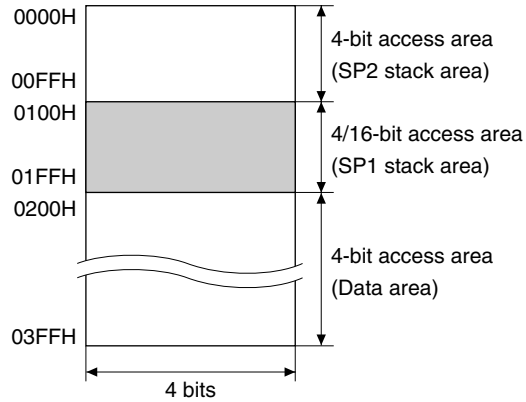


Fig. 3.3.1 Configuration of data RAM

3.4 Data ROM

The data ROM is a mask ROM for loading various static data such as a character generator, and has a capacity of 3,072 words × 4 bits. The data ROM is assigned to addresses 8000H to 8BFFH on the data memory map, and the data can be read using the same data memory access instructions as the RAM.

CHAPTER 4 PERIPHERAL CIRCUITS AND OPERATION

The peripheral circuits of S1C63406 (timer, I/O, etc.) are interfaced with the CPU in the memory mapped I/O method. Thus, all the peripheral circuits can be controlled by accessing the I/O memory on the memory map using the memory operation instructions. The following sections explain the detailed operation of each peripheral circuit.

4.1 Memory Map

The S1C63406 data memory consists of 1,024-word RAM, 3,072-word data ROM, 540-bit display memory and 50-word peripheral I/O memory. Figure 4.1.1 shows the overall memory map of the S1C63406, and Tables 4.1.1(a)–(d) the peripheral circuits' (I/O space) memory maps.

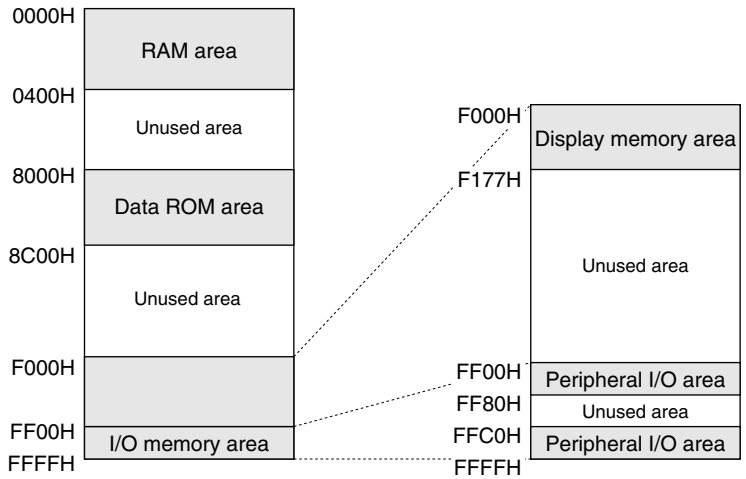


Fig. 4.1.1 Memory map

Note: Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the display memory area and the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to Section 4.7.4, "Display memory", for the display memory, and the I/O memory maps shown in Tables 4.1.1 (a)–(d) for the peripheral I/O area.

Table 4.1.1 (a) I/O memory map (FF00H–FF4AH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF00H	CLKCHG	OSCC	VDC1	VDC0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VDC1	0			CPU operating voltage switch [VDC1, 0]: 0 / 1 / 2 / 3; V_{D1} (V): 1.1 / 1.3 / 1.5 / 1.7
					VDC0	0			
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting [SVDS3–0]: 0 1.30 V, 1 1.40 V, 2 1.50 V, 3 1.60 V, 4 1.70 V, 5 1.80 V, 6 1.90 V, 7 2.00 V, 8 2.10 V, 9 2.20 V, 10 2.30 V, 11 2.40 V, 12 2.50 V, 13 2.60 V, 14 2.70 V, 15 2.80 V
					SVDS2	0			
	R/W				SVDS1	0			
					SVDS0	0			
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
FF06H	FOUTE	FOFQ2	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT enable
					FOFQ2	0			FOUT frequency selection [FOFQ2–0]: 0 Frequency $f_{OSC1}/64$, 1 $f_{OSC1}/32$, 2 $f_{OSC1}/16$, 3 $f_{OSC1}/8$, 4 $f_{OSC1}/4$, 5 f_{OSC1}, 6 $f_{OSC3}/2$, 7 f_{OSC3}
	R/W				FOFQ1	0			
					FOFQ0	0			
FF07H	HLMOD	0	WDEN	WDRST	HLMOD	0	On	Off	Heavy load protection
					0 *3	– *2			Unused
	R/W	R	R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)
FF42H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
	R				K01	– *2	High	Low	
					K00	– *2	High	Low	
FF43H	0	0	K0NR1	K0NR0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		K0NR1	0			K0 interrupt noise rejector [K0NR1, 0]: 0 NR, 1 Off, 2 0.5ms, 3 2.0ms, 4 7.8ms
					K0NR0	0			
FF46H	R13	R12	R11	R10	R13	1	High	Low	R13 output port data (FOUTE=0) / Fix at "1" when FOUT is used (FOUTE=1)
					R12	1	High	Low	R12 output port data (PTOUT=0) / Fix at "1" when TOUT is used (PTOUT=1)
	R/W				R11	1	High	Low	R11 output port data
					R10	1	High	Low	R10 output port data
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register / General-purpose register when SIF (clock sync. slave) is selected
					IOC22	0	Output	Input	P22 I/O control register / General-purpose register when SIF (clock sync.) is selected
	R/W				IOC21	0	Output	Input	P21 I/O control register (ESIF=0) / General-purpose register when SIF is selected
					IOC20	0	Output	Input	P20 I/O control register (ESIF=0) / General-purpose register when SIF is selected
FF49H	PPL23	PPL22	PPL21	PPL20	PPL23	1	On	Off	P23 pull-up control register / General-purpose register when SIF (clock sync. slave) is selected
					PPL22	1	On	Off	P22 pull-up control register / General-purpose register when SIF (clock sync. master) is selected / $\overline{SCLK}$ (I) pull-up control register when SIF (clock sync. slave) is selected
	R/W				PPL21	1	On	Off	P21 pull-up control register (ESIF=0) / General-purpose register when SIF is selected
					PPL20	1	On	Off	P20 pull-up control register (ESIF=0) / SIN pull-up control register when SIF is selected
FF4AH	P23 (XSRDY)	P22 (XSCLK)	P21 (SOUT)	P20 (SIN)	P23	– *2	High	Low	P23 I/O port data / General-purpose register when SIF (clock sync. slave) is selected
					P22	– *2	High	Low	P22 I/O port data / General-purpose register when SIF (clock sync.) is selected
	R/W				P21	– *2	High	Low	P21 I/O port data (ESIF=0) / General-purpose register when SIF is selected
					P20	– *2	High	Low	P20 I/O port data (ESIF=0) / General-purpose register when SIF is selected

Remarks

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

Table 4.1.1 (b) I/O memory map (FF54H–FF7AH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF54H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF55H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
					KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0	1	0	General-purpose register
					LDUTY0	0	1/8	1/9	LCD drive duty switch
					VCCHG	0	V_{C2}	V_{C1}	LCD regulated voltage switch
	R/W				LPWR	0	On	Off	LCD power On/Off
FF61H	EXLCDC	ALOFF	ALON	LPAGE	EXLCDC	0	1	0	General-purpose register
					ALOFF	1	All Off	Normal	LCD all OFF control
					ALON	0	All On	Normal	LCD all ON control
	R/W				LPAGE	0	1	0	General-purpose register
FF62H	LC3	LC2	LC1	LC0	LC3	– *2			LCD contrast adjustment [LC3–0] 0 – 15 Contrast Light – Dark
					LC2	– *2			
					LC1	– *2			
	R/W				LC0	– *2			
FF70H	0	SMD1	SMD0	ESIF	0 *3	– *2			Unused
					SMD1	0			Serial I/F mode selection [SMD1, 0] 0 1 Mode Clk-sync. master Clk-sync. slave [SMD1, 0] 2 3 Mode Async. 7-bit Async. 8-bit
					SMD0	0			
	R	R/W			ESIF	0	SIF	I/O	Serial I/F enable (P2x port function selection)
FF71H	EPR	PMD	SCS1	SCS0	EPR	0	Enable	Disable	Parity enable register
					PMD	0	Odd	Even	Parity mode selection
					SCS1	0			Clock source selection [SCS1, 0] 0 1 2 3 Mode 1200bps 600bps 2400bps PT
	R/W				SCS0	0			
FF72H	RXTRG	RXEN	TXTRG	TXEN	RXTRG	0	Run	Stop	Serial I/F receive status (reading)
							Trigger	–	Serial I/F receive trigger (writing)
					RXEN	0	Enable	Disable	Serial I/F receive enable
					TXTRG	0	Run	Stop	Serial I/F transmit status (reading)
	R/W						Trigger	–	Serial I/F transmit trigger (writing)
					TXEN	0	Enable	Disable	Serial I/F transmit enable
FF73H	0	FER	PER	OER	0 *3	– *2			Unused
					FER	0	Error	No error	Framing error flag status (reading)
							Reset	–	Framing error flag reset (writing)
					PER	0	Error	No error	Parity error flag status (reading)
							Reset	–	Parity error flag reset (writing)
	R	R/W			OER	0	Error	No error	Overrun error flag status (reading)
							Reset	–	Overrun error flag reset (writing)
FF74H	TRXD3	TRXD2	TRXD1	TRXD0	TRXD3	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					TRXD2	– *2	High	Low	
					TRXD1	– *2	High	Low	
	R/W				TRXD0	– *2	High	Low	LSB
FF75H	TRXD7	TRXD6	TRXD5	TRXD4	TRXD7	– *2	High	Low	MSB
					TRXD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					TRXD5	– *2	High	Low	
	R/W				TRXD4	– *2	High	Low	
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
					TM1	0			Clock timer data (64 Hz)
	R				TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
					TM5	0			Clock timer data (4 Hz)
	R				TM4	0			Clock timer data (8 Hz)

Table 4.1.1 (c) I/O memory map (FF7CH–FFCBH)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF7CH	0	0	SWRST	SWRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/100 sec)
					SWD2	0			
	R				SWD1	0			
					SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/10 sec)
					SWD6	0			
	R				SWD5	0			
					SWD4	0			
FFC0H	MODE16	EVCNT	FCSEL	PLPOL	MODE16	0	16bit × 1	8bit × 2	8 bits × 2 or 16 bits × 1 timer mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
	R/W				FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
					PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB Programmable timer 0 reload data (low-order 4 bits) LSB
					RLD02	0			
	R/W				RLD01	0			
					RLD00	0			
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB Programmable timer 0 reload data (high-order 4 bits) LSB
					RLD06	0			
	R/W				RLD05	0			
					RLD04	0			
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB Programmable timer 1 reload data (low-order 4 bits) LSB
					RLD12	0			
	R/W				RLD11	0			
					RLD10	0			
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB Programmable timer 1 reload data (high-order 4 bits) LSB
					RLD16	0			
	R/W				RLD15	0			
					RLD14	0			
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB Programmable timer 0 data (low-order 4 bits) LSB
					PTD02	0			
	R				PTD01	0			
					PTD00	0			
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB Programmable timer 0 data (high-order 4 bits) LSB
					PTD06	0			
	R				PTD05	0			
					PTD04	0			
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB Programmable timer 1 data (low-order 4 bits) LSB
					PTD12	0			
	R				PTD11	0			
					PTD10	0			
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB Programmable timer 1 data (high-order 4 bits) LSB
					PTD16	0			
	R				PTD15	0			
					PTD14	0			

Table 4.1.1 (d) I/O memory map (FFE2H–FFFBH)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FFE2H	GPR23	GPR22	EIPT1	EIPT0	GPR23	0	1	0	General-purpose register
					GPR22	0	1	0	General-purpose register
	R/W				EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
					EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	GPR33	EISER	EISTR	EISRC	GPR33	0	1	0	General-purpose register
					EISER	0	Enable	Mask	Interrupt mask register (Serial I/F error)
	R/W				EISTR	0	Enable	Mask	Interrupt mask register (Serial I/F transmit completion)
					EISRC	0	Enable	Mask	Interrupt mask register (Serial I/F receive completion)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE7H	GPR73	GPR72	EISW1	EISW10	GPR73	0	1	0	General-purpose register
					GPR72	0	1	0	General-purpose register
	R/W				EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFEBH	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	ISER	ISTR	ISRC	0 *3	– *2	(R)	(R)	Unused
					ISER	0	Yes	No	Interrupt factor flag (Serial I/F error)
	R	R/W			ISTR	0	(W)	(W)	Interrupt factor flag (Serial I/F transmit completion)
					ISRC	0	Reset	Invalid	Interrupt factor flag (Serial I/F receive completion)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFFBH	IK03	IK02	IK01	IK00	IK03	0	(R)	(R)	Interrupt factor flag (K03)
					IK02	0	Yes	No	Interrupt factor flag (K02)
	R/W				IK01	0	(W)	(W)	Interrupt factor flag (K01)
					IK00	0	Reset	Invalid	Interrupt factor flag (K00)

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

The S1C63406 has a built-in watchdog timer that operates with a 256 Hz divided clock from the OSC1 as the source clock. The watchdog timer starts operating after initial reset, however, it can be stopped by the software. The watchdog timer must be reset cyclically by the software while it operates. If the watchdog timer is not reset in at least 3–4 seconds, it generates a non-maskable interrupt (NMI) to the CPU.
Figure 4.2.1.1 is the block diagram of the watchdog timer.

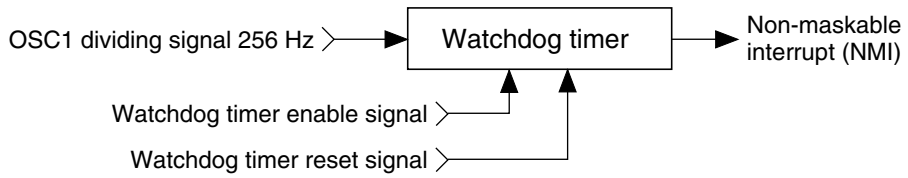


Fig. 4.2.1.1 Watchdog timer block diagram

The watchdog timer contains a 10-bit binary counter, and generates the non-maskable interrupt when the last stage of the counter (0.25 Hz) overflows.
Watchdog timer reset processing in the program's main routine enables detection of program overrun, such as when the main routine's watchdog timer processing is bypassed. Ordinarily this routine is incorporated where periodic processing takes place, just as for the timer interrupt routine.
The watchdog timer operates in the HALT mode. If a HALT status continues for 3–4 seconds, the non-maskable interrupt releases the HALT status.

4.2.2 Interrupt function

If the watchdog timer is not reset periodically, the non-maskable interrupt (NMI) is generated to the core CPU. Since this interrupt cannot be masked, it is accepted even in the interrupt disable status (I flag = "0"). However, it is not accepted when the CPU is in the interrupt mask state until SP1 and SP2 are set as a pair, such as after initial reset or during re-setting the stack pointer. The interrupt vector of NMI is assigned to 0100H in the program memory.

4.2.3 I/O memory of watchdog timer

Table 4.2.3.1 shows the I/O address and control bits for the watchdog timer.

Table 4.2.3.1 Control bits of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	HLMOD	0	WDEN	WDRST	HLMOD	0	On	Off	Heavy load protection
					0 *3	– *2			Unused
	R/W	R	R/W	W	WDEN	1	Enable	Disable	Watchdog timer enable
					WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

WDEN: Watchdog timer enable register (FF07H•D1)

Selects whether the watchdog timer is used (enabled) or not (disabled).

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

When "1" is written to the WDEN register, the watchdog timer starts count operation. When "0" is written, the watchdog timer does not count and does not generate the interrupt (NMI).
At initial reset, this register is set to "1".

WDRST: Watchdog timer reset (FF07H•D0)

Resets the watchdog timer.

When "1" is written: Watchdog timer is reset
When "0" is written: No operation
Reading: Always "0"

When "1" is written to WDRST, the watchdog timer is reset and restarts immediately after that. When "0" is written, no operation results.
This bit is dedicated for writing, and is always "0" for reading.

4.2.4 Programming notes

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

4.3 Oscillation Circuit

4.3.1 Configuration of oscillation circuit

The S1C63406 has two oscillation circuits (OSC1 and OSC3). OSC1 is either a crystal or CR oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is a CR, crystal or ceramic oscillation circuit. When processing with the S1C63406 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage V_{D1} must be switched according to the oscillation circuit to be used. Figure 4.3.1.1 is the block diagram of this oscillation system.

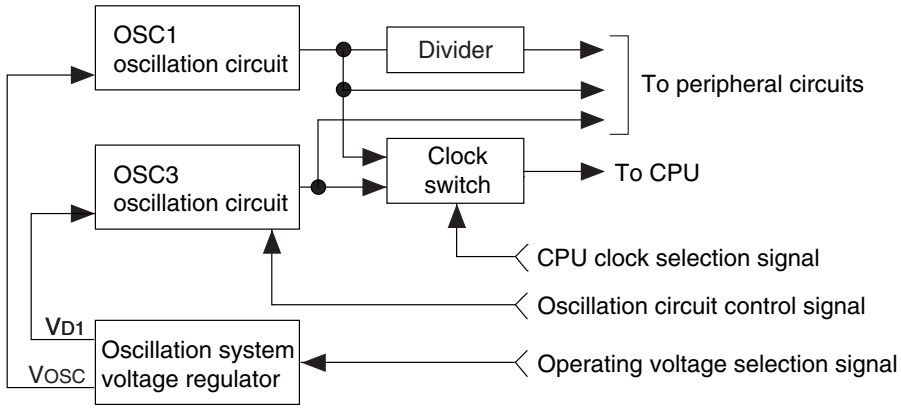
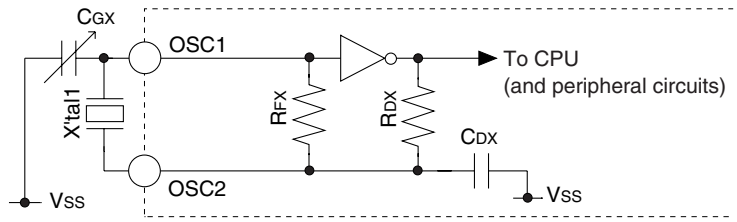


Fig. 4.3.1.1 Oscillation system block diagram

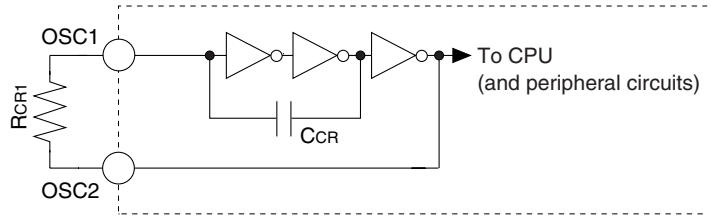
Note: The S1C63406 supports the SLEEP function. The OSC3 oscillation circuit stops in the SLEEP mode. The OSC1 oscillation circuit stops clock supply to the divider and peripheral circuits, however, the oscillation continues. To prevent improper operation after the CPU wakes up, be sure to run the CPU with the OSC1 clock before setting the CPU in the SLEEP mode.

4.3.2 OSC1 oscillation circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. Either crystal or CR can be selected for the oscillator type by mask option. The oscillation frequency of the crystal oscillation circuit is 32.768 kHz (Typ.) and the CR oscillation circuit is 60 kHz (Typ.).
This circuit operates with the VOSC (1.3 V Typ.) voltage output from the oscillation system voltage regulator.
Figure 4.3.2.1 is the block diagram of the OSC1 oscillation circuit.



(a) Crystal oscillation circuit



(b) CR oscillation circuit

Fig. 4.3.2.1 OSC1 oscillation circuit

As shown in Figure 4.3.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal1) of 32.768 kHz (Typ.) between the OSC1 and OSC2 terminals and the trimmer capacitor (CGX) between the OSC1 and VSS terminals when crystal oscillation is selected.

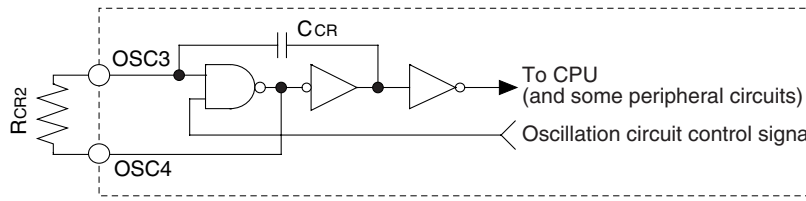
The CR oscillation circuit can be configured simply by connecting the resistor RCR1 between the OSC1 and OSC2 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics" for resistance value of RCR1.

Note: • *The current consumption of CR oscillation is larger than crystal oscillation.*

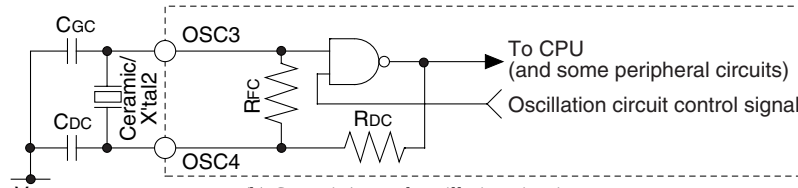
• *Be aware that the CR oscillation frequency changes slightly.*
Pay special attention to the circuits that use fOSC1 as the source clock, such as the timer (time lag) and the LCD frame frequency (display quality, flicker in low frequency).

4.3.3 OSC3 oscillation circuit

The S1C63406 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 4.2 MHz) for high speed operation and the source clock for peripheral circuits needing a high speed clock (programmable timer, FOUT output). The mask option enables selection of CR, crystal or ceramic oscillation circuit.
This circuit operates with the V_{D1} voltage and the voltage level must be switched when the OSC3 oscillation is turned ON and OFF (see the next section for details).
Figure 4.3.3.1 is the block diagram of the OSC3 oscillation circuit.



(a) CR oscillation circuit



(b) Ceramic/cryctal oscillation circuit

Fig. 4.3.3.1 OSC3 oscillation circuit

As shown in Figure 4.3.3.1, the CR oscillation circuit can be configured simply by connecting the resistor R_{CR2} between the OSC3 and OSC4 terminals when CR oscillation is selected. See Chapter 7, "Electrical Characteristics", for resistance value of R_{CR2}.
When crystal or ceramic oscillation is selected, the crystal or ceramic oscillation circuit can be configured by connecting a crystal or ceramic oscillator (Max. 4.2 MHz) between the OSC3 and OSC4 terminals, capacitor C_{GC} between the OSC3 and OSC4 terminals, and capacitor C_{DC} between the OSC4 and V_{SS} terminals. See Chapter 7, "Electrical Characteristics", for capacitor values of C_{GC} and C_{DC}. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

4.3.4 Switching of operating voltage

The CPU system clock is switched to OSC1 or OSC3 by the software (CLKCHG register). In this case, to obtain stable operation, the operating voltage V_{D1} for the internal circuits must be switched by the software (VDC1 and VDC0 registers). The power supply circuit supports the following four voltage levels. When switching the V_{D1} level, select one according to the oscillation frequency.

1. V_{D1} = 1.1 V (VDC1, VDC0 = "0H")
   This mode is provided for low-power operation. Set this mode when the system runs with the OSC1 clock (80 kHz Max.). Do not turn the OSC3 oscillation circuit on in this mode. The CLKCHG register is disabled by the hardware in this mode.
2. V_{D1} = 1.3 V (VDC1, VDC0 = "1H")
   Set this mode when using the OSC3 CR oscillation clock (700 kHz Max.). Do not set this mode if the frequency is higher than 700 kHz or OSC3 is not CR oscillation circuit.
3. V_{D1} = 1.5 V (VDC1, VDC0 = "2H")
   Set this mode when using the OSC3 CR oscillation clock (2.2 MHz Max.). Do not set this mode if OSC3 is not CR oscillation circuit or the OSC3 CR oscillation clock more than 2.2 MHz is used. This mode can be set even if a 700 kHz or less OSC3 CR oscillation clock is used. However it is not recommended for low-power operation.
4. V_{D1} = 1.7 V (VDC1, VDC0 = "3H")
   Set this mode when using the OSC3 crystal, ceramic or CR oscillation clock (4.2 MHz Max.). This mode can be set even if the OSC3 CR oscillation clock less than 2.2 MHz is used. However it is not recommended for low-power operation.

When OSC3 is to be used as the CPU system clock, it should be done as the following procedure using the software: first switch the operating voltage V_{D1}, turn the OSC3 oscillation ON after waiting 2.5 msec or more for the above operation to stabilize, switch the clock after waiting 5 msec or more for oscillation stabilization.
When switching from OSC3 to OSC1, turn the OSC3 oscillation circuit OFF after switching the clock then set the operating voltage V_{D1} to 1.1 V.

OSC1 → OSC3

1. Set VDC (1 and 0) to "1", "2" or "3".
2. Maintain 2.5 msec or more.
3. Set OSCC to "1" (OSC3 oscillation ON).
4. Maintain 5 msec or more.
5. Set CLKCHG to "1" (OSC1 → OSC3).

OSC3 → OSC1

1. Set CLKCHG to "0" (OSC3 → OSC1).
2. Set OSCC to "0" (OSC3 oscillation OFF).
3. Set VDC (1 and 0) to "0" (V_{D1} = 1.1 V).

4.3.5 Clock frequency and instruction execution time

Table 4.3.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 4.3.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μsec)		
	1-cycle instruction	2-cycle instruction	3-cycle instruction
OSC1: 32.768 kHz	61	122	183
OSC1: 60 kHz	33	67	100
OSC3: 2 MHz	1	2	3
OSC3: 3.58 MHz	0.56	1.12	1.68
OSC3: 4 MHz	0.5	1	1.5

4.3.6 I/O memory of oscillation circuit

Table 4.3.6.1 shows the I/O address and the control bits for the oscillation circuit.

Table 4.3.6.1 Control bits of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF00H	CLKCHG	OSCC	VDC1	VDC0	CLKCHG	0	OSC3	OSC1	CPU clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VDC1	0			CPU operating voltage switch [VDC1, 0] / V_{D1} (V): 0 = 1.1, 1 = 1.3, 2 = 1.5, 3 = 1.7
					VDC0	0			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

VDC1, VDC0: CPU operating voltage switching register (FF00H•D1, D0)

Switchs the operating voltage V_{D1}.

Table 4.3.6.2 CPU operating voltage and oscillation frequency

VDC1	VDC0	V_{D1}	Oscillation circuit (frequency)
1	1	1.7 V	OSC3 CR, ceramic or crystal (4.2 MHz max.)
1	0	1.5 V	OSC3 CR (2.2 MHz max.)
0	1	1.3 V	OSC3 CR (700 kHz max.)
0	0	1.1 V	OSC1 Crystal or CR (80 kHz max.)

When switching the CPU system clock, the operating voltage V_{D1} should also be switched according to the clock frequency.
When switching from OSC1 to OSC3, first set V_{D1} to the appropriate level. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, turn the OSC3 oscillation OFF after switching to OSC1, and then set V_{D1} to 1.1 V to reduce current consumption. When the VDC register is set to "0", do not turn the OSC3 oscillation ON.
At initial reset, this register is set to "0".

OSCC: OSC3 oscillation control register (FF00H•D2)

Controls oscillation ON/OFF for the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When it is necessary to operate the CPU at high speed, set OSCC to "1". At other times, set it to "0" to reduce current consumption. Furthermore, it is necessary to switch the operating voltage V_{D1} when turning the OSC3 oscillation circuit ON and OFF.
At initial reset, this register is set to "0".

CLKCHG: CPU system clock switching register (FF00H•D3)

The CPU's operation clock is selected with this register.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When the CPU clock is to be OSC3, set CLKCHG to "1"; for OSC1, set CLKCHG to "0".
After turning the OSC3 oscillation ON (OSCC = "1"), switching of the clock should be done after waiting 5 msec or more.
When OSC3 oscillation is OFF (OSCC = "0"), setting of CLKCHG = "1" becomes invalid and switching to OSC3 is not performed.
At initial reset, this register is set to "0".

4.3.7 Programming notes

(1) When switching the CPU system clock from OSC1 to OSC3, first set V_{D1}. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(4) The S1C63406 supports the SLEEP function. The OSC3 oscillation circuit stops in the SLEEP mode. The OSC1 oscillation circuit stops clock supply to the divider and peripheral circuits, however, the oscillation continues. To prevent improper operation after the CPU wakes up, be sure to run the CPU with the OSC1 clock before setting the CPU in the SLEEP mode.

4.4 Input Ports (K00–K03)

4.4.1 Configuration of input ports

The S1C63406 has four bits of general-purpose input ports. Each of the input port terminals (K00–K03) provides internal pull-up resistor. Pull-up resistor can be selected for each bit with the mask option.
Figure 4.4.1.1 shows the configuration of input port. Selection of "With pull-up resistor" with the mask option suits input from the push switch, key matrix, and so forth. When "Gate direct" is selected, the port can be used for slide switch input and interfacing with other LSIs.

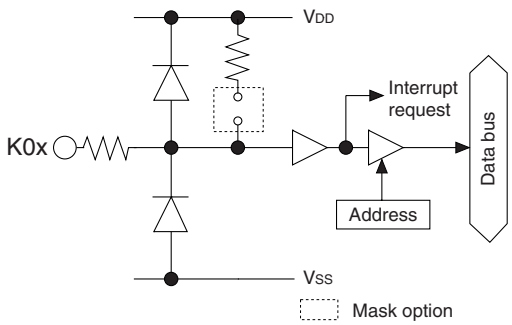


Fig. 4.4.1.1 Configuration of input port

4.4.2 Mask option

Internal pull-up resistor can be selected for each of the four bits of the input ports (K00–K03) with the input port mask option.
When "Gate direct" is selected, take care that the floating status does not occur for the input. Select "With pull-up resistor" for input ports that are not being used.

4.4.3 Interrupt function

All four bits of the input ports (K00–K03) provide the interrupt function. The conditions for issuing an interrupt can be set by the software. Further, whether to mask the interrupt function can be selected by the software.
Figure 4.4.3.1 shows the configuration of K00–K03 interrupt circuit.

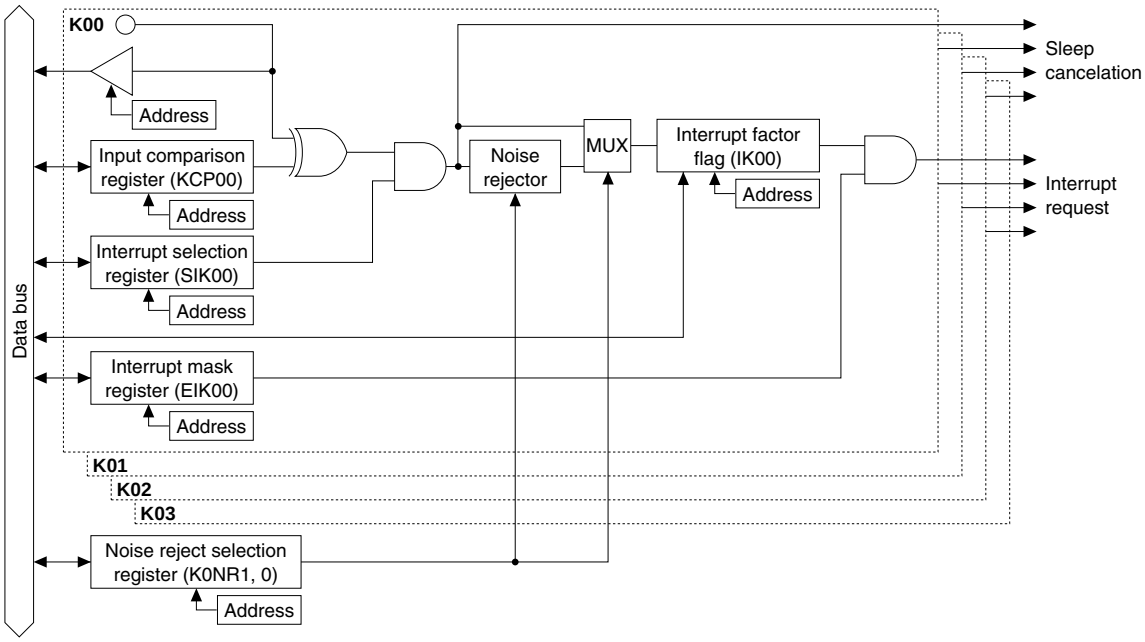


Fig. 4.4.3.1 Input interrupt circuit configuration

The interrupt selection registers (SIK00–SIK03) and input comparison registers (KCP00–KCP03) are individually provided for the input ports K00–K03.

The interrupt selection registers (SIK0x) select the ports to be used for generating input interrupts or canceling the SLEEP mode. Writing "1" into an interrupt selection register incorporates that port into the interrupt generation conditions. The changing the port where the interrupt selection register has been set to "0" does not affect the generation of the interrupt.

The input interrupt timing can select that the interrupt be generated at the rising edge of the input or that it be generated at the falling edge according to the set value of the input comparison registers (KCP0x).

By setting these two conditions, an interrupt request signal and a wake up signal are generated at the rising or falling edge (selected by KCP0x) of the signal input to the port (selected by SIK0x).

When an interrupt factor is generated, the interrupt factor flag (IK00–IK03) is set to "1". At the same time, an interrupt rquest is generated to the CPU if the corresponding interrupt mask register (EIK00–EIK03) is set to "1".
When the interrupt mask registers (EIK0x) is set to "0", the interrupt request is masked and no interrupt is generated to the CPU. However, the SLEEP mode can be cancelled regardless of the interrupt enable register setting.

The input interrupt circuit has a noise rejector to avoid unnecessary interrupt generation due to noise or chattering. This noise rejector allows selection of a noise-reject width from among three types shown in Table 4.4.3.1. Use the K0NR1 and K0NR0 registers to select a noise-reject width. If a pulse shorter than the selected width is input to the port, an interrupt is not generated. When high speed response is required, the noise rejecter can be disconnected from the input line.

Table 4.4.3.1 Setting up noise rejector

K0NR1	K0NR0	Noise-reject width
1	1	7.8 msec
1	0	2.0 msec
0	1	0.5 msec
0	0	OFF (bypassed)

(When f_{OSC1} = 32.768 kHz)

Notes:
- *Be sure to turn the noise rejector OFF before executing the SLP instruction.*
- *Reactivating from SLEEP status can only be done by generation of an input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt selection register (SIK0x = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the input port interrupt using the corresponding interrupt mask register (EIK0x = "1") before executing the SLP instruction to run input interrupt handler routine after SLEEP status is released.*
- *Each input port (K00–K03) has a different interrupt factor, thus the input interrupt is controlled individually. Be aware that this interrupt configuration is different from that of the previous models.*

4.4.4 I/O memory of input ports

Table 4.4.4.1 shows the I/O addresses and the control bits for the input ports.

Table 4.4.4.1 Control bits of input ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF42H	K03	K02	K01	K00	K03	– *2	High	Low	K00–K03 input port data
					K02	– *2	High	Low	
					K01	– *2	High	Low	
	R				K00	– *2	High	Low	
FF43H	0	0	K0NR1	K0NR0	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		R/W		K0NR1	0			K0 interrupt noise rejector [K0NR1, 0]: 0 = NR, 1 = Off, 2 = 0.5ms, 3 = 2.0ms, 3 = 7.8ms
					K0NR0	0			
FF54H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF55H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
					KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
FFEBH	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
	R/W				EIK00	0	Enable	Mask	Interrupt mask register (K00)
FFFBH	IK03	IK02	IK01	IK00	IK03	0	(R)	(R)	Interrupt factor flag (K03)
					IK02	0	Yes	No	Interrupt factor flag (K02)
					IK01	0	(W)	(W)	Interrupt factor flag (K01)
	R/W				IK00	0	Reset	Invalid	Interrupt factor flag (K00)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

K00–K03: K0 port input port data (FF42H)

Input data of the input port terminals can be read with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The reading is "1" when the terminal voltage of the four bits of the input ports (K00–K03) goes high (V_{DD}), and "0" when the voltage goes low (V_{SS}).
These bits are dedicated for reading, so writing cannot be done.

SIK00–SIK03: K0 port interrupt selection register (FF24H)

Selects the ports to be used for the K00–K03 input interrupts.

When "1" is written: Enable
When "0" is written: Disable
Reading: Valid

Enables the interrupt for the input ports (K00–K03) for which "1" has been written into the interrupt selection registers (SIK00–SIK03). The input port set for "0" does not affect the interrupt generation condition.
Reactivating from SLEEP status can only be done by generation of an input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt selection register (SIK0x = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction.
At initial reset, these registers are set to "0".

KCP00–KCP03: K0 port input comparison register (FF55H)

Interrupt conditions for terminals K00–K03 can be set with these registers.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

The interrupt conditions can be set for the rising or falling edge of input for each of the four bits (K00–K03), through the input comparison registers (KCP00–KCP03).
A comparison is done only with the ports that are enabled by the interrupt among K00–K03 by means of the SIK00–SIK03 registers.
At initial reset, these registers are set to "1".

K0NR0, K0NR1: K0 interrupt noise rejector selection register (FF43H•D0, D1)

Selects the noise-reject width.

Table 4.4.4.2 Setting up noise rejector

K0NR1	K0NR0	Noise-reject width
1	1	7.8 msec
1	0	2.0 msec
0	1	0.5 msec
0	0	OFF (bypassed)

(When f_{OSC1} = 32.768 kHz)

Be sure to turn the noise rejector OFF before executing the SLP instruction.
At initial reset, these registers are set to "0".

EIK00–EIK03: K0 input interrupt mask register (FFEBH)

Masks the input interrupt request to the CPU.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

When "1" is written to the EIK0x register, the input interrupt request will be generated to the CPU. When "0" is written, no input interrupt will be generated from the corresponding port.
The wake up signal to release the SLEEP mode will be generated even if this register is set to "0". However, enable the input port interrupt using the corresponding interrupt mask register before executing the SLP instruction to run input interrupt handler routine after SLEEP status is released.
At initial reset, this register is set to "0".

IK00–IK03: K0 input interrupt factor flag (FFFBH)

This flag indicates the occurrence of input interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

IK0x is the interrupt factor flag corresponding to the K0x port. From the status of this flag, the software can decide whether an input interrupt has occurred.
The interrupt factor flag is set to "1" when the interrupt condition is established regardless of the interrupt mask register setting. However, the interrupt does not occur to the CPU when the interrupt is masked.
This flag is reset to "0" by writing "1".
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, this flag is set to "0".

4.4.5 Programming notes

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

(2) Be sure to turn the noise rejector OFF before executing the SLP instruction.

(3) Reactivating from SLEEP status can only be done by generation of an input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt selection register (SIK0x = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the input port interrupt using the corresponding interrupt mask register (EIK0x = "1") before executing the SLP instruction to run input interrupt handler routine after SLEEP status is released.

(4) Each input port (K00–K03) has a different interrupt factor, thus the input interrupt is controlled individually. Be aware that this interrupt configuration is different from that of the previous models.

(5) The K03 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K03 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

(6) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.5 Output Ports (R10–R13)

4.5.1 Configuration of output ports

The S1C63406 has 4 bits of general output ports.
Output specifications of the output ports can be selected individually with the mask option. Two kinds of output specifications are available: complementary output and N-channel open drain output.
Figure 4.5.1.1 shows the configuration of the output port.

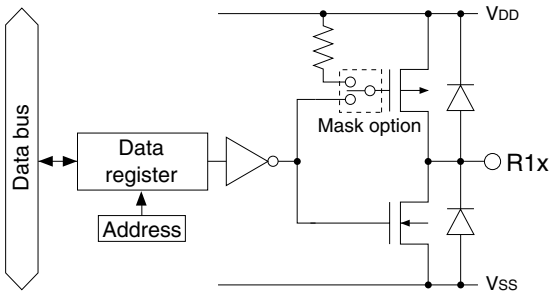


Fig. 4.5.1.1 Configuration of output port

The R12 and R13 output terminals are shared with special output terminals (TOUT, FOUT), and this function is selected by the software.
At initial reset, these are all set to the general purpose output port.
Table 4.5.1.1 shows the setting of the output terminals by function selection.

Table 4.5.1.1 Function setting of output terminals

Terminal name	Terminal status at initial reset	Special output	
		TOUT	FOUT
R10	R10 (High level output)	R10	R10
R11	R11 (High level output)	R11	R11
R12	R12 (High level output)	TOUT	
R13	R13 (High level output)		FOUT

When using the output port (R12, R13) as the special output port, the data register must be fixed at "1".

4.5.2 Mask option

Output specifications of the output ports can be selected by mask option.
The output specifications of the output ports R10–R13 can be selected from either complementary output or N-channel open drain output individually (in 1-bit units).
However, when N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the output port.

4.5.3 DC output

The R10–R13 output ports can be used as general-purpose DC output ports.
When "1" is written to the R1x data register, the corresponding output port terminal goes high. When "0" is written, the port terminal goes low.

4.5.4 Special output

In addition to the regular DC output, special output can be selected for the output ports R12 and R13 as shown in Table 4.5.4.1 with the software.
Figure 4.5.4.1 shows the configuration of the R12 and R13 output ports.

Table 4.5.4.1 Special output

Terminal	Special output	Output control register
R13	FOUT	FOUTE
R12	TOUT	PTOUT

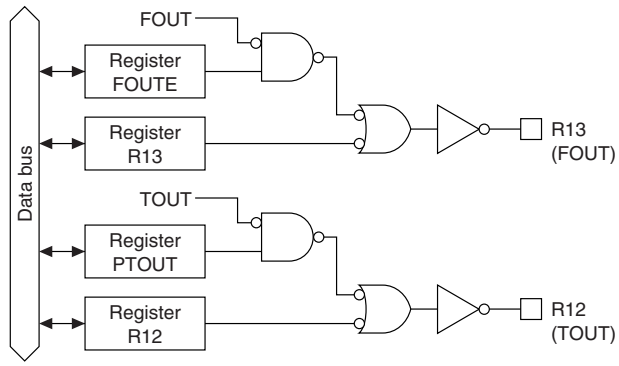


Fig. 4.5.4.1 Configuration of R12 and R13 output ports

At initial reset, the output port data register is set to "1", so the output terminal goes high (V_{DD}).
When using the output port (R12, R13) as the special output port, fix the data register (R12, R13) at "1" and the respective signal should be turned ON and OFF using the special output control register.

Note: Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R12 and R13 registers when the special output has been selected.

- **TOUT (R12)**

  The R12 terminal can output a TOUT signal.
  The TOUT signal is the clock that is output from the programmable timer, and can be used to provide a clock signal to an external device.
  To output the TOUT signal, fix the R12 register at "1" and turn the signal ON and OFF using the PTOUT register. It is, however, necessary to control the programmable timer.
  Refer to Section 4.10, "Programmable Timer" for details of the programmable timer.

Note: A hazard may occur when the TOUT signal is turned ON and OFF.

Figure 4.5.4.2 shows the output waveform of the TOUT signal.

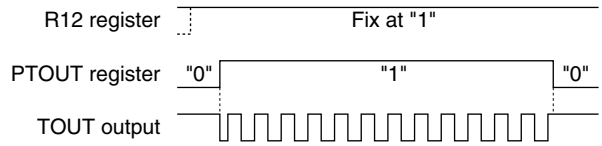


Fig. 4.5.4.2 Output waveform of TOUT signal

- **FOUT (R13)**

The R13 terminal can output a FOUT signal.
The FOUT signal is a clock that is output from the oscillation circuit or a clock that the f_{OSC1} clock has divided in the internal circuit, and can be used to provide a clock signal to an external device.
To output the FOUT signal, fix the R13 register at "1" and turn the signal ON and OFF using the FOUTE register.
The frequency of the output clock may be selected from among 8 types shown in Table 4.5.4.2 by setting the FOFQ0–FOFQ2 registers.

Table 4.5.4.2 FOUT clock frequency

FOFQ2	FOFQ1	FOFQ0	Clock frequency
1	1	1	f_{OSC3}
1	1	0	$f_{OSC3}/2$
1	0	1	f_{OSC1}
1	0	0	$f_{OSC1}/4$
0	1	1	$f_{OSC1}/8$
0	1	0	$f_{OSC1}/16$
0	0	1	$f_{OSC1}/32$
0	0	0	$f_{OSC1}/64$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

Note: A hazard may occur when the FOUT signal is turned ON and OFF.

Figure 4.5.4.3 shows the output waveform of the FOUT signal.

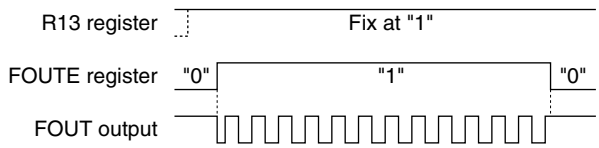


Fig. 4.5.4.3 Output waveform of FOUT signal

4.5.5 I/O memory of output ports

Table 4.5.5.1 shows the I/O addresses and control bits for the output ports.

Table 4.5.5.1 Control bits of output ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF06H	FOUTE	FOFQ2	FOFQ1	FOFQ0	FOUTE	0	Enable	Disable	FOUT enable
					FOFQ2	0			FOUT frequency selection [FOFQ2–0] 0: Frequency fosc1/64; 1: fosc1/32; 2: fosc1/16; 3: fosc1/8; 4: fosc1/4; 5: fosc1; 6: fosc3/2; 7: fosc3
					FOFQ1	0			
	R/W				FOFQ0	0			
FF46H	R13	R12	R11	R10	R13	1	High	Low	R13 output port data (FOUTE=0) / Fix at "1" when FOUT is used (FOUTE=1)
					R12	1	High	Low	R12 output port data (PTOUT=0) / Fix at "1" when TOUT is used (PTOUT=1)
	R/W				R11	1	High	Low	R11 output port data
					R10	1	High	Low	R10 output port data
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
	R/W				CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
					CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

R10–R13: R1 output port data register (FF46H)

Set the output data for the output ports.

When "1" is written: High level output
When "0" is written: Low level output
Reading: Valid

The output port terminals output the data written in the corresponding data registers without changing it. When "1" is written to the register, the output port terminal goes high (V_{DD}), and when "0" is written, the output port terminal goes low (V_{SS}).
When the output ports R12 and R13 are used for special output (TOUT, FOUT), fix the R12 register and the R13 register at "1".
At initial reset, these registers are all set to "1".

PTOUT: TOUT output control register (FFC1H•D2)

Controls the TOUT output.

When "1" is written: TOUT output ON
When "0" is written: TOUT output OFF
Reading: Valid

By writing "1" to the PTOUT register when the R12 register has been set to "1", the TOUT signal is output from the R12 terminal. When "0" is written, the R12 terminal goes high (V_{DD}).
When using the R12 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

FOUTE: FOUT output control register (FF06H•D3)

Controls the FOUT output.

When "1" is written: FOUT output ON
When "0" is written: FOUT output OFF
Reading: Valid

By writing "1" to the FOUTE register when the R13 register has been set to "1" , an FOUT signal is output from the R13 terminal. When "0" is written, the R13 terminal goes high (V_{DD}).
When using the R13 output port for DC output, fix this register at "0".
At initial reset, this register is set to "0".

FOFQ0–FOFQ2: FOUT frequency selection register (FF06H•D0–D2)

Selects a frequency of the FOUT signal.

Table 4.5.5.2 FOUT clock frequency

FOFQ2	FOFQ1	FOFQ0	Clock frequency
1	1	1	f_{OSC3}
1	1	0	$f_{OSC3}/2$
1	0	1	f_{OSC1}
1	0	0	$f_{OSC1}/4$
0	1	1	$f_{OSC1}/8$
0	1	0	$f_{OSC1}/16$
0	0	1	$f_{OSC1}/32$
0	0	0	$f_{OSC1}/64$

f_{OSC1}: Clock that is output from the OSC1 oscillation circuit
f_{OSC3}: Clock that is output from the OSC3 oscillation circuit

At initial reset, this register is set to "0".

4.5.6 Programming notes

(1) When using the output port (R12, R13) as the special output port, fix the data register (R12, R13) at "1". Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R12 and R13 registers when the special output has been selected.

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output.
Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

4.6 I/O Ports (P20–P23)

4.6.1 Configuration of I/O ports

The S1C63406 has four bits of general-purpose I/O ports.
Figure 4.6.1.1 shows the configuration of the I/O port.

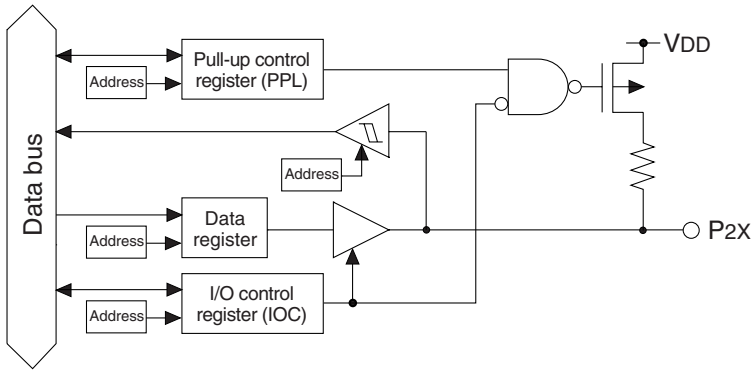


Fig. 4.6.1.1 Configuration of I/O port

The I/O port terminals P20–P23 are shared with the serial interface input/output terminals. The software can select the function to be used.
At initial reset, these terminals are all set to the I/O port.
Table 4.6.1.1 shows the setting of the input/output terminals by function selection.

Table 4.6.1.1 Function setting of input/output terminals

Terminal	Terminal status at initial reset	Serial I/F		
		Master	Slave	Async.
P20	P20 (Input & pull-up)	SIN(I)	SIN(I)	SIN(I)
P21	P21 (Input & pull-up)	SOUT(O)	SOUT(O)	SOUT(O)
P22	P22 (Input & pull-up)	$\overline{\text{SCLK}}$(O)	$\overline{\text{SCLK}}$(I)	P22
P23	P23 (Input & pull-up *)	P23	$\overline{\text{SRDY}}$(O)	P23

When these ports are used as I/O ports, the ports can be set to either input mode or output mode individually (in 1-bit unit). Modes can be set by writing data to the I/O control registers.
Refer to Section 4.11, "Serial Interface", for control of the serial interface.

4.6.2 Mask option

In the I/O ports, the output specification during output mode can be selected from either complementary output or N-channel open drain output in 1-bit units.
When N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the port.

The output specification selected by mask option are effective even when I/O ports are used as the serial interface output port.

4.6.3 I/O control registers and input/output mode

Input or output mode can be set for the I/O ports by writing data into the corresponding I/O control registers IOC2x.

To set the input mode, write "0" to the I/O control register. When an I/O port is set to input mode, it becomes high impedance status and works as an input port.
However, when the pull-up explained in the following section has been set by software, the input line is pulled up only during this input mode.

To set the output mode, write "1" is to the I/O control register. When an I/O port is set to output mode , it works as an output port, it outputs a high level (V_{DD}) when the port output data is "1", and a low level (V_{SS}) when the port output data is "0".

If perform the read out in each mode; when output mode, the register value is read out, and when input mode, the port value is read out.

At initial reset, the I/O control registers are set to "0", and the I/O ports enter the input mode.

The I/O control registers of the ports that are set as input/output for the serial interface can be used as general purpose registers that do not affect the I/O control. (See Table 4.6.1.1.)

4.6.4 Pull-up during input mode

A pul-up resistor that operates during the input mode is built into each I/O port of the S1C63406.

The pull-up resistor becomes effective by writing "1" to the pull-up control register PPL2x that corresponds to each port, and the input line is pulled up during the input mode. When "0" has been written, no pull-up is done.
At initial reset, the pull-up control registers are set to "1".

The pull-up control registers of the ports, that are set as output for the serial interface, can be used as general purpose registers that do not affect the pull-up control. (See Table 4.6.1.1.)
The pull-up control registers of the port, that are set as input for the serial interface, function the same as the I/O port.

4.6.5 I/O memory of I/O ports

Table 4.6.5.1 shows the I/O addresses and the control bits for the I/O ports.

Table 4.6.5.1 Control bits of I/O ports

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF48H	IOC23	IOC22	IOC21	IOC20	IOC23	0	Output	Input	P23 I/O control register General-purpose register when SIF (clock sync. slave) is selected
					IOC22	0	Output	Input	P22 I/O control register General-purpose register when SIF (clock sync.) is selected
	R/W				IOC21	0	Output	Input	P21 I/O control register (ESIF=0) General-purpose register when SIF is selected
					IOC20	0	Output	Input	P20 I/O control register (ESIF=0) General-purpose register when SIF is selected
FF49H	PPL23	PPL22	PPL21	PPL20	PPL23	1	On	Off	P23 pull-up control register General-purpose register when SIF (clock sync. slave) is selected
					PPL22	1	On	Off	P22 pull-up control register General-purpose register when SIF (clock sync. master) is selected
	R/W								$\overline{SCLK}$ (I) pull-up control register when SIF (clock sync. slave) is selected
					PPL21	1	On	Off	P21 pull-up control register (ESIF=0) General-purpose register when SIF is selected
					PPL20	1	On	Off	P20 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF4AH	P23 (XSRDY)	P22 (XSCLK)	P21 (SOUT)	P20 (SIN)	P23	– *2	High	Low	P23 I/O port data General-purpose register when SIF (clock sync. slave) is selected
					P22	– *2	High	Low	P22 I/O port data General-purpose register when SIF (clock sync.) is selected
	R/W				P21	– *2	High	Low	P21 I/O port data (ESIF=0) General-purpose register when SIF is selected
					P20	– *2	High	Low	P20 I/O port data (ESIF=0) General-purpose register when SIF is selected
FF70H	0	SMD1	SMD0	ESIF	0 *3	– *2			Unused
					SMD1	0			Serial I/F mode selection [SMD1, 0]: 0 = Mode: Clk-sync. master; 1 = Clk-sync. slave; 2 = Async. 7-bit; 3 = Async. 8-bit
					SMD0	0			
	R	R/W			ESIF	0	SIF	I/O	Serial I/F enable (P2x port function selection)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (FF70H•D0)

Selects function for P20–P23.

When "1" is written: Serial interface input/output port
When "0" is written: I/O port
Reading: Valid

When using the serial interface, write "1" to this register and when P20–P23 are used as the I/O port, write "0". The terminal configuration within P20–P23 that are used for the serial interface is decided by the transfer mode (7-bit asynchronous, 8-bit asynchronous, clock synclonous slave, clock synchronous master) selected with the SMD1 and SMD0 registers.
In the clock synchronous slave mode, all the P20–P23 ports are set to the serial interface input/output port. In the clock synchronous master mode, P20–P22 are set to the serial interface input/output port and P23 can be used as the I/O port. In the 8/7-bit asynchronous mode, P20 and P21 are set to the serial interface input/output port and P22 and P23 can be used as the I/O port.
At initial reset, this register is set to "0".

P20–P23: P2 I/O port data register (FF4AH)

I/O port data can be read and output data can be set through these registers.

• ***When writing data***

When "1" is written: High level
When "0" is written: Low level

When an I/O port is set to the output mode, the written data is output unchanged from the I/O port terminal. When "1" is written as the port data, the port terminal goes high (V_{DD}), and when "0" is written, the terminal goes low (V_{SS}).
Port data can be written also in the input mode.

• ***When reading data***

When "1" is read: High level
When "0" is read: Low level

The terminal voltage level of the I/O port is read out. When the I/O port is in the input mode the voltage level being input to the port terminal can be read out; in the output mode the register value can be read. When the terminal voltage is high (V_{DD}) the port data that can be read is "1", and when the terminal voltage is low (V_{SS}) the data is "0".
When the PPL register is set to "1", the built-in pull-up resister goes ON during input mode, so that the I/O port terminal is pulled up.

The data registers of the port, which are set for the input/output of the serial interface, become general-purpose registers that do not affect the input/output.

Note: When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

IOC20–IOC23: P2 port I/O control register (FF48H)

The input and output modes of the I/O ports are set with these registers.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

The input and output modes of the I/O ports are set in 1-bit unit.
Writing "1" to the I/O control register makes the corresponding I/O port enter the output mode, and writing "0" induces the input mode.
At initial reset, these registers are all set to "0", so the I/O ports are in the input mode.
The I/O control registers of the port, which are set for the input/output of the serial interface, become general-purpose registers that do not affect the input/output.

PPL20–PPL23: P2 port pull-up control register (FF49H)

The pull-up during the input mode are set with these registers.

When "1" is written: pull-up ON
When "0" is written: pull-up OFF
Reading: Valid

The built-in pull-up resistor which is turned ON during input mode is set to enable in 1-bit units.
By writing "1" to the pull-up control register, the corresponding I/O ports are pulled up (during input mode), while writing "0" turns the pull-up function OFF.
At initial reset, these registers are all set to "1", so the pull-up function is set to ON.

The pull-up control registers of the ports that are set as output for the serial interface can be used as general purpose registers that do not affect the pull-up control.
The pull-up control registers of the port that are set as input for the serial interface function the same as the I/O port.

4.6.6 Programming note

When in the input mode, I/O ports are changed from low to high by pull-up resistor, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.

$10 \times C \times R$

C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

4.7 LCD Driver (COM0–COM8, SEG0–SEG59)

4.7.1 Configuration of LCD driver

The S1C63406 has 9 common terminals (COM0–COM8) and 60 segment terminals (SEG0–SEG59), so that it can drive a dot matrix type LCD with a maximum of 540 (60 × 9) dots.
The driving method is 1/8 duty or 1/9 duty dynamic drive with four voltages (1/4 bias), V_{C1}, V_{C2}, V_{C4} and V_{C5}.
LCD display ON/OFF can be controlled by the software.

4.7.2 Power supply for LCD driving

V_{C1}–V_{C5} are driving voltages (1/4 bias) for the LCD that are generated by the LCD system voltage circuit. Turning the LCD system voltage circuit ON or OFF is controlled with the LPWR register. When LPWR is set to "1", the LCD system voltage circuit outputs the LCD drive voltages V_{C1}–V_{C5} to the LCD driver.

The LCD system voltage circuit generates V_{C1} or V_{C2} with the voltage regulator incorporated in itself, and generates three other voltages by boosting or reducing the voltage V_{C1} or V_{C2}. Table 4.7.2.1 shows the V_{C1}, V_{C2}, V_{C4} and V_{C5} voltage values and boost/reduce status.

Table 4.7.2.1 LCD drive voltage when generated internally

LCD drive voltage	V_{DD} = 1.3–3.6 V	V_{DD} = 2.5–3.6 V
V_{C1} (0.975–1.2 V)	V_{C1} (standard)	1/2 × V_{C2}
V_{C2} (1.950–2.4 V)	2 × V_{C1}	V_{C2} (standard)
V_{C4} (2.925–3.6 V)	3 × V_{C1}	3/2 × V_{C2}
V_{C5} (3.900–4.8 V)	4 × V_{C1}	2 × V_{C2}

∗ The LCD drive voltage can be adjusted by the software (see Section 4.7.5). Values in the table are typical values.

Select either V_{C1} standard or V_{C2} standard using the VCCHG register.
When "1" is written to the VCCHG register, V_{C2} standard is selected and when "0" is written, V_{C1} standard is selected. At initial reset, V_{C1} standard (VCCHG = "0") is set.

Note: Current consumption will be increased for a cycle of 1 kHz to stabilize the LCD power quickly after setting LPWR on.

4.7.3 LCD display control (ON/OFF) and switching of duty

(1) Display ON/OFF control

The S1C63406 incorporates the ALON and ALOFF registers to blink display. When "1" is written to ALON, all the dots go ON, and when "1" is written to ALOFF, all the dots go OFF. At such a time, an ON waveform or an OFF waveform is output from SEG terminals. When "0" is written to these registers, normal display is performed. Furthermore, when "1" is written to both of the ALON and ALOFF, ALON (all ON) has priority over the ALOFF (all OFF).

(2) Switching of drive duty

In the S1C63406, the drive duty can be set to 1/8 or 1/9 by the software. This setting is done using the LDUTY0 register as shown in Table 4.7.3.1.

Table 4.7.3.1 LCD drive duty setting

LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	1/8	COM0–COM7	480 (60 × 8)
0	1/9	COM0–COM8	540 (60 × 9)

Table 4.7.3.2 shows the frame frequencies corresponding to the OSC1 oscillation frequency and drive duty.

Table 4.7.3.2 Frame frequency

OSC1 oscillation frequency	When 1/8 duty is selected	When 1/9 duty is selected
32.768 kHz	32 Hz	28.4 Hz
60 kHz	58.6 Hz	52.0 Hz

Figure 4.7.3.1 shows the dynamic drive waveform for 1/4 bias.

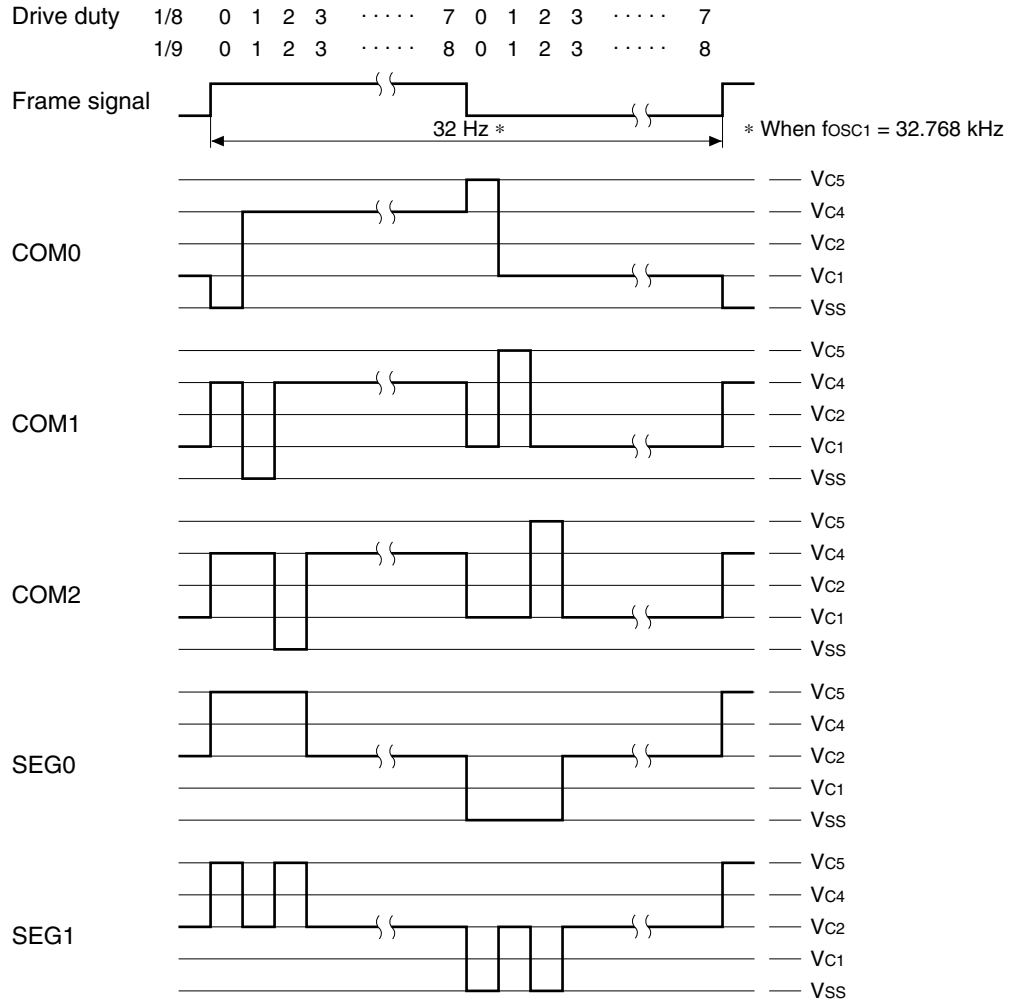


Fig. 4.7.3.1 LCD drive waveform (1/4 bias)

4.7.4 Display memory

The display memory is allocated to F000H–F176H in the data memory area and the addresses and the data bits correspond to COM and SEG outputs as shown in Figure 4.7.4.1.

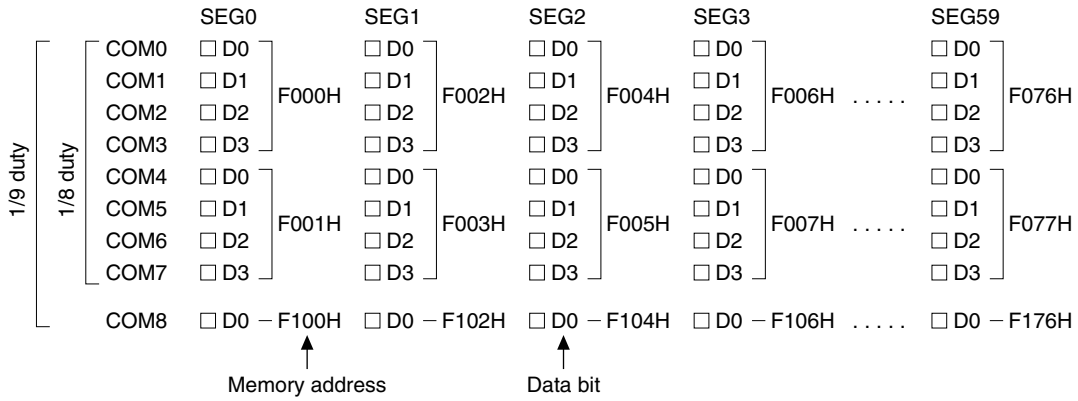


Fig. 4.7.4.1 Correspondence between display memory and LCD dot matrix

When a bit in the display memory is set to "1", the corresponding LCD dot goes ON, and when it is set to "0", the dot goes OFF.
At initial reset, the data memory content becomes undefined hence, there is need to initialize using the software.
The display memory has read / write capability, and the addresses that have not been used for LCD display can be used as general purpose registers.

Note: When a program that access no memory mounted area (F078H–F0FFH, F101H, F103H, · · ·, F177H) is made, the operation is not guaranteed.

4.7.5 LCD contrast adjustment

In the S1C63406, the LCD contrast can be adjusted by the software.
It is realized by controlling the voltages V_{C1}–V_{C5} output from the LCD system voltage circuit. The contrast can be adjusted to 16 levels as shown in Table 4.7.5.1. When VCCHG = "0", V_{C1} is changed within the range from 0.975 V to 1.2 V, and other voltages change according to V_{C1}. When VCCHG = "1", V_{C2} is changed within the range from 1.950 V to 2.4 V, and other voltages change according to V_{C2}.

Table 4.7.5.1 LCD contrast

No.	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	↓
15	1	1	1	1	dark

At room temperature, use setting number 7 or 8 as standard.
Since the contents of LC0–LC3 are undefined at initial reset, initialize it by the software.

4.7.6 I/O memory of LCD driver

Table 4.7.6.1 shows the I/O addresses and the control bits for the LCD driver. Figure 4.7.6.1 shows the display memory map.

Table 4.7.6.1 LCD driver control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF60H	LDUTY1	LDUTY0	VCCHG	LPWR	LDUTY1	0	1	0	General-purpose register
					LDUTY0	0	1/8	1/9	LCD drive duty switch
	R/W				VCCHG	0	V_{C2}	V_{C1}	LCD regulated voltage switch
					LPWR	0	On	Off	LCD power On/Off
FF61H	EXLCDC	ALOFF	ALON	LPAGE	EXLCDC	0	1	0	General-purpose register
					ALOFF	1	All Off	Normal	LCD all OFF control
	R/W				ALON	0	All On	Normal	LCD all ON control
					LPAGE	0	1	0	General-purpose register
FF62H	LC3	LC2	LC1	LC0	LC3	– *2			LCD contrast adjustment
					LC2	– *2			[LC3–0] 0 – 15
	R/W				LC1	– *2			Contrast Light – Dark
					LC0	– *2			

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

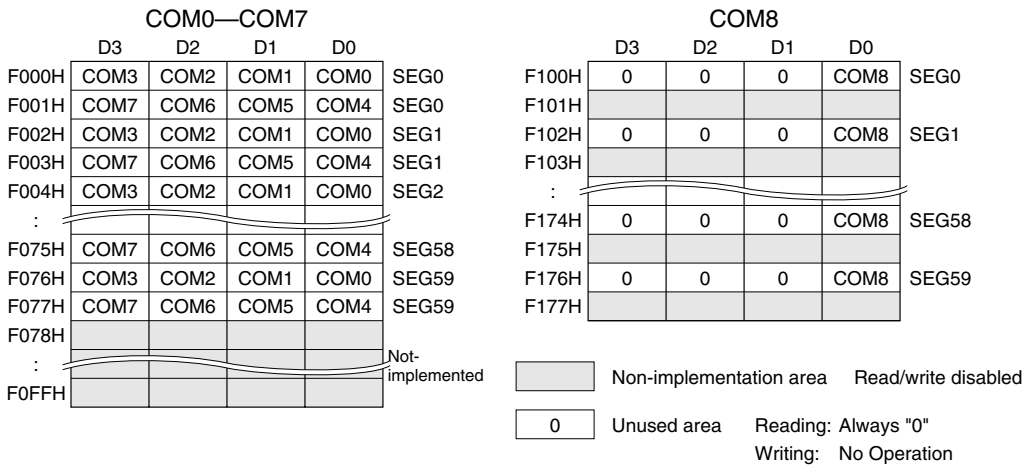


Fig. 4.7.6.1 Display memory map

LPWR: LCD power control (ON/OFF) register (FF60H•D0)

Turns the LCD system voltage circuit ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

When "1" is written to the LPWR register, the LCD system voltage circuit goes ON and generates the LCD drive voltage. When "0" is written, all the LCD drive voltages go to V_{SS} level.
It takes about 100 msec for the LCD drive voltage to stabilize after starting up the LCD system voltage circuit by writing "1" to the LPWR register.
At initial reset, this register is set to "0".

VCCHG: LCD regulated voltage switching register (FF60H•D1)

Selects the reference voltage for the LCD drive voltage.

When "1" is written: V_{C2}
When "0" is written: V_{C1}
Reading: Valid

When "1" is written to the VCCHG register, the LCD system voltage circuit generates the LCD drive voltage as V_{C2} standard. When "0" is written, it becomes V_{C1} standard. Select V_{C2} when power supply voltage is 2.5 V or more, otherwise, select V_{C1}.
At initial reset, this register is set to "0".

LDUTY0: LCD drive duty switching register (FF60H•D2)

Selects the LCD drive duty.

Table 4.7.6.2 Drive duty setting

LDUTY0	Drive duty	Common terminal used	Maximum segment number
1	1/8	COM0–COM7	480 (60 × 8)
0	1/9	COM0–COM8	540 (60 × 9)

At initial reset, this register is set to "0".

ALON: LCD all ON control register (FF61H•D1)

Displays the all LCD dots ON.

When "1" is written: All LCD dots displayed
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALON register, all the LCD dots goes ON, and when "0" is written, it returns to normal display.
This function outputs an ON waveform to the SEG terminals, and does not affect the content of the display memory.
ALON has priority over ALOFF.
At initial reset, this register is set to "0".

ALOFF: LCD all OFF control register (FF61H•D2)

Fade outs the all LCD dots.

When "1" is written: All LCD dots fade out
When "0" is written: Normal display
Reading: Valid

By writing "1" to the ALOFF register, all the LCD dots goes OFF, and when "0" is written, it returns to normal display.
This function outputs an OFF waveform to the SEG terminals, and does not affect the content of the display memory.
At initial reset, this register is set to "1".

LC3–LC0: LCD contrast adjustment register (FF62H)

Adjusts the LCD contrast.

LC3–LC0 = 0000B light
: :
LC3–LC0 = 1111B dark

At room temperature, use setting number 7 or 8 as standard.
At initial reset, LC0–LC3 are undefined.

4.7.7 Programming notes

(1) Current consumption will be increased for a cycle of 1 kHz to stabilize the LCD power quickly after setting LPWR on.

(2) When a program that access no memory mounted area (F078H–F0FFH, F101H, F103H, · · ·, F177H) is made, the operation is not guaranteed.

(3) Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

4.8 Clock Timer

4.8.1 Configuration of clock timer

The S1C63406 has a built-in clock timer that uses OSC1 (crystal oscillator) as the source oscillator. The clock timer is configured of an 8-bit binary counter that serves as the input clock, fOSC1 divided clock output from the prescaler. Timer data (128–16 Hz and 8–1 Hz) can be read out by the software.
Figure 4.8.1.1 is the block diagram for the clock timer.

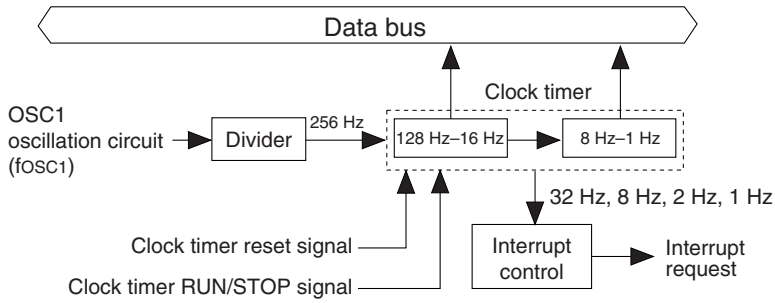


Fig. 4.8.1.1 Block diagram for the clock timer

Ordinarily, this clock timer is used for all types of timing functions such as clocks.

Note: When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

4.8.2 Data reading and hold function

The 8 bits timer data are allocated to the address FF79H and FF7AH.

<FF79H>	D0: TM0 = 128 Hz	D1: TM1 = 64 Hz	D2: TM2 = 32 Hz	D3: TM3 = 16 Hz
<FF7AH>	D0: TM4 = 8 Hz	D1: TM5 = 4 Hz	D2: TM6 = 2 Hz	D3: TM7 = 1 Hz

Since the clock timer data has been allocated to two addresses, a carry is generated from the low-order data within the count (TM0–TM3: 128–16 Hz) to the high-order data (TM4–TM7: 8–1 Hz). When this carry is generated between the reading of the low-order data and the high-order data, a content combining the two does not become the correct value (the low-order data is read as FFH and the high-order data becomes the value that is counted up 1 from that point).
The high-order data hold function in the S1C63406 is designed to operate to avoid this. This function temporarily stops the counting up of the high-order data (by carry from the low-order data) at the point where the low-order data has been read and consequently the time during which the high-order data is held is the shorter of the two indicated here following.

1. Period until it reads the high-order data.
2. 0.48–1.5 msec (Varies due to the read timing.)

Note: Since the low-order data is not held when the high-order data has previously been read, the low-order data should be read first.

4.8.3 Interrupt function

The clock timer can cause interrupts at the falling edge of 32 Hz, 8 Hz, 2 Hz and 1 Hz signals. Software can set whether to mask any of these frequencies.
Figure 4.8.3.1 is the timing chart of the clock timer.

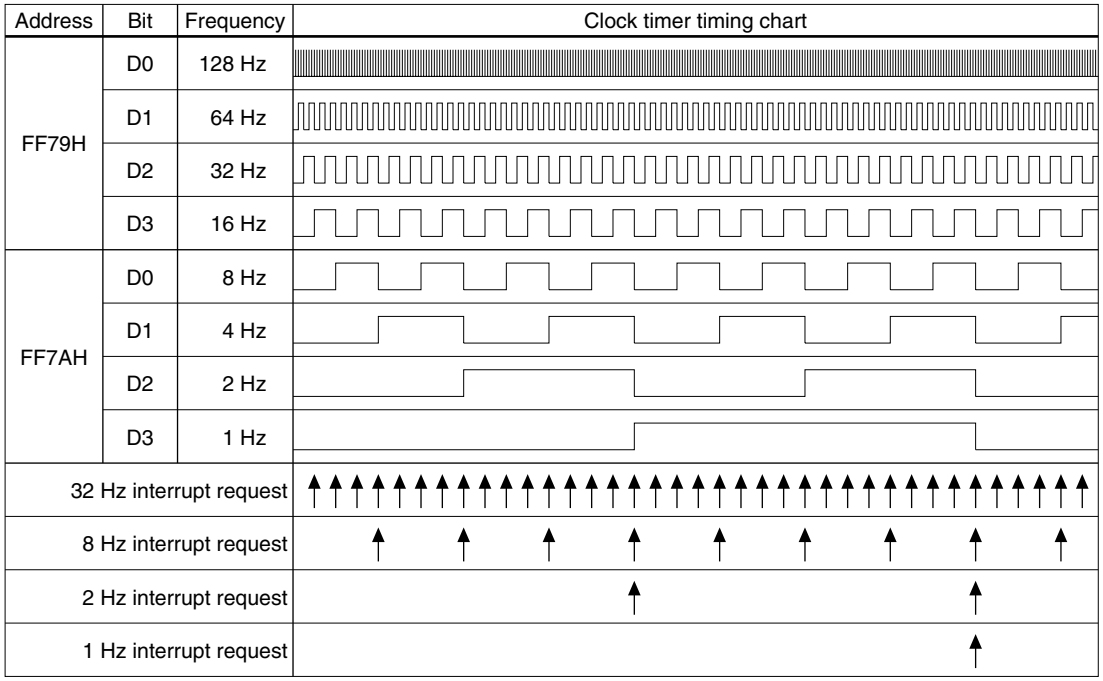


Fig. 4.8.3.1 Timing chart of clock timer

As shown in Figure 4.8.3.1, interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). At this time, the corresponding interrupt factor flag (IT0, IT1, IT2, IT3) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT0, EIT1, EIT2, EIT3). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

4.8.4 I/O memory of clock timer

Table 4.8.4.1 shows the I/O addresses and the control bits for the clock timer.

Table 4.8.4.1 Control bits of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF78H	0	0	TMRST	TMRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	TMRST*3	Reset	Reset	Invalid	Clock timer reset (writing)
					TMRUN	0	Run	Stop	Clock timer Run/Stop
FF79H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
FF7AH	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
	R/W				EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
					EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
	R/W				IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
					IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

TM0–TM7: Timer data (FF79H, FF7AH)

The 128–1 Hz timer data of the clock timer can be read out with these registers. These eight bits are read only, and writing operations are invalid.

By reading the low-order data (FF79H), the high-order data (FF7AH) is held until reading or for 0.48–1.5 msec (one of shorter of them).

At initial reset, the timer data is initialized to "00H".

TMRST: Clock timer reset (FF78H•D1)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

The clock timer is reset by writing "1" to TMRST. When the clock timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to TMRST.

This bit is write-only, and so is always "0" at reading.

TMRUN: Clock timer RUN/STOP control register (FF78H•D0)

Controls RUN / STOP of the clock timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The clock timer enters the RUN status when "1" is written to the TMRUN register, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.
At initial reset, this register is set to "0".

EIT0: 32 Hz interrupt mask register (FFE6H•D0)
EIT1: 8 Hz interrupt mask register (FFE6H•D1)
EIT2: 2 Hz interrupt mask register (FFE6H•D2)
EIT3: 1 Hz interrupt mask register (FFE6H•D3)

These registers are used to select whether to mask the clock timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EIT0, EIT1, EIT2, EIT3) are used to select whether to mask the interrupt to the separate frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz).
At initial reset, these registers are set to "0".

IT0: 32 Hz interrupt factor flag (FFF6H•D0)
IT1: 8 Hz interrupt factor flag (FFF6H•D1)
IT2: 2 Hz interrupt factor flag (FFF6H•D2)
IT3: 1 Hz interrupt factor flag (FFF6H•D3)

These flags indicate the status of the clock timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags (IT0, IT1, IT2, IT3) correspond to the clock timer interrupts of the respective frequencies (32 Hz, 8 Hz, 2 Hz, 1 Hz). The software can judge from these flags whether there is a clock timer interrupt. However, even if the interrupt is masked, the flags are set to "1" at the falling edge of the signal.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.8.5 Programming notes

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

4.9 Stopwatch Timer

4.9.1 Configuration of stopwatch timer

The S1C63406 has 1/100 sec unit and 1/10 sec unit stopwatch timer built-in. The stopwatch timer is configured with a 2 levels 4-bit BCD counter which has an input clock approximating 100 Hz signal (signal divided from OSC1 to the closest 100 Hz) and data can be read in units of 4 bits by software. Figure 4.9.1.1 shows the configuration of the stopwatch timer.

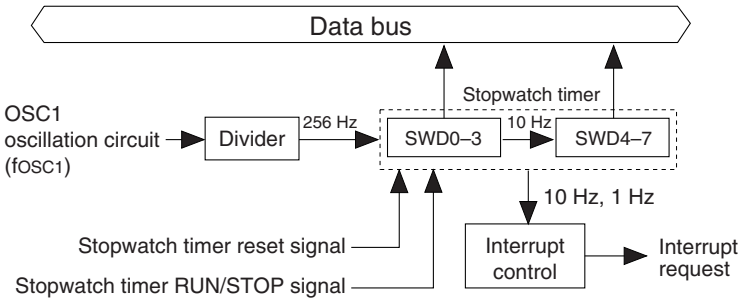


Fig. 4.9.1.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

Note: When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, this timer can not be used for the stopwatch function.

4.9.2 Count-up pattern

The stopwatch timer is configured of 4-bit BCD counters SWD0–SWD3 and SWD4–SWD7.
The counter SWD0–SWD3, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWD4–SWD7 has an approximated 10 Hz signal generated by the counter SWD0–SWD3 for the input clock. In count-up every 1/10 sec, and generated 1 Hz signal.
Figure 4.9.2.1 shows the count-up pattern of the stopwatch timer.

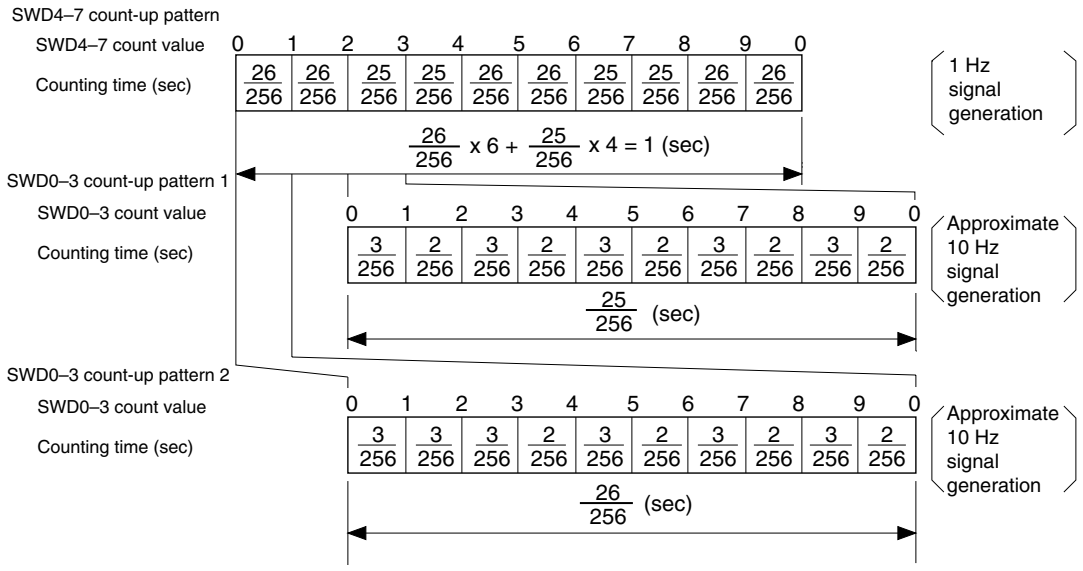


Fig. 4.9.2.1 Count-up pattern of stopwatch timer

SWD0–SWD3 generates an approximated 10 Hz signal from the basic 256 Hz signal (f_{OSC1} dividing clock). The count-up intervals are 2 / 256 sec and 3 / 256 sec, so that finally two patterns are generated: 25 / 256 sec and 26 / 256 sec intervals. Consequently, these patterns do not amount to an accurate 1 / 100 sec. SWD4–SWD7 counts the approximated 10 Hz signals generated by the 25 / 256 sec and 26 / 256 sec intervals in the ratio of 4 : 6, to generate a 1 Hz signal. The count-up intervals are 25 / 256 sec and 26 / 256 sec, which do not amount to an accurate 1 / 10 sec.

4.9.3 Interrupt function

The stopwatch timers SWD0–SWD3 and SWD4–SWD7, through their respective overflows, can generate 10 Hz (approximate 10 Hz) and 1 Hz interrupts.
Figure 4.9.3.1 shows the timing chart for the stopwatch timer.

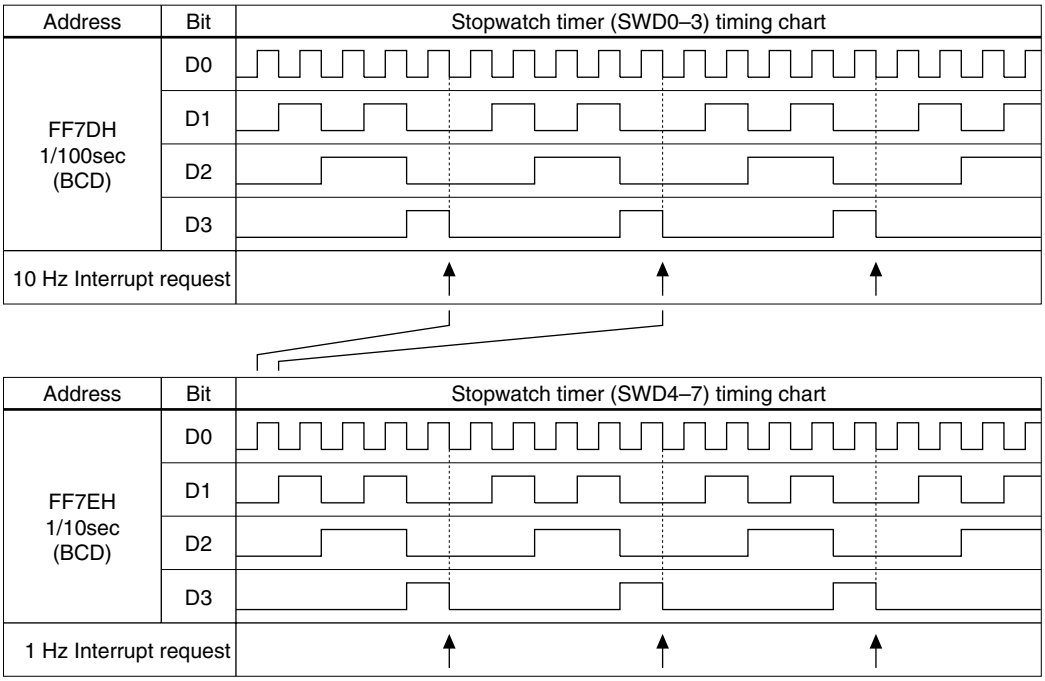


Fig. 4.9.3.1 Timing chart for stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWD0–SWD3 and SWD4–SWD7 (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW10 and ISW1) are set to "1".
The respective interrupts can be masked separately using the interrupt mask registers (EISW10 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

4.9.4 I/O memory of stopwatch timer

Table 4.9.4.1 shows the I/O addresses and the control bits for the stopwatch timer.

Table 4.9.4.1 Control bits of stopwatch timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF7CH	0	0	SWRST	SWRUN	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R		W	R/W	SWRST*3	Reset	Reset	Invalid	Stopwatch timer reset (writing)
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
FF7DH	SWD3	SWD2	SWD1	SWD0	SWD3	0			Stopwatch timer data BCD (1/100 sec)
	R				SWD2	0			
					SWD1	0			
					SWD0	0			
FF7EH	SWD7	SWD6	SWD5	SWD4	SWD7	0			Stopwatch timer data BCD (1/10 sec)
	R				SWD6	0			
					SWD5	0			
					SWD4	0			
FFE7H	GPR73	GPR72	EISW1	EISW10	GPR73	0	1	0	General-purpose register
	R/W				GPR72	0	1	0	General-purpose register
					EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
					EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SWD0–SWD7: Stopwatch timer data (FF7DH, FF7EH)

The 1/100 sec and the 1/10 sec data (BCD) can be read from SWD0–SWD3 and SWD4–SWD7, respectively. These eight bits are read only, and writing operations are invalid.
At initial reset, the timer data is initialized to "00H".

SWRST: Stopwatch timer reset (FF7CH•D1)

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

The stopwatch timer is reset by writing "1" to SWRST. All timer data is set to "0". When the stopwatch timer is reset in the RUN status, operation restarts immediately. Also, in the STOP status the reset data is maintained. No operation results when "0" is written to SWRST.
This bit is write-only, and so is always "0" at reading.

SWRUN: Stopwatch timer RUN/STOP control register (FF7CH•D0)

Controls RUN/STOP of the stopwatch timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The stopwatch timer enters the RUN status when "1" is written to the SWRUN register, and the STOP status when "0" is written.
In the STOP status, the timer data is maintained until the next RUN status or the timer is reset. Also, when the STOP status changes to the RUN status, the data that is maintained can be used for resuming the count.

When data of the counter is read at run mode, proper reading may not be obtained due to the carry from low-order digits (SWD0–SWD3) into high-order digits (SWD4–SWD7) (i.e., in case SWD0–SWD3 and SWD4–SWD7 reading span the timing of the carry). To avoid this occurrence, perform the reading after suspending the counter once and then set the SWRUN to "1" again.
Moreover, it is required that the suspension period not exceed 976 µsec (1/4 cycle of 256 Hz).
At initial reset, this register is set to "0".

EISW10: 10Hz interrupt mask register (FFE7H•D0)
EISW1: 1Hz interrupt mask register (FFE7H•D1)
These registers are used to select whether to mask the stopwatch timer interrupt.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

The interrupt mask registers (EISW10, EISW1) are used to select whether to mask the interrupt to the separate frequencies (10 Hz, 1 Hz).
At initial reset, these registers are set to "0".

ISW10: 10 Hz interrupt factor flag (FFF7H•D0)
ISW1: 1 Hz interrupt factor flag (FFF7H•D1)
These flags indicate the status of the stopwatch timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags ISW10 and ISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively. The software can judge from these flags whether there is a stopwatch timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the overflow of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.9.5 Programming notes

(1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µsec (1/4 cycle of 256 Hz).

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, this timer can not be used for the stopwatch function.

4.10 Programmable Timer

4.10.1 Configuration of programmable timer

The S1C63406 has two 8-bit programmable timer systems (timer 0 and timer 1) built-in.
Timer 0 and timer 1 are composed of 8-bit presettable down counters and they can be used as 8-bit × 2 channel programmable timers or a 16-bit × 1 channel programmable timer by software setting. Timer 0 also has an event counter function using the K03 terminal.
Figure 4.10.1.1 shows the configuration of the programmable timer.

The programmable timer is designed to count down from the initial value set in the counter with software. An underflow according to the initial value occurs by counting down and is used for the following functions:

- Presetting the initial value to the counter to generate the periodical underflow signal
- Generating an interrupt
- Generating a TOUT signal output from the R12 terminal
- Generating the synchronous clock source for the serial interface (timer 1 underflow is used, and it is possible to set the transfer rate)

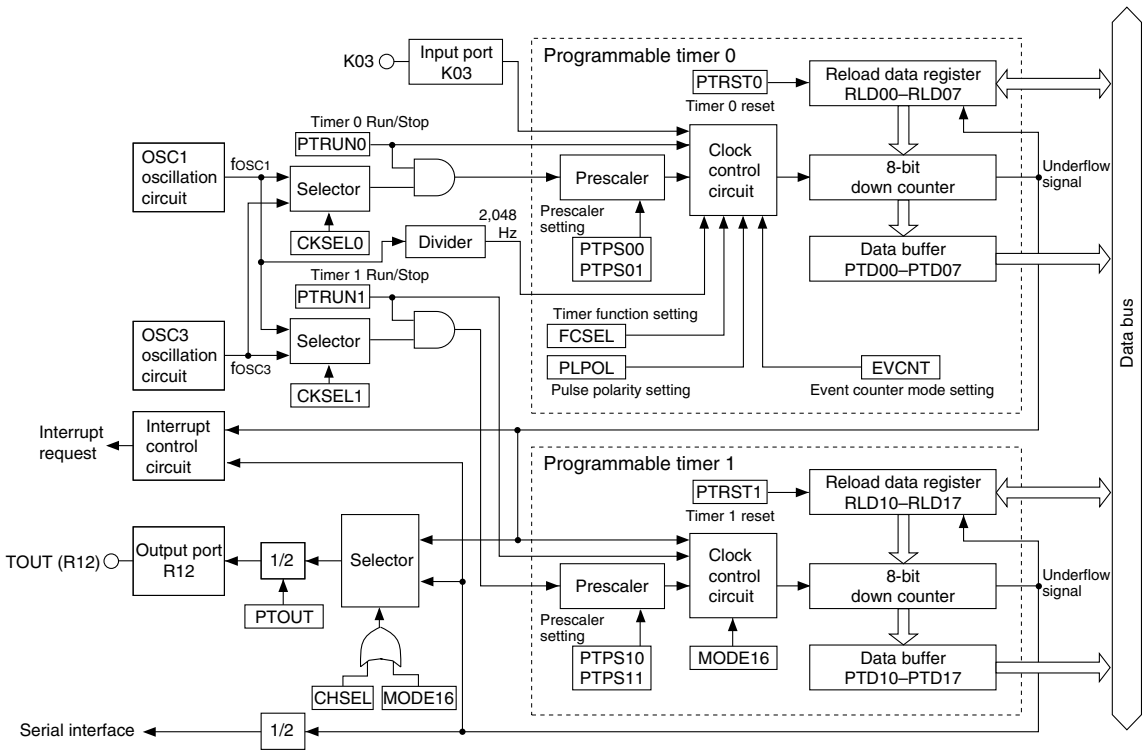


Fig. 4.10.1.1 Configuration of programmable timer

4.10.2 Tow separate 8-bit timer (MODE16 = "0") operation

4.10.2.1 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The registers PTRUN0 (timer 0) and PTRUN1 (timer 1) are provided to control the RUN / STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN / STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

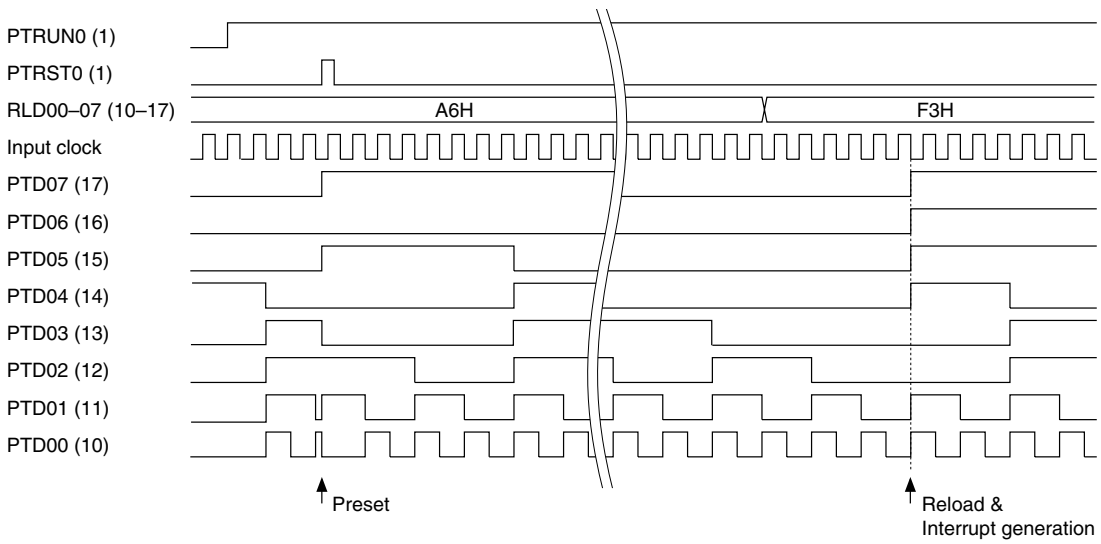


Fig. 4.10.2.1.1 Basic operation timing of down counter

4.10.2.2 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source. Timer 0 can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", timer 0 operates in the timer mode.
Timer 1 operates only in the timer mode.
At initial reset, this mode is set.

Refer to Section 4.10.2.1, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The timer 0 has an event counter function that counts an external clock input to the I/O port K03. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT. The timer 1 operates only in the timer mode, and cannot be used as an event counter.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.10.2.2.1.

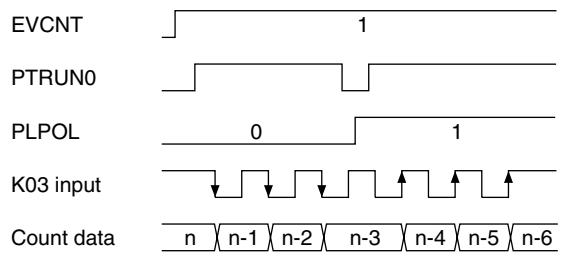


Fig. 4.10.2.2.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K03 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec or more to count reliably. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K03 terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
Figure 4.10.2.2.2 shows the count down timing with noise rejecter.

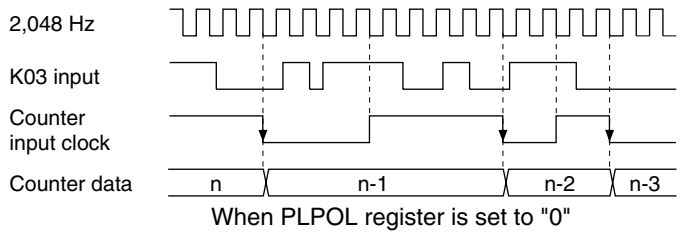


Fig. 4.10.2.2.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K03 input as the clock.
Refer to Section 4.10.2.1, "Setting of initial value and counting down" for basic operation and control.

4.10.2.3 Setting of input clock in timer mode

Timer 0 and timer 1 each include a prescaler. The prescalers generate the input clock for each timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit.
The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software for timer 0 and timer 1 individually.
The set input clock is used for the count clock during operation in the timer mode. When the timer 0 is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to each prescaler from either OSC1 or OSC3. This selection is done using the source clock selection registers CKSEL0 (timer 0) and CKSEL1 (timer 1); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of several msec to several 10 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for each prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00 / PTPS01 (timer 0) and PTPS10 / PTPS11 (timer 1).
Table 4.10.2.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.10.2.3.1 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0) or PTRUN1 (timer 1), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.10.2.4 Interrupt function

The programmable timer can generate an interrupt due to an underflow of the timer 0 and timer 1. See Figure 4.10.2.1.1 for the interrupt timing.

An underflow of timer 0 and timer 1 sets the corresponding interrupt factor flag IPT0 (timer 0) or IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT0 (timer 0) or EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.10.2.5 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of timer 0 or timer 1. The TOUT signal is generated by dividing the underflows in 1/2. It is possible to select which timer's underflow is to be used by the TOUT output channel selection register CHSEL. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected.
Figure 4.10.2.5.1 shows the TOUT signal waveform when the channel is changed.

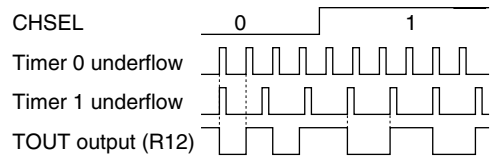


Fig. 4.10.2.5.1 TOUT signal waveform at channel change

The TOUT signal can be output from the R12 terminal. Programmable clocks can be supplied to external devices.
Figure 4.10.2.5.2 shows the configuration of the R12 port.

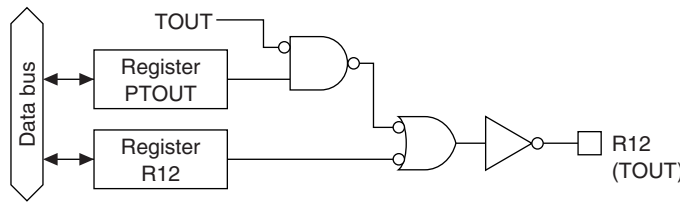


Fig. 4.10.2.5.2 Configuration of R12

The output of the TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R12 terminal and when "0" is written, the terminal goes high (V_{DD}) level. However, the data register R12 must always be "1".

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
Figure 4.10.2.5.3 shows the output waveform of the TOUT signal.

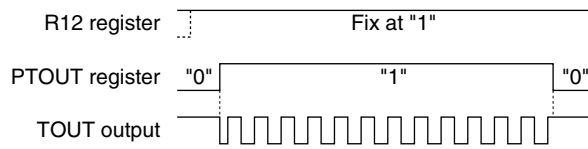


Fig. 4.10.2.5.3 Output waveform of the TOUT signal

4.10.2.6 Transfer rate setting for serial interface

The signal that is made from underflows of timer 1 by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting timer 1 into RUN state (PTRUN1 = "1"). It is not necessary to control with the PTOUT register.

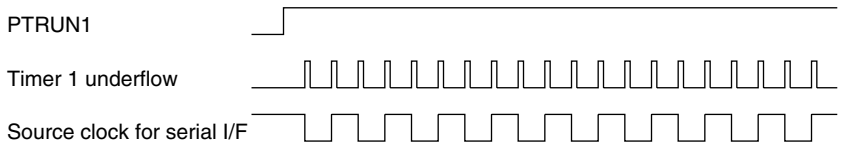


Fig. 4.10.2.6.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

RLD1X = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1
fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1X)

4.10.3 One channel × 16-bit timer (MODE16 = "1") operation

Timer 0 and timer 1 are chained together to form 16-bit down counter low byte in timer 0, high byte in timer 1.

4.10.3.1 Setting of initial value and counting down

Timers 0 and 1 each have a down counter and reload data register.

The reload data registers RLD00–RLD07 (timer 0) and RLD10–RLD17 (timer 1) are used to set the initial value to the down counter.
By writing "1" to the timer reset bit PTRST0 (timer 0) or PTRST1 (timer 1), the down counter loads the initial value set in the reload register RLD. Therefore, down-counting is executed from the stored initial value by the input clock.

The register PTRUN0 (timer 0) is used to control the RUN/STOP for timers 0 and 1. By writing "1" to the register after presetting the reload data to the down counter, the down counter starts counting down. Writing "0" stops the input count clock and the down counter stops counting. This control (RUN/STOP) does not affect the counter data. The counter maintains its data while stopped, and can restart counting continuing from that data.

The counter data can be read via the data buffers PTD00–PTD07 (timer 0) and PTD10–PTD17 (timer 1) in optional timing. However, the counter has the data hold function the same as the clock timer, that holds the high-order data when the low-order data is read in order to prevent the borrowing operation between low- and high-order reading, therefore be sure to read the low-order data first.

The counter reloads the initial value set in the reload data register RLD when an underflow occurs through the count down. It continues counting down from the initial value after reloading.
In addition to reloading the counter, this underflow signal controls the interrupt generation, pulse (TOUT signal) output and clock supplying to the serial interface.

4.10.3.2 Counter mode

The programmable timer can operate in two counter modes, timer mode and event counter mode. It can be selected by software.

(1) Timer mode

The timer mode counts down using the prescaler output as an input clock. In this mode, the programmable timer operates as a periodical timer using the OSC1 or OSC3 oscillation clock as a clock source. The programmable timer can operate in both the timer mode and the event counter mode. The mode can be switched using the timer 0 counter mode selection register EVCNT. When the EVCNT register is set to "0", the programmable timer operates in the timer mode.
At initial reset, this mode is set.

Refer to Section 4.10.3.1, "Setting of initial value and counting down" for basic operation and control.

The input clock in the timer mode is generated by the prescaler built into the programmable timer. The prescaler generates the input clock by dividing the OSC1 or OSC3 oscillation clock. Refer to the next section for setting the input clock.

(2) Event counter mode

The programmable timer has an event counter function that counts an external clock input to the I/O port K03. This function is selected by writing "1" to the timer 0 counter mode selection register EVCNT.

In the event counter mode, the clock is supplied to timer 0 from outside of the IC, therefore, the settings of the timer 0 prescaler division ratio selection registers PTPS00 and PTPS01 and the settings of the timer 0 source clock selection register CKSEL0 become invalid.

Count down timing can be selected from either the falling or rising edge of the input clock using the timer 0 pulse polarity selection register PLPOL. When "0" is written to the PLPOL register, the falling edge is selected, and when "1" is written, the rising edge is selected. The count down timing is shown in Figure 4.10.3.2.1.

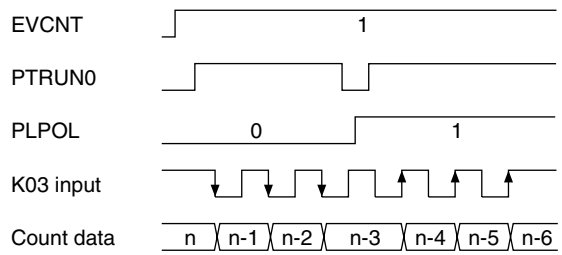


Fig. 4.10.3.2.1 Timing chart in event counter mode

The event counter mode also includes a noise reject function to eliminate noise such as chattering on the external clock (K03 input signal). This function is selected by writing "1" to the timer 0 function selection register FCSEL.
When "with noise rejector" is selected, an input pulse width for both low and high levels must be 0.98 msec or more to count reliably. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K03 terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
Figure 4.10.3.2.2 shows the count down timing with noise rejecter.

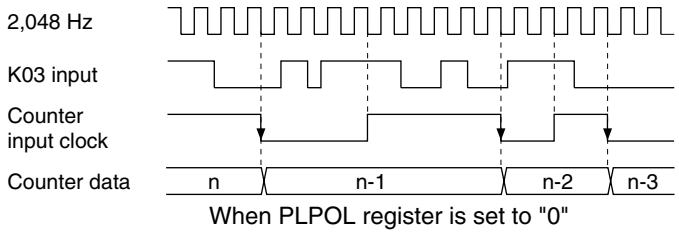


Fig. 4.10.3.2.2 Count down timing with noise rejecter

The operation of the event counter mode is the same as the timer mode except it uses the K03 input as the clock.
Refer to Section 4.10.3.1, "Setting of initial value and counting down" for basic operation and control.

4.10.3.3 Setting of input clock in timer mode

The 16 bit programmable timer include a prescaler. The prescalers generate the input clock for this programmable timer by dividing the source clock supplied from the OSC1 or OSC3 oscillation circuit. The source clock (OSC1 or OSC3) and the division ratio of the prescaler can be selected with software. The set input clock is used for the count clock during operation in the timer mode. When the 16 bit programmable timer is used in the event counter mode, the following settings become invalid.

The input clock is set in the following sequence.

(1) Selection of source clock

Select the source clock input to the prescaler from either OSC1 or OSC3. This selection is done using the source clock selection register CKSEL0 (timer 0); when "0" is written to the register, OSC1 is selected and when "1" is written, OSC3 is selected.
When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(2) Selection of prescaler division ratio

Select the division ratio for the prescaler from among 4 types. This selection is done using the prescaler division ratio selection registers PTPS00 / PTPS01 (timer 0). Table 4.10.3.3.1 shows the correspondence between the setting value and the division ratio.

Table 4.10.3.3.1 Selection of prescaler division ratio

PTPS01	PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

By writing "1" to the register PTRUN0 (timer 0), the prescaler inputs the source clock and outputs the clock divided by the selected division ratio. The counter starts counting down by inputting the clock.

4.10.3.4 Interrupt function

The programmable timer can generate an interrupt due to an underflow.

An underflow of this 16 bit programmable timer sets the corresponding interrupt factor flag IPT1 (timer 1) to "1", and generates an interrupt. The interrupt can also be masked by setting the corresponding interrupt mask register EIPT1 (timer 1). However, the interrupt factor flag is set to "1" by an underflow of the corresponding timer regardless of the interrupt mask register setting.

4.10.3.5 Setting of TOUT output

The programmable timer can generate a TOUT signal due to an underflow of this 16 bit programmable timer. The TOUT signal is generated by dividing the underflows in 1/2.

The TOUT signal can be output from the R12 terminal. Programmable clocks can be supplied to external devices.
Figure 4.10.3.5.1 shows the configuration of the R12 port.

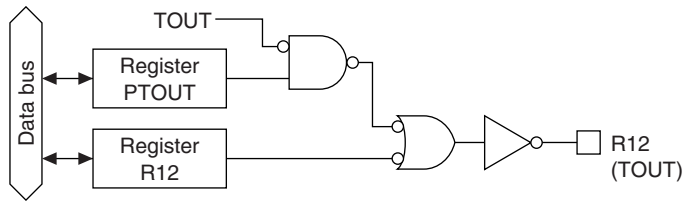


Fig. 4.10.3.5.1 Configuration of R12

The output of a TOUT signal is controlled by the PTOUT register. When "1" is written to the PTOUT register, the TOUT signal is output from the R12 terminal and when "0" is written, the terminal goes high (V_{DD}) level. However, the data register R12 must always be "1".

Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.
Figure 4.10.3.5.2 shows the output waveform of the TOUT signal.

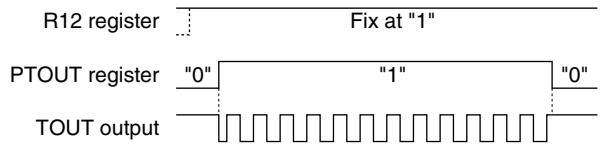


Fig. 4.10.3.5.2 Output waveform of the TOUT signal

4.10.3.6 Transfer rate setting for serial interface

The signal that is made from underflows of the 16 bit programmable timer by dividing them in 1/2, can be used as the clock source for the serial interface.
The programmable timer outputs the clock to the serial interface by setting this 16 bit programmable timer into RUN state (PTRUN0 = "1"). It is not necessary to control with the PTOUT register.

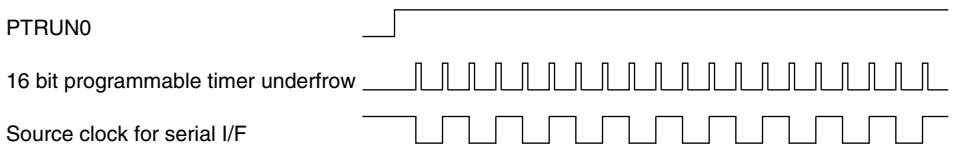


Fig. 4.10.3.6.1 Synchronous clock of serial interface

A setting value for the RLD1X register according to a transfer rate is calculated by the following expression:

RLD1X, RLD0X = fosc / (2 ∗ bps ∗ division ratio of the prescaler) - 1

fosc: Oscillation frequency (OSC1/OSC3)
bps: Transfer rate
(00H can be set to RLD1X)

4.10.4 I/O memory of programmable timer

Table 4.10.4.1 shows the I/O addresses and the control bits for the programmable timer.

Table 4.10.4.1 Control bits of programmable timer

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FFC0H	MODE16	EVCNT	FCSEL	PLPOL	MODEL16	0	16 bit × 1	8 bit × 2	8 bit × 2 or 16 bit × 1 timer mode selection
					EVCNT	0	Event ct.	Timer	Timer 0 counter mode selection
					FCSEL	0	With NR	No NR	Timer 0 function selection (for event counter mode)
	R/W				PLPOL	0	↑	↓	Timer 0 pulse polarity selection (for event counter mode)
FFC1H	CHSEL	PTOUT	CKSEL1	CKSEL0	CHSEL	0	Timer1	Timer0	TOUT output channel selection
					PTOUT	0	On	Off	TOUT output control
					CKSEL1	0	OSC3	OSC1	Prescaler 1 source clock selection
	R/W				CKSEL0	0	OSC3	OSC1	Prescaler 0 source clock selection
FFC2H	PTPS01	PTPS00	PTRST0	PTRUN0	PTPS01	0			Prescaler 0 division ratio selection [PTPS01, 00]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS00	0			
	R/W		W	R/W	PTRST0*3	– *2	Reset	Invalid	Timer 0 reset (reload)
					PTRUN0	0	Run	Stop	Timer 0 Run/Stop
FFC3H	PTPS11	PTPS10	PTRST1	PTRUN1	PTPS11	0			Prescaler 1 division ratio selection [PTPS11, 10]: 0 = 1/1, 1 = 1/4, 2 = 1/32, 3 = 1/256
					PTPS10	0			
	R/W		W	R/W	PTRST1*3	– *2	Reset	Invalid	Timer 1 reset (reload)
					PTRUN1	0	Run	Stop	Timer 1 Run/Stop
FFC4H	RLD03	RLD02	RLD01	RLD00	RLD03	0			MSB
					RLD02	0			Programmable timer 0 reload data (low-order 4 bits)
					RLD01	0			
	R/W				RLD00	0			LSB
FFC5H	RLD07	RLD06	RLD05	RLD04	RLD07	0			MSB
					RLD06	0			Programmable timer 0 reload data (high-order 4 bits)
					RLD05	0			
	R/W				RLD04	0			LSB
FFC6H	RLD13	RLD12	RLD11	RLD10	RLD13	0			MSB
					RLD12	0			Programmable timer 1 reload data (low-order 4 bits)
					RLD11	0			
	R/W				RLD10	0			LSB
FFC7H	RLD17	RLD16	RLD15	RLD14	RLD17	0			MSB
					RLD16	0			Programmable timer 1 reload data (high-order 4 bits)
					RLD15	0			
	R/W				RLD14	0			LSB
FFC8H	PTD03	PTD02	PTD01	PTD00	PTD03	0			MSB
					PTD02	0			Programmable timer 0 data (low-order 4 bits)
					PTD01	0			
	R				PTD00	0			LSB
FFC9H	PTD07	PTD06	PTD05	PTD04	PTD07	0			MSB
					PTD06	0			Programmable timer 0 data (high-order 4 bits)
					PTD05	0			
	R				PTD04	0			LSB
FFCAH	PTD13	PTD12	PTD11	PTD10	PTD13	0			MSB
					PTD12	0			Programmable timer 1 data (low-order 4 bits)
					PTD11	0			
	R				PTD10	0			LSB
FFCBH	PTD17	PTD16	PTD15	PTD14	PTD17	0			MSB
					PTD16	0			Programmable timer 1 data (high-order 4 bits)
					PTD15	0			
	R				PTD14	0			LSB
FFE2H	GPR23	GPR22	EIPT1	EIPT0	GPR23	0	1	0	General-purpose register
					GPR22	0	1	0	General-purpose register
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
	R/W				EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)

*1 Initial value at initial reset *2 Not set in the circuit *3 Constantly "0" when being read

CKSEL0: Prescaler 0 source clock selection register (FFC1H•D0)
CKSEL1: Prescaler 1 source clock selection register (FFC1H•D1)
Selects the source clock of the prescaler.

When "1" is written: OSC3 clock
When "0" is written: OSC1 clock
Reading: Valid

The source clock for the prescaler is selected from OSC1 or OSC3. When "0" is written to the CKSEL0 register, the OSC1 clock is selected as the input clock for the prescaler 0 (for timer 0) and when "1" is written, the OSC3 clock is selected.
Same as above, the source clock for prescaler 1 is selected by the CKSEL1 register.
When the event counter mode is selected to timer 0, the setting of the CKSEL0 register becomes invalid.
At initial reset, these registers are set to "0".

PTPS00, PTPS01: Timer 0 prescaler division ratio selection register (FFC2H•D2, D3)
PTPS10, PTPS11: Timer 1 prescaler division ratio selection register (FFC3H•D2, D3)
Selects the division ratio of the prescaler.
Two bits of PTPS00 and PTPS01 are the prescaler division ratio selection register for timer 0, and two bits of PTPS10 and PTPS11 are for timer 1. The prescaler division ratios that can be set by these registers are shown in Table 4.10.4.2.

Table 4.10.4.2 Selection of prescaler division ratio

PTPS11 PTPS01	PTPS10 PTPS00	Prescaler division ratio
1	1	Source clock / 256
1	0	Source clock / 32
0	1	Source clock / 4
0	0	Source clock / 1

When the event counter mode is selected to timer 0, the setting of the PTPS00 and PTPS01 becomes invalid.
At initial reset, these registers are set to "0".

EVCNT: Timer 0 counter mode selection register (FFC0H•D2)
Selects a counter mode for timer 0.

When "1" is written: Event counter mode
When "0" is written: Timer mode
Reading: Valid

The counter mode for timer 0 is selected from either the event counter mode or timer mode. When "1" is written to the EVCNT register, the event counter mode is selected and when "0" is written, the timer mode is selected.
At initial reset, this register is set to "0".

MODE16: 8-bit × 2 or 16-bit × 1 timer mode selection register (FFC0H•D3)
Selects 8-bit × 2 channels mode (timer 0 and timer 1) or 16-bit × 1 channel mode.

When "1" is written: 16-bit × 1 channel
When "0" is written: 8-bit × 2 channels (timer 0 and timer 1)
Reading: Valid

When 8-bit × 2 channels is selected, timer 0 and timer 1 can be used independently.
When 16-bit × 1 channel is selected, timer 0 and timer 1 are chained together and are used as a 16-bit programmable timer. The clock is input to timer 0 and interrupts will be generated from timer 1.
At initial reset, this register is set to "0".

FCSEL: Timer 0 function selection register (FFC0H•D1)

Selects whether the noise rejector of the clock input circuit will be used or not in the event counter mode.

When "1" is written: With noise rejecter
When "0" is written: Without noise rejecter
Reading: Valid

When "1" is written to the FCSEL register, the noise rejecter is used and counting is done by an external clock (K03) with 0.98 msec or more pulse width. (The noise rejecter allows the counter to input the clock at the second falling edge of the internal 2,048 Hz signal after changing the input level of the K03 terminal. Consequently, the pulse width of noise that can reliably be rejected is 0.48 msec or less.)
When "0" is written to the FCSEL register, the noise rejector is not used and the counting is done directly by an external clock input to the K03 terminal.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

PLPOL: Timer 0 pulse polarity selection register (FFC0H•D0)

Selects the count pulse polarity in the event counter mode.

When "1" is written: Rising edge
When "0" is written: Falling edge
Reading: Valid

The count timing in the event counter mode (timer 0) is selected from either the falling edge of the external clock input to the K03 terminal or the rising edge. When "0" is written to the PLPOL register, the falling edge is selected and when "1" is written, the rising edge is selected.
Setting of this register is effective only when timer 0 is used in the event counter mode.
At initial reset, this register is set to "0".

RLD00–RLD07: Timer 0 reload data register (FFC4H, FFC5H)
RLD10–RLD17: Timer 1 reload data register (FFC6H, FFC7H)

Sets the initial value for the counter.
The reload data written in this register is loaded to the respective counters. The counter counts down using the data as the initial value for counting.
Reload data is loaded to the counter when the counter is reset by writing "1" to the PTRST0 or PTRST1 register, or when counter underflow occurs.
At initial reset, these registers are set to "00H".

PTD00–PTD07: Timer 0 counter data (FFC8H, FFC9H)
PTD10–PTD17: Timer 1 counter data (FFCAH, FFCBH)

Count data in the programmable timer can be read from these latches.
The low-order 4 bits of the count data in timer 0 can be read from PTD00–PTD03, and the high-order data can be read from PTD04–PTD07. Similarly, for timer 1, the low-order 4 bits can be read from PTD10–PTD13, and the high-order data can be read from PTD14–PTD17.
Since the high-order 4 bits are held by reading the low-order 4 bits, be sure to read the low-order 4 bits first.
Since these latches are exclusively for reading, the writing operation is invalid.
At initial reset, these counter data are set to "00H".

PTRST0: Timer 0 reset (reload) (FFC2H•D1)
PTRST1: Timer 1 reset (reload) (FFC3H•D1)
Resets the timer and presets reload data to the counter.

When "1" is written: Reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" to PTRST0, the reload data in the reload register PLD00–PLD07 is preset to the counter in timer 0. Similarly, the reload data in PLD10–PLD17 is preset to the counter in timer 1 by PTRST1.
When the counter is preset in the RUN status, the counter restarts immediately after presetting. In the case of STOP status, the reload data is preset to the counter and is maintained.
No operation results when "0" is written.
Since these bits are exclusively for writing, always set to "0" during reading.

PTRUN0: Timer 0 RUN/STOP control register (FFC2H•D0)
PTRUN1: Timer 1 RUN/STOP control register (FFC3H•D0)
Controls the RUN / STOP of the counter.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

The counter in timer 0 starts counting down by writing "1" to the PTRUN0 register and stops by writing "0".
In STOP status, the counter data is maintained until the counter is reset or is set in the next RUN status. When STOP status changes to RUN status, the data that has been maintained can be used for resuming the count.
Same as above, the timer 1 counter is controlled by the PTRUN1 register.
At initial reset, these registers are set to "0".

CHSEL: TOUT output channel selection register (FFC1H•D3)
Selects the channel used for TOUT signal output.

When "1" is written: Timer 1
When "0" is written: Timer 0
Reading: Valid

This register selects which timer's underflow (timer 0 or timer 1) is used to generate a TOUT signal. When "0" is written to the CHSEL register, timer 0 is selected and when "1" is written, timer 1 is selected. In the 16-bit × 2 channels mode (MODE16 = "1"), timer 1 is always selected regardless of this register setting.
At initial reset, this register is set to "0".

PTOUT: TOUT output control register (FFC1H•D2)
Turns TOUT signal output ON and OFF.

When "1" is written: ON
When "0" is written: OFF
Reading: Valid

PTOUT is the output control register for the TOUT signal. When "1" is written to the register, the TOUT signal is output from the R12 terminal and when "0" is written, the terminal goes high (V_{DD}) level. However, the data register R12 must always be "1".
At initial reset, this register is set to "0".

EIPT0: Timer 0 interrupt mask register (FFE2H•D0)
EIPT1: Timer 1 interrupt mask register (FFE2H•D1)

These registers are used to select whether to mask the programmable timer interrupt or not.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Timer 0 and timer 1 interrupts can be masked individually by the interrupt mask registers EIPT0 (timer 0) and EIPT1 (timer 1).
At initial reset, these registers are set to "0".

IPT0: Timer 0 interrupt factor flag (FFF2H•D0)
IPT1: Timer 1 interrupt factor flag (FFF2H•D1)

These flags indicate the status of the programmable timer interrupt.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

The interrupt factor flags IPT0 and IPT1 correspond to timer 0 and timer 1 interrupts, respectively. The software can judge from these flags whether there is a programmable timer interrupt. However, even if the interrupt is masked, the flags are set to "1" by the underflows of the corresponding counters.
These flags are reset to "0" by writing "1" to them.
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.10.5 Programming notes

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).
For the 16 bit × 1 mode, be sure to read as following sequence:
(PTD00–PTD03) → (PTD04–PTD07) → (PTD10–PTD13) → (PTD14–PTD17)
The read sequence time should be within 1.46 msec.

(2) The programmable timer actually enters RUN / STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0 / PTRUN1 register. Consequently, when "0" is written to the PTRUN0 / PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0 / PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 4.10.5.1 shows the timing chart for the RUN / STOP control.

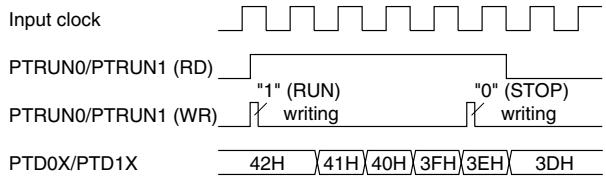


Fig. 4.10.5.1 Timing chart for RUN/STOP control

It is the same even in the event counter mode. Therefore, be aware that the counter does not enter RUN / STOP status if a clock is not input after setting the RUN / STOP control register (PTRUN0).

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1/2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time interval of at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit.
At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(5) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(6) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

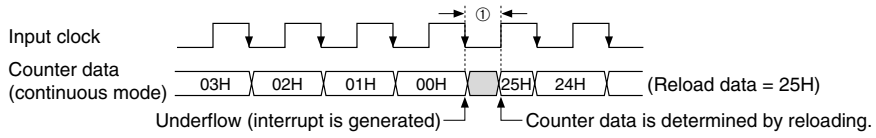


Fig. 4.10.5.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with OSC3 (high-speed clock).

4.11 Serial Interface

4.11.1 Configuration of serial interface

The S1C63406 incorporates a full duplex serial interface (when asynchronous system is selected) that allows the user to select either clock synchronous system or asynchronous system.
The data transfer method can be selected in software.
When the clock synchronous system is selected, 8-bit data transfer is possible.
When the asynchronous system is selected, either 7-bit or 8-bit data transfer is possible, and a parity check of received data and the addition of a parity bit for transmitting data can automatically be done by selecting in software.
Figure 4.11.1.1 shows the configuration of the serial interface.

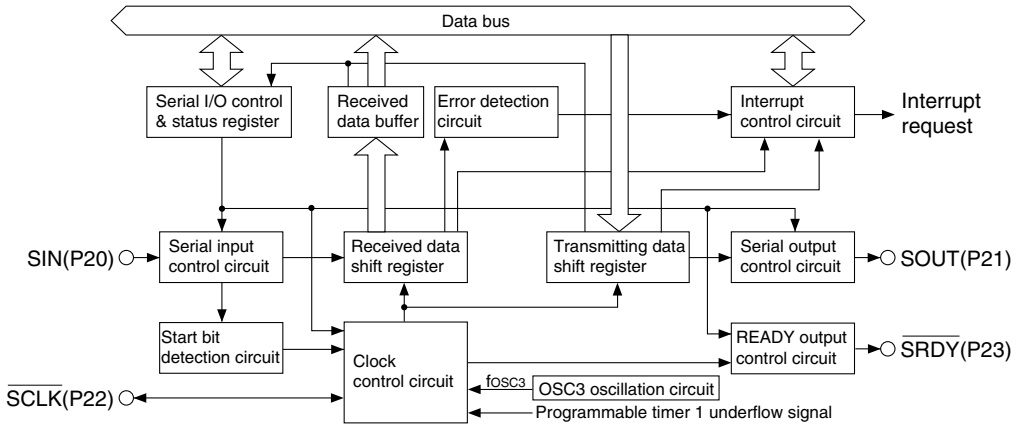


Fig. 4.11.1.1 Configuration of serial interface

Serial interface input/output terminals, SIN, SOUT, $\overline{SCLK}$ and $\overline{SRDY}$ are shared with the I/O ports P20–P23. In order to utilize these terminals for the serial interface input/output terminals, proper settings have to be made with registers ESIF, SMD0 and SMD1. (At initial reset, these terminals are set as I/O port terminals.)
The direction of I/O port terminals set for serial interface input/output terminals are determined by the signal and transfer mode for each terminal. Furthermore, the settings for the corresponding I/O control registers for the I/O ports become invalid.

Table 4.11.1.1 Configuration of input/output terminals

Terminal	When serial interface is selected
P20	SIN
P21	SOUT
P22	$\overline{SCLK}$
P23	$\overline{SRDY}$

* The terminals used may change according to the transfer mode.

SIN and SOUT are serial data input and output terminals which function identically in clock synchronous system and asynchronous system. $\overline{SCLK}$ is exclusively for use with clock synchronous system and functions as a synchronous clock input/output terminal. $\overline{SRDY}$ is exclusively for use in clock synchronous slave mode and functions as a send-receive ready signal output terminal.
When asynchronous system is selected, since $\overline{SCLK}$ and $\overline{SRDY}$ are superfluous, the I/O port terminals P22 and P23 can be used as I/O ports.
In the same way, when clock synchronous master mode is selected, since $\overline{SRDY}$ is superfluous, the I/O port terminal P23 can be used as I/O port.

4.11.2 Mask option

Since the input / output terminals of the serial interface is shared with the I / O ports (P20–P23), the mask option that selects the output specification for the I / O port is also applied to the serial interface.
The output specification of the terminals SOUT, $\overline{\text{SCLK}}$ (for clock synchronous master mode) and $\overline{\text{SRDY}}$ (for clock synchronous slave mode) that are used as output in the input / output port of the serial interface is respectively selected by the mask options of P21, P22 and P23. Either complementary output or N-channel open drain output can be selected as the output specification. However, when N-channel open drain output is selected, do not apply a voltage exceeding the power supply voltage to the terminal.

4.11.3 Transfer modes

There are four transfer modes for the serial interface and mode selection is made by setting the two bits of the mode selection registers SMD0 and SMD1 as shown in the table below.

Table 4.11.3.1 Transfer modes

SMD1	SMD0	Mode
1	1	8-bit asynchronous
1	0	7-bit asynchronous
0	1	Clock synchronous slave
0	0	Clock synchronous master

Table 4.11.3.2 Terminal settings corresponding to each transfer mode

Mode	SIN	SOUT	$\overline{\text{SCLK}}$	$\overline{\text{SRDY}}$
Asynchronous 8-bit	Input	Output	P22	P23
Asynchronous 7-bit	Input	Output	P22	P23
Clock synchronous slave	Input	Output	Input	Output
Clock synchronous master	Input	Output	Output	P23

At initial reset, transfer mode is set to clock synchronous master mode.

Clock synchronous master mode

In this mode, the internal clock is utilized as a synchronous clock for the built-in shift registers, and 8-bit clock synchronous serial transfers can be performed with this serial interface as the master.
The synchronous clock is also output from the $\overline{\text{SCLK}}$ terminal which enables control of the external (slave side) serial I / O device. Since the $\overline{\text{SRDY}}$ terminal is not utilized in this mode, it can be used as an I / O port.
Figure 4.11.3.1(a) shows the connection example of input / output terminals in the clock synchronous master mode.

Clock synchronous slave mode

In this mode, a synchronous clock from the external (master side) serial input / output device is utilized and 8-bit clock synchronous serial transfers can be performed with this serial interface as the slave.
The synchronous clock is input to the $\overline{\text{SCLK}}$ terminal and is utilized by this interface as the synchronous clock.
Furthermore, the $\overline{\text{SRDY}}$ signal indicating the transmit-receive ready status is output from the $\overline{\text{SRDY}}$ terminal in accordance with the serial interface operating status.
In the slave mode, the settings for registers SCS0 and SCS1 used to select the clock source are invalid.
Figure 4.11.3.1(b) shows the connection example of input / output terminals in the clock synchronous slave mode.

7-bit asynchronous mode

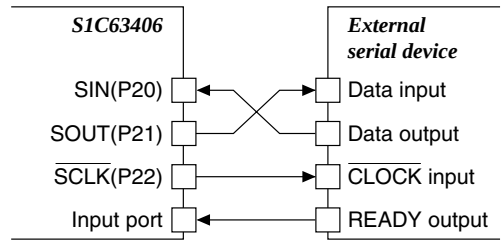
In this mode, 7-bit asynchronous transfer can be performed. Parity check during data reception and addition of parity bit (odd / even / none) during transmitting can be specified and data processed in 7 bits with or without parity. Since this mode employs the internal clock, the $\overline{\text{SCLK}}$ terminal is not used. Furthermore, since the $\overline{\text{SRDY}}$ terminal is not utilized either, both of these terminals can be used as I / O ports.

Figure 4.11.3.1(c) shows the connection example of input / output terminals in the asynchronous mode.

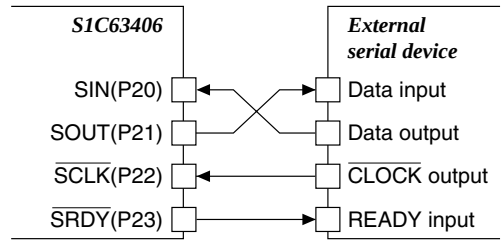
8-bit asynchronous 8-bit mode

In this mode, 8-bit asynchronous transfer can be performed. Parity check during data reception and addition of parity bit (odd / even / none) during transmitting can be specified and data processed in 8 bits with or without parity. Since this mode employs the internal clock, the $\overline{\text{SCLK}}$ terminal is not used. Furthermore, since the $\overline{\text{SRDY}}$ terminal is not utilized either, both of these terminals can be used as I / O ports.

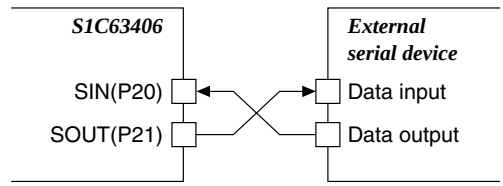
Figure 4.11.3.1(c) shows the connection example of input / output terminals in the asynchronous mode.



(a) Clock synchronous master mode



(b) Clock synchronous slave mode



(c) Asynchronous 7-bit/8-bit mode

Fig. 4.11.3.1 Connection examples of serial interface I/O terminals

4.11.4 Clock source

There are four clock sources and selection is made by setting the two bits of the clock source selection register SCS0 and SCS1 as shown in table below.

Table 4.11.4.1 Clock source

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	fOSC3 / 93
0	1	fOSC3 / 372
0	0	fOSC3 / 186

This register setting is invalid in clock synchronous slave mode and the external clock input from the $\overline{SCLK}$ terminal is used.
When the "programmable timer" is selected, the programmable timer 1 underflow signal is divided by 1/2 and this signal used as the clock source. With respect to the transfer rate setting, see "4.10 Programmable Timer". At initial reset, the synchronous clock is set to "fOSC3 / 186".

Whichever clock is selected, the signal is further divided by 1/16 and then used as the synchronous clock. Furthermore, external clock input is used as is for $\overline{SCLK}$ in clock synchronous slave mode.

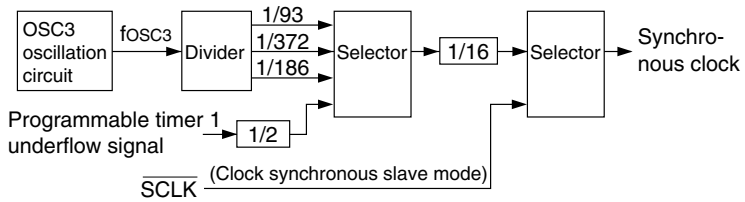


Fig. 4.11.4.1 Division of the synchronous clock

Table 4.11.4.2 shows an examples of transfer rates and OSC3 oscillation frequencies when the clock source is set to programmable timer.

Table 4.11.4.2 OSC3 oscillation frequencies and transfer rates

Transfer rate	fOSC3 = 3.580 MHz	
(bps)	PSC1X	RLD1X
19,200	0 (1/1)	05H
9,600	0 (1/1)	0BH
4,800	0 (1/1)	16H
2,400	0 (1/1)	2EH
1,200	0 (1/1)	5CH
600	0 (1/1)	B9H
300	1 (1/4)	5CH
150	1 (1/4)	B9H

When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of several msec to several 10 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Characteristics".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

4.11.5 Transmit-receive control

Below is a description of the registers which handle transmit-receive control. With respect to transmit-receive control procedures and operations, please refer to the following sections in which these are discussed on a mode by mode basis.

Shift register and receive data buffer

Exclusive shift registers for transmitting and receiving are installed in this serial interface. Consequently, duplex communication simultaneous transmit and receive is possible when the asynchronous system is selected.

Data being transmitted are written to TRXD0–TRXD7 and converted to serial through the shift register and is output from the SOUT terminal.

In the reception section, a receive data buffer is installed separate from the shift register.
Data being received are input to the SIN terminal and is converted to parallel through the shift register and written to the receive data buffer.
Since the receive data buffer can be read even during serial input operation, the continuous data is received efficiently.
However, since buffer functions are not used in clock synchronous mode, be sure to read out data before the next data reception begins.

Transmit enable register and transmit control bit

For transmit control, use the transmit enable register TXEN and transmit control bit TXTRG.

The transmit enable register TXEN is used to set the transmit enable / disable status. When "1" is written to this register to set the transmitting enable status, clock input to the shift register is enabled and the system is ready to transmit data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.

The transmit control bit TXTRG is used as the trigger to start transmitting data.
Data to be transmitted is written to the transmit data shift register, and when transmitting preparations a recomplete, "1" is written to TXTRG whereupon data transmitting begins.
When interrupt has been enabled, an interrupt is generated when the transmission is completed. If there is subsequent data to be transmitted it can be sent using this interrupt.
In addition, TXTRG can be read as a status bit. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
For details on timing, see the timing chart which gives the timing for each mode.

When not transmitting, set TXEN to "0" to disable transmition.

Receive enable register, receive control bit

For receiving control, use the receive enable register RXEN and receive control bit RXTRG.
Receive enable register RXEN is used to set receiving enable / disable status. When "1" is written into this register to set the receiving enable status, clock input to the shift register is enabled and the system is ready to receive data. In the clock synchronous mode, synchronous clock input / output from the $\overline{\text{SCLK}}$ terminal is also enabled.
With the above setting, receiving begins and serial data input from the SIN terminal goes to the shift register.
The operation of the receive control bit RXTRG is slightly different depending on whether a clock synchronous system or an asynchronous system is being used.
In the clock synchronous system, the receive control bit TXTRG is used as the trigger to start receiving data.
When received data has been read and the preparation for next data receiving is completed, write "1" into RXTRG to start receiving. (When "1" is written to RXTRG in slave mode, $\overline{\text{SRDY}}$ switches to "0".)

In an asynchronous system, RXTRG is used to prepare for next data receiving. After reading the received data from the receive data buffer, write "1" into RXTRG to signify that the receive data buffer is empty. If "1" is not written into RXTRG, the overrun error flag OER will be set to "1" when the next receiving operation is completed. (An overrun error will be generated when receiving is completed between reading the received data and the writing of "1" to RXTRG.)
In addition, RXTRG can be read as a status bit. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
For details on timing, see the timing chart which gives the timing for each mode.

When you do not receive, set RXEN to "0" to disable receiving.

4.11.6 Operation of clock synchronous transfer

Clock synchronous transfer involves the transfer of 8-bit data by synchronizing it to eight clocks. The same synchronous clock is used by both the transmitting and receiving sides.
When the serial interface is used in the master mode, the clock signal selected using SCS0 and SCS1 is further divided by 1/16 and employed as the synchronous clock. This signal is then sent via the $\overline{\text{SCLK}}$ terminal to the slave side (external serial I/O device).
When used in the slave mode, the clock input to the $\overline{\text{SCLK}}$ terminal from the master side (external serial input/output device) is used as the synchronous clock.

In the clock synchronous mode, since one clock line ($\overline{\text{SCLK}}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)

Transfer data is fixed at 8 bits and both transmitting and receiving are conducted with the LSB (bit 0) coming first.

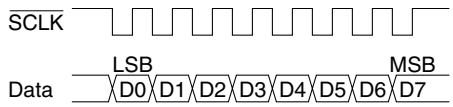


Fig. 4.11.6.1 Transfer data configuration using clock synchronous mode

Below is a description of initialization when performing clock synchronous transfer, transmit-receive control procedures and operations.
With respect to serial interface interrupt, see "4.11.8 Interrupt function".

Initialization of serial interface

When performing clock synchronous transfer, the following initial settings must be made.

(1) Setting of transmitting/receiving disable

To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection

Because serial interface input/output ports SIN, SOUT, $\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ are set as I/O port terminals P20–P23 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use.

(3) Setting of transfer mode

Select the clock synchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

Master mode: SMD0 = "0", SMD1 = "0"
Slave mode: SMD0 = "1", SMD1 = "0"

(4) Clock source selection

In the master mode, select the synchronous clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 4.11.4.1.)
This selection is not necessary in the slave mode.

The parity enable register EPR is also assigned to this address, however, since parity is not necessary in the clock synchronous mode, parity check will not take place regardless of how they are set.

(5) Clock source control

When the master mode is selected and programmable timer for the clock source is selected, set transfer rate on the programmable timer side. (See "4.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "4.3 Oscillation Circuit".)
Note that the frequency of the serial interface clock is limited to a maximum of 2 MHz.

Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN and the receive enable register RXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7.

(4) In case of the master mode, confirm the receive ready status on the slave side (external serial input / output device), if necessary. Wait until it reaches the receive ready status.

(5) Write "1" in the transmit control bit TXTRG and start transmitting.

In the master mode, this control causes the synchronous clock to change to enable and to be provided to the shift register for transmitting and output from the $\overline{\text{SCLK}}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{\text{SCLK}}$ terminal.
The transmitting data of the shift register shifts one bit at a time at each falling edge of the synchronous clock and is output from the SOUT terminal. When the final bit (MSB) is output, the SOUT terminal is maintained at that level, until the next transmitting begins.

The transmitting complete interrupt factor flag ISTR is set to "1" at the point where the data transmitting of the shift register is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

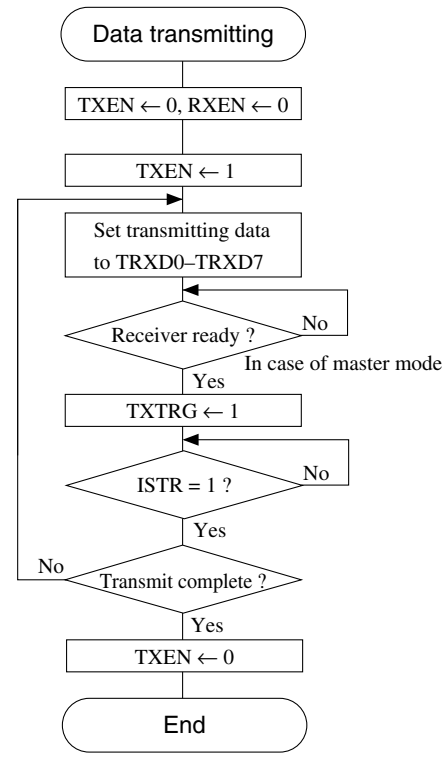


Fig. 4.11.6.2 Transmit procedure in clock synchronous mode

Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN and transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) In case of the master mode, confirm the transmit ready status on the slave side (external serial input/output device), if necessary. Wait until it reaches the transmit ready status.

(4) Write "1" in the receive control bit RXTRG and start receiving.

In the master mode, this control causes the synchronous clock to change to enable and is provided to the shift register for receiving and output from the $\overline{SCLK}$ terminal.
In the slave mode, it waits for the synchronous clock to be input from the $\overline{SCLK}$ terminal. The received data input from the SIN terminal is successively incorporated into the shift register in synchronization with the rising edge of the synchronous clock.
At the point where the data of the 8th bit has been incorporated at the final (8th) rising edge of the synchronous clock, the content of the shift register is sent to the receive data buffer and the receiving complete interrupt factor flag ISRC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point.

(5) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

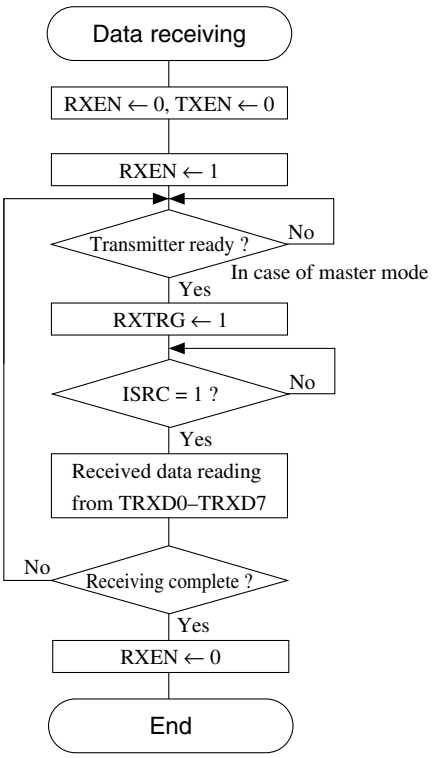


Fig. 4.11.6.3 Receiving procedure in clock synchronous mode

Transmit/receive ready ($\overline{SRDY}$) signal

When this serial interface is used in the clock synchronous slave mode (external clock input), an $\overline{SRDY}$ signal is output to indicate whether or not this serial interface can transmit/receive to the master side (external serial input/output device). This signal is output from the $\overline{SRDY}$ terminal and when this interface enters the transmit or receive enable (READY) status, it becomes "0" (Low level) and becomes "1" (High level) when there is a BUSY status, such as during transmit/receive operation.
The $\overline{SRDY}$ signal changes the "1" to "0," immediately after writing "1" into the transmit control bit TXTRG or the receive control bit RXTRG and returns from "0" to "1", at the point where the first synchronous clock has been input (falling edge).
When you have set in the master mode, control the transfer by inputting the same signal from the slave side using the input port or I/O port. At this time, since the $\overline{SRDY}$ terminal is not set and instead P23 functions as the I/O port, you can apply this port for said control.

Timing chart

The timing chart for the clock synchronous system transmission is shown in Figure 4.11.6.4.

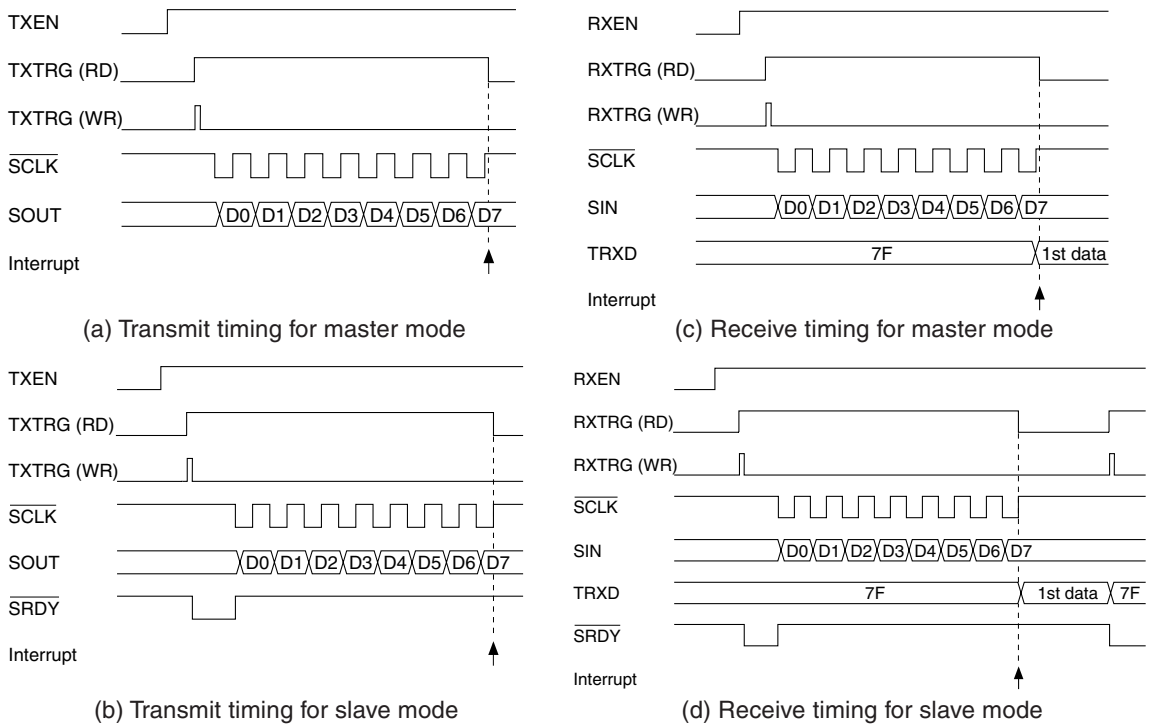


Fig. 4.11.6.4 Timing chart (clock synchronous system transmission)

4.11.7 Operation of asynchronous transfer

Asynchronous transfer is a mode that transfers by adding a start bit and a stop bit to the front and the back of each piece of serial converted data. In this mode, there is no need to use a clock that is fully synchronized clock on the transmit side and the receive side, but rather transmission is done while adopting the synchronization at the start / stop bits that have attached before and after each piece of data. The RS-232C interface functions can be easily realized by selecting this transfer mode.
This interface has separate transmit and receive shift registers and is designed to permit full duplex transmission to be done simultaneously for transmitting and receiving.

For transfer data in the 7-bit asynchronous mode, either 7 bits data (no parity) or 7 bits data + parity bit can be selected. In the 8-bit asynchronous mode, either 8 bits data (no parity) or 8 bits data + parity bit can be selected.
Parity can be even or odd, and parity checking of received data and adding a party bit to transmitting data will be done automatically. Thereafter, it is not necessary to be conscious of parity itself in the program.
The start bit and stop bit are respectively fixed at one bit and data is transmitted and received by placing the LSB (bit 0) at the front.

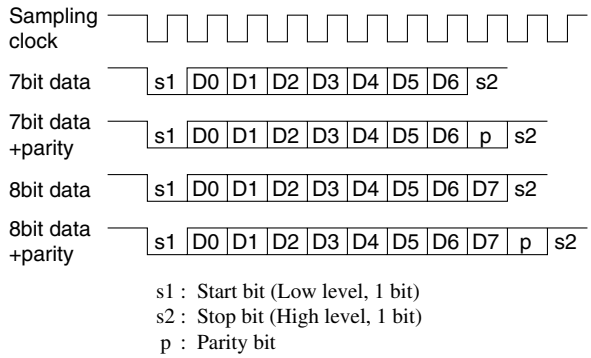


Fig. 4.11.7.1 Transfer data configuration for asynchronous system

Here following, we will explain the control sequence and operation for initialization and transmitting / receiving in case of asynchronous data transfer. See "4.11.8 Interrupt function" for the serial interface interrupts.

Initialization of serial interface

The below initialization must be done in cases of asynchronous system transfer.

(1) Setting of transmitting/receiving disable

To set the serial interface into a status in which both transmitting and receiving are disabled, "0" must be written to both the transmit enable register TXEN and the receive enable register RXEN. Fix these two registers to a disable status until data transfer actually begins.

(2) Port selection

Because serial interface input / output terminals SIN and SOUT are set as I / O port terminals P20 and P21 at initial reset, "1" must be written to the serial interface enable register ESIF in order to set these terminals for serial interface use.
$\overline{\text{SCLK}}$ and $\overline{\text{SRDY}}$ terminals set in the clock synchronous mode are not used in the asynchronous mode. These terminals function as I / O port terminals P22 and P23.

(3) Setting of transfer mode

Select the asynchronous mode by writing the data as indicated below to the two bits of the mode selection registers SMD0 and SMD1.

7-bit mode: SMD0 = "0", SMD1 = "1"
8-bit mode: SMD0 = "1", SMD1 = "1"

(4) Parity bit selection

When checking and adding parity bits, write "1" into the parity enable register EPR to set to "with parity check". As a result of this setting, in the 7-bit asynchronous mode, it has a 7 bits data + parity bit configuration and in the 8-bit asynchronous mode it has an 8 bits data + parity bit configuration.In this case, parity checking for receiving and adding a party bit for transmitting is done automatically in hardware. Moreover, when "with parity check" has been selected, "odd" or "even" parity must be further selected in the parity mode selection register PMD.
When "0" is written to the PMD register to select "without parity check" in the 7-bit asynchronous mode, data configuration is set to 7 bits data (no parity) and in the 8-bit asynchronous mode (no parity) it is set to 8 bits data (no parity) and parity checking and parity bit adding will not be done.

(5) Clock source selection

Select the clock source by writing data to the two bits of the clock source selection registers SCS0 and SCS1. (See Table 4.11.4.1.)

(6) Clock source control

When the programmable timer is selected for the clock source, set transfer rate on the programmable timer side. (See "4.10 Programmable Timer".)
When the divided signal of OSC3 oscillation circuit is selected for the clock source, be sure that the OSC3 oscillation circuit is turned ON prior to commencing data transfer. (See "4.3 Oscillation Circuit".)

Data transmit procedure

The control procedure and operation during transmitting is as follows.

(1) Write "0" in the transmit enable register TXEN to reset the serial interface.

(2) Write "1" in the transmit enable register TXEN to set into the transmitting enable status.

(3) Write the transmitting data into TRXD0–TRXD7.
Also, when 7-bit data is selected, the TRXD7 data becomes invalid.

(4) Write "1" in the transmit control bit TXTRG and start transmitting.
This control causes the shift clock to change to enable and a start bit (LOW) is output to the SOUT terminal in synchronize to its rising edge. The transmitting data set to the shift register is shifted one bit at a time at each rising edge of the clock thereafter and is output from the SOUT terminal. After the data output, it outputs a stop bit (HIGH) and HIGH level is maintained until the next start bit is output.

The transmitting complete interrupt factor flag ISTR is set to "1" at the point where the data transmitting is completed. When interrupt has been enabled, a transmitting complete interrupt is generated at this point.
Set the following transmitting data using this interrupt.

(5) Repeat steps (3) to (4) for the number of bytes of transmitting data, and then set the transmit disable status by writing "0" to the transmit enable register TXEN, when the transmitting is completed.

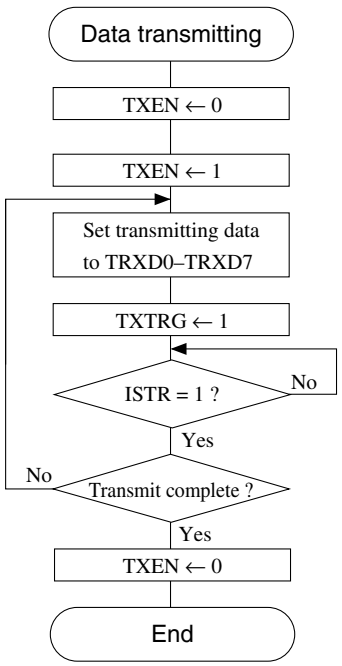


Fig. 4.11.7.2 Transmit procedure in asynchronous mode

Data receive procedure

The control procedure and operation during receiving is as follows.

(1) Write "0" in the receive enable register RXEN to set the receiving disable status and to reset the respective PER, OER, FER flags that indicate parity, overrun and framing errors.

(2) Write "1" in the receive enable register RXEN to set into the receiving enable status.

(3) The shift clock will change to enable from the point where the start bit (LOW) has been input from the SIN terminal and the receive data will be synchronized to the rising edge following the second clock, and will thus be successively incorporated into the shift register.
After data bits have been incorporated, the stop bit is checked and, if it is not HIGH, it becomes a framing error and the error interrupt factor flag ISER is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
When receiving is completed, data in the shift register is transferred to the receive data buffer and the receiving complete interrupt flag ISRC is set to "1". When interrupt has been enabled, a receiving complete interrupt is generated at this point. (When an overrun error is generated, the interrupt factor flag ISRC is not set to "1" and a receiving complete interrupt is not generated.)
If "with parity check" has been selected, a parity check is executed when data is transferred into the receive data buffer from the shift register and if a parity error is detected, the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error mentioned above.

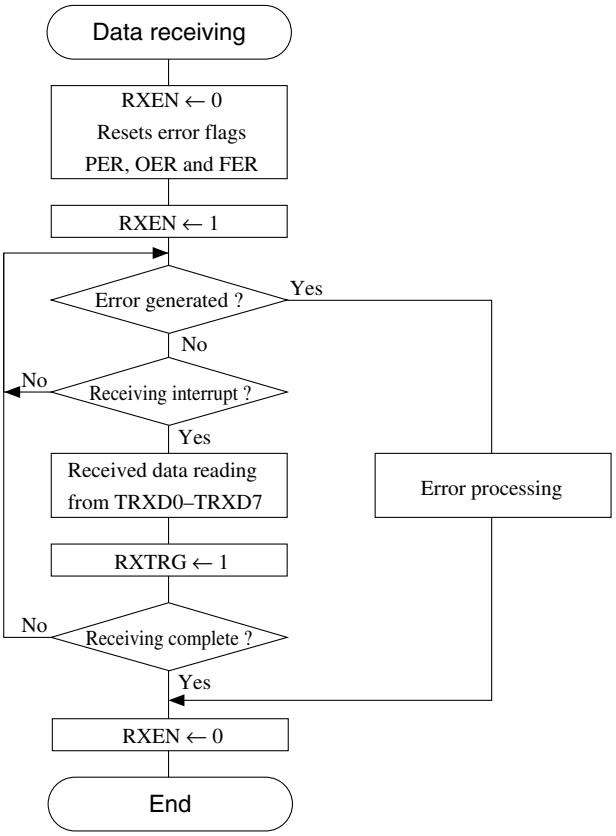


Fig. 4.11.7.3 Receiving procedure in asynchronous mode

(4) Read the received data from TRXD0–TRXD7 using receiving complete interrupt.

(5) Write "1" to the receive control bit RXTRG to inform that the receive data has been read out.
When the following data is received prior to writing "1" to RXTRG, it is recognized as an overrun error and the error interrupt factor flag is set to "1". When the interrupt has been enabled, an error interrupt is generated at this point just as in the framing error and parity error mentioned above.

(6) Repeat steps (3) to (5) for the number of bytes of receiving data, and then set the receive disable status by writing "0" to the receive enable register RXEN, when the receiving is completed.

Receive error

During receiving the following three types of errors can be detected by an interrupt.

(1) Parity error

When writing "1" to the EPR register to select "with parity check", a parity check (vertical parity check) is executed during receiving. After each data bit is sent a parity check bit is sent. The parity check bit is a "0" or a "1". Even parity checking will cause the sum of the parity bit and the other bits to be even. Odd parity causes the sum to be odd. This is checked on the receiving side.
The parity check is performed when data received in the shift register is transferred to the receive data buffer. It checks whether the parity check bit is a "1" or a "0" (the sum of the bits including the parity bit) and the parity set in the PMD register match. When it does not match, it is recognized as an parity error and the parity error flag PER and the error interrupt factor flag ISER is set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
The PER flag is reset to "0" by writing "1".
Even when this error has been generated, the received data corresponding to the error is transferred in the receive data buffer and the receive operation also continues.
The received data at this point cannot assured because of the parity error.

(2) Framing error

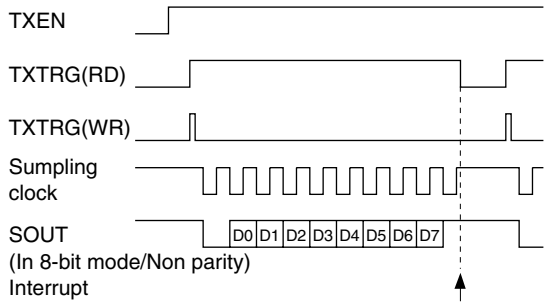
In asynchronous transfer, synchronization is adopted for each character at the start bit ("0") and the stop bit ("1"). When receiving has been done with the stop bit set at "0", the serial interface judges the synchronization to be off and a framing error is generated. When this error is generated, the framing error flag FER and the error interrupt factor flag ISER are set to "1". When interrupt has been enabled, an error interrupt is generated at this point.
The FER flag is reset to "0" by writing "1".
Even when this error has been generated, the received data for it is loaded into the receive data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receipt, such data cannot be assured.
Even when this error has been generated, the received data corresponding to the error is transferred in the receive data buffer and the receive operation also continues. However, even when it does not become a framing error with the following data receiving, such data cannot be assured.

(3) Overrun error

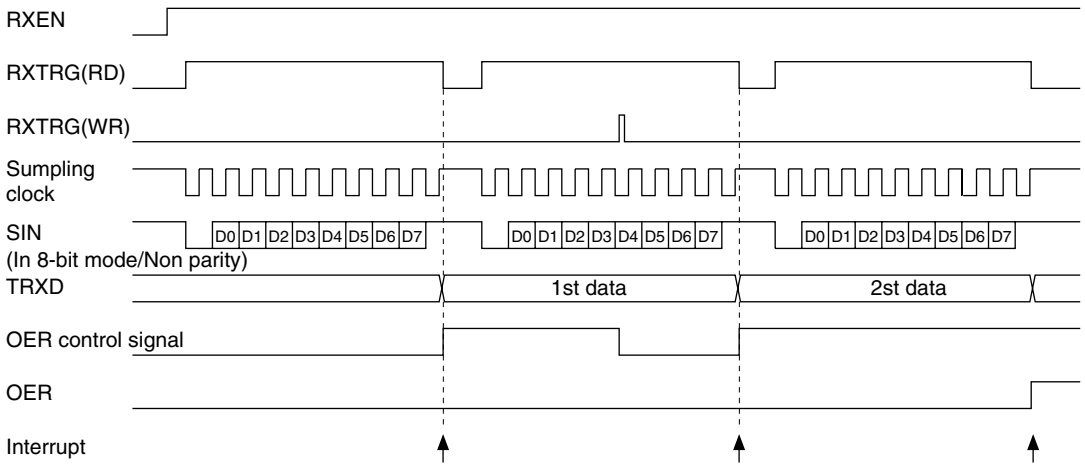
When the next data is received before "1" is written to RXTRG, an overrun error will be generated, because the previous receive data will be overwritten. When this error is generated, the overrun error flag OER and the error interrupt factor flag ISER are set to "1". When interrupt has been enabled, an error interrupt is generated at this point. The OER flag is reset to "0" by writing "1" into it.
Even when this error has been generated, the received data corresponding to the error is transferred in the receive data buffer and the receive operation also continues.
Furthermore, when the timing for writing "1" to RXTRG and the timing for the received data transfer to the receive data buffer overlap, it will be recognized as an overrun error.

Timing chart

Figure 4.11.7.4 show the asynchronous transfer timing chart.



(a) Transmit timing



(b) Receive timing

Fig. 4.11.7.4 Timing chart (asynchronous transfer)

4.11.8 Interrupt function

This serial interface includes a function that generates the below indicated three types of interrupts.

- Transmitting complete interrupt
- Receiving complete interrupt
- Error interrupt

The interrupt factor flag ISxx and the interrupt mask register EISxx for the respective interrupt factors are provided and then the interrupt can be disabled / enabled by the software.
Figure 4.11.8.1 shows the configuration of the serial interface interrupt circuit.

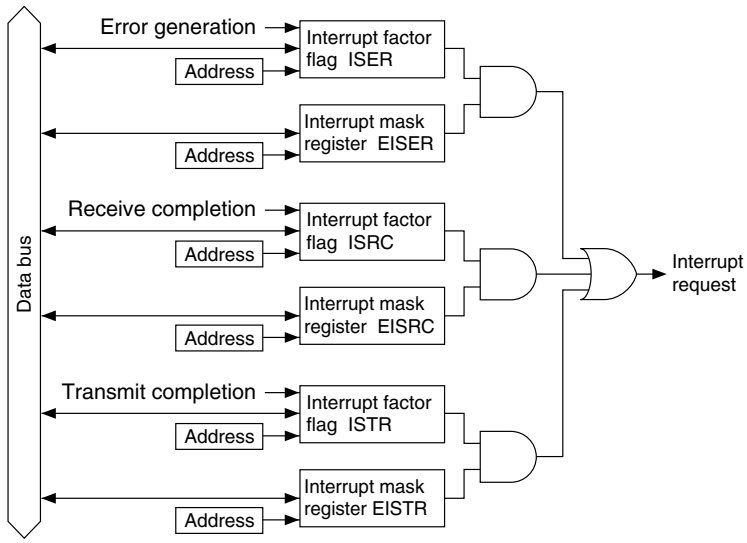


Fig. 4.11.8.1 Configuration of serial interface interrupt circuit

Transmit completion interrupt

This interrupt factor is generated at the point where the sending of the data written into the shift register has been completed and sets the interrupt factor flag ISTR to "1". When set in this manner, if the corresponding interrupt mask register EISTR is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
When the interrupt mask register EISTR has been set to "0" and interrupt has been disabled, no interrupt is generated to the CPU. Even in this case, the interrupt factor flag ISTR is set to "1".
The interrupt factor flag ISTR is reset to "0" by writing "1".
The following transmitting data can be set and the transmitting can be started (writing "1" to TXTRG) after this interrupt factor occurs.

Receive completion interrupt

This interrupt factor is generated at the point where receiving has been completed and the receive data incorporated into the shift register has been transferred into the receive data buffer and it sets the interrupt factor flag ISRC to "1". When set in this manner, if the corresponding interrupt mask register EISRC is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
When the interrupt mask register EISRC has been set to "0" and interrupt has been disabled, no interrupt is generated to the CPU. Even in this case, the interrupt factor flag ISRC is set to "1".
The interrupt factor flag ISRC is reset to "0" by writing "1".
The generation of this interrupt factor allows reading of the received data.
Also, the interrupt factor flag ISRC is set to "1" when a parity error or framing error is generated.

Error interrupt

This interrupt factor is generated at the point where a parity error, framing error or overrun error is detected during receiving and it sets the interrupt factor flag ISER to "1". When set in this manner, if the corresponding interrupt mask register EISER is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
When the interrupt mask register EISER has been set to "0" and interrupt has been disabled, an interrupt is not generated to the CPU. Even in this case, the interrupt factor flag ISER is set to "1".
The interrupt factor flag ISER is reset to "0" by writing "1".
Since all three types of errors result in the same interrupt factor, you should identify the error that has been generated by the error flags PER (parity error), OER (overrun error) and FER (framing error).

4.11.9 I/O memory of serial interface

Table 4.11.9.1 show the serial interface control bits and their addresses.

Table 4.11.9.1 Serial interface control bits

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF49H	PPL23	PPL22	PPL21	PPL20	PPL23	1	On	Off	P23 pull-up control register General-purpose register when SIF (clock sync. slave) is selected
					PPL22	1	On	Off	P22 pull-up control register General-purpose register when SIF (clock sync. master) is selected
									$\overline{SCLK}$ (I) pull-up control register when SIF (clock sync. slave) is selected
	R/W				PPL21	1	On	Off	P21 pull-up control register (ESIF=0) General-purpose register when SIF is selected
					PPL20	1	On	Off	P20 pull-up control register (ESIF=0) SIN pull-up control register when SIF is selected
FF70H	0	SMD1	SMD0	ESIF	0 *3	– *2			Unused
					SMD1	0			Serial I/F mode selection [SMD1, 0]: 0 = Mode Clk-sync. master; 1 = Clk-sync. slave; 2 = Mode Async. 7-bit; 3 = Mode Async. 8-bit
					SMD0	0			
	R	R/W			ESIF	0	SIF	I/O	Serial I/F enable (P2x port function selection)
FF71H	EPR	PMD	SCS1	SCS0	EPR	0	Enable	Disable	Parity enable register
					PMD	0	Odd	Even	Parity mode selection
	R/W				SCS1	0			Clock source selection [SCS1, 0]: 0 = 1200bps; 1 = 600bps; 2 = 2400bps; 3 = PT
					SCS0	0			
FF72H	RXTRG	RXEN	TXTRG	TXEN	RXTRG	0	Run	Stop	Serial I/F receive status (reading)
							Trigger	–	Serial I/F receive trigger (writing)
					RXEN	0	Enable	Disable	Serial I/F receive enable
					TXTRG	0	Run	Stop	Serial I/F transmit status (reading)
	R/W						Trigger	–	Serial I/F transmit trigger (writing)
					TXEN	0	Enable	Disable	Serial I/F transmit enable
FF73H	0	FER	PER	OER	0 *3	– *2			Unused
					FER	0	Error	No error	Framing error flag status (reading)
							Reset	–	Framing error flag reset (writing)
					PER	0	Error	No error	Parity error flag status (reading)
	R	R/W					Reset	–	Parity error flag reset (writing)
					OER	0	Error	No error	Overrun error flag status (reading)
							Reset	–	Overrun error flag reset (writing)
FF74H	TRXD3	TRXD2	TRXD1	TRXD0	TRXD3	– *2	High	Low	Serial I/F transmit/receive data (low-order 4 bits)
					TRXD2	– *2	High	Low	
					TRXD1	– *2	High	Low	
	R/W				TRXD0	– *2	High	Low	LSB
FF75H	TRXD7	TRXD6	TRXD5	TRXD4	TRXD7	– *2	High	Low	MSB
					TRXD6	– *2	High	Low	Serial I/F transmit/receive data (high-order 4 bits)
					TRXD5	– *2	High	Low	
	R/W				TRXD4	– *2	High	Low	
FFE3H	GPR33	EISER	EISTR	EISRC	GPR33	0	1	0	General-purpose register
					EISER	0	Enable	Mask	Interrupt mask register (Serial I/F error)
					EISTR	0	Enable	Mask	Interrupt mask register (Serial I/F transmit completion)
	R/W				EISRC	0	Enable	Mask	Interrupt mask register (Serial I/F receive completion)
FFF3H	0	ISER	ISTR	ISRC	0 *3	– *2	(R)	(R)	Unused
					ISER	0	Yes	No	Interrupt factor flag (Serial I/F error)
	R	R/W			ISTR	0	(W)	(W)	Interrupt factor flag (Serial I/F transmit completion)
					ISRC	0	Reset	Invalid	Interrupt factor flag (Serial I/F receive completion)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

ESIF: Serial interface enable register (P2 port function selection) (FF70H•D0)

Sets P20–P23 to the input/output port for the serial interface.

When "1" is written: Serial interface
When "0" is written: I/O port
Reading: Valid

The ESIF is the serial interface enable register and P20–P23 terminals become serial input/output terminals (SIN, SOUT, $\overline{\text{SCLK}}$, $\overline{\text{SRDY}}$) when "1" is written, and they become I/O port terminals when "0" is written.
Also, see Table 4.11.3.2 for the terminal settings according to the transfer modes.
At initial reset, this register is set to "0".

PPL20: SIN pull-up control register (FF49H•D0)
PPL22: $\overline{\text{SCLK}}$ pull-up control register (FF49H•D2)

Sets the pull-up of the SIN terminal and the $\overline{\text{SCLK}}$ terminals (in the slave mode).

When "1" is written: Pull-up ON
When "0" is written: Pull-up OFF
Reading: Valid

Sets the pull-up resistor built into the SIN (P20) and $\overline{\text{SCLK}}$ (P22) terminals to ON or OFF.
$\overline{\text{SCLK}}$ pull-up is effective only in the slave mode. In the master mode, the PPL22 register can be used as a general purpose register.
At initial reset, these registers are set to "1" and the lines are pulled up.

SMD0, SMD1: Serial interface mode selection register (FF70H•D1, D2)

Set the transfer modes as shown in Table 4.11.9.2.

Table 4.11.9.2 Transfer mode settings

SMD1	SMD0	Mode
1	1	8-bit asynchronous
1	0	7-bit asynchronous
0	1	Clock synchronous slave
0	0	Clock synchronous master

SMD0 and SMD1 can also read out.
At initial reset, this register is set to "0".

SCS0, SCS1: Clock source selection register (FF71H•D0, D1)

Select the clock source as shown in Table 4.11.9.3.

Table 4.11.9.3 Clock source selection

SCS1	SCS0	Clock source
1	1	Programmable timer
1	0	f_{OSC3} / 93
0	1	f_{OSC3} / 372
0	0	f_{OSC3} / 186

SCS0 and SCS1 can also be read out.
In the clock synchronous slave mode, setting of this register is invalid.
At initial reset, this register is set to "0".

EPR: Parity enable register (FF71H•D3)

Selects the parity function.

When "1" is written: With parity
When "0" is written: Non parity
Reading: Valid

Selects whether or not to check parity of the received data and to add a parity bit to the transmitting data. When "1" is written to EPR, the most significant bit of the received data is considered to be the parity bit and a parity check is executed. A parity bit is added to the transmitting data. When "0" is written, neither checking is done nor is a parity bit added.
Parity is valid only in asynchronous mode and the EPR setting becomes invalid in the clock synchronous mode.
At initial reset, this register is set to "0".

PMD: Parity mode selection register (FF71H•D2)

Selects odd parity / even parity.

When "1" is written: Odd parity
When "0" is written: Even parity
Reading: Valid

When "1" is written to PMD, odd parity is selected and even parity is selected when "0" is written. The parity check and addition of a parity bit is only valid when "1" has been written to EPR. When "0" has been written to EPR, the parity setting by PMD becomes invalid.
At initial reset, this register is set to "0".

TXEN: Transmit enable register (FF72H•D0)

Sets the serial interface to the transmit enabled status.

When "1" is written: Transmit enabled
When "0" is written: Transmit disabled
Reading: Valid

When "1" is written to TXEN, the serial interface shifts to the transmit enabled status and shifts to the transmit disabled status when "0" is written.
Set TXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, this register is set to "0".

TXTRG: Transmit trigger/status (FF72H•D1)

Functions as the transmit start trigger and the operation status indicator (transmitting / stop status).

When "1" is read: During transmitting
When "0" is read: During stop

When "1" is written: Start transmitting
When "0" is written: Invalid

Starts transmitting when "1" is written to TXTRG after writing the transmitting data.
TXTRG can be read as the status. When set to "1", it indicates transmitting operation, and "0" indicates transmitting stop.
At initial reset, TXTRG is set to "0".

RXEN: Receive enable register (FF72H•D2)

Sets the serial interface to the receive enabled status.

When "1" is written: Receive enabled
When "0" is written: Receive disabled
Reading: Valid

When "1" is written to RXEN, the serial interface shifts to the receive enabled status and shifts to the receive disabled status when "0" is written.
Set RXEN to "0" when making the initial settings of the serial interface and similar operations.
At initial reset, this register is set to "0".

RXTRG: Receive trigger/status (FF72H•D3)

Functions as the receive start trigger or preparation for the following data receiving and the operation status indicator (during receiving / during stop).

When "1" is read: During receiving
When "0" is read: During stop

When "1" is written: Start receiving / following data receiving preparation
When "0" is written: Invalid

RXTRG has a slightly different operation in the clock synchronous system and the asynchronous system.

The RXTRG in the clock synchronous system is used as the trigger for starting receive operation.
Write "1" into RXTRG to start receiving at the point where the receive data has been read and the following receive preparation has been done. (In the slave mode, $\overline{\text{SRDY}}$ becomes "0" at the point where "1" has been written into into the RXTRG.)

In the asynchronous system, RXTRG is used for preparation of the following data receiving. Read the received data located in the receive data buffer and write "1" into RXTRG to inform that the receive data buffer has shifted to empty. When "1" has not been written to RXTRG, the overrun error flag OER is set to "1" at the point where the following receiving has been completed. (When the receiving has been completed between the operation to read the received data and the operation to write "1" into RXTRG, an overrun error occurs.)

In addition, RXTRG can be read as the status. In either clock synchronous mode or asynchronous mode, when RXTRG is set to "1", it indicates receiving operation and when set to "0", it indicates that receiving has stopped.
At initial reset, RXTRG is set to "0".

TRXD0–TRXD7: Transmit/receive data (FF74H, FF75H)

During transmitting

Transmitting data is set.

When "1" is written: High level
When "0" is written: Low level

Write the transmitting data prior to starting transmition.
In the case of continuous transmitting, wait for the transmit completion interrupt, then write the data.
The TRXD7 becomes invalid for the 7-bit asynchronous mode.
Converted serial data for which the bits set at "1" as High (V_{DD}) level and for which the bits set at "0" as Low (V_{SS}) level are output from the SOUT terminal.

During receiving

The received data is stored.

When "1" is read: High level
When "0" is read: Low level

The data from the receive data buffer can be read out.
Since the sift register is provided separately from this buffer, reading can be done during a receive operation in the asynchronous mode. (The buffer function is not used in the clock synchronous mode.)

Read the data after waiting for a receive completion interrupt.
When performing parity check in the 7-bit asynchronous mode, "0" is loaded into the 8th bit (TRXD7) that corresponds to the parity bit.
The serial data input from the SIN terminal is level converted, making the High (V_{DD}) level bit "1" and the Low (V_{SS}) level bit "0" and is then loaded into this buffer.
At initial reset, the buffer content is undefined.

OER: Overrun error flag (FF73H•D0)

Indicates the generation of an overrun error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

OER is an error flag that indicates the generation of an overrun error and becomes "1" when an error has been generated.
An overrun error is generated when a receiving of data has completed prior to writing "1" to RXTRG in the asynchronous mode.
OER is reset to "0" by writing "1".
OER is set to "0" at initial reset or when RXEN is set to "0".

PER: Parity error flag (FF73H•D1)

Indicates the generation of a parity error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

PER is an error flag that indicates the generation of a parity error and becomes "1" when an error has been generated.
When a parity check is performed in the asynchronous mode, a parity error will be generated if data that does not match the parity is received.
PER is reset to "0" by writing "1".
PER is set to "0" at initial reset or when RXEN is set to "0".

FER: Framing error flag (FF73H•D2)

Indicates the generation of a framing error.

When "1" is read: Error
When "0" is read: No error

When "1" is written: Reset to "0"
When "0" is written: Invalid

FER is an error flag that indicates the generation of a framing error and becomes "1" when an error has been generated.
When the stop bit for the receiving in the asynchronous mode has become "0", a framing error is generated.
FER is reset to "0" by writing "1".
FER is set to "0" at initial reset or when RXEN is set to "0".

EISRC, EISTR, EISER: Interrupt mask registers (FFE3H•D0, D1, D2)

Enables or disables the generation of an interrupt for the CPU.

When "1" is written: Enabled
When "0" is written: Disabled
Reading: Valid

EISRC, EISTR and EISER are interrupt mask registers that respectively correspond to the interrupt factors for receivie completion, transmit completion and receive error. Interrupts set to "1" are enabled and interrupts set to "0" are disabled.
At initial reset, these registers are set to "0".

ISRC, ISTR, ISER: Interrupt factor flags (FFF3H•D0, D1, D2)

Indicates the serial interface interrupt generation status.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred

When "1" is written: Flag is reset
When "0" is written: Invalid

ISRC, ISTR and ISER are interrupt factor flags that respectively correspond to the interrupts for receivie completion, transmit completion and receive error, and are set to "1" by generation of each factor.
Transmit completion interrupt factor is generated at the point where the data transmition of the shift register has been completed.
Receive completion interrupt factor is generated at the point where the received data has been transferred into the receive data buffer.
Receive error interrupt factor is generated when a parity error, framing error or overrun error has been detected during data receiving.
When set in this manner, if the corresponding interrupt enable mask is set to "1" and the CPU is set to interrupt enabled status (I flag = "1"), an interrupt will be generated to the CPU.
Regardless of the interrupt mask register setting, the interrupt factor flag will be set to "1" by the occurrence of an interrupt generation condition.
The interrupt factor flag is reset to "0" by writing "1".
After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.
At initial reset, these flags are set to "0".

4.11.10 Programming notes

(1) Be sure to initialize the serial interface mode in the transmit / receive disabled status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)
Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISER is set to "1" prior to the receive completion interrupt factor flag ISRC for the time indicated in Table 4.11.10.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag ISRC to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag ISRC is not set to "1" and a receiving complete interrupt is not generated.

Table 4.11.10.1 Time difference between ISER and ISRC on error generation

Clock source	Time difference
f_{OSC3} / n	1/2 cycles of f_{OSC3} / n
Programmable timer	1 cycle of timer 1 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Chracteristics".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

(6) Be aware that the maximum clock frequency for the serial interface is limited to 2 MHz.

(7) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.12 SVD (Supply Voltage Detection) Circuit

4.12.1 Configuration of SVD circuit

The S1C63406 has a built-in SVD (supply voltage detection) circuit, so that the software can find when the source voltage lowers.
Turning the SVD circuit ON / OFF and the SVD criteria voltage setting can be done with software.
Figure 4.12.1.1 shows the configuration of the SVD circuit.

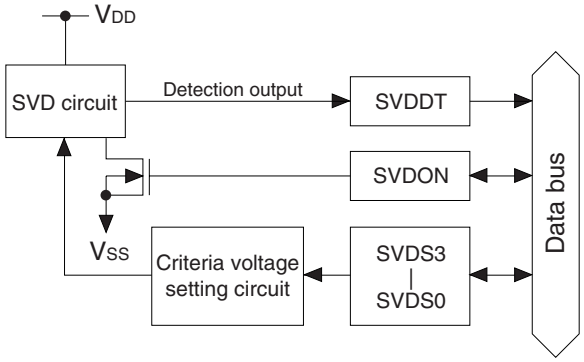


Fig. 4.12.1.1 Configuration of SVD circuit

4.12.2 SVD operation

The SVD circuit compares the criteria voltage set by software and the supply voltage (V_{DD} terminal–V_{SS} terminal) and sets its results into the SVDDT latch. By reading the data of this SVDDT latch, it can be determined by means of software whether the supply voltage is normal or has dropped.
The criteria voltage can be set for the 16 types shown in Table 4.12.2.1 by the SVDS3–SVDS0 registers.
When "0" is written to the SVDS3–SVDS0 register, the supply voltage detection voltage is set to 1.30 V.
When "8" is written to the SVDS3–SVDS0 register, it is set to 2.10 V.

Table 4.12.2.1 Criteria voltage setting

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
0	1	1	1	2.00
0	1	1	0	1.90
0	1	0	1	1.80
0	1	0	0	1.70
0	0	1	1	1.60
0	0	1	0	1.50
0	0	0	1	1.40
0	0	0	0	1.30

SVDS3	SVDS2	SVDS1	SVDS0	Criteria voltage (V)
1	1	1	1	2.80
1	1	1	0	2.70
1	1	0	1	2.60
1	1	0	0	2.50
1	0	1	1	2.40
1	0	1	0	2.30
1	0	0	1	2.20
1	0	0	0	2.10

When the SVDON register is set to "1", source voltage or external voltage detection by the SVD circuit is executed. As soon as the SVDON register is reset to "0", the result is loaded to the SVDDT latch and the SVD circuit goes OFF.
To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

When the SVD circuit is ON, the IC draws a large current, so keep the SVD circuit off unless it is.

4.12.3 I/O memory of SVD circuit

Table 4.12.3.1 shows the I/O addresses and the control bits for the SVD circuit.

Table 4.12.3.1 Control bits of SVD circuit

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF04H	SVDS3	SVDS2	SVDS1	SVDS0	SVDS3	0			SVD criteria voltage setting
					SVDS2	0			[SVDS3–0] 0 1 2 3 4 5 6 7
	R/W				SVDS1	0			Voltage(V) 1.30 1.40 1.50 1.60 1.70 1.80 1.90 2.00
					SVDS0	0			[SVDS3–0] 8 9 10 11 12 13 14 15
									Voltage(V) 2.10 2.20 2.30 2.40 2.50 2.60 2.70 2.80
FF05H	0	0	SVDDT	SVDON	0 *3	– *2			Unused
					0 *3	– *2			Unused
	R			R/W	SVDDT	0	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

SVDS3–SVDS0: SVD criteria voltage setting register (FF04H)

Criteria voltage for SVD is set as shown in Table 4.12.2.1.
At initial reset, this register is set to "0".

SVDON: SVD control (ON/OFF) register (FF05H•D0)

Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

When the SVDON register is set to "1", a source voltage detection is executed by the SVD circuit. As soon as SVDON is reset to "0", the result is loaded to the SVDDT latch. To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec.
At initial reset, this register is set to "0".

SVDDT: SVD data (FF05H•D1)

This is the result of supply voltage detection.

When "0" is read: Supply voltage (V_{DD}–V_{SS}) ≥ Criteria voltage
When "1" is read: Supply voltage (V_{DD}–V_{SS}) < Criteria voltage
Writing: Invalid

The result of supply voltage detection at time of SVDON is set to "0" can be read from this latch.
At initial reset, SVDDT is set to "0".

4.12.4 Programming notes

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.

1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

4.13 Heavy Load Protection Function

4.13.1 Outline of heavy load protection function

The S1C63406 has a heavy load protection function for when the battery load becomes heavy, such as when an external lamp is lit or the buzzer is on (piezoelectric buzzer is driven). In such case, the heavy load protection function is suitable.
The normal mode (heavy load protection function is off) changes to the heavy load protection mode (heavy load protection function is on) when the software changes the mode to the heavy load protection mode (HLMOD = "1").

Note: In the heavy load protection mode, more current is consumed than in the normal mode. Unless necessary, do not select the heavy load protection mode with the software.

4.13.2 I/O memory of heavy load protection function

Table 4.13.2.1 shows the I/O address and the control bit for the heavy load protection function.

Table 4.13.2.1 Control bit of heavy load protection function

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
FF07H	HLMOD	0	WDEN	WDRST	HLMOD	0	On	Off	Heavy load protection
					0 *3	– *2			Unused
					WDEN	1	Enable	Disable	Watchdog timer enable
	R/W	R	R/W	W	WDRST*3	Reset	Reset	Invalid	Watchdog timer reset (writing)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

HLMOD: Heavy load protection (FF07H•D3)

Heavy load protection On/Off is controlled with this register.

When "1" is written: Heavy load protection on
When "0" is written: Heavy load protection off
Reading: Valid

The device enters the heavy load protection mode by writing "1" to HLMOD, and returns to the normal mode by writing "0".
At initial reset, this register is set to "0".

4.13.3 Programming note

Be aware that current consumption increases in the heavy load protection mode.

4.14 Interrupt and HALT/SLEEP

<Interrupt types>

The S1C63406 provides the following interrupt functions.

External interrupt:	• input port interrupt	(4 systems)
Internal interrupt:	• Watchdog timer interrupt	(NMI, 1 system)
	• Programmable timer interrupt	(2 systems)
	• Serial interface interrupt	(3 systems)
	• Timer interrupt	(4 systems)
	• Stopwatch timer interrupt	(2 systems)

To authorize interrupt, the interrupt flag must be set to "1" (EI) and the necessary related interrupt mask registers must be set to "1" (enable).
When an interrupt occurs the interrupt flag is automatically reset to "0" (DI), and interrupts after that are inhibited.

The watchdog timer interrupt is an NMI (non-maskable interrupt), therefore, the interrupt is generated regardless of the interrupt flag setting. Also the interrupt mask register is not provided. However, it is possible to not generate NMI since software can stop the watchdog timer operation.

Figure 4.14.1 shows the configuration of the interrupt circuit.

Note: After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

<HALT/SLEEP>

The S1C63406 has HALT and SLEEP functions that considerably reduce current consumption when it is not necessary.
The CPU enters HALT status when the HALT instruction is executed.
In HALT status, the operation of the CPU is stopped. However, timers continue counting since the oscillation circuit operates. Reactivating the CPU from HALT status is done by generating a hardware interrupt request including NMI.
When the CPU enters SLEEP status as the result of the SLP instruction, the CPU stops its operation, the OSC3 oscillation circuit and supplying the OSC1 clock to the divider and peripheral circuits. However, the OSC1 oscillation circuit does not stop its oscillation.
Reactivating from SLEEP status can only be done by generation of an input port interrupt factor. Therefore, set the following flag and the registers for the K0x port to be used to cancel SLEEP status before executing the SLP instruction.

- Interrupt flag (I flag) = "1" (interrupts are enabled)
- Interrupt selection register SIK0x = "1" (the K0x input port interrupt is selected)
- Interrupt mask register EIK0x = "1" (the K0x input port interrupt is enabled)
- Noise rejector selection register K0NR1–K0NR0 = "00" (noise rejector is bypassed)

When SLEEP status is canceled by an input interrupt, wait for oscillation to stabilize, then restart the CPU operation (input port interrupt processing).
Refer to the "S1C63000 Core CPU Manual" for transition to the HALT/SLEEP status and timing of its cancellation.

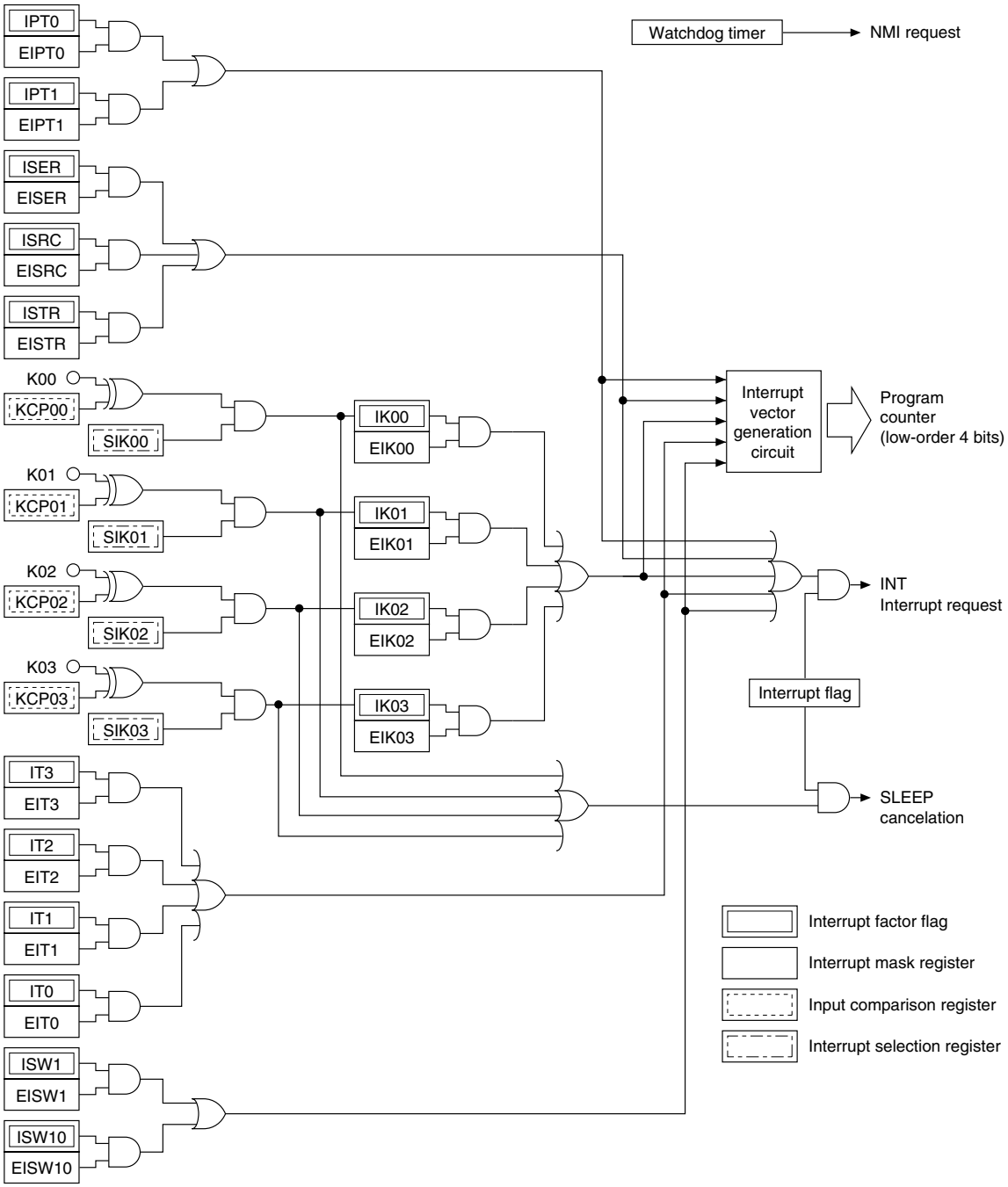


Fig. 4.14.1 Configuration of the interrupt circuit

4.14.1 Interrupt factor

Table 4.14.1.1 shows the factors for generating interrupt requests.

The interrupt flags are set to "1" depending on the corresponding interrupt factors.
The CPU operation is interrupted when an interrupt factor flag is set to "1" if the following conditions are established.

- The corresponding mask register is "1" (enabled)
- The interrupt flag is "1" (EI)

The interrupt factor flag is reset to "0" when "1" is written.
At initial reset, the interrupt factor flags are reset to "0".

* Since the watchdog timer's interrupt is NMI, the interrupt is generated regardless of the setting above, and no interrupt factor flag is provided.

Table 4.14.1.1 Interrupt factors

Interrupt factor	Interrupt factor flag	
Programmable timer 1 (counter = 0)	IPT1	(FFF2H•D1)
Programmable timer 0 (counter = 0)	IPT0	(FFF2H•D0)
Serial interface (receive error)	ISER	(FFF3H•D2)
Serial interface (receive completion)	ISRC	(FFF3H•D0)
Serial interface (transmit completion)	ISTR	(FFF3H•D1)
K03 input (falling edge or rising edge)	IK03	(FFFBH•D3)
K02 input (falling edge or rising edge)	IK02	(FFFBH•D2)
K01 input (falling edge or rising edge)	IK01	(FFFBH•D1)
K00 input (falling edge or rising edge)	IK00	(FFFBH•D0)
Clock timer 1 Hz (falling edge)	IT3	(FFF6H•D3)
Clock timer 2 Hz (falling edge)	IT2	(FFF6H•D2)
Clock timer 8 Hz (falling edge)	IT1	(FFF6H•D1)
Clock timer 32 Hz (falling edge)	IT0	(FFF6H•D0)
Stopwatch timer (1 Hz)	ISW1	(FFF7H•D1)
Stopwatch timer (10 Hz)	ISW10	(FFF7H•D0)

Note: After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

4.14.2 Interrupt mask

The interrupt factor flags can be masked by the corresponding interrupt mask registers.
The interrupt mask registers are read / write registers. They are enabled (interrupt authorized) when "1" is written to them, and masked (interrupt inhibited) when "0" is written to them.
At initial reset, the interrupt mask register is set to "0".
Table 4.14.2.1 shows the correspondence between interrupt mask registers and interrupt factor flags.

Table 4.14.2.1 Interrupt mask registers and interrupt factor flags

Interrupt mask register		Interrupt factor flag	
EIPT1	(FFE2H•D1)	IPT1	(FFF2H•D1)
EIPT0	(FFE2H•D0)	IPT0	(FFF2H•D0)
EISER	(FFE3H•D2)	ISER	(FFF3H•D2)
EISRC	(FFE3H•D0)	ISRC	(FFF3H•D0)
EISTR	(FFE3H•D1)	ISTR	(FFF3H•D1)
EIK03	(FFEBH•D3)	IK03	(FFFBH•D3)
EIK02	(FFEBH•D2)	IK02	(FFFBH•D2)
EIK01	(FFEBH•D1)	IK01	(FFFBH•D1)
EIK00	(FFEBH•D0)	IK00	(FFFBH•D0)
EIT3	(FFE6H•D3)	IT3	(FFF6H•D3)
EIT2	(FFE6H•D2)	IT2	(FFF6H•D2)
EIT1	(FFE6H•D1)	IT1	(FFF6H•D1)
EIT0	(FFE6H•D0)	IT0	(FFF6H•D0)
EISW1	(FFE7H•D1)	ISW1	(FFF7H•D1)
EISW10	(FFE7H•D0)	ISW10	(FFF7H•D0)

4.14.3 Interrupt vector

When an interrupt request is input to the CPU, the CPU begins interrupt processing. After the program being executed is terminated, the interrupt processing is executed in the following order.

1 The content of the flag register is evacuated, then the I flag is reset.

2 The address data (value of program counter) of the program to be executed next is saved in the stack area (RAM).

3 The interrupt request causes the value of the interrupt vector (0100H–010AH) to be set in the program counter.

4 The program at the specified address is executed (execution of interrupt processing routine by software).

Table 4.14.3.1 shows the correspondence of interrupt requests and interrupt vectors.

Table 4.14.3.1 Interrupt request and interrupt vectors

Interrupt vector	Interrupt factor	Priority
0100H	Watchdog timer	High
0102H	Programmable timer	↑
0104H	Serial interface	
0106H	K00–K03 input	
0108H	Clock timer	↓
010AH	Stopwatch timer	Low

The four low-order bits of the program counter are indirectly addressed through the interrupt request.

4.14.4 I/O memory of interrupt

Table 4.14.4.1 shows the I/O addresses and the control bits for controlling interrupts.

Table 4.14.4.1 Control bits of interrupt

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
FF54H	SIK03	SIK02	SIK01	SIK00	SIK03	0	Enable	Disable	K00–K03 interrupt selection register
					SIK02	0	Enable	Disable	
					SIK01	0	Enable	Disable	
	R/W				SIK00	0	Enable	Disable	
FF55H	KCP03	KCP02	KCP01	KCP00	KCP03	1	↓	↑	K00–K03 input comparison register
					KCP02	1	↓	↑	
					KCP01	1	↓	↑	
	R/W				KCP00	1	↓	↑	
FFE2H	GPR23	GPR22	EIPT1	EIPT0	GPR23	0	1	0	General-purpose register
					GPR22	0	1	0	General-purpose register
					EIPT1	0	Enable	Mask	Interrupt mask register (Programmable timer 1)
	R/W				EIPT0	0	Enable	Mask	Interrupt mask register (Programmable timer 0)
FFE3H	GPR33	EISER	EISTR	EISRC	GPR33	0	1	0	General-purpose register
					EISER	0	Enable	Mask	Interrupt mask register (Serial I/F error)
					EISTR	0	Enable	Mask	Interrupt mask register (Serial I/F transmit completion)
	R/W				EISRC	0	Enable	Mask	Interrupt mask register (Serial I/F receive completion)
FFE6H	EIT3	EIT2	EIT1	EIT0	EIT3	0	Enable	Mask	Interrupt mask register (Clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (Clock timer 2 Hz)
					EIT1	0	Enable	Mask	Interrupt mask register (Clock timer 8 Hz)
	R/W				EIT0	0	Enable	Mask	Interrupt mask register (Clock timer 32 Hz)
FFE7H	GPR73	GPR72	EISW1	EISW10	GPR73	0	1	0	General-purpose register
					GPR72	0	1	0	General-purpose register
					EISW1	0	Enable	Mask	Interrupt mask register (Stopwatch timer 1 Hz)
	R/W				EISW10	0	Enable	Mask	Interrupt mask register (Stopwatch timer 10 Hz)
FFEBH	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
					EIK01	0	Enable	Mask	Interrupt mask register (K01)
	R/W				EIK00	0	Enable	Mask	Interrupt mask register (K00)
FFF2H	0	0	IPT1	IPT0	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		IPT1	0	(W)	(W)	Interrupt factor flag (Programmable timer 1)
					IPT0	0	Reset	Invalid	Interrupt factor flag (Programmable timer 0)
FFF3H	0	ISER	ISTR	ISRC	0 *3	– *2	(R)	(R)	Unused
					ISER	0	Yes	No	Interrupt factor flag (Serial I/F error)
	R	R/W			ISTR	0	(W)	(W)	Interrupt factor flag (Serial I/F transmit completion)
					ISRC	0	Reset	Invalid	Interrupt factor flag (Serial I/F receive completion)
FFF6H	IT3	IT2	IT1	IT0	IT3	0	(R)	(R)	Interrupt factor flag (Clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (Clock timer 2 Hz)
					IT1	0	(W)	(W)	Interrupt factor flag (Clock timer 8 Hz)
	R/W				IT0	0	Reset	Invalid	Interrupt factor flag (Clock timer 32 Hz)
FFF7H	0	0	ISW1	ISW10	0 *3	– *2	(R)	(R)	Unused
					0 *3	– *2	Yes	No	Unused
	R		R/W		ISW1	0	(W)	(W)	Interrupt factor flag (Stopwatch timer 1 Hz)
					ISW10	0	Reset	Invalid	Interrupt factor flag (Stopwatch timer 10 Hz)
FFFBH	IK03	IK02	IK01	IK00	IK03	0	(R)	(R)	Interrupt factor flag (K03)
					IK02	0	Yes	No	Interrupt factor flag (K02)
					IK01	0	(W)	(W)	Interrupt factor flag (K01)
	R/W				IK00	0	Reset	Invalid	Interrupt factor flag (K00)

*1 Initial value at initial reset

*2 Not set in the circuit

*3 Constantly "0" when being read

EIPT1, EIPT0: Interrupt mask registers (FFE2H•D1, D0)
IPT1, IPT0: Interrupt factor flags (FFF2H•D1, D0)
Refer to Section 4.10, "Programmable Timer".

EISER, EISTR, EISRC: Interrupt mask registers (FFE3H•D2–D0)
ISER, ISTR, ISRC: Interrupt factor flags (FFF3H•D2–D0)
Refer to Section 4.11, "Serial Interface".

KCP03–KCP00: Input comparison registers (FF55H)
SIK03–SIK00: Interrupt selection registers (FF54H)
EIK03–EIK00: Interrupt mask registers (FFEBH)
IK03–IK00: Interrupt factor flags (FFFBH)
Refer to Section 4.4, "Input Ports".

EIT3–EIT0: Interrupt mask registers (FFE6H)
IT3–IT0: Interrupt factor flags (FFF6H)
Refer to Section 4.8, "Clock Timer".

EISW1, EISW10: Interrupt mask registers (FFE7H•D1, D0)
ISW1, ISW10: Interrupt factor flags (FFF7H•D1, D0)
Refer to Section 4.9, "Stopwatch Timer".

4.14.5 Programming notes

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine. Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

(4) Reactivating from SLEEP status can only be done by generation of an input port interrupt factor. Therefore, set the following flag and the registers for the K0x port to be used to cancel SLEEP status before executing the SLP instruction.
- Interrupt flag (I flag) = "1" (interrupts are enabled)
- Interrupt selection register SIK0x = "1" (the K0x input port interrupt is selected)
- Interrupt mask register EIK0x = "1" (the K0x input port interrupt is enabled)
- Noise rejector selection register K0NR1–K0NR0 = "00" (noise rejector is bypassed)

CHAPTER 5 SUMMARY OF NOTES

5.1 Notes for Low Current Consumption

The S1C63406 contains control registers for each of the circuits so that current consumption can be reduced.
These control registers reduce the current consumption through programs that operate the circuits at the minimum levels.
The following lists the circuits that can control operation and their control registers. Refer to these when programming.

Table 5.1.1 Circuits and control registers

Circuit (and item)	Control register
CPU	HALT instruction
CPU operating frequency	CLKCHG, OSCC
Internal logic system voltage regulator	VDC1, VDC0
LCD system voltage circuit	LPWR, VCCHG
SVD circuit	SVDON
Heavy load protection	HLMOD

Refer to Chapter 7, "Electrical Characteristics" for current consumption.

Below are the circuit statuses at initial reset.

CPU: Operating status

CPU operating frequency: Low speed side (CLKCHG = "0")
OSC3 oscillation circuit is in OFF status (OSCC = "0")

Internal logic system voltage regulator: Low speed side 1.1 V (VDC1–VDC0 = "0H")

LCD system voltage circuit: OFF status (LPWR = "0")
V_{S2} standard (VCCHG = "1") when V_{DD} is 2.5 V or more

SVD circuit: OFF status (SVDON = "0")

Heavy load protection: OFF status (HLMOD = "0")

The reset circuit increases current consumption. In particular, current consumption in reset status will be greatly increased. See Chapter 7, "Electrical Characteristics", for details. Also, be careful about panel selection because the current consumption can differ by the order of several µA on account of the LCD panel characteristics.

5.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mind when programming.

Memory and stack

(1) Memory is not implemented in unused areas within the memory map. Further, some non-implementation areas and unused (access prohibition) areas exist in the display memory area and the peripheral I/O area. If the program that accesses these areas is generated, its operation cannot be guaranteed. Refer to Section 4.7.4, "Display memory", for the display memory, and the I/O memory maps shown in Tables 4.1.1 (a)–(d) for the peripheral I/O area.

(2) Part of the RAM area is used as a stack area for subroutine call and register evacuation, so pay attention not to overlap the data area and stack area.

(3) The S1C63000 core CPU handles the stack using the stack pointer for 4-bit data (SP2) and the stack pointer for 16-bit data (SP1).
16-bit data are accessed in stack handling by SP1, therefore, this stack area should be allocated to the area where 4-bit/16-bit access is possible (0100H to 01FFH). The stack pointers SP1 and SP2 change cyclically within their respective range: the range of SP1 is 0000H to 03FFH and the range of SP2 is 0000H to 00FFH. Therefore, pay attention to the SP1 value because it may be set to 0200H or more exceeding the 4-bit/16-bit accessible range in the S1C63406 or it may be set to 00FFH or less. Memory accesses except for stack operations by SP1 are 4-bit data access.
After initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set by software. Further, if either SP1 or SP2 is re-set when both are set already, the interrupts including NMI are masked again until the other is re-set. Therefore, the settings of SP1 and SP2 must be done as a pair.

Watchdog timer

(1) When the watchdog timer is being used, the software must reset it within 3-second cycles.

(2) Because the watchdog timer is set in operation state by initial reset, set the watchdog timer to disabled state (not used) before generating an interrupt (NMI) if it is not used.

Oscillation circuit

(1) When switching the CPU system clock from OSC1 to OSC3, first set V_{D1}. After that maintain 2.5 msec or more, and then turn the OSC3 oscillation ON.
When switching from OSC3 to OSC1, set V_{D1} after switching to OSC1 and turning the OSC3 oscillation OFF.

(2) It takes at least 5 msec from the time the OSC3 oscillation circuit goes ON until the oscillation stabilizes. Consequently, when switching the CPU operation clock from OSC1 to OSC3, do this after a minimum of 5 msec have elapsed since the OSC3 oscillation went ON.
Further, the oscillation stabilization time varies depending on the external oscillator characteristics and conditions of use, so allow ample margin when setting the wait time.

(3) When switching the clock form OSC3 to OSC1, use a separate instruction for switching the OSC3 oscillation OFF. An error in the CPU operation can result if this processing is performed at the same time by the one instruction.

(4) The S1C63406 supports the SLEEP function. The OSC3 oscillation circuit stops in the SLEEP mode. The OSC1 oscillation circuit stops clock supply to the divider and peripheral circuits, however, the oscillation continues. To prevent improper operation after the CPU wakes up, be sure to run the CPU with the OSC1 clock before setting the CPU in the SLEEP mode.

Input port

(1) When input ports are changed from low to high by pull-up resistors, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate waiting time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

(2) Be sure to turn the noise rejector OFF before executing the SLP instruction.

(3) Reactivating from SLEEP status can only be done by generation of an input interrupt factor. Therefore when using the SLEEP function, it is necessary to set the interrupt selection register (SIK0x = "1") of the port to be used for releasing SLEEP status before executing the SLP instruction. Furthermore, enable the input port interrupt using the corresponding interrupt mask register (EIK0x = "1") before executing the SLP instruction to run input interrupt handler routine after SLEEP status is released.

(4) Each input port (K00–K03) has a different interrupt factor, thus the input interrupt is controlled individually. Be aware that this interrupt configuration is different from that of the previous models.

(5) The K03 terminal functions as the clock input terminal for the programmable timer, and the input signal is shared with the input port and the programmable timer. Therefore, when the K03 terminal is set to the clock input terminal for the programmable timer, take care of the interrupt setting.

Output port

(1) When using the output port (R12, R13) as the special output port, fix the data register (R12, R13) at "1". Be aware that the output terminal is fixed at a low (V_{SS}) level the same as the DC output if "0" is written to the R12 and R13 registers when the special output has been selected.

(2) A hazard may occur when the FOUT signal and the TOUT signal are turned ON and OFF.

(3) When f_{OSC3} is selected for the FOUT signal frequency, it is necessary to control the OSC3 oscillation circuit before output. Refer to Section 4.3, "Oscillation Circuit", for the control and notes.

I/O port

When I/O ports are changed from low to high by pull-up resistor in the input mode, the rise of the waveform is delayed on account of the time constant of the pull-up resistor and input gate capacitance. Hence, when fetching input ports, set an appropriate wait time.
Particular care needs to be taken of the key scan during key matrix configuration.
Make this waiting time the amount of time or more calculated by the following expression.
$10 \times C \times R$
C: terminal capacitance 5 pF + parasitic capacitance ? pF
R: pull-up resistance 300 kΩ

LCD driver

(1) Current consumption will be increased for a cycle of 1 kHz to stabilize the LCD power quickly after setting LPWR on.

(2) When a program that access no memory mounted area (F078H–F0FFH, F101H, F103H, · · ·, F177H) is made, the operation is not guaranteed.

(3) Because at initial reset, the contents of display memory and LC3–LC0 (LCD contrast) are undefined, there is need to initialize by the software. Furthermore, take care of the registers LPWR and ALOFF because these are set so that the display goes OFF.

Clock timer

(1) Be sure to read timer data in the order of low-order data (TM0–TM3) then high-order data (TM4–TM7).

(2) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, the clock timer can not be used for the clock function.

Stopwatch timer

(1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 µsec (1/4 cycle of 256 Hz).

(2) When the CR oscillation circuit is selected as the OSC1 oscillation circuit by mask option, the frequencies and times differ from the values described in this section because the oscillation frequency will be 60 kHz (Typ.). Therefore, this timer can not be used for the stopwatch function.

Programmable timer

(1) When reading counter data, be sure to read the low-order 4 bits (PTD00–PTD03, PTD10–PTD13) first. Furthermore, the high-order 4 bits (PTD04–PTD07, PTD14–PTD17) should be read within 0.73 msec (when f_{OSC1} is 32.768 kHz) of reading the low-order 4 bits (PTD00–PTD03, PTD10–PTD13).

(2) The programmable timer actually enters RUN / STOP status in synchronization with the falling edge of the input clock after writing to the PTRUN0 / PTRUN1 register. Consequently, when "0" is written to the PTRUN0 / PTRUN1 register, the timer enters STOP status at the point where the counter is decremented (-1). The PTRUN0 / PTRUN1 register maintains "1" for reading until the timer actually stops.
Figure 5.2.1 shows the timing chart for the RUN / STOP control.

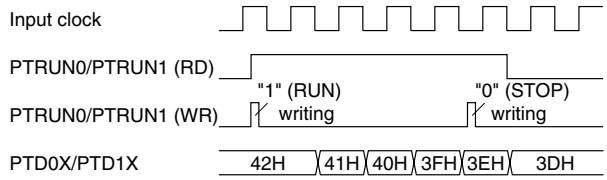


Fig. 5.2.1 Timing chart for RUN/STOP control

(3) Since the TOUT signal is generated asynchronously from the PTOUT register, a hazard within 1 / 2 cycle is generated when the signal is turned ON and OFF by setting the register.

(4) When the OSC3 oscillation clock is selected for the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the programmable timer. However the OSC3 oscillation circuit requires a time at least 5 msec from turning the circuit ON until the oscillation stabilizes. Therefore, allow an adequate interval from turning the OSC3 oscillation circuit ON to starting the programmable timer. Refer to Section 4.3, "Oscillation Circuit", for the control and notes of the OSC3 oscillation circuit. At initial reset, the OSC3 oscillation circuit is set in the OFF state.

(5) For the reason below, pay attention to the reload data write timing when changing the interval of the programmable timer interrupts while the programmable timer is running.
The programmable timer counts down at the falling edge of the input clock and at the same time it generates an interrupt if the counter underflows. Then it starts loading the reload data to the counter and the counter data is determined at the next rising edge of the input clock (period shown in as ① in the figure).

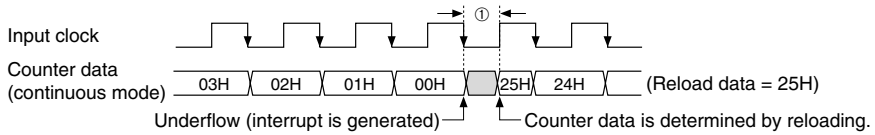


Fig. 5.2.2 Reload timing for programmable timer

To avoid improper reloading, do not rewrite the reload data after an interrupt occurs until the counter data is determined including the reloading period ①. Be especially careful when using the OSC1 (low-speed clock) as the clock source of the programmable timer and the CPU is operating with OSC3 (high-speed clock).

Serial interface

(1) Be sure to initialize the serial interface mode in the transmit / receive disabled status (TXEN = RXEN = "0").

(2) Do not perform double trigger (writing "1") to TXTRG (RXTRG) when the serial interface is in the transmitting (receiving) operation.

(3) In the clock synchronous mode, since one clock line ($\overline{SCLK}$) is shared for both transmitting and receiving, transmitting and receiving cannot be performed simultaneously. (Half duplex only is possible in clock synchronous mode.)
Consequently, be sure not to write "1" to RXTRG (TXTRG) when TXTRG (RXTRG) is "1".

(4) When a parity error or flaming error is generated during receiving in the asynchronous mode, the receiving error interrupt factor flag ISER is set to "1" prior to the receive completion interrupt factor flag ISRC for the time indicated in Table 5.2.1. Consequently, when an error is generated, you should reset the receiving complete interrupt factor flag ISRC to "0" by providing a wait time in error processing routines and similar routines.
When an overrun error is generated, the receiving complete interrupt factor flag ISRC is not set to "1" and a receiving complete interrupt is not generated.

Table 5.2.1 Time difference between ISER and ISRC on error generation

Clock source	Time difference
fOSC3 / n	1/2 cycles of fOSC3 / n
Programmable timer	1 cycle of timer 1 underflow

(5) When the demultiplied signal of the OSC3 oscillation circuit is made the clock source, it is necessary to turn the OSC3 oscillation ON, prior to using the serial interface.
A time interval of 5 msec, from the turning ON of the OSC3 oscillation circuit to until the oscillation stabilizes, is necessary, due to the oscillation element that is used. Consequently, you should allow an adequate waiting time after turning ON of the OSC3 oscillation, before starting transmitting / receiving of serial interface. (The oscillation start time will vary somewhat depending on the oscillator and on the externally attached parts. Refer to the oscillation start time example indicated in Chapter 7, "Electrical Chracteristics".)
At initial reset, the OSC3 oscillation circuit is set to OFF status.

(6) Be aware that the maximum clock frequency for the serial interface is limited to 2 MHz.

SVD circuit

(1) To obtain a stable detection result, the SVD circuit must be ON for at least l00 µsec. So, to obtain the SVD detection result, follow the programming sequence below.
1. Set SVDON to "1"
2. Maintain for 100 µsec minimum
3. Set SVDON to "0"
4. Read SVDDT

(2) The SVD circuit should normally be turned OFF because SVD operation increase current consumption.

Heavy load protection function

Be aware that current consumption increases in the heavy load protection mode.

Interrupt

(1) The interrupt factor flags are set when the interrupt condition is established, even if the interrupt mask registers are set to "0".

(2) After an interrupt occurs, the same interrupt will occur again if the interrupt enabled state (I flag = "1") is set or the RETI instruction is executed unless the interrupt factor flag is reset. Therefore, be sure to reset (write "1" to) the interrupt factor flag in the interrupt service routine before shifting to the interrupt enabled state.

(3) After an initial reset, all the interrupts including NMI are masked until both the stack pointers SP1 and SP2 are set with the software. Be sure to set the SP1 and SP2 in the initialize routine.
Further, when re-setting the stack pointer, the SP1 and SP2 must be set as a pair. When one of them is set, all the interrupts including NMI are masked and interrupts cannot be accepted until the other one is set.

(4) When using the SLEEP function, set the following flag and the registers for the K0x port to be used to cancel SLEEP status before executing the SLP instruction.
- Interrupt flag (I flag) = "1" (interrupts are enabled)
- Interrupt selection register SIK0x = "1" (the K0x input port interrupt is selected)
- Interrupt mask register EIK0x = "1" (the K0x input port interrupt is enabled)
- Noise rejector selection register K0NR1–K0NR0 = "00" (noise rejector is bypassed)

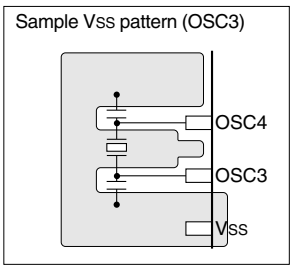
5.3 Notes on Mounting

<Oscillation Circuit>

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1, OSC2, OSC3 and OSC4 terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the right hand figure, make a V_{SS} pattern as large as possible at circumscription of the OSC1, OSC2, OSC3 and OSC4 terminals and the components connected to these terminals. Furthermore, do not use this V_{SS} pattern for any purpose other than the oscillation system.



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 / OSC3 and V_{DD}, please keep enough distance between OSC1 / OSC3 and V_{DD} or other signals on the board pattern.

<Reset Circuit>

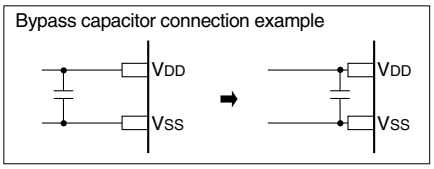
- The power-on reset signal which is input to the $\overline{RESET}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When the built-in pull-up resistor for the $\overline{RESET}$ terminal is used, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{RESET}$ terminal in the shortest line.

<Power Supply Circuit>

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the V_{DD} and V_{SS} terminal with patterns as short and large as possible.

  (2) When connecting between the V_{DD} and V_{SS} terminals with a bypass capacitor, the terminals should be connected as short as possible.

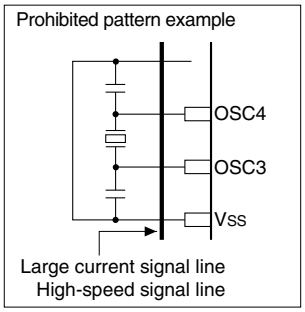


  (3) Components which are connected to the V_{D1} and V_{C1}–V_{C5} terminals, such as capacitors and resistors, should be connected in the shortest line.
  In particular, the V_{C1}–V_{C5} voltages affect the display quality.

- Do not connect anything to the V_{C1}–V_{C5} terminals when the LCD driver is not used.

<Arrangement of Signal Lines>

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction.
  Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



<Precautions for Visible Radiation (when bare chip is mounted)>

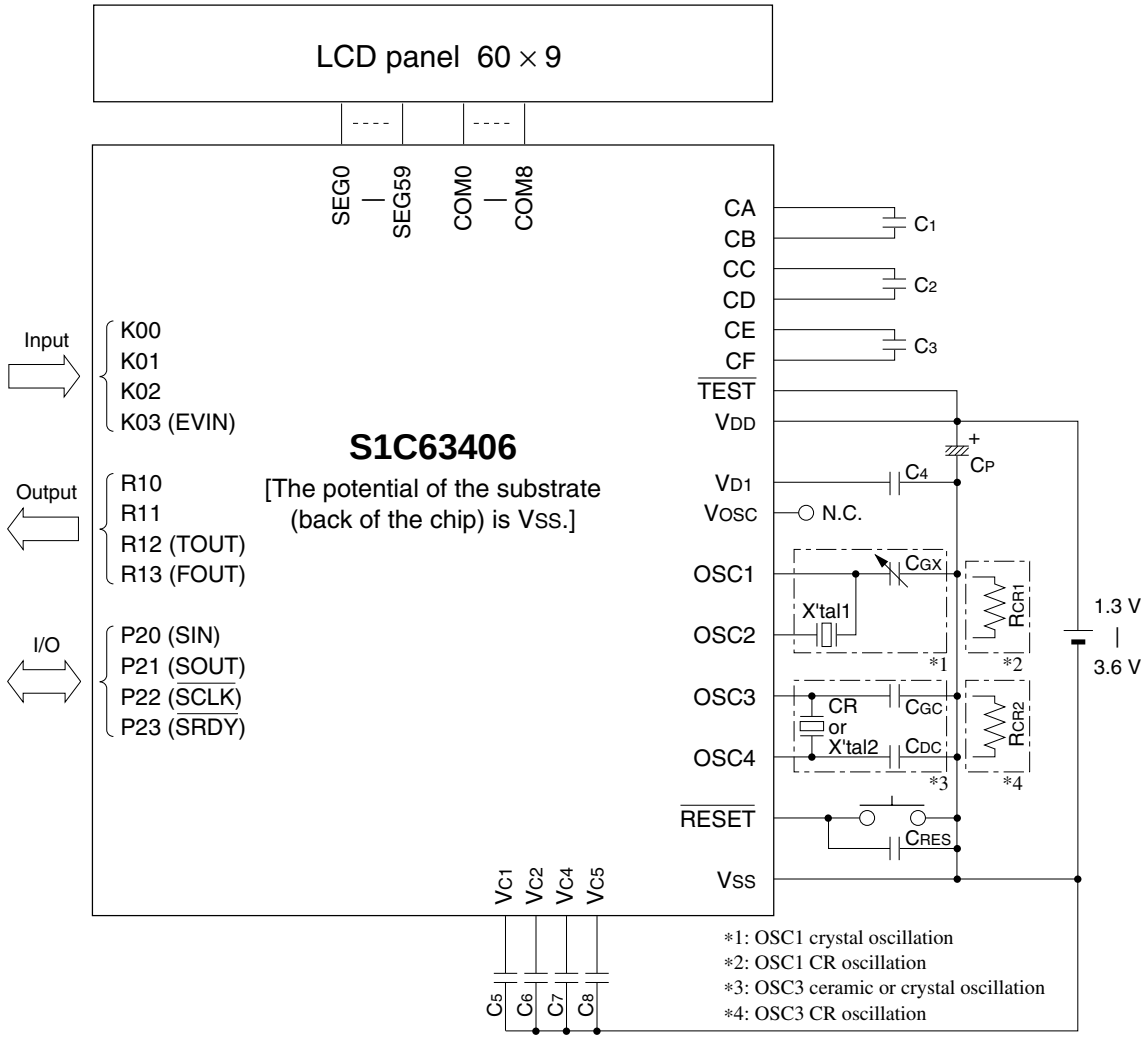
- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiations.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 6 BASIC EXTERNAL WIRING DIAGRAM



X'tal1	Crystal oscillator	32.768 kHz, CI (Max.) = 34 kΩ
CGX	Trimmer capacitor	5–25 pF
RCR1	Resistor for OSC1 CR oscillation	680 kΩ (60 kHz)
CR	Ceramic oscillator	3.58 MHz
X'tal2	Crystal oscillator	4 MHz
CGC	Gate capacitor	30 pF (ceramic), 15 pF (cryctal)
CDC	Drain capacitor	30 pF (ceramic), 15 pF (cryctal)
RCR2	Resistor for OSC3 CR oscillation	820Ω (2MHz, VD1 = 1.5V)
C1–C8	Capacitor	0.1 µF
CP	Capacitor	3.3 µF
CRES	$\overline{\text{RESET}}$ terminal capacitor	0.47 µF

Note: The above table is simply an example, and is not guaranteed to work.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Rating

(VSS=0V)

Item	Symbol	Rated value	Unit
Supply voltage	VDD	-0.5 to 4.7	V
Input voltage (1)	VI	-0.5 to VDD + 0.3	V
Input voltage (2)	VIOSC	-0.5 to VD1 + 0.3	V
Permissible total output current *1	ΣIVDD	10	mA
Operating temperature	Topr	-40 to 85	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	PD	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package.

7.2 Recommended Operating Conditions

(Ta=-40 to 85°C)

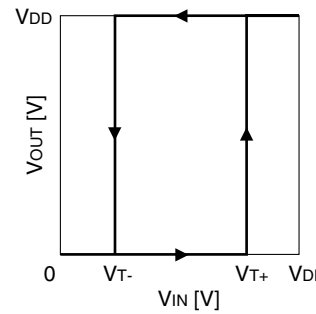
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VDD	VSS=0V, OSC3=OFF, OSC1=80kHz Max.	1.3		3.6	V
		VSS=0V, OSC3=700kHz Max.	1.4		3.6	V
		VSS=0V, OSC3=2.2MHz Max.	1.6		3.6	V
		VSS=0V, OSC3=4.2MHz Max.	1.8		3.6	V
Oscillation frequency	fOSC1	Crystal oscillation	30	32.768	80	kHz
		CR oscillation	30	60	80	kHz
	fOSC3	VDD=1.4–3.6V, CR oscillation	30	500	700	kHz
		VDD=1.6–3.6V, CR oscillation	0.03	1	2.2	MHz
		VDD=1.8–3.6V, CR oscillation	0.03	2	4.2	MHz
		VDD=1.8–3.6V, Ceramic oscillation	0.03	3.58	4.2	MHz
		VDD=1.8–3.6V, Crystal oscillation	0.03	4	4.2	MHz

7.3 DC Characteristics

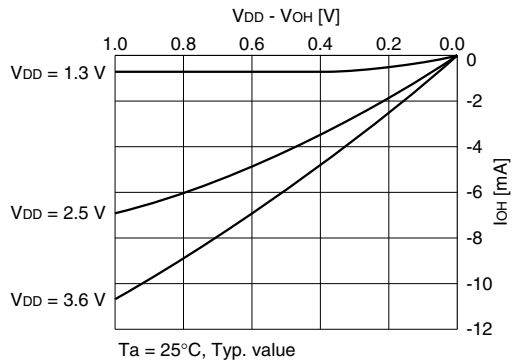
Unless otherwise specified: V_{DD}=3.6V, V_{SS}=0V, Ta=25°C, V_{D1}/V_{OSC}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		K0x	0.8·V_{DD}		V_{DD}	V
Low level input voltage	V_{IL}		K0x	0		0.2·V_{DD}	V
High level schmitt input voltage	V_{T+}		P2x, $\overline{RESET}$, $\overline{TEST}$	0.5·V_{DD}		0.9·V_{DD}	V
Low level schmitt input voltage	V_{T-}		P2x, $\overline{RESET}$, $\overline{TEST}$	0.1·V_{DD}		0.5·V_{DD}	V
Input leak current	I_{LIH}		K0x, P2x, $\overline{RESET}$, $\overline{TEST}$	-1.0		1.0	µA
	I_{LIL}		K0x, P2x, $\overline{RESET}$, $\overline{TEST}$	-1.0		1.0	µA
Input pull-up resistance	R_{IN}		K0x, P2x, $\overline{RESET}$	100	300	500	kΩ
Input terminal capacitance	C_{IN}	V_{IN}=0V, f=32kHz	K0x, P2x			15	pF
High level output current *1	I_{OH}	V_{OH1}=0.9·V_{DD}, V_{DD}=1.3V	R1x, P2x			-0.3	mA
Low level output current *1	I_{OL}	V_{OL1}=0.1·V_{DD}, V_{DD}=1.3V	R1x, P2x	0.3			mA
Output leak current	I_{LOH}		R1x, P2x	-1.0		1.0	µA
	I_{LOL}		R1x, P2x	-1.0		1.0	µA
Common output current	I_{COMH}	V_{OH2}=V_{C5}-0.05V	COMx			-25	µA
	I_{COML}	V_{OL2}=V_{SS}+0.05V		25			µA
Segment output current	I_{SEGH}	V_{OH3}=V_{C5}-0.05V	SEGxx			-10	µA
	I_{SEGL}	V_{OL3}=V_{SS}+0.05V		10			µA

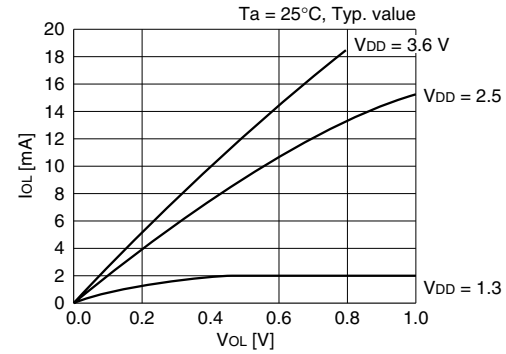
*1 See the characteristic curve as reference for the actual output current value.



High-level output current characteristic (reference value)



Low-level output current characteristic (reference value)



7.4 Analog Circuit Characteristics and Power Current Consumption

LCD driver

Unless otherwise specified:

V_{DD}=3.6V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=5pF, Ta=25°C, V_{D1}/V_{OSC}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.1µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (when V_{C1} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)	LC0–3="0"		0.98		V
			LC0–3="1"		0.99		
			LC0–3="2"		1.01		
			LC0–3="3"		1.02		
			LC0–3="4"		1.04		
			LC0–3="5"		1.05		
			LC0–3="6"		1.07		
			LC0–3="7"	Typ.	1.08	Typ.	
			LC0–3="8"	×0.88	1.10	×1.12	
			LC0–3="9"		1.11		
			LC0–3="10"		1.13		
			LC0–3="11"		1.14		
			LC0–3="12"		1.16		
			LC0–3="13"		1.17		
			LC0–3="14"		1.19		
			LC0–3="15"		1.20		
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2·V_{C1} ×0.9		2·V_{C1}	V
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3·V_{C1} ×0.9		3·V_{C1}	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		4·V_{C1} ×0.9		4·V_{C1}	V
LCD drive voltage (when V_{C2} standard is selected)	V_{C1}	Connect 1 MΩ load resistor between V_{SS} and V_{C1} (without panel load)		1/2·V_{C2} ×0.95		1/2·V_{C2} +0.1	V
	V_{C2}	Connect 1 MΩ load resistor between V_{SS} and V_{C2} (without panel load)	LC0–3="0"		1.95		V
			LC0–3="1"		1.98		
			LC0–3="2"		2.01		
			LC0–3="3"		2.04		
			LC0–3="4"		2.07		
			LC0–3="5"		2.10		
			LC0–3="6"		2.13		
			LC0–3="7"	Typ.	2.16	Typ.	
			LC0–3="8"	×0.88	2.19	×1.12	
			LC0–3="9"		2.22		
			LC0–3="10"		2.25		
			LC0–3="11"		2.28		
			LC0–3="12"		2.31		
			LC0–3="13"		2.34		
			LC0–3="14"		2.37		
			LC0–3="15"		2.40		
	V_{C4}	Connect 1 MΩ load resistor between V_{SS} and V_{C4} (without panel load)		3/2·V_{C2} ×0.95		3/2·V_{C2}	V
	V_{C5}	Connect 1 MΩ load resistor between V_{SS} and V_{C5} (without panel load)		2·V_{C2} ×0.95		2·V_{C2}	V

SVD circuit

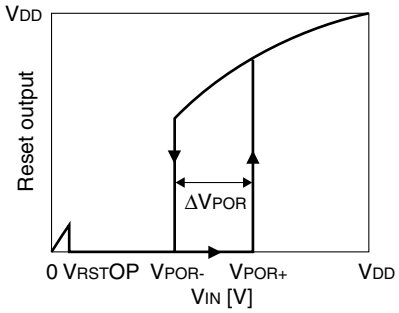
Unless otherwise specified: V_{SS}=0V, Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SVD voltage	V_{SVD}	SVDS0–3="0"	Typ. ×0.93	1.30	Typ. ×1.07	V
		SVDS0–3="1"		1.40		
		SVDS0–3="2"		1.50		
		SVDS0–3="3"		1.60		
		SVDS0–3="4"		1.70		
		SVDS0–3="5"		1.80		
		SVDS0–3="6"		1.90		
		SVDS0–3="7"		2.00		
		SVDS0–3="8"		2.10		
		SVDS0–3="9"		2.20		
		SVDS0–3="10"		2.30		
		SVDS0–3="11"		2.40		
		SVDS0–3="12"		2.50		
		SVDS0–3="13"		2.60		
		SVDS0–3="14"		2.70		
		SVDS0–3="15"		2.80		
SVD circuit response time	t_{SVD}				100	µs

Reset circuit

Unless otherwise specified: V_{DD}=3.6V, V_{SS}=0V, Ta=25°C

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Rreset detection voltage	V_{RST+}	V_{DD}=L to H	When 1.8V option is selected	Typ. ×0.99	1.72	Typ. ×1.01	V
			When 1.6V option is selected		1.52		V
			When 1.4V option is selected		1.32		V
	V_{RST-}	V_{DD}=H to L	When 1.8V option is selected	Typ. ×0.99	1.68	Typ. ×1.01	V
			When 1.6V option is selected		1.48		V
			When 1.4V option is selected		1.28		V
Hysteresis voltage	ΔV_{RST}	V_{DD}=L to H to L		30	40	50	mV
Detection voltage temperature coefficient	$V_{RST}/\Delta T$	Ta=-40 to +85°C			-0.06		%/°C
Reset circuit response time	t_{RST+}	(V_{RST}-Typ.-0.2V) →(V_{RST}+Typ.+0.2V)	When 1.8V option is selected			30	µs
			When 1.6V option is selected			30	µs
			When 1.4V option is selected			30	µs
	t_{RST-}	(V_{RST}-Typ.+0.2V) →(V_{RST}+Typ.-0.2V)	When 1.8V option is selected			20	µs
			When 1.6V option is selected			20	µs
			When 1.4V option is selected			20	µs
Limit operation voltage	V_{RSTOP}				0.65	0.95	V



Current consumption

Unless otherwise specified: V_{DD}=3.6V, V_{SS}=0V, Ta=25°C, V_{D1}/V_{OSC}/V_{C1}/V_{C2}/V_{C4}/V_{C5} are internal voltage, C_1–C_8=0.1µF, No panel load, Not in heavy load protection mode

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Current consumption during SLEEP	I_{SLP}	OSC1=32kHz crystal	LCD off	*1		1.2	2.5	µA
Current consumption during HALT	I_{HALT1}	OSC1=32kHz crystal	LCD off	*2		1.3	2.6	µA
			LCD on (V_{C1} std.)	*2		3.0	6	µA
			LCD on (V_{C2} std.)	*2		2.5	5	µA
	I_{HALT2}	OSC1=60kHz CR	LCD off	*2		3.5	7	µA
			LCD on (V_{C1} std.)	*2		6.2	13	µA
			LCD on (V_{C2} std.)	*2		4.6	10	µA
	I_{HALT3}	OSC1=32kHz crystal LCD off	Reset circuit (1.8V option)	*3		3.2	7	µA
			Reset circuit (1.6V option)	*3		3.5	7.5	µA
			Reset circuit (1.4V option)	*3		3.8	8	µA
Current consumption during execution (software duty = 100%)	I_{EXE}	OSC1=32kHz crystal	LCD off	*2		3.0	5	µA
		OSC1=60kHz CR	LCD off	*2		7.0	10	µA
		OSC3=500kHz CR	LCD off	*4		130	200	µA
		OSC3=1MHz CR	LCD off	*4		260	400	µA
		OSC3=2MHz CR	LCD off	*4		520	800	µA
		OSC3=3.58MHz ceramic	LCD off	*4		670	1100	µA
		OSC3=4MHz crystal	LCD off	*4		780	1200	µA
Heavy load protection current	I_{HVLD}	OSC1=32kHz crystal, LCD off, HLMOD register="1"		*2		30	45	µA
Current consumption in reset status	I_{RSTON}	OSC1=32kHz crystal, V_{DD}=1.29V, when reset circuit option is selected		*5		17	25	µA
LCD circuit current	I_{LCD1}	V_{DD}=3.6V, V_{C1} standard, f_{OSC1}=32.768kHz		*6		1.7	4	µA
	I_{LCD2}	V_{DD}=3.6V, V_{C2} standard, f_{OSC1}=32.768kHz		*6		1.2	3	µA
SVD circuit curent	I_{SVD}	V_{DD}=1.3 to 3.6V, during supply voltage detection				5.5	7	µA
Reset circuit current	I_{RST}	V_{DD}=3.6V		*7		2.5	4	µA

*1 OSC1=ON (clock is not supplied to the divider and peripheral circuit), OSC3=OFF, CPU clock=OSC1, SVD=OFF, reset circuit is not selected

*2 OSC1=ON, OSC3=OFF, CPU clock=OSC1, SVD=OFF, reset circuit is not selected

*3 OSC1=ON, OSC3=OFF, CPU clock=OSC1, SVD=OFF, reset circuit is selected

*4 OSC1=ON, OSC3=ON, CPU clock=OSC3, SVD=OFF, reset circuit is not selected

*5 Reset status due to supply voltage detection by the reset circuit, OSC1=ON, OSC3=ON, CPU clock=OSC3, SVD=OFF, reset circuit is selected, LCD OFF, higher V_{DD} increases current consumption.

*6 When LPWR = "1", current consumption is increased for a cycle of 2 kHz, then it is decreased and stabilized. Also current consumption of the LCD circuit varies according to the OSC1 clock frequency.

*7 Current consumption of the reset circuit varies slightly depending on the option selected. The table lists the values when 1.4 V option is selected (1.4 V option has the largest current consumption under the same V_{DD} conditions).

7.5 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

Unless otherwise specified: V_{DD}=1.3 to 3.6V, V_{SS}=0V, f_{OSC1}=32.768kHz, C_G=25pF, C_D=built-in, Ta=-40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta				3	s
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		14		pF
Frequency/voltage deviation	Δf/ΔV	V_{DD}=1.3 to 3.6V			5	ppm
Frequency/IC deviation	Δf/ΔIC		-10		10	ppm
Frequency adjustment range	Δf/ΔC_G	C_G=5 to 25pF	10	20		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{DD})	3.6			V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{SS}	200			MΩ

OSC1 CR oscillation circuit

Unless otherwise specified: V_{DD}=1.3 to 3.6V, V_{SS}=0V, R_{CR1}=680kΩ, Ta=-40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}	R_{CR1}=constant	-25		25	%
Oscillation start time	tsta				100	µs

OSC3 ceramic oscillation circuit

Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ceramic oscillator: 3.58MHz, C_{GC}=C_{DC}=30pF, Ta=-40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta				5	ms

OSC3 crystal oscillation circuit

Unless otherwise specified: V_{DD}=1.8 to 3.6V, V_{SS}=0V, Crystal oscillator: 4MHz, C_{GC}=C_{DC}=15pF, Ta=-40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta				10	ms

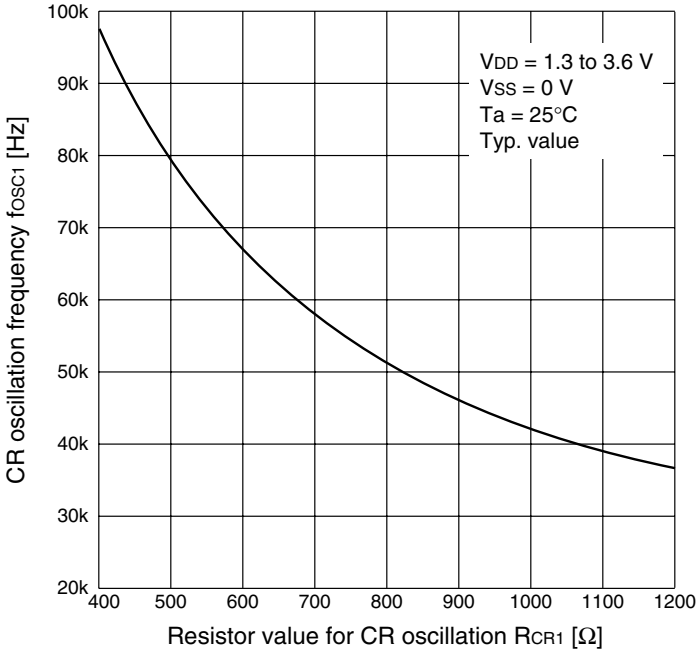
OSC3 CR oscillation circuit

Unless otherwise specified: V_{DD}=1.4 to 3.6V, V_{SS}=0V, Ta=-40 to 85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}	V_{DD}=1.8 to 3.6V (VDC=3), R_{CR2}=constant	-25		25	%
		V_{DD}=1.6 to 3.6V (VDC=2), R_{CR2}=constant	-25		25	%
		V_{DD}=1.4 to 3.6V (VDC=1), R_{CR2}=constant	-25		25	%
Oscillation start time	tsta				100	µs

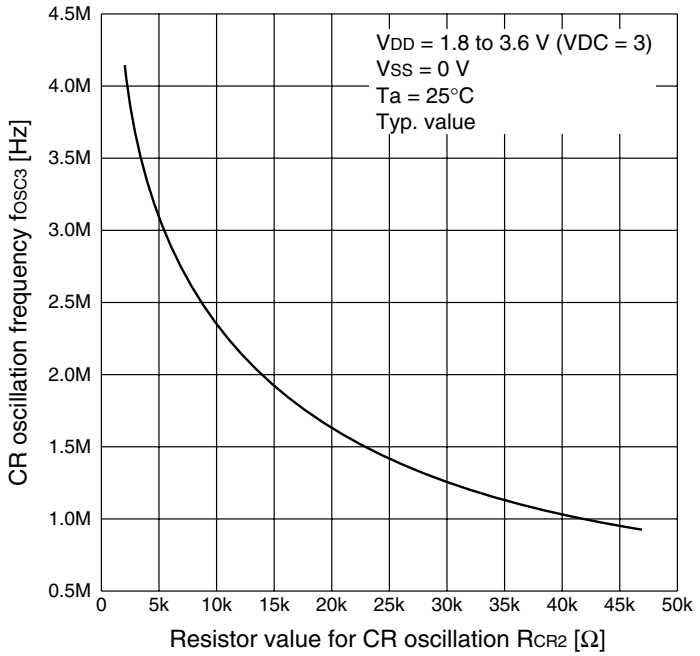
OSC1 CR oscillation frequency-resistance characteristic

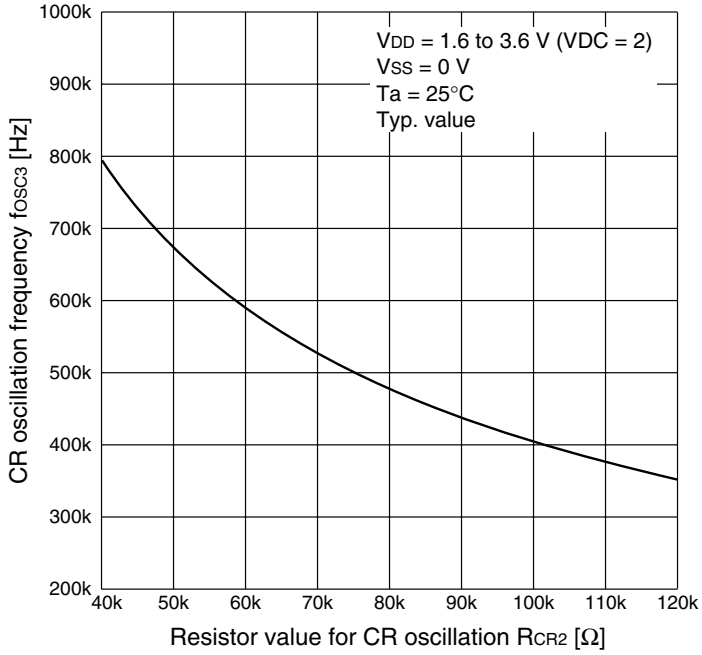
The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.

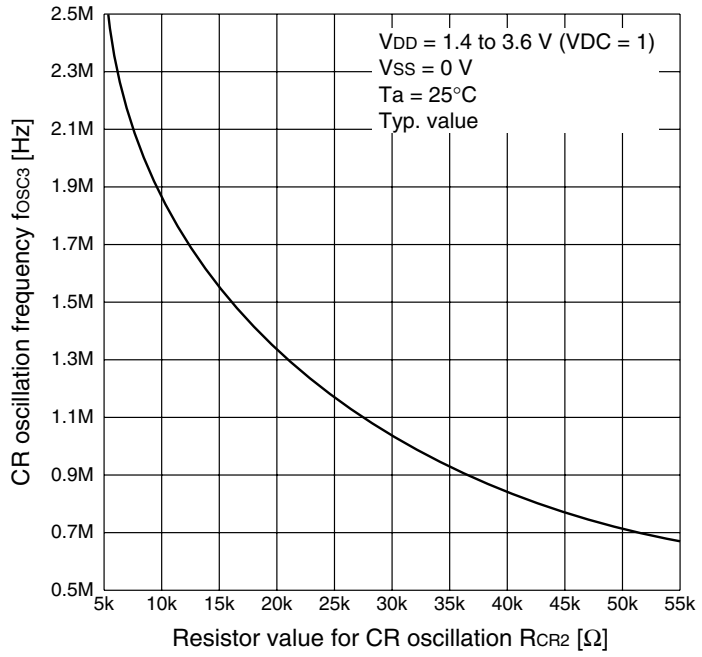


OSC3 CR oscillation frequency-resistance characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.




VDD = 1.6 to 3.6 V (VDC = 2)
VSS = 0 V
Ta = 25°C
Typ. value
CR oscillation frequency fOSC3 [Hz]
1000k
900k
800k
700k
600k
500k
400k
300k
200k
40k
50k
60k
70k
80k
90k
100k
110k
120k
Resistor value for CR oscillation RCR2 [Ω]


VDD = 1.4 to 3.6 V (VDC = 1)
VSS = 0 V
Ta = 25°C
Typ. value
CR oscillation frequency fOSC3 [Hz]
2.5M
2.3M
2.1M
1.9M
1.7M
1.5M
1.3M
1.1M
0.9M
0.7M
0.5M
5k
10k
15k
20k
25k
30k
35k
40k
45k
50k
55k
Resistor value for CR oscillation RCR2 [Ω]

7.6 Serial Interface AC Characteristics

Clock synchronous master mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			5	µs
Receiving data input set-up time	tsms	10			µs
Receiving data input hold time	tsmh	5			µs

• During 1 MHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tsmd			200	ns
Receiving data input set-up time	tsms	400			ns
Receiving data input hold time	tsmh	200			ns

Note that the maximum clock frequency is limited to 2 MHz.

Clock synchronous slave mode

• During 32 kHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			10	µs
Receiving data input set-up time	tsss	10			µs
Receiving data input hold time	tssh	5			µs

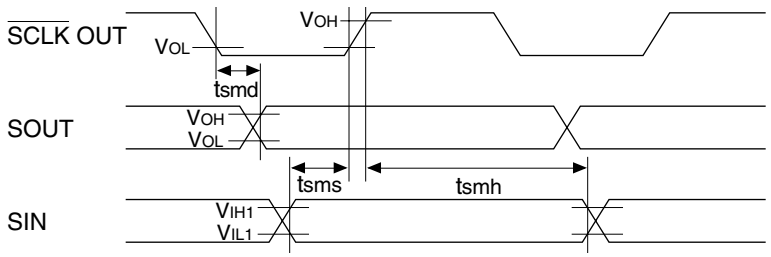
• During 1 MHz operation

Condition: V_{DD}=3.0V, V_{SS}=0V, Ta=-40 to 85°C, V_{IH1}=0.8V_{DD}, V_{IL1}=0.2V_{DD}, V_{OH}=0.8V_{DD}, V_{OL}=0.2V_{DD}

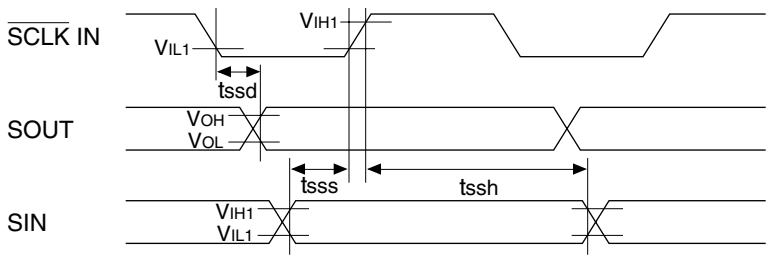
Item	Symbol	Min.	Typ.	Max.	Unit
Transmitting data output delay time	tssd			500	ns
Receiving data input set-up time	tsss	400			ns
Receiving data input hold time	tssh	200			ns

Note that the maximum clock frequency is limited to 2 MHz.

<Master mode>



<Slave mode>



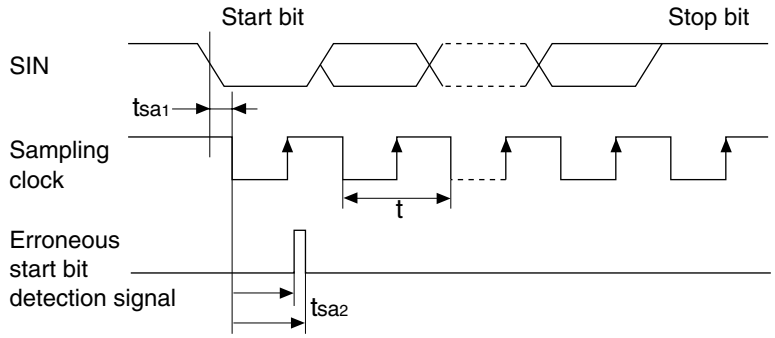
Asynchronous system

Condition: VDD=1.4 to 3.6V, VSS=0V, Ta=-40 to 85°C

Item	Symbol	Min.	Typ.	Max.	Unit
Start bit detection error time *1	t_{SA1}	0		t/16	s
Erroneous start bit detection range time *2	t_{SA2}	9t/16		10t/16	s

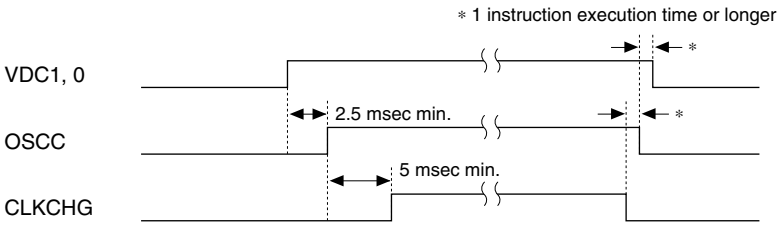
*1 Start bit detection error time is a logical delay time from inputting the start bit until internal sampling begins operating. (Time as far as AC is excluded.)

*2 Erroneous start bit detection range time is a logical range to detect whether a LOW level (start bit) has been input again after a start bit has been detected and the internal sampling clock has started. When a HIGH level is detected, the start bit detection circuit is reset and goes into a wait status until the next start bit. (Time as far as AC is excluded.)



7.7 Timing Chart

System clock switching

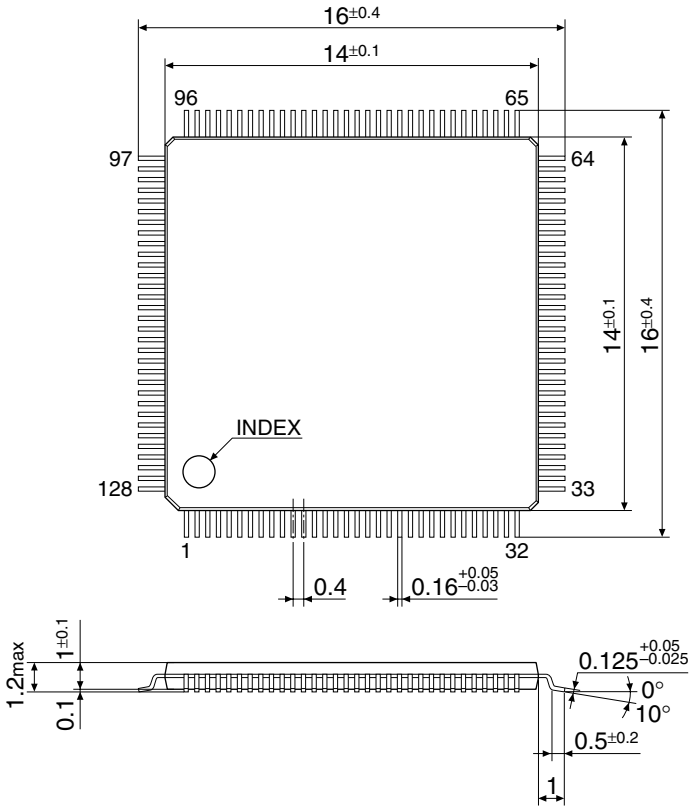


CHAPTER 8 PACKAGE

8.1 Plastic Package

TQFP15-128pin

(Unit: mm)

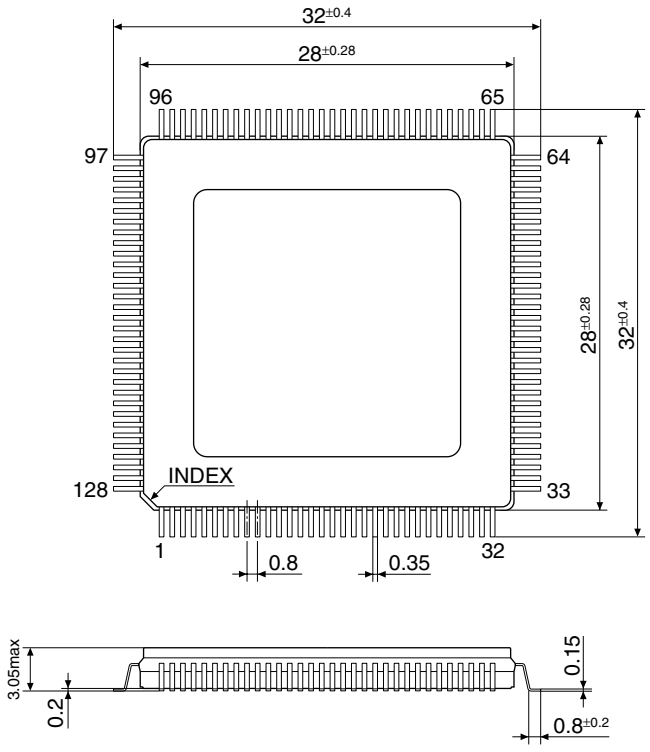


The dimensions are subject to change without notice.

8.2 Ceramic Package for Test Samples

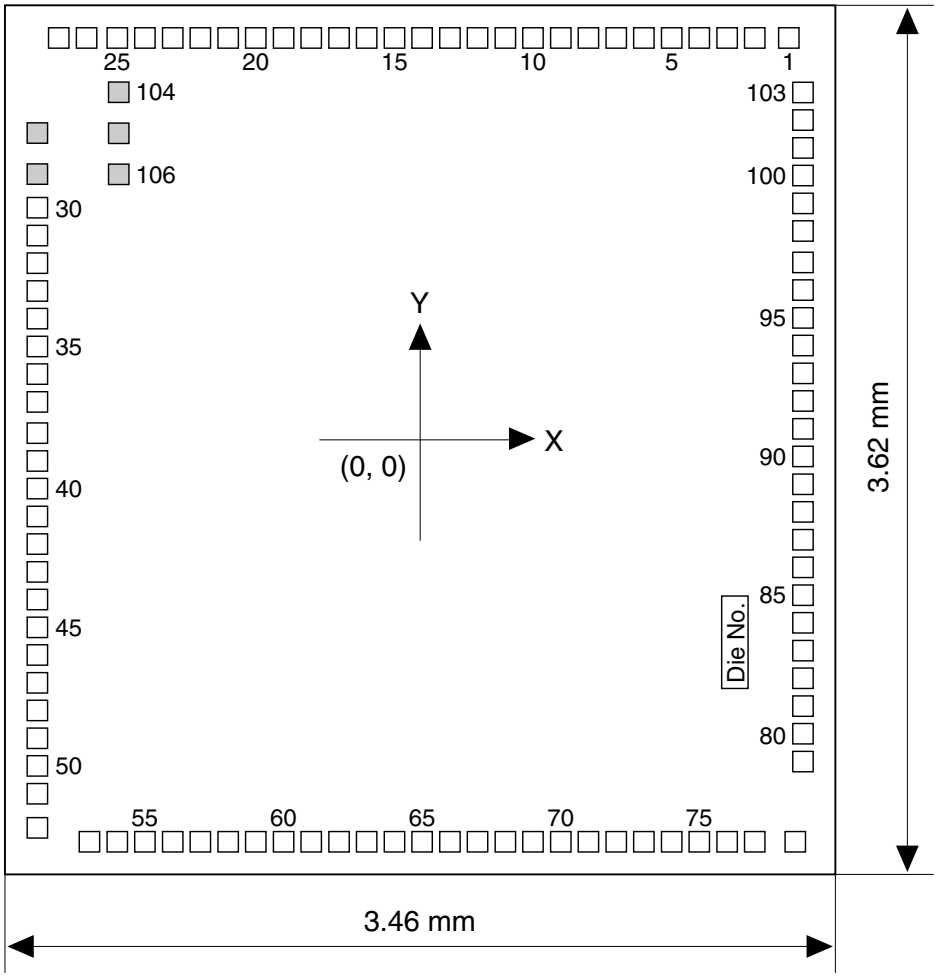
QFP8-128pin

(Unit: mm)



CHAPTER 9 PAD LAYOUT

9.1 Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 100 µm

9.2 Pad Coordinates

Unit: µm

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	CF	1,536	1,674	37	COM7	-1,595	158	73	SEG35	932	-1,674
2	V_{C5}	1,394	1,674	38	SEG0	-1,595	28	74	SEG36	1,048	-1,674
3	V_{C4}	1,279	1,674	39	SEG1	-1,595	-88	75	SEG37	1,163	-1,674
4	V_{C2}	1,163	1,674	40	SEG2	-1,595	-203	76	SEG38	1,279	-1,674
5	V_{C1}	1,048	1,674	41	SEG3	-1,595	-319	77	SEG39	1,394	-1,674
6	K00	932	1,674	42	SEG4	-1,595	-434	78	SEG40	1,563	-1,674
7	K01	817	1,674	43	SEG5	-1,595	-550	79	SEG41	1,595	-1,340
8	K02	701	1,674	44	SEG6	-1,595	-665	80	SEG42	1,595	-1,224
9	K03	586	1,674	45	SEG7	-1,595	-781	81	SEG43	1,595	-1,109
10	R10	470	1,674	46	SEG8	-1,595	-896	82	SEG44	1,595	-993
11	R11	355	1,674	47	SEG9	-1,595	-1,012	83	SEG45	1,595	-878
12	R12	239	1,674	48	SEG10	-1,595	-1,127	84	SEG46	1,595	-762
13	R13	124	1,674	49	SEG11	-1,595	-1,243	85	SEG47	1,595	-647
14	P20	8	1,674	50	SEG12	-1,595	-1,358	86	SEG48	1,595	-531
15	P21	-107	1,674	51	SEG13	-1,595	-1,474	87	SEG49	1,595	-416
16	P22	-223	1,674	52	SEG14	-1,595	-1,616	88	SEG50	1,595	-300
17	P23	-338	1,674	53	SEG15	-1,378	-1,674	89	SEG51	1,595	-185
18	V_{DD}	-454	1,674	54	SEG16	-1,262	-1,674	90	SEG52	1,595	-69
19	V_{D1}	-569	1,674	55	SEG17	-1,147	-1,674	91	SEG53	1,595	46
20	OSC4	-685	1,674	56	SEG18	-1,031	-1,674	92	SEG54	1,595	162
21	OSC3	-800	1,674	57	SEG19	-916	-1,674	93	SEG55	1,595	277
22	V_{OSC}	-916	1,674	58	SEG20	-800	-1,674	94	SEG56	1,595	393
23	OSC2	-1,031	1,674	59	SEG21	-685	-1,674	95	SEG57	1,595	508
24	OSC1	-1,147	1,674	60	SEG22	-569	-1,674	96	SEG58	1,595	624
25	V_{SS}	-1,262	1,674	61	SEG23	-454	-1,674	97	SEG59	1,595	739
26	$\overline{\text{RESET}}$	-1,390	1,674	62	SEG24	-338	-1,674	98	COM8	1,595	870
27	$\overline{\text{TEST}}$	-1,506	1,674	63	SEG25	-223	-1,674	99	CA	1,595	985
28	N.C.	-1,595	1,278	64	SEG26	-107	-1,674	100	CB	1,595	1,101
29	N.C.	-1,595	1,107	65	SEG27	8	-1,674	101	CC	1,595	1,216
30	COM0	-1,595	967	66	SEG28	124	-1,674	102	CD	1,595	1,332
31	COM1	-1,595	851	67	SEG29	239	-1,674	103	CE	1,595	1,447
32	COM2	-1,595	736	68	SEG30	355	-1,674	104	N.C.	-1,256	1,448
33	COM3	-1,595	620	69	SEG31	470	-1,674	105	N.C.	-1,256	1,277
34	COM4	-1,595	505	70	SEG32	586	-1,674	106	N.C.	-1,256	1,106
35	COM5	-1,595	389	71	SEG33	701	-1,674	–			
36	COM6	-1,595	274	72	SEG34	817	-1,674	–			

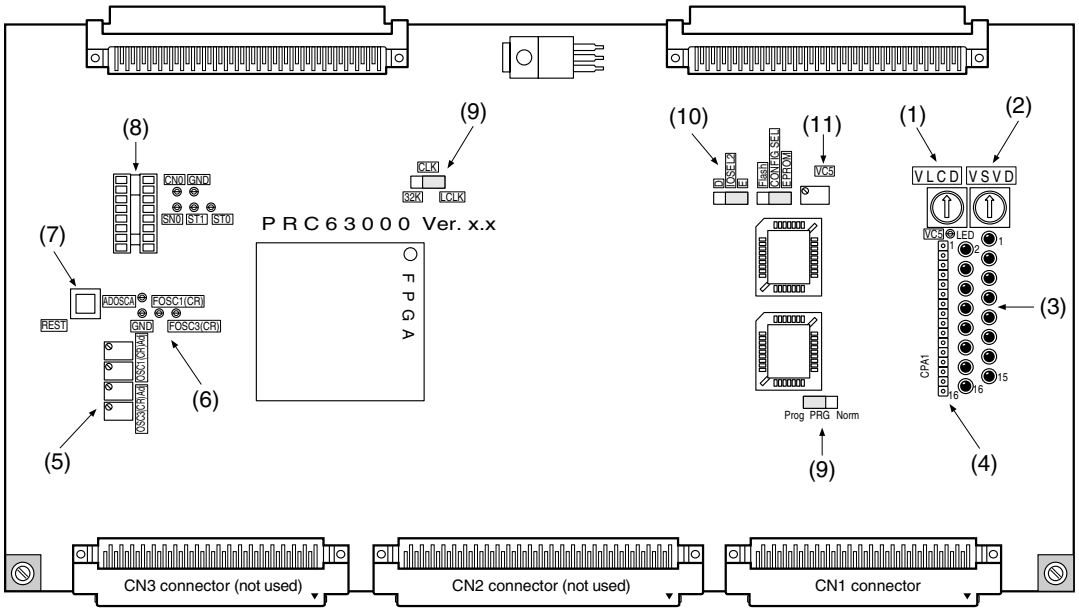
APPENDIX S5U1C63000P MANUAL (PERIPHERAL CIRCUIT BOARD FOR S1C63406)

This manual describes how to use the Peripheral Circuit Board for the S1C63406 (S5U1C63000P), which provides emulation functions when mounted on the debugging tool for the S1C63 Family of 4-bit single-chip microcomputers, the ICE (S5U1C63000H1/S5U1C63000H2).

This description of the S1C63 Family Peripheral Circuit Board (S5U1C63000P) provided in this document assumes that circuit data for the S1C63406 has already been downloaded to the board. For information on downloading various circuit data and on common board specifications, please see the S5U1C63000P Manual (S1C63 Family Peripheral Circuit Board) included with the product. Please refer to the user's manual provided with your ICE for detailed information on its functions and method of use.

A.1 Names and Functions of Each Part

The following explains the names and functions of each part of the board (S5U1C63000P).



(1) VLCD

Unused.

(2) VSVD

This control allows you to vary the power supply voltage artificially in order to verify the operation of the power supply voltage detect function (SVD). Keep in mind that a single control position indicates two voltage values.

SVD levels	0	1	2	3	4	5	6	7
	8	9	10	11	12	13	14	15

(For example, SVD levels 0 and 8 are at the same control position.)

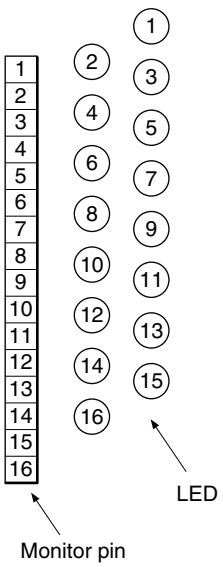
(3) Register monitor LEDs

These LEDs correspond one-to-one to the registers listed below. The LED lights when the data is logic "1" and goes out when the data is logic "0".
VDC0–1, OSCC, CLKCHG, SVDON, SVDDT, HLMOD, LPWR, VCCHG

(4) Register monitor pins

These pins correspond one-to-one to the registers listed below. The pin outputs a high for logic "1" and a low for logic "0".

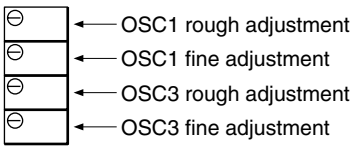
Monitor		LED	
Pin No.	Name	LED No.	Name
1	DONE *	1	DONE *
2	VDC0	2	VDC0
3	VDC1	3	VDC1
4	OSCC	4	OSCC
5	CLKCHG	5	CLKCHG
6	SVDON	6	SVDON
7	SVDDT	7	SVDDT
8	HLMOD	8	HLMOD
9	LPWR	9	LPWR
10	VCCHG	10	VCCHG
11	–	11	–
12	–	12	–
13	–	13	–
14	–	14	–
15	–	15	–
16	–	16	–



∗ DONE: The monitor pin outputs a high while the LED lights when initialization of this board completes without problems.

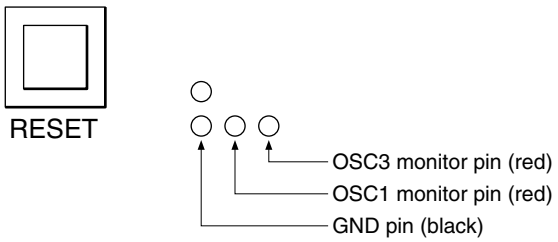
(5) CR oscillation frequency adjusting control

When OSC1 and / or OSC3 are set for a CR oscillation circuit by a mask option, this control allows you to adjust the oscillation frequency. The oscillation frequency can be adjusted in the range of approx. 20 kHz to 500 kHz for OSC1 and approx. 100 kHz to 8 MHz for OSC3. Note that the actual IC does not operate with all of these frequencies; refer to Section 4.3, "Oscillation Circuit", to select the appropriate operating frequency.



(6) CR oscillation frequency monitor pins

These pins allow you to monitor the clock waveform from the CR oscillation circuit with an oscilloscope. Note that these pins always output a signal waveform whether or not the oscillation circuit is operating.



(7) RESET switch

This switch initializes the internal circuits of this board and feeds a reset signal to the ICE.

(8) Monitor pins and external part connecting socket

These parts are currently unused.

(9) CLK and PRG switch

If power to the ICE is shut down before circuit data downloading is complete, the circuit configuration in this board will remain incomplete, and the debugger may not be able to start when you power on the ICE once again. In this case, temporarily power off the ICE and set CLK to the 32K position and the PRG switch to the Prog position, then switch on power for the ICE once again. This should allow the debugger to start up, allowing you to download circuit data. After downloading the circuit data, temporarily power off the ICE and reset CLK and PRG to the LCLK and the Norm position, respectively. Then power on the ICE once again.

(10) IOSEL2

When downloading circuit data, set IOSEL2 to the "E" position. Otherwise, set to the "D" position.

(11) VC5

This control allows fine adjustment of the LCD drive voltage. Note, however, that only the LCD contrast register can adjust the LCD drive voltage in the actual IC.

A.2 Connecting to the Target System

This section explains how to connect the S5U1C63000P to the target system.
To connect this board (S5U1C63000P) to the target system, use the I/O connecting cables supplied with the board (80-pin/40-pin × 2, flat type). Take care when handling the connectors, since they conduct electrical power (V_{DD} = +3.3 V).

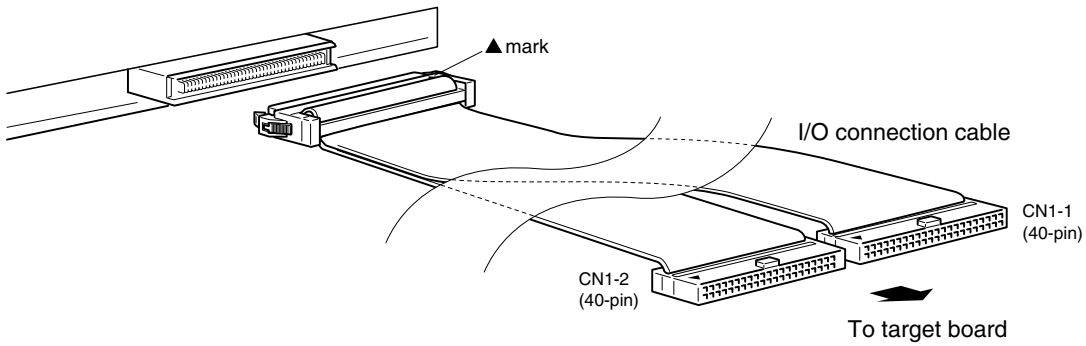


Fig. A.2.1 Connecting the S5U1C63000P to the target system

Table A.2.1 I/O connector pin assignment

40-pin CN1-1 connector		40-pin CN1-2 connector	
No.	Pin name	No.	Pin name
1	VDD (=3.3 V)	1	VDD (=3.3 V)
2	VDD (=3.3 V)	2	VDD (=3.3 V)
3	K00	3	R10
4	K01	4	R11
5	K02	5	R12
6	K03	6	R13
7	Cannot be connected	7	Cannot be connected
8	Cannot be connected	8	Cannot be connected
9	Cannot be connected	9	Cannot be connected
10	Cannot be connected	10	Cannot be connected
11	VSS	11	VSS
12	VSS	12	VSS
13	P20	13	Cannot be connected
14	P21	14	Cannot be connected
15	P22	15	Cannot be connected
16	P23	16	Cannot be connected
17	Cannot be connected	17	Cannot be connected
18	Cannot be connected	18	Cannot be connected
19	Cannot be connected	19	Cannot be connected
20	Cannot be connected	20	Cannot be connected
21	VDD (=3.3 V)	21	VDD (=3.3 V)
22	VDD (=3.3 V)	22	VDD (=3.3 V)
23	Cannot be connected	23	Cannot be connected
24	Cannot be connected	24	Cannot be connected
25	Cannot be connected	25	Cannot be connected
26	Cannot be connected	26	Cannot be connected
27	Cannot be connected	27	Cannot be connected
28	Cannot be connected	28	Cannot be connected
29	Cannot be connected	29	Cannot be connected
30	Cannot be connected	30	ECLK3 *
31	VSS	31	VSS
32	VSS	32	VSS
33	Cannot be connected	33	Cannot be connected
34	Cannot be connected	34	Cannot be connected
35	Cannot be connected	35	Cannot be connected
36	Cannot be connected	36	Cannot be connected
37	Cannot be connected	37	Cannot be connected
38	Cannot be connected	38	$\overline{\text{RESET}}$
39	VSS	39	VSS
40	VSS	40	VSS

*: The ECLK3 pin is only provided for this board to input the OSC3 external clock. This allows you to configure the OSC3 clock with the desired oscillation frequency. However, the OSC3 external clock input to this pin is enabled only when external input is selected by the function option generator.

A.3 Usage Precautions

To ensure correct use of this board (S5U1C63000P), please observe the following precautions.

A.3.1 Operational precautions

(1) Before inserting or removing cables, turn off power to all pieces of connected equipment.

(2) Do not turn on power or load mask option data if all of the input ports (K00–K03) are held low. Doing so may activate the multiple key entry reset function.

(3) Before debugging, always be sure to load mask option data.

A.3.2 Differences with the actual IC

(1) Differences in I/O

<Interface power supply>

This board and target system interface voltage is set to +3.3 V. To obtain the same interface voltage as in the actual IC, attach a level shifter circuit, etc. on the target system side to accommodate the required interface voltage.

<Each output port's drive capability>

The drive capability of each output port on this board is higher than that of the actual IC. When designing application system and software, refer to Chapter 7, "Electrical Characteristics", to confirm each output port's drive capability.

<Each port's protective diode>

All I/O ports incorporate a protective diode for V_{DD} and V_{SS}, and the interface signals between this board and the target system are set to +3.3 V. Therefore, this board and the target system cannot be interfaced with voltages exceeding V_{DD} by setting the output ports for open-drain mode.

<Pull-up resistance value>

The pull-up resistance values on this board are set to 220 kΩ which differ from those for the actual IC. For the resistance values on the actual IC, refer to Chapter 7, "Electrical Characteristics".
Note that when using pull-up resistors to pull the input pins high, the input pins may require a certain period to reach a valid high level. Exercise caution if a key matrix circuit is configured using a combination of output and input ports, since rise delay times on these input ports differ from those of the actual IC.

(2) Differences in current consumption

The amount of current consumed by this board differs significantly from that of the actual IC. Inspecting the LEDs on this board may help you keep track of approximate current consumption. The following factors/components greatly affect device current consumption:

<Those which can be verified by LEDs and monitor pins>

a) Run and Halt execution ratio (verified by LEDs and monitor pins on the ICE)
b) CPU operating voltage change (VDC0, VDC1)
c) OSC3 oscillation on/off (OSCC)
d) CPU clock change (CLKCHG)
e) SVD circuit on/off (SVDON)
f) Heavy load protection mode (HLMOD)
g) LCD power supply on/off (LPWR)
h) LCD constant-voltage change (VCCHG)

<Those that can only be counteracted by system or software>

i) Current consumed by the internal pull-up resistors
j) Input ports in a floating state

(3) Functional precautions

<LCD power supply circuit>

There is a finite delay time from the point at which the LCD power supply circuit (LPWR) turns on until an LCD drive waveform is output. On this board, this delay is set to approx. 125 msec, which differs from that of the actual IC.

<SVD circuit>

- Although the S1C63406 has a function for detecting externally sourced voltages, this board is unable to detect externally sourced voltages. The SVD function is realized by artificially varying the power supply voltage using the VSVD control on this board.
- There is a finite delay time from when the power to the SVD circuit turns on until actual detection of the voltage. On this board, this delay is set to 61–92 µsec, which differs from that of the actual IC. Refer to Section 4.12, "SVD Circuit", when setting the appropriate wait time for the actual IC.

<Oscillation circuit>

- A wait time is required before oscillation stabilizes after the OSC3 oscillation control circuit (OSCC) is turned on. On this board, even when OSC3 oscillation is changed (CLKCHG) without a wait time, OSC3 will function normally. Refer to Section 4.3, "Oscillation Circuit", when setting the appropriate wait time for the actual IC.
- Use separate instructions to switch the clock from OSC3 to OSC1 and to turn off the OSC3 oscillation circuit. If executed simultaneously with a single instruction, these operations, although good with this board, may not function properly well with the actual IC.
- Because the logic level of the oscillation circuit is high, the timing at which the oscillation starts on this board differs from that of the actual IC.
- This board contains oscillation circuits for OSC1 and OSC3. Keep in mind that even though the actual IC may not have a resonator connected to its OSC3, its emulator can operate with the OSC3 circuit.
- It is necessary to select the appropriate operating voltage for the internal circuits before the OSC3 oscillation circuit can be turned on in the actual IC. Be aware that this board can operate normally even if an illegal voltage is selected.
- When using an external clock for OSC3, adjust the amplitude of the clock to 3.3 V ± 5% and the duty ratio to 50% ± 10%, and input it to the ECLK3 pin with V_{SS} as the ground.

<Access to undefined address space>

If any undefined space in the S1C63406's internal ROM / RAM or I / O is accessed for data read or write operations, the read / written value is indeterminate. Additionally, it is important to remain aware that indeterminate state differs between this board and the actual IC. Note that the ICE (S5U1C63000H1 / S5U1C63000H2) incorporates the program break function caused by accessing to an undefined address space.

<Reset circuit>

Keep in mind that the operation sequence from when the ICE and this board are powered on until the time at which the program starts running differs from the sequence from when the actual IC is powered on till the program starts running. This is because this board becomes capable of operating as a debugging system after the user program and optional data are downloaded. When operating the ICE after placing it in free-running mode, always apply a system reset. A system reset can be performed by pressing the reset switch on this board, by a reset pin input, or by holding the input ports low simultaneously.

<Internal power supply circuit>

- Although this board contains the VDC0–1, HLMOD and VCCHG registers, it does not actually exercise power supply control by these register. Refer to respective peripheral sections to set the correct voltage. Also, when switching the control voltages, consult the technical manual to determine the appropriate wait time to be inserted.
- The LCD drive voltage on this board is not identical to that on the actual IC.
- Since the usable operating frequency range depends on the device's internal operating voltage, refer to Section 4.3, "Oscillation Circuit", to ensure that the device will not be operated with an inappropriate combination of the operating frequency and the internal power supply.
- This board has a control (VC5) for fine adjustment of the LCD drive voltage. Note, however, that the actual IC only allows LCD contrast adjustment by software.

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