19-2207; Rev 0; 10/01

Low-Noise, Fibre Channel Transimpedance Amplifiers

General Description

The MAX3275/MAX3277 transimpedance amplifiers provide a compact low-power solution for communication up to 2.125Gbps. They feature 300nA input-referred noise at 2.1GHz bandwidth (BW) with 0.85pF input capacitance. The parts also have 2mAp-p AC input overload.

The MAX3277 is identical to the MAX3275, but with the output polarities inverted for optimum packaging flexibility. Both parts operate from a single 3.3V supply and consume only 83mW. The MAX3275/MAX3277 are compact 24mil x 47mil die and require no external compensation capacitor. A space-saving filter connection is provided for positive bias to the photodiode through an on-chip 600Ω resistor to V_{CC}. These features allow easy assembly into a TO-46 or TO-56 header with a photodiode.

The MAX3275/MAX3277 and MAX3274*/MAX3276* limiting amplifiers provide a two-chip solution for dual-rate, fibre channel receiver applications.

**Future product.*

Applications

Dual-Rate Fibre Channel Optical Receivers

Gigabit Ethernet Optical Receivers

Features

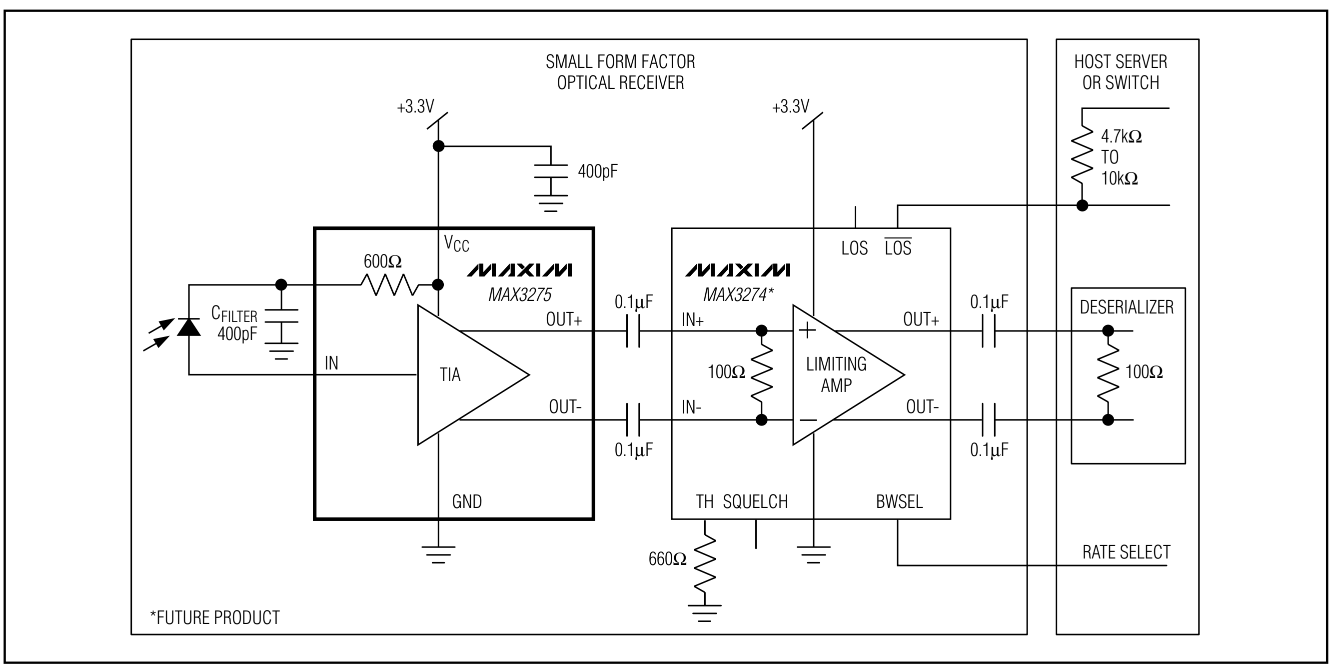
- **Up to 2.125Gbps (NRZ) Data Rates**
- **7psp-p Deterministic Jitter for <100µAp-p Input Current**
- **300nA$_{RMS}$ Input-Referred Noise at 2.1GHz Bandwidth**
- **25mA Supply Current at +3.3V**
- **2.3GHz Small-Signal Bandwidth**
- **2.0mAp-p AC Overload**
- **Die Size: 24mil x 47mil**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3275U/D	0°C to +85°C	Dice**
MAX3277U/D	0°C to +85°C	Dice**

***Dice are guaranteed to operate from 0°C to +85°C, but are tested only at T_A = +25°C.*

Typical Application Circuit



Low-Noise, Fibre Channel Transimpedance Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC})................................-0.5V to +4.0V
Continuous CML Output Current
(OUT+, OUT-) ....-25mA to +25mA
Continuous Input Current (IN)..............................-4mA to +4mA
Continuous Input Current (FILTER).......................-8mA to +8mA
Operating Junction Temperature Range (T_J)....-55°C to +150°C
Storage Ambient Temperature Range (T_{STG}) ...-55°C to +150°C
Die Attach Temperature..+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, source capacitance (C_{IN}) = 0.85pF, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	Including output termination current		25	41	mA
Small-Signal Bandwidth	BW	-3dB, C_{IN} = 0.6pF (Note 3)	2.0	2.7	3.3	GHz
		-3dB, C_{IN} = 0.85pF (Note 3)	1.7	2.3	2.7	
Low-Frequency Cutoff		-3dB, input current = 40µA (Note 3)		65		kHz
Input Bias Voltage					1.0	V
Input Resistance				40		Ω
Input-Referred Noise	I_N	C_{IN} = 0.6pF, BW = 0.8GHz (Notes 3, 4)		185	250	nA_{RMS}
		C_{IN} = 0.6pF, BW = 1.6GHz (Notes 3, 4)		245	350	
		C_{IN} = 0.6pF, BW = 2.1GHz (Notes 3, 4)		275	380	
		C_{IN} = 0.85pF, BW = 0.8GHz (Notes 3, 4)		193	275	
		C_{IN} = 0.85pF, BW = 1.6GHz (Notes 3, 4)		272	400	
		C_{IN} = 0.85pF, BW = 2.1GHz (Notes 3, 4)		300	430	
AC Input Overload		(Notes 3, 5)	2			mAp-p
DC Input Overload		(Note 5)	1			mA
Filter Resistance			510	600	690	Ω
Output Resistance (OUT+, OUT-)		Single-ended	42.5	50	57.5	Ω
Deterministic Jitter	DJ	1mAp-p < input < 2mAp-p (Notes 3, 6, 7)		15	40	psp-p
		100µAp-p < input ≤ 1mAp-p (Notes 3, 6, 7)		15	31	
		10µAp-p < input ≤ 100µAp-p (Notes 3, 6, 7)		7	16	
Transimpedance		Differential output	2.8	3.3	3.8	kΩ
Transimpedance Linear Range		0.95 < linearity < 1.05 (Note 8)	50			µAp-p
Data Output Swing		Input > 100µAp-p (Note 9)	220	300	500	mVp-p
Output Data-Transition Time		Input > 200µAp-p, 20% to 80% rise/fall time (Notes 3, 10)		90	140	ps
Output Return Loss		Freq ≤ 1GHz		15		dB
		1GHz < freq ≤ 2GHz		10		
Power-Supply Rejection	PSR	f < 1MHz (Note 11)		40		dB
		1MHz ≤ f < 10MHz (Note 11)		34		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, source capacitance (C_{IN}) = 0.85pF, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

Note 1: Die parameters are production tested at room temperature only, but are guaranteed by design and characterization from 0°C to +85°C.

Note 2: Source capacitance represents the total capacitance at the IN pad during characterization of the noise and bandwidth parameters.

Note 3: Guaranteed by design and characterization.

Note 4: Measured using an RF-power meter with no pattern applied at the input. The TIA output is bandwidth limited for measurement using a 4th-order Bessel Thompson filter. The -3dB frequency of the filter matches the frequency (0.8GHz, 1.6GHz, or 2.1GHz) for the specified noise BW.

Note 5: DC offset and deterministic jitter may exceed specification if AC or DC overload conditions are exceeded.

Note 6: Using fibre channel K28.5± pattern. The input bandwidth is limited to 0.75 × (2.125Gbps) by a 4th-order Bessel Thompson filter. Measured differentially across an AC-coupled 100Ω external load.

Note 7: K28.5± pattern: (00111110101100000101).

Note 8: Gain may vary ±5% relative to reference measured with 30µAp-p input.

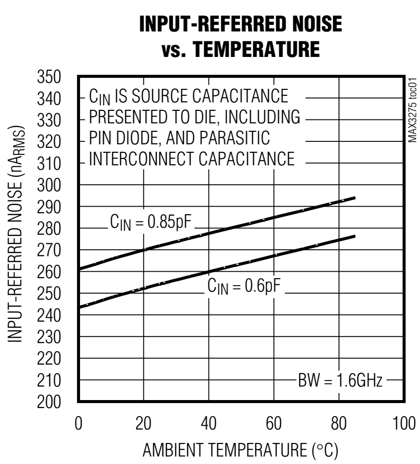
Note 9: Production tested with 1mAp-p input.

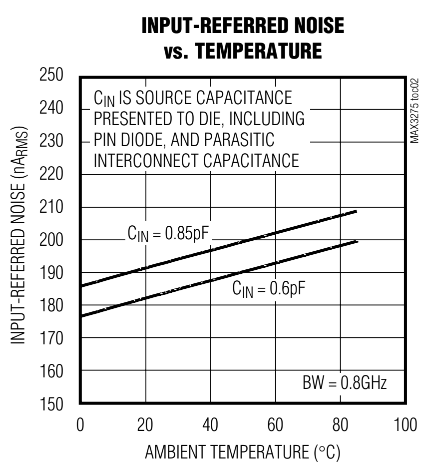
Note 10: Using a K28.7 (0011111000) pattern. Measured differentially across an AC-coupled 100Ω external load.

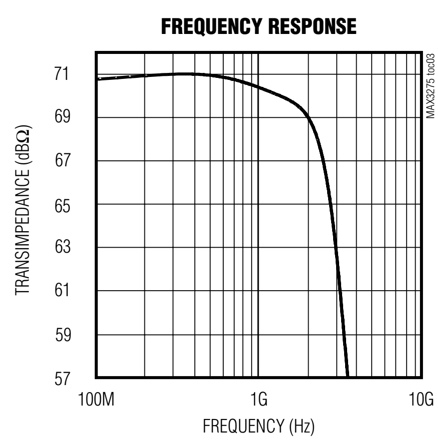
Note 11: Power-supply rejection PSR = -20log($\Delta V_{OUT}/\Delta V_{CC}$), where ΔV_{OUT} is the differential output voltage and ΔV_{CC} is the noise on V_{CC}.

Typical Operating Characteristics

(V_{CC} = +3.3V, C_{IN} = 0.85pF, T_A = +25°C, unless otherwise noted.)

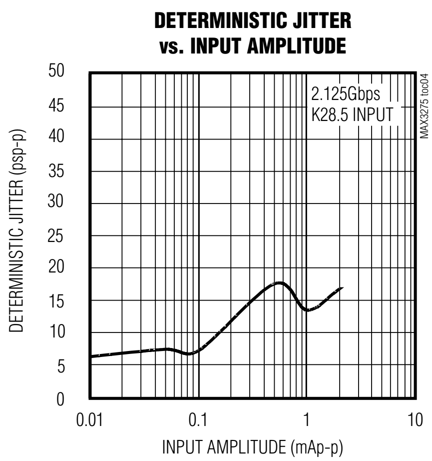


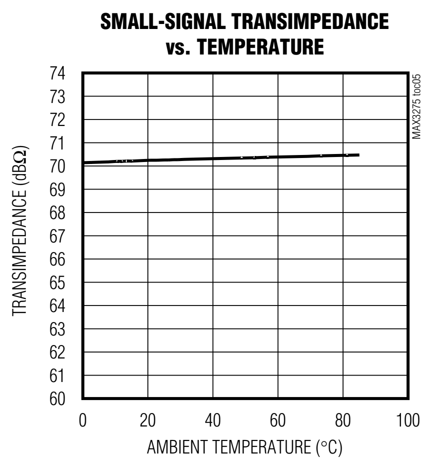


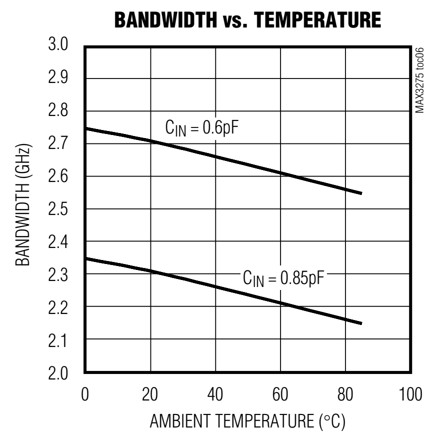


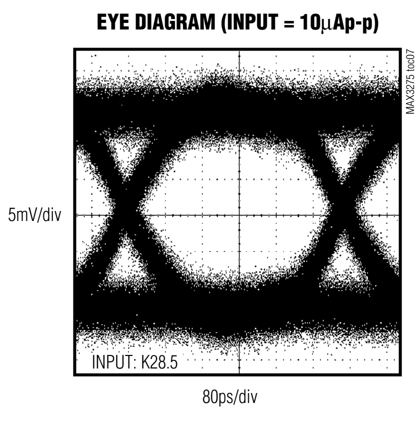
Typical Operating Characteristics (continued)

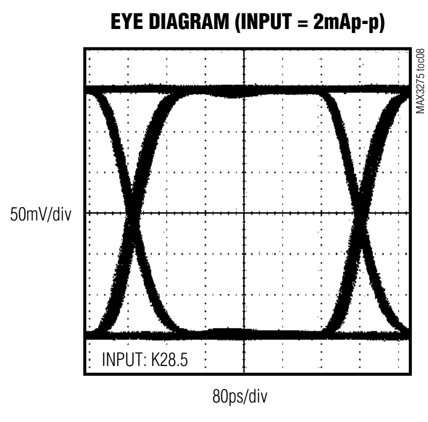
(V_{CC} = +3.3V, C_{IN} = 0.85pF, T_A = +25°C, unless otherwise noted.)

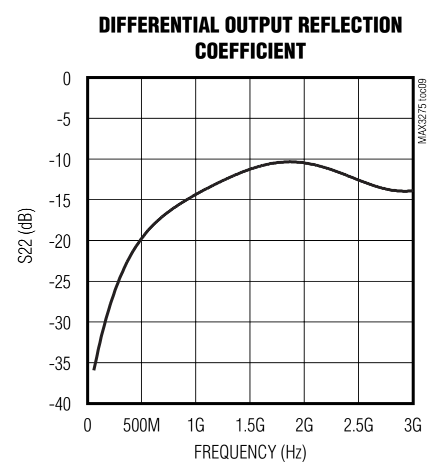


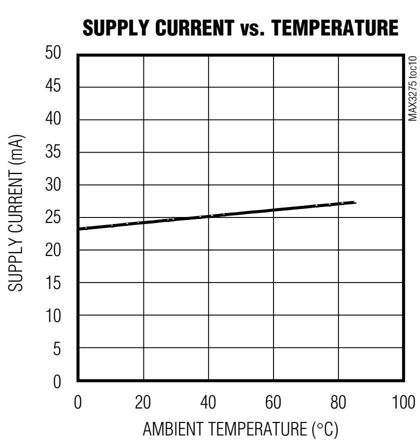


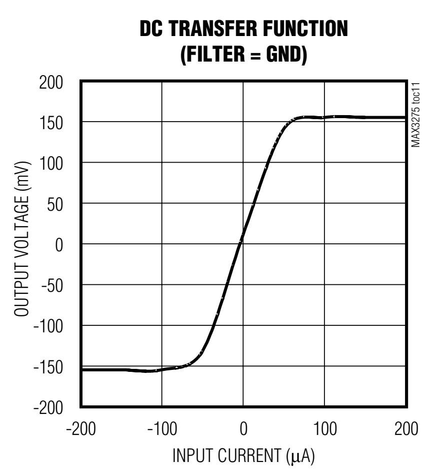












Pad Description

MAX3275 BOND PAD	MAX3277 BOND PAD	NAME	FUNCTION
1, 9	1, 9	V_{CC}	Supply Voltage
2, 5	2, 5	GND	Circuit Ground
3	4	OUT-	Inverting Data Output. Current flowing into IN causes the voltage at OUT- to decrease.
4	3	OUT+	Noninverting Data Output. Current flowing into IN causes the voltage at OUT+ to increase.
6	6	N.C.	No Connection. Not internally connected.
7	7	FILTER	Provides bias voltage for the photodiode through a 600Ω resistor to V_{CC}. When grounded, this pin disables the DC cancellation amplifier to allow a DC path from IN to OUT+ and OUT- for testing.
8	8	IN	TIA Input. Signal current from photodiode flows into this pin.

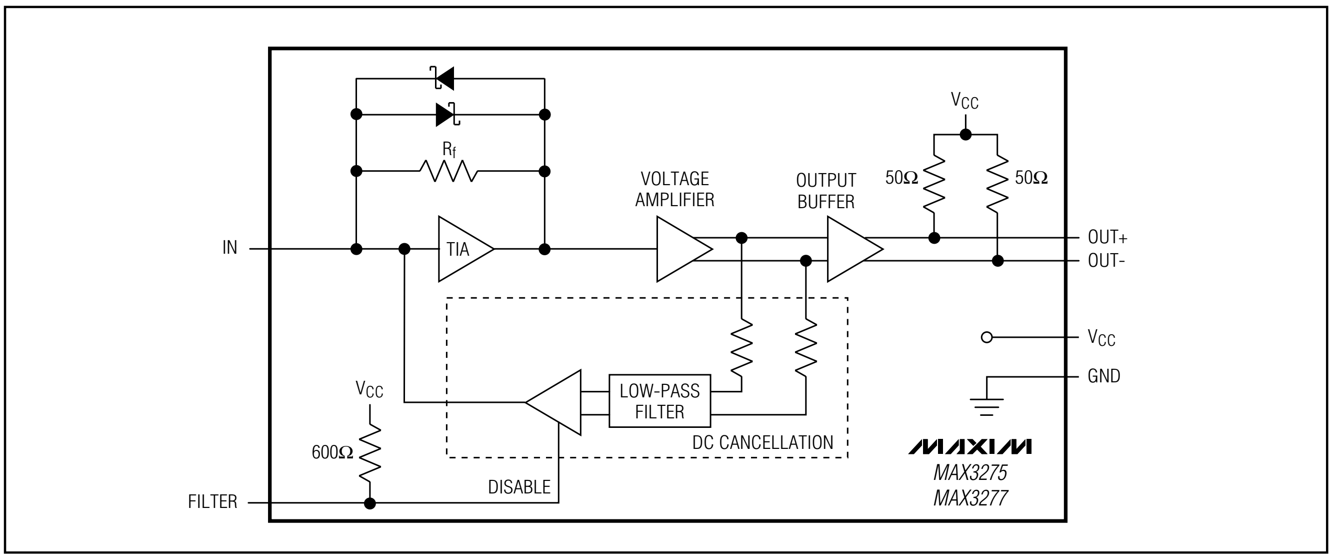


Figure 1. Functional Diagram

Detailed Description

The MAX3275/MAX3277 are transimpedance amplifiers designed for up to 2.125Gbps fibre channel applications. A functional diagram of the MAX3275/MAX3277 is shown in Figure 1. The MAX3275/MAX3277 comprises a transimpedance amplifier stage, a voltage amplifier stage, an output buffer, and a direct-current feedback cancellation circuit.

Transimpedance Amplifier Stage

The signal current at the input flows into the summing node of a high-gain amplifier. Shunt feedback through the resistor R_F converts this current to a voltage. In parallel with the feedback are two back-to-back Schottky diodes that clamp the output signal for large input currents as shown in Figure 2.

Voltage Amplifier Stage

The voltage amplifier stage provides gain and converts the single-ended input to differential outputs.

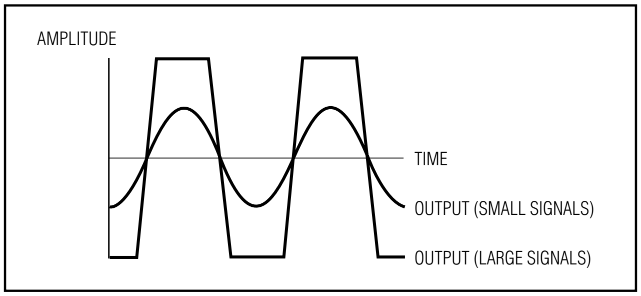


Figure 2. MAX3275/MAX3277 Limited Output

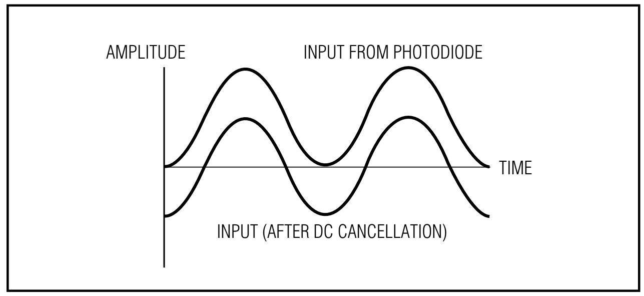


Figure 3. DC Cancellation Effect on Input

Output Buffer

The output buffer provides a reverse-terminated voltage output. The buffer is designed to drive a 100Ω differential load between OUT+ and OUT-. The output current is divided between internal 50Ω resistors and the external load resistor.

For optimum supply-noise rejection, the MAX3275/MAX3277 should be terminated with a differential load. If a single-ended output is required, the unused output should be terminated in a similar manner. The MAX3275/MAX3277 will not drive a DC-coupled, 50Ω grounded load; however, it will drive a compatible 50Ω CML input.

DC Cancellation Circuit

The direct-current (DC) cancellation circuit uses low-frequency feedback to remove the DC component of the input signal (Figure 3). This feature centers the input signal within the transimpedance amplifier's linear range, thereby reducing pulse-width distortion caused by large input signals. Pulse-width distortion in small signals will not be corrected.

The DC cancellation circuit is internally compensated and therefore does not require external capacitors. This circuit minimizes pulse-width distortion for data sequences that exhibit a 50% mark density and 8b/10b coding. A mark density significantly different from 50% will cause the MAX3275/MAX3277 to generate pulse-width distortion.

DC cancellation current is drawn from the input and creates noise. For low-level signals with little or no DC component, the added noise is insignificant.

Applications Information

Optical Power Relations

Many of the MAX3275/MAX3277 specifications relate to the input signal amplitude. When working with optical receivers, the input is sometimes expressed in terms of average optical power and extinction ratio. Figure 4 and Table 1 show relations that are helpful for converting optical power to input signal when designing with the MAX3275/MAX3277. (Refer to Application note HFAN–3.0.0 *Accurately Estimating Optical Receiver Sensitivity*.)

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P_0 + P_1)/2$
Extinction Ratio	r_e	$r_e = P_1/P_0$
Optical Power of a 1	P_1	$P_1 = 2P_{AVG}(r_e)/(r_e + 1)$
Optical Power of a 0	P_0	$P_0 = 2P_{AVG}/(r_e + 1)$
Signal Amplitude	P_{IN}	$P_{IN} = P_1 - P_0$ $P_{IN} = 2P_{AVG}(r_e - 1)/(r_e + 1)$

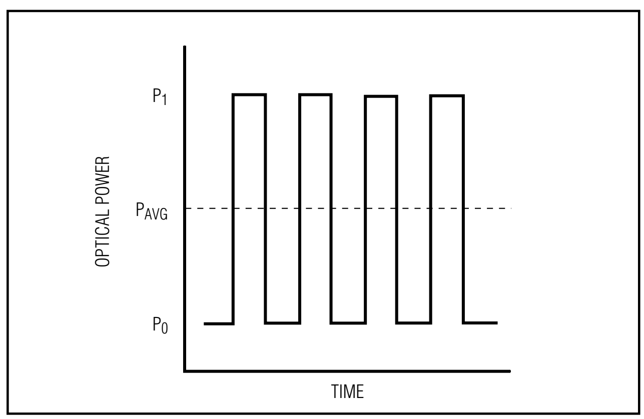


Figure 4. Optical Power Relations

Optical Sensitivity Calculation

The input-referred RMS noise current (I_N) of the MAX3275/MAX3277 generally determines the receiver sensitivity. To obtain a system bit error rate (BER) of 1E-12, the signal-to-noise ratio must always exceed 14.1. The input sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\ \log\left(\frac{14.1 I_N (r_e + 1) \times 1000}{2\rho (r_e - 1)}\right) \text{dBm}$$

where ρ is the photodiode responsivity in A/W and I_N is RMS current in Amps.

Input Optical Overload

The overload is the largest input that the MAX3275/MAX3277 accept while meeting specifications. The optical overload can be estimated in terms of average power with the following equation:

$$\text{Overload} = 10\ \log\left(\frac{(2E-3)\,(r_e + 1) \times 1000}{2\rho (r_e - 1)}\right) \text{dBm}$$

Optical Linear Range

The MAX3275/MAX3277 have high gain, which limits the output when the input signal exceeds 50µAp-p. The MAX3275/MAX3277 operate in a linear range (10% linearity) for inputs not exceeding:

$$\text{Linear Range} = 10\ \log\left(\frac{(50E-6)\,(r_e + 1) \times 1000}{2\rho (r_e - 1)}\right) \text{dBm}$$

Layout Considerations

Noise performance and bandwidth will be adversely affected by capacitance at the IN pad. Minimize capacitance on this pad and select a low-capacitance photodiode. Assembling the MAX3275/MAX3277 in die form using chip and wire technology provides the best possible performance. Figure 5 shows a suggested layout for a TO header for the MAX3275/MAX3277. Special care should be taken to ensure that ESD at IN does not exceed 500V.

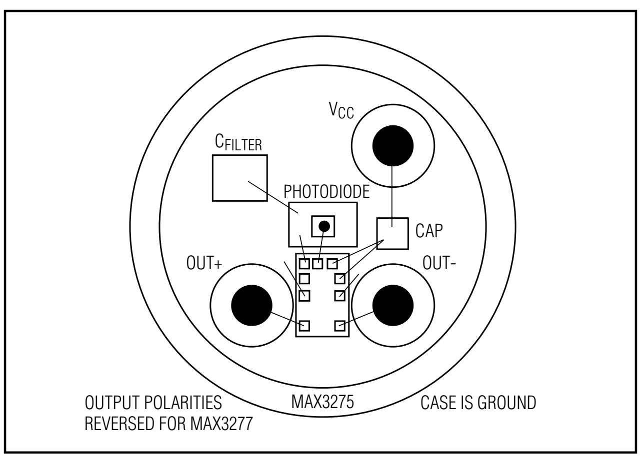


Figure 5. Suggested Layout for TO-46 Header

Photodiode Filter

Supply voltage noise at the cathode of the photodiode produces a current $I = C_{PD}\ \Delta V/\Delta t$, which reduces the receiver sensitivity (C_{PD} is the photodiode capacitance). The filter resistor of the MAX3275/MAX3277, combined with an external capacitor, can be used to reduce this noise (see the *Typical Application Circuit*). Current generated by supply noise voltage is divided between C_{FILTER} and C_{PD}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(C_{FILTER})$$

If the amount of tolerable noise is known, the filter capacitor can be easily selected:

$$C_{FILTER} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(I_{NOISE})$$

For example, with maximum noise voltage = 100mVp-p, C_{PD} = 0.85pF, R_{FILTER} = 600Ω, and I_{NOISE} selected to be 350nA:

$$C_{FILTER} = (100mV)(0.85pF) / (600\Omega)(350nA) = 400pF$$

Wire Bonding

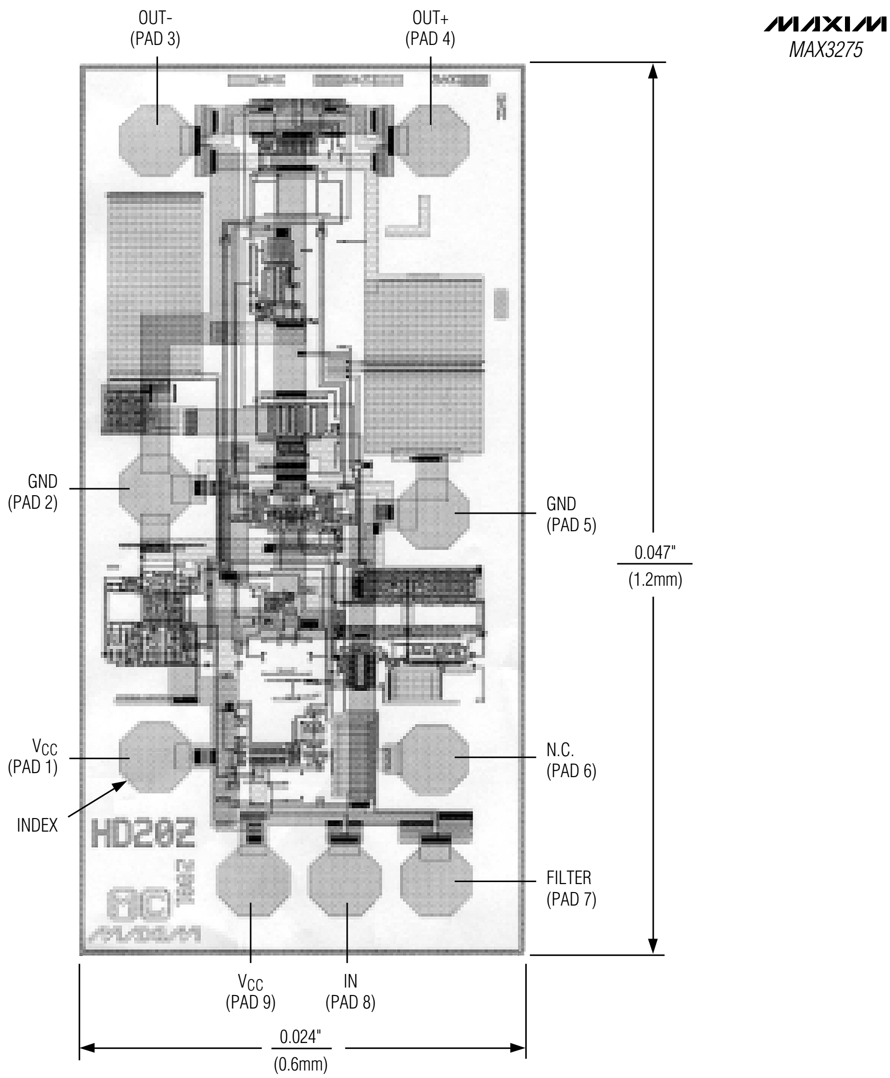
For high-current density and reliable operation, the MAX3275/MAX3277 use gold metalization. Connections to the die should be made with gold wire only, using ball-bonding techniques. Wedge bonding is not recommended. Die thickness is typically 15mils (0.4mm).

Pad Coordinates

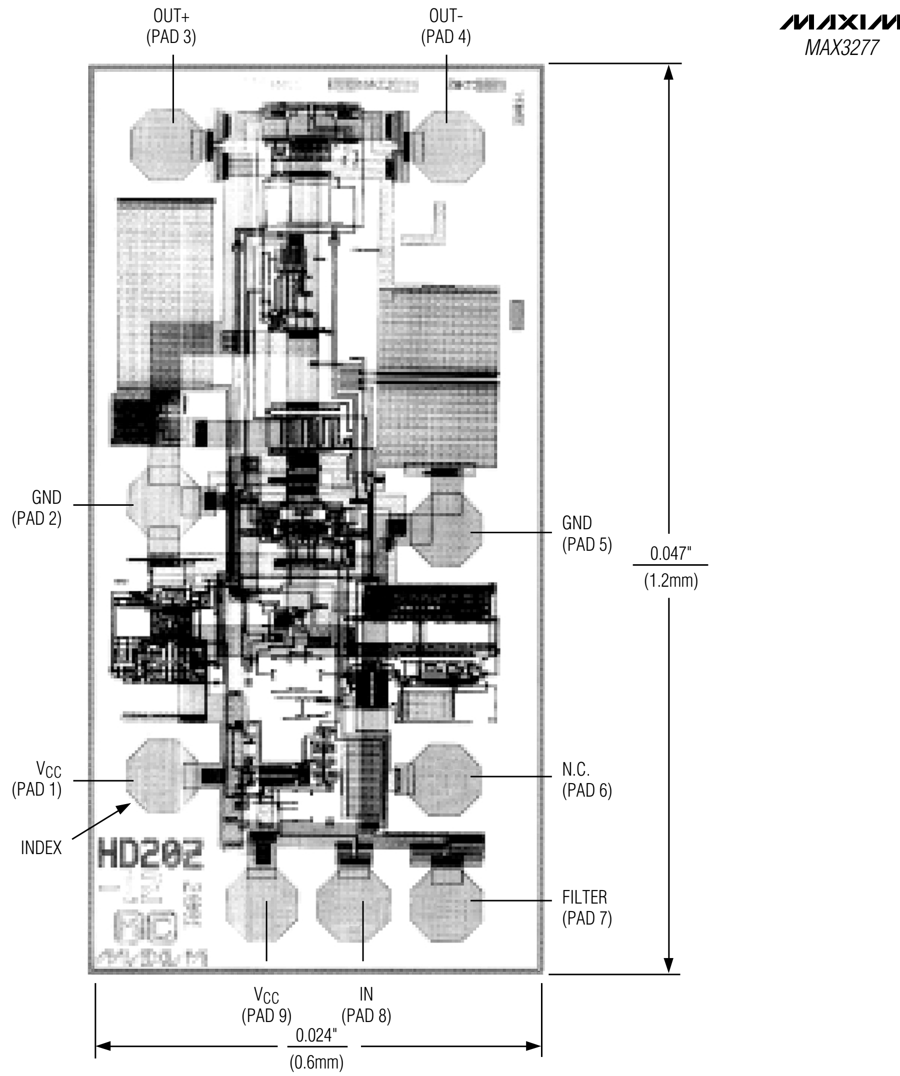
PAD#	COORDINATES (µm)
1	16, 39
2	16, 372
3	16, 806
4	358, 806
5	358, 341
6	358, 36
7	362, -116
8	250, -116
9	138, -116

Low-Noise, Fibre Channel Transimpedance Amplifiers

Chip Topographies



Chip Topographies (continued)



Chip Information

TRANSISTOR COUNT: 301

SUBSTRATE: ISOLATED

PROCESS: SiGe BIPOLAR