MINDSPEED
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1.25Gbps Limiting Amplifier   MC2046-2/C

Postamplifier/Quantiser for Gigabit Ethernet and Fiber Channel Applications

Main Features:

- Low-cost IC, available as die or in QSOP16 and TSSOP20 packages. Fabricated in advanced sub-micron BiCMOS process.
- Very wide range of operation; suitable for up to 1.5Gbps. 4mV input sensitivity at 1.25Gbps.
- Pin-compatible, superior replacement for Motorola MC10SX1125
- Microcosm MC2044C/MC2045-2 Pin-Compatible.
- Programmable input-signal level detect. (On-chip default, saving external components)
- Fully differential
- 3.3 volt operation. (5v supported)
- CMOS and PECL Link-Status variants.

Ordering Information

| Part Number	Pin Package
MC2046CT20	TSSOP20
MC2046T20	TSSOP20
MC2046Q16	QSOP16
MC2046CQ16	QSOP16
MC2046DIEWP	Waffle Pack
MC2046WAFER	Expanded whole 8" on a 10" grip ring

General Description:

The MC2046-2/C is a 2nd-generation, integrated, high gain limiting amplifier intended for high speed fiberoptics based communications. Normally placed following the photodetector and transimpedance or pre-amplifier, the limiting amplifier provides the necessary gain to give PECL compatible logic outputs.

The MC2046-2/C also includes a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled.

Capable of operating over a very wide frequency range, the MC2046-2 supports most fiberoptic industry standards, but it is especially suited to 1.06Gbps Fiber Channel and 1.25Gbps Ethernet. It is pin and functionally compatible with the Motorola MC10SX1125 and earlier Microcosm Post-amplifiers.

The MC2046-2 die has both PECL and CMOS Status outputs. Packaged, the MC2046-2 has PECL Status outputs and the MC2046-2C has CMOS Status outputs.
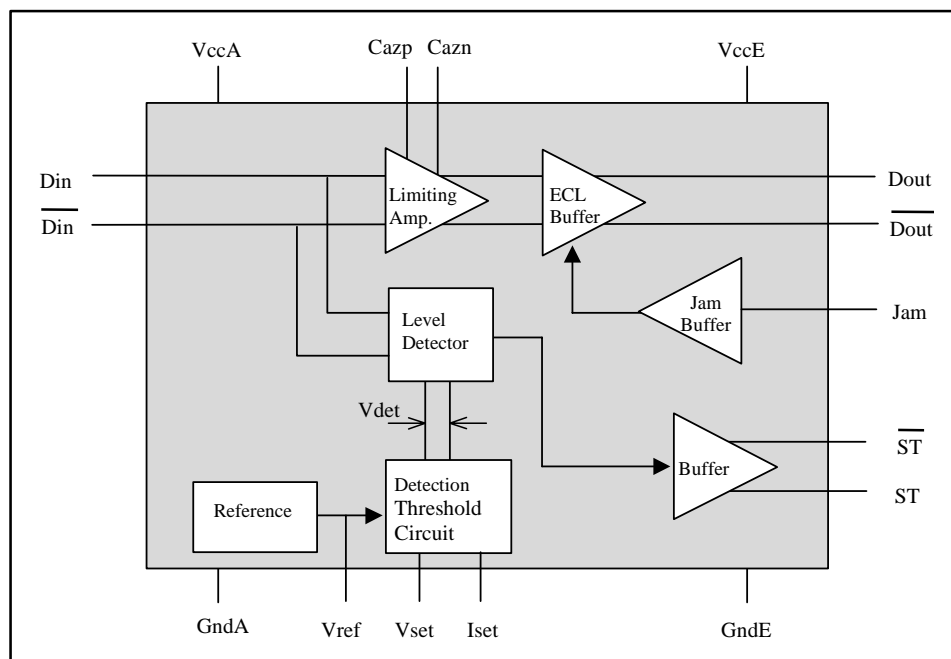
Pin descriptions

TSSOP 20 Or Die Pin No.	QSOP16 Pin No.	Name	Function
1	1	Cazn	Auto-zero capacitor pin. Connect Caz between this pin and Pin2.
2	2	Cazp	See Pin 1
3	-	Iset	May be left unconnected or else may connect resistor for programming threshold detection level – See description of Detection Threshold Circuit.
4	3	GndA	Ground pin for analogue section. Connect to most negative supply. Must be at same potential as GndE.
5	4	Din	Differential Data Input.
6	5	Dinb	Inverse Differential Data Input
7	6	VccA	Supply pin for analogue section. Connect to most positive supply. Must be at the same potential as VccE
8	7	Vref	Test point for on-chip voltage reference. This pin may be left unconnected or else a capacitor may be connected between this pin and the positive supply.
11	8	Jam	ECL and CMOS compatible logic input. When HIGH, data outputs Dout and Doutb are disabled (Dout being held LOW and Doutb being held HIGH).
12	9	STb[1]	Signal detect status output. LOW when input signal level is above detection threshold. This output may be connected to the Jam input pin.
13	10	ST[1]	Signal detect status output. HIGH when input signal level is above detection threshold.
14,15	11	GndE	Ground pin for PECL output stage. Connect to the most negative supply. Must be at the same potential as GndA
16	12	Doutb	PECL compatible differential data output. In phase with input Dinb-Din.
17	13	Dout	PECL compatible differential data output. In phase with input Din-Dinb.
18,19	14	VccE	Supply pin for PECL output stage. Connect to the most positive supply. Must be at the same potential as VccA.
20	16	Vset	Input threshold-level setting circuit. Connect to Analogue Ground via a resistor. See Application diagram. Must be connected to ground even if function not required.

[1] MC2046-2 - ECL outputs are 100k compatible. MC2046-2C - CMOS output levels.

Absolute maximum ratings

Symbol	Parameter	Rating	Units
Vcc	Power supply (Vcc-Gnd)	6	V
Ta	Operating ambient	-40 to +85	°C
Tstg	Storage temperature	-65 to +150	°C

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Recommended operating conditions

Symbol	Parameter	Rating	Units
Vcc	Power supply (Vcc-Gnd)	3.0 to 5.5	V
Ta	Operating ambient	-40 to +85	°C

DC Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter		Min.	Typ.	Max.	Units
Vin	Minimum input signal	Single-ended	-	-	0.002	Vp
		Differential	-	-	0.004	Vp-p
	Maximum input signal	Single-ended	1	-	-	Vp
		Differential	2	-	-	Vp-p
Vos	Input offset voltage		-	-	tba	µV
Vn	Input RMS noise		-	-	93	µV
Vth	Level detect programmability	min	-	-	2	mVp-p
		max	100	-	-	mVp-p
Vhys	Level detect hysteresis (optical)		1.75	2.25	2.75	dB
Iinl	JAM input current (at 0V)		-10	-	10	µA
V_{OH}	Data output HIGH		-1.051	-	-0.879	V
V_{OL}	Data output LOW		-1.892	-	-1.548	V
V_{OH}-V_{OL}	Differential Data output		0.627	-	0.879	V
Icc	Supply current (no ECL loads)		-	-	40	mA

AC Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter	Min.	Typ.	Max.	Units
BWL	Lower -3dB frequency	-	-	3	KHz
BWU	Upper -3dB frequency	1000	-	-	MHz
Rin	Differential input resistance	2.8	-	9.7	kOhms
Cin	Input capacitance	-	-	2	pF
Tpwd	Pulse Width Distortion	-	-	30	pS
Tr,Tf	ECL out rise/fall times (20-80% points)	-	200	250	pS
Raz	Auto-zero output resistance	-	25	-	kOhms
Tld	Level detect time constant	0.5	1	2.0	µS

Microcosm MC2046-2/MC2046-2C/MC2044C compatibility

The MC2046-2/C and MC2044C are pin-compatible and functionally identical, except that the MC2044C has lower internal bandwidth to improve input sensitivity. In all cases, the C suffix indicates CMOS level Link-Status outputs, while the absence of the C indicates PECL levels.

Signal Path Description

Input biasing
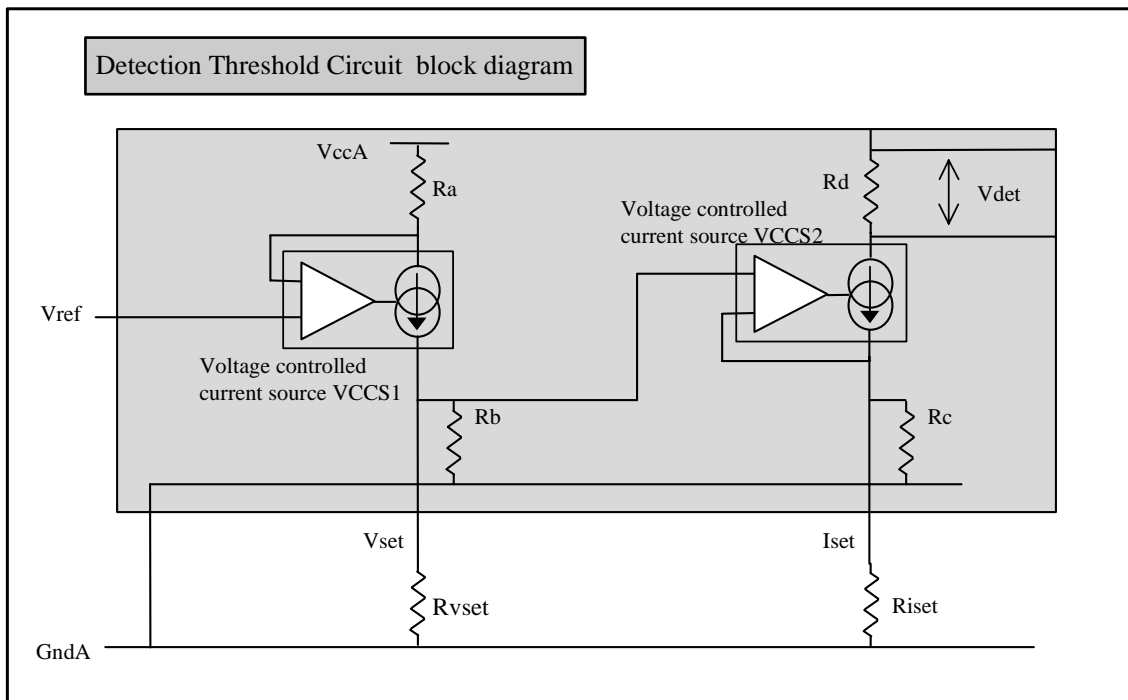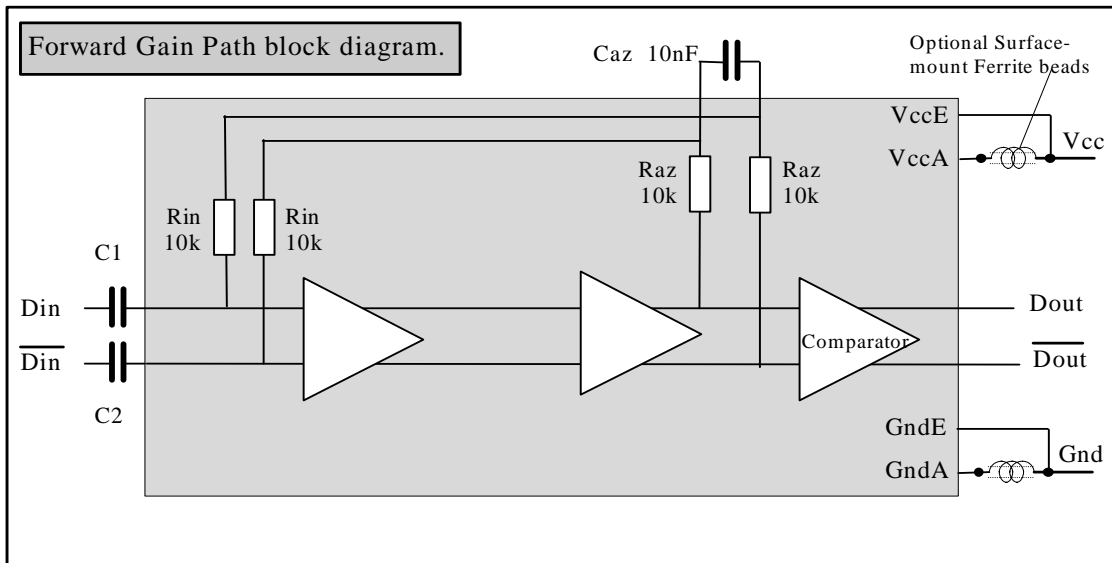
The Data Input pins are internally DC biased at approx. $VccA - 1V$, via the Rin resistors. Although the MC2046-2 can be DC coupled, normally it will be AC coupled, using capacitors C1 & C2. Note that Rin and C1,2 form a filter to low frequencies. The capacitors must therefore be large enough to pass the lowest input frequencies (consecutive '1's or '0's) of interest. For example, setting C1,2 to 10nF will give a typical -3dB point of approx. 10KHz.

Autozero circuit

The MC2046-2 includes an autozero circuit. In the absence of data, the feedback amplifier and summing circuit cancel the inherent offset voltage of the signal path, keeping the comparator at its toggle point. The time constant of this circuit is set by the combination of Raz and Caz, but is not critical. Caz is normally set to 100nF.

Power supply decoupling & optimising sensitivity

Generally, a 4-layer board is required to achieve maximum sensitivity. A good layout on a 4+ layer board should mean ferrite suppressors (as shown) are unnecessary. Contact Microcosm for further assistance in this area.

Forward Gain Path block diagram.

Caz 10nF

Optional Surface-mount Ferrite beads

VccE

VccA

Vcc

Raz 10k

Raz 10k

Rin 10k

Rin 10k

C1

Din

$\overline{\text{Din}}$

C2

Comparator

Dout

$\overline{\text{Dout}}$

GndE

GndA

Gnd

Detection Threshold Circuit block diagram

VccA

Ra

Rd

Vdet

Voltage controlled current source VCCS2

Vref

Voltage controlled current source VCCS1

Rb

Rc

Vset

Iset

Rvset

Riset

GndA

Level detector

The MC2046-2 provides for programmable input-signal level detection, and this may be used to automatically force the Data Outputs to a known state if the input signal falls below threshold. This is normally used to allow data to propagate only when the signal is above the users' Bit-Error-Rate (BER) requirement. It therefore also stops the data outputs toggling due to noise when no signal is present.

Referring to the block diagram shown on the front page, the Detection Threshold Circuit produces a differential signal "Vdet". The Level Detector compares the input differential peak amplitude with this voltage. The Detection Threshold Circuit is shown here in detail.

Vref is 0.5V below VccA. R_{vset} and R_{iset} are optional and, if connected, appear in parallel with on-chip resistors R_b and R_c, respectively. For the following, let R_b' be the parallel combination of R_b and R_{vset}, and let R_c' be the parallel combination of R_c and R_{iset}.

Voltage controlled current source VCCS1 causes the current through R_a to be 0.5V/R_a. The voltage at pin Vset is defined by this current and resistance R_b'. This voltage is applied across resistance R_c' by voltage controlled current source VCCS2. The current through R_d is thus defined and the voltage Vdet is given by:

$$\text{Vdet} = 0.5\text{V} \frac{R_b'.R_d}{R_a.R_c'}$$

The nominal values of the on-chip resistors are

R_a	2.8KΩ
R_b	5.6KΩ
R_c	1.2KΩ
R_d	60Ω

The absolute values of these resistors have uncertainty of +/-20%, however the ratios are well defined.

With neither Rvset nor Riset connected:

Detection Level = Vdet = 50mV (i.e. 50mV diff peak or 100mVdiff peak - peak
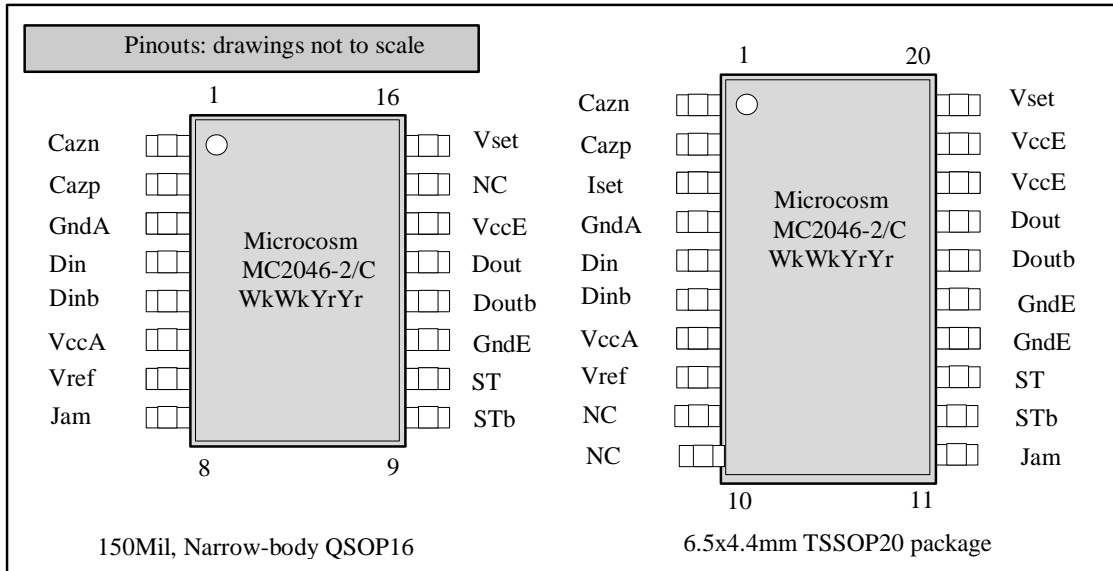
With R$_{vset}$ resistor connected:

$$\text{Detection Level} = \text{Vdet} = \frac{\text{V(Vset)}}{20} = 0.025\text{V} \frac{(R_b//R_{vset})}{R_a} \text{ Vdiff peak}$$

Application Note on 50Ω loads.

When running PECL outputs into a capacitively coupled 50Ω load, 180Ω pull-down resistors are recommended.

If higher impedance lines are used to matched to a higher impedance load, then larger pull-down resistors may be used.

Die layout (not to scale)

Iset Cazp Cazn Vset VccE VccE

GndA
Din
Dinb
VccA

MC2046-2   Microcosm C 1998

Dout
Doutb
GndE
GndE

1.12mm

1.49mm

Vref Jam StB-ECL StB-C St-ECL St-C

I/O Pad openings are 90μ square
Pad pitch min. 130μ

Pinouts: drawings not to scale

150Mil, Narrow-body QSOP16

1   16
Cazn   Vset
Cazp   NC
GndA   VccE
Din   Microcosm   Dout
Dinb   MC2046-2/C Doutb
VccA   WkWkYrYr   GndE
Vref   ST
Jam   STb
8   9

6.5x4.4mm TSSOP20 package

1   20
Cazn   Vset
Cazp   VccE
Iset   VccE
GndA   Microcosm   Dout
Din   MC2046-2/C Doutb
Dinb   WkWkYrYr   GndE
VccA   GndE
Vref   ST
NC   STb
NC   Jam
10   11

This specification is derived from simulation results and tests on engineering samples. These specifications may yet change prior to full product release.

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