NL84620
4Kx64 (256K)

SyncCAM-1
Synchronous Content Addressable Memory (SyncCAM®)

Description
The NL84620 is a 256K bit Synchronous Content Addressable Memory (SyncCAM®). The device performs high-speed parallel search operations on memory tables while simultaneously capturing and manipulating data from a data stream. Its primary application is as an address filter or an address translator for Fast Ethernet, Gigabit Ethernet, and ATM switches.

Features
- Match Flag times: 18/21/28 ns
- CAM Index output (flow through mode): 21/25/33 ns
- CAM Index output (pipelined mode): 10/12/16 ns
- Sustained searches of up to 40 Million/Second
- Separate 64-bit Comparand I/O bus, 64-bit Results bus and 14-bit Instruction bus
- Two validity bits (Skip and Empty) for each location define the location as Valid, Skip, Empty or RAM
- Four 64-bit wide Mask Registers for easy masking of compare or write operations
- 14-bit instruction bus enables single cycle execution of all instructions
- Depth-expansion with no glue logic required
- 3.3V TTL compatible CMOS, 292-pin PBGA Package

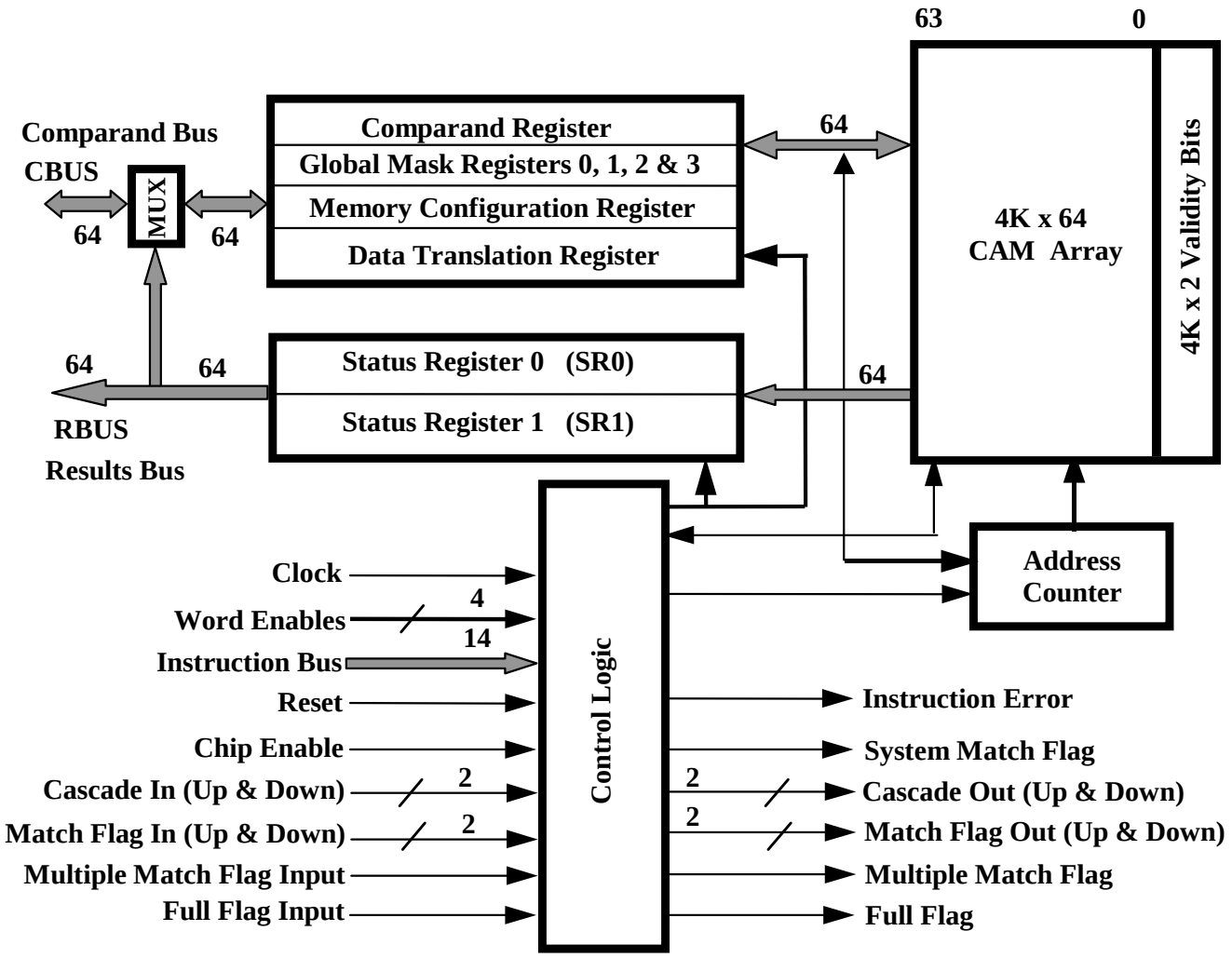


Figure 1 NL84620 Block Diagram

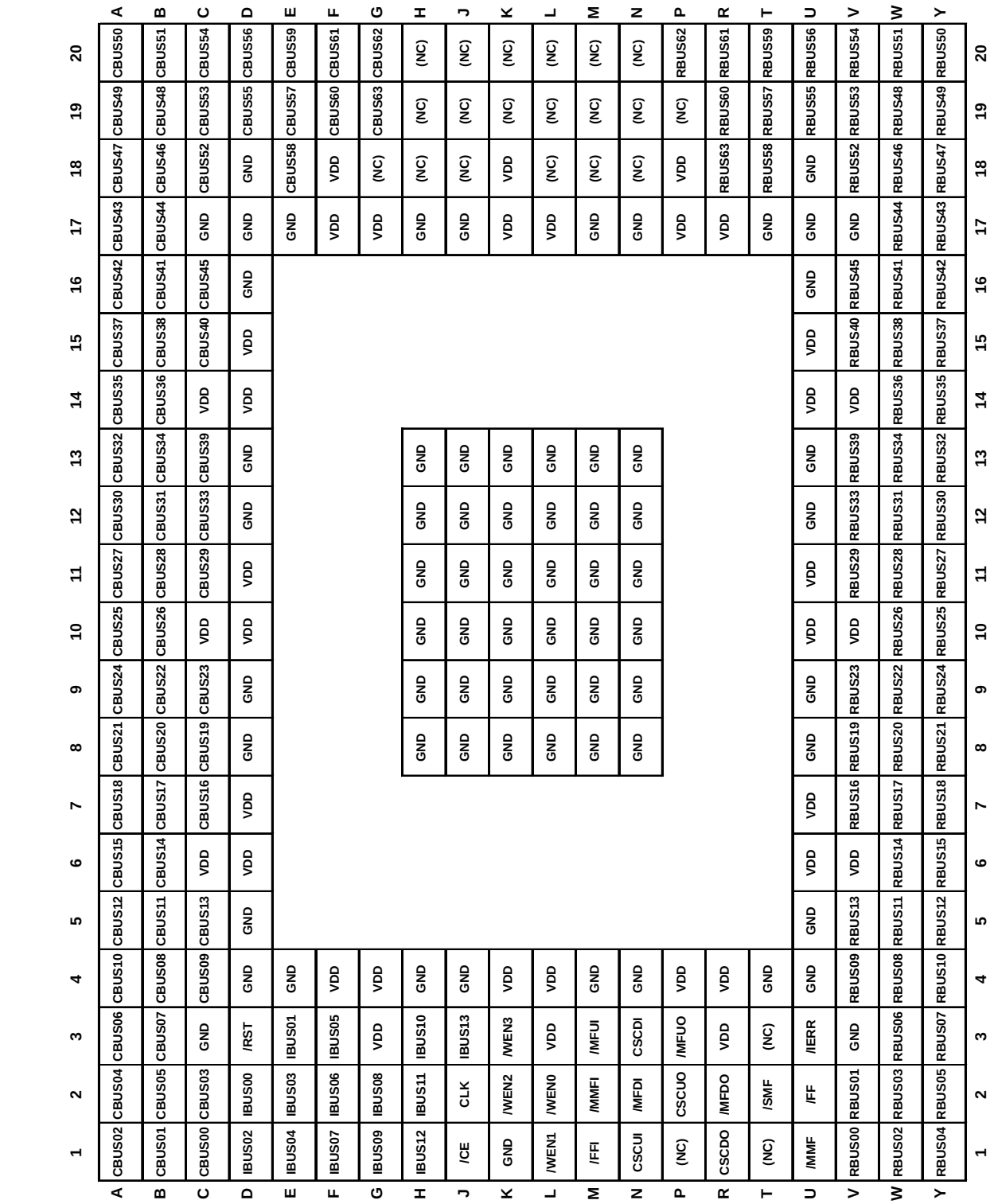


Figure 2 NL84620 Ball Assignment (292 PBGA, Top view)

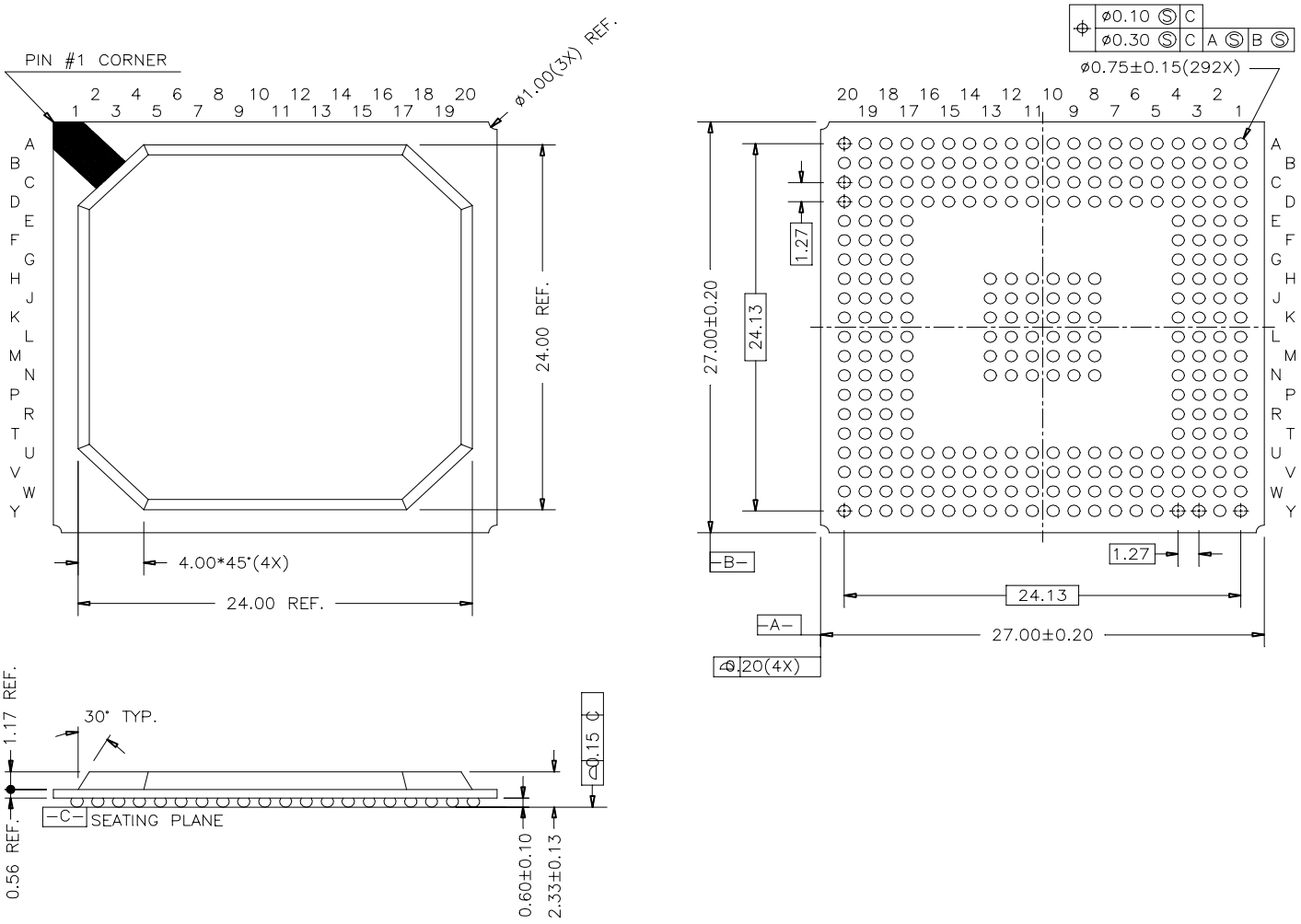


Figure 3: 292 PBGA Package Dimensions

1.0 Functional Description

The NL84620 is a Synchronous Content Addressable Memory (SyncCAM) designed for use as an address filter or an address translator in 100/1000 Mb/s Ethernet and ATM switches and routers. This device can also be used to implement fast routing tables in Internet Protocol (IP) switches. The NL84620 has a total associative memory capacity of 256K bits organized as 4K x 64 bits.

A bi-directional 64-bit Comparand Bus (CBUS) enables all internal registers and memory to be accessed. An output only, 64-bit Results Bus (RBUS) provides status information after a compare operation. A 14-bit Instruction Bus (IBUS) allows instructions to be presented to the device once every cycle. All operations on the device are timed synchronously with the rising edge of a free running clock. This architecture permits back-to-back compare cycles to be executed without any bus latencies.

The Comparand Register (CR) is a 64-bit register that enables one to write the comparand data (key) and compare it with the contents of memory. This is the only register that enables a user to store and compare data with memory.

The NL84620 has four Global Mask Registers (GMR3-GMR0) that can each be selected on an operation-by-operation basis for write or compare operations. For a write operation, when the bits in these registers are programmed with '1's, the corresponding bits in memory will be masked, i.e. will not be written into. For compare operations, the corresponding bits in the associative data word will be forced to a match.

The 16-bit Device Configuration Register (DCR) enables the user to configure the device operation. The user can configure the RBUS to be in pipeline or flow through mode, RBUS output to be in Status Register 0 (SR0) or Status Register 1 (SR1) format, address counter to be incremented automatically during write and so on. See Table 3d for a complete list.

The Memory Configuration Register (MCR) is a 64-bit wide register used as a mask during Compare instruction cycles. It provides compare masking capability in addition to the global masks. This memory configuration register is always used during comparison as opposed to the global mask registers, which may or may not be selected during comparison. After reset, all bits are '0' indicating no masking of any bits during comparison.

The Data Translation Register (DTR) is a 64-bit register that allows manipulation of data stored in it.

Status Registers SR0 and SR1 hold status information after compare, read, write or copy operations.

A 12-bit Address Counter (ACR) supplies the address to the memory array. This counter may be loaded with any valid start address and can be configured to increment once every cycle for read or write operations. This allows data to be loaded into or read out of the memory continuously.

Four Word Enable (/WEN3-/WEN0) inputs allow access to the internal registers and memory on 16-bit boundaries. These inputs also allow for bus matching on the comparand bus with no glue logic.

The NL84620 can be clocked up to frequencies of 40MHz with a free running clock. A Chip Enable (/CE) input allows the device to be selected or deselected similar to any memory device. The device has flag inputs and outputs that enable depth cascading with no glue logic. The Instruction Error pin (/IERR) asserts an active low when erroneous Opcodes are presented to the device.

2.0 Pin Description

2.1 Clock (CLK):
This is a free running clock that is used to time all transactions on the CAM. The rising edge of the clock is the timing reference.

2.2 Chip Enable (/CE):
This is a synchronous input that selects the device for all operations, when asserted Low. When asserted High, the device is deselected and is in idle mode. In idle mode, the CBUS and the RBUS are high-z. For single device operation, when the device is deselected (/CE asserted High) the Match, Multiple Match and System Match Flags are High and Full Flag is Low. For depth cascaded devices, the deselected devices will pass the flag input states through to the flag outputs. When /CE is taken from a "1" to a "0" (idle to active), a NOP is necessary for the device (and the devices in the cascade chain, if applicable) to be activated. See Table 1.

2.3 Reset (/RST):
This is an asynchronous input and provides the hardware reset for the device. During initialization, this pin must be asserted low for a minimum of *three (3) cycles*. This will set all CAM words to empty, initialize the control logic, and clear all registers. The reset operation must be followed by at least one NOP instruction. Table 2 and Tables 3a-g illustrate the state of the part after reset.

2.4 Full Flag Input (/FFI):
This input is provided for depth cascading multiple CAMs. When asserted low, this pin will allow data to be written into the CAM at the next free address (NFA) using the "Write to memory at NFA" instruction provided the device is not full. However, write to memory at address specified by the address counter is not affected by full flag input or output. For single device operation, the /FFI pin is tied to ground. For depth cascaded devices, the highest priority device has its /FFI input tied to ground, all other devices in the cascade having the /FFI tied to the Full Flag output (/FF) of the next higher priority device. Refer to the depth cascading section for more details.

2.5 Match Flag Up Input (/MFUI):
This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices, the lowest priority device has its /MFUI pin connected to VDD. All other devices in the cascade have their /MFUI pin tied to the Match Flag Up Output (/MFUO) of the next Lower priority device. Refer to the depth cascading section for more details.

2.6 Match Flag Down Input (/MFDI):
This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices, the highest Priority device has its /MFDI pin connected to VDD. All other devices in the cascade have their /MFDI pin tied to the Match Flag Down Output (/MFDO) of the next higher priority device. Refer to the depth cascading section for more details.

2.7 Multiple Match Flag Input (/MMFI):
This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to VDD. For depth cascaded devices the highest priority device has its /MMFI tied to VDD. All other devices in the cascade have their /MMFI pin tied to the Multiple Match Flag (/MMF) of the next higher Priority device. Refer to the depth cascading section for more details.

2.8 Cascade Down Input (CSCDI):
This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to ground. For depth cascaded devices the highest priority device has its CSCDI connected to ground. All other devices in the cascade have their CSCDI pin tied to the CSCDO of the next higher priority device. Refer to the depth cascading section for more details.

2.9 Cascade Up Input (CSCUI):
This input is provided for depth cascading multiple CAMs. For single device operation, this pin is tied to ground. For depth cascaded devices the lowest Priority device has its CSCUI connected to ground. All other devices in the cascade have their CSCUI pin tied to the CSCUO of the next lower priority device. Refer to the depth expansion section for more details.

2.10 Word Enable (/WEN_0,1,2,3):
This is a synchronous input and enables access to the CAM array and all the registers with 16-bit granularity. For 64-bit entities in the CAM, /WEN_3 enables access to bits 63-48, /WEN_2 to bits 47-32, /WEN_1 to bits 31-16 and /WEN_0 to bits 15-0. These control pins are effective only for read and write to memory and the registers; for all other operations they are a "don't care".

2.11 Instruction Bus ($IBUS_{13}$.$IBUS_0$):
This is a synchronous 14-bit bus that provides the operation code (Opcode) to the CAM.

2.12 Comparand Bus ($CBUS_{63}$.$CBUS_0$):
This is a 64-bit synchronous I/O bus that conveys data to and from the memory and the registers.

2.13 Instruction Error (/IERR):
This is a synchronous output and will be asserted low whenever an erroneous Opcode is detected. An erroneous Opcode is one that does not conform to the listed Opcodes for the SyncCAM. In a depth cascade all devices will provide the Instruction Error output. The user is advised against issuing erroneous Opcodes, as the results will be non-deterministic.

2.14 Cascade Down Output (CSCDO):
This output is provided for depth cascading multiple CAMs. For single device operation this pin must be left unconnected. For depth cascaded devices, the highest priority device has its CSCDO connected to the CSCDI of the next lower priority device. Refer to the depth expansion section for more details.

2.15 Cascade Up Output (CSCUO):
This output is provided for depth cascading multiple CAMs. For single device operation this pin must be left unconnected. For depth cascaded devices, the lowest priority device has its CSCUO connected to the CSCUI of the next higher priority device. Refer to the depth expansion section for more details.

2.16 Full Flag (/FF):
This is a synchronous output and is updated after Write to Memory, Copy to Memory, set VBITs or Set Full Flag operations. After reset, this pin is high. When the device is full, /FF is asserted low. For depth cascaded devices, /FF is connected to /FFI of the next lower priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /FFI through to /FF.

2.17 Match Flag Up Output (/MFUO)
This synchronous output is provided for depth cascading CAMs. This output is updated for all compare operations. After reset, /MFUO is high. For depth cascaded devices, the /MFUO of a device is connected to the /MFUI of the next higher priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /MFUI through to /MFUO.

2.18 Match Flag Down Output (/MFDO)
This synchronous output is provided for depth cascading CAMs. This output is updated for all compare operations. After reset, /MFDO is high. For depth cascaded devices, the /MFDO of a device is connected to the /MFDI of the next lower priority device. For depth cascaded devices, when single device mode is selected, deselected devices pass /MFDI through to /MFDO.

2.19 System Match Flag (/SMF)
This synchronous output provides the System Match Flag (either for single device or cascaded devices). This output is updated for all compare operations. After reset /SMF is high. Functionally this output is identical to /MFDO. When cascading, the /SMF is provided by the lowest priority CAM. The /SMF from all other CAMs in the cascade may be left unconnected.

2.20 Multiple Match Flag (/MMF)

This synchronous output provides the Multiple Match Flag (either for single device or cascaded devices). This output is updated for all compare operations. After reset /MMF is high. In depth cascaded systems the lowest priority device provides the /MMF. For cascaded devices, when single device mode is selected, the deselected devices pass /MMFI through to /MMF.

2.21 Results Bus ($RBUS_{63}$ - $RBUS_0$)

This is a 64-bit synchronous bus (RBUS) that outputs the results of a Compare operation. During a compare operation, when there is no match, RBUS is High-Z. For a compare operation, when there is a match, this bus outputs the CAM index of the Highest Priority Match (HPM), the Device ID, status of the flags and a portion of the memory at the HPM address.

The following describes the RBUS format:
The CAM index of HPM or the NFA will be output on RBUS[63] through RBUS[52]. The lower 12 bits of Device ID are output on RBUS[51] through RBUS[40]. Bits RBUS[39] through RBUS[37] are reserved and will read '0'. RBUS[36] is the match flag status of the device. RBUS[35] is the multiple match flag status of the device. RBUS[34] is the full flag status of the device. RBUS[33] and RBUS[32] will reflect the state of validity bits (skip and empty, respectively) when a Compare operation is issued referencing to the validity bits.

RBUS[31] through RBUS[0] reflect a portion of memory at the HPM address.

The RBUS can be selected to output data in either SR0 format (default after Reset) SR1 format (See figure 3). Programming the Device Configuration Register selects this format.

When SR0 format is selected, the CAM index (address) will appear on $RBUS_{63}$-$RBUS_{52}$, the lower 12 bits of the device ID will appear on $RBUS_{51}$ - $RBUS_{40}$, $RBUS_{39}$ - $RBUS_{37}$ is reserved and will always read a '0'. $RBUS_{36}$ is the match flag status and will reflect the state of the external /MF pin. $RBUS_{35}$ is the multiple match flag status and will reflect the external /MMF state. $RBUS_{34}$ is the Full Flag status and will reflect the state of the external Full Flag State. $RBUS_{33}$ is the Skip bit and will reflect the Skip Bit State of the word in memory that was accessed in the current cycle. $RBUS_{32}$ is the Empty bit and will reflect the state of the empty bit of the word in memory that was accessed in the current cycle. $RBUS_{31}$ $RBUS_0$ will reflect 32-bits of the HPM word in the memory.
When SR1 format is selected, the CAM index (address) will appear on $RBUS_{63}$-$RBUS_{52}$, the lower 4 bits of the device ID will appear on $RBUS_{51}$-$RBUS_{48}$. $RBUS_{47}$-$RBUS_0$ will reflect 48 bits of the HPM word in the memory.

RBUS is active only during the cycle when a compare instruction results in a match. During a compare cycle, when there is no match, RBUS is in high-z.

The SyncCAM can be set to operate in either **flow through** or **pipeline** mode. In the flow through mode the results of a compare instruction are output on RBUS in the same cycle with zero cycle latency. In the pipelined mode the results of a compare instruction are output on RBUS in the following cycle. However, the Match Flag is available in flow through mode only and is output in the current clock cycle. The format of the RBUS data in the pipeline mode is the same as described above for the flow through mode.

The user can program bit b7 in the device configuration register to setup the RBUS to be in pipeline or flow through mode. When bit b7 is set to '1' the RBUS will operate in pipeline mode. When this bit is set to '0' the RBUS will operate in flow through mode. **The default mode after reset is the flow through mode.**

Table 1: Logical State of the Outputs with /CE high

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results bus	RBUS	High-Z
Match Flag Down Output	/MFDO	Same as Match Flag Down Input (/MFDI)
Match Flag Up Output	/MFUO	Same as Match Flag Up Input (/MFUI)
System Match Flag	/SMF	Same as Match Flag Down Input (/MFDI)
Multiple Match Flag	/MMF	Same as Multiple Match Flag Input (/MMFI)
Full Flag	/FF	Same as Full Flag Input (/FFI).
Instruction Error	/IERR	High

Table 2: Logical State of the Outputs after Hardware or Software Reset

Output	Pin/Bus Name	Logical State
Comparand Bus	CBUS	High-Z
Results Bus	RBUS	High-Z
Match Flag Down Output	/MFDO	High
Match Flag Up Output	/MFUO	High
System Match Flag	/SMF	High
Multiple Match Flag	/MMF	High
Full Flag	/FF	High
Instruction Error	/IERR	High

Table 3a: Address Counter, NFAR, and HPM Registers after Hardware or Software Reset

b11	b10	b9	b8	b7	b6	B5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0

Table 3b: Status Register 0 (SR0) after Hardware or Software Reset

b63 b52	b51 b40	b39 b37	b36	b35	b34	b33	b32	b31 b0
CAM Address	Device ID	RSV	MF	MMF	FF	S	E	Memory Data
0 0 0 Hex	0 0 0 Hex *	000	1	1	1	0	1	0000 0000 Hex

* Only the lower 12-bits of the Device ID Register will appear. This field is unchanged after software reset.

Table 3c: Status Register 1 (SR1) after Hardware or Software Reset

b63 b52	b51 b48	b47 b0
CAM Address	Device ID	Memory Data
0 0 0 Hex	0 Hex *	0000 0000 0000 Hex

* Only the lower 4-bits of the Device ID Register will appear. This field is unchanged after software reset.

Table 3d: Device Configuration Register (DCR) after Hardware or Software Reset

b15 b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type	802.3 <->802.5	P/FL	SR0/1	RSV	ACNT	RSV	RSV	RSV	C_MAP
000 0000*	0	0	0	0	0	0	0	0	0

* 000 0000 indicates a 4K x 64 SyncCAM. This entry is read only.

Table 3e: Memory Configuration, Global Mask Registers after Hardware or Software Reset

b63	b0
0000 0000 0000 0000 Hex	

Table 3f: Device ID Register after Hardware Reset (Device ID is not altered by Software Reset)

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3g: State of the SyncCAM after Hardware or Software Reset

#	Memory, Registers and Outputs	Status after Hardware Reset	Status after Software Reset
1	Device ID Register	All bits reset to ‘0’	Remains **unchanged**
2	Memory Configuration Register	All bits reset to ‘0’	All bits reset to ‘0’
3	Address Counter	All bits reset to ‘0’	All bits reset to ‘0’
4	Next Free Address Register	All bits reset to ‘0’	All bits reset to ‘0’
5	Global Mask Registers	All bits reset to ‘0’	All bits reset to ‘0’
6	Data Translation Register	All bits reset to ‘0’	All bits reset to ‘0’
7	Status Register 0 & 1	See table 3b & 3c	See table 3b & 3c
8	Device Configuration Register	See table 3d	See table 3d
9	Memory	Unknown	Unknown
10	VBITs in Memory	Skip=0; Empty=1	Skip=0; Empty=1
11	Full Flag	Reset to ‘1’	Reset to ‘1’
12	Comparand Bus (CBUS)	High-Z	High-Z
13	Results Bus (RBUS)	High-Z	High-Z
14	Match Flag Down Output (/MFDO)	High	High
15	Match Flag Up Output (/MFUO)	High	High
16	System Match Flag (/SMF)	High	High
17	Multiple Match Flag (/MMF)	High	High
18	Cascade Up Output (CSCUO **)**	High	High
19	Cascade Down Output (CSCDO **)**	High	High

Table 3h: CBUS State under Operating Mode and Control Inputs

Control Inputs State	Comparand Bus (CBUS) State
Reset (/RST) = Low	High-Z
Chip Enable (/CE) = High	High-Z
Chip Enable (/CE) = Low	/WEN_X that are ‘0’ enable corresponding 16-bits; others are High-Z

Global Device Mode Operation, /RST=‘1’, /CE=‘0’	
Highest Priority Device (/MFDI=‘1’ & /MFDO=‘0’)	/WEN_X that are ‘0’ enable corresponding 16-bits; others are High-Z
Device with Next Free Address (/FFI=‘0’ & /FF =‘1’)	/WEN_X that are ‘0’ enable corresponding 16-bits; others are High-Z
All Other Devices	High-Z

Single Device Mode Operation, /RST=‘1’, /CE=‘0’	
Selected Device (Device with Matching Device ID)	/WEN_X that are ‘0’ enable corresponding 16-bits; others are High-Z
All Other Devices	High-Z

Table 3i: Device Configuration Register Format

b15 b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
CAM Type	802.3-802.5	FL/P	SR0/SR1	RSV	ACNT	RSV	RSV	RSV	C_MAP

Notes:

b15-b9 CAM Type field. Reads "000 0000" for 4K x 64 SyncCAM. This CAM Type field is read only.

b8 When set to '1' this bit enables **802.3 <-> 802.5 translation**. When set to '0' this bit disables translation. This bit is set to '0' after reset (Hardware or Software)

b7 When this bit is set to '1' the RBUS operates in **Pipeline mode**. When this bit is set to '0' the RBUS operates in **Flow through mode**. This bit is set to '0' after reset. (Hardware or Software)

b6 When this bit is set to '1', the RBUS reflects **SR1** format. When this bit is set to '0' the RBUS reflects **SR0 format.** This bit is set to '0' after reset. (Hardware or Software)

b5 Reserved. Will read '0'.

b4 When set to '1' this bit enables the **Address counter** to be **incremented**. When set to '0' it disables the address counter incrementing. This bit is set to '0' after reset. (Hardware or Software)

b3-1 Reserved. Will read '0'.

b0 This is the C_MAP bit. This enables one to map different regions of memory onto **SR0** and **SR1**. Please see chart below for details. After reset this bit is set to '0' (Hardware or Software).

Table 3j: Status Register 0 (SR0) Format

b63 b52	b51 b40	b39 b37	b36	b35	b34	b33	b32	b31 b0
CAM Index	Device ID	RSV	MF	MMF	FF	S	E	Memory Data

Notes:

b63-b52 CAM Index field. Updated after all compare instructions. Updated with Highest Priority Match (HPM) index when there is a match.

b51-b40 Lower 12 bits of the 16-bit Device ID. Updated when Device ID is written.

b39-b37 Reserved; will read '000'**.**

b36 Match flag. Updated after all compare operations; reflects the internal match flag status.

b35 Multiple match flag. Updated after all compare operations; reflects the internal multiple match flag status.

b34 Full flag. Updated after write to memory, copy to memory, set VBITs instructions; reflects internal full flag status.

b33-b32 VBITs (skip and empty). Updated after all compare operations with the type of words compared; updated with the settings of VBITs after write to memory or copy to memory; updated with VBITs after set VBITs operation.

b31-b0 Updated after all compare operations. Reflects portion of the memory at HPM address.

Table 3k: Status Register 1 (SR1) Format

b63 b52	b51 b48	b47 b0
CAM Index	Device ID	Memory Data

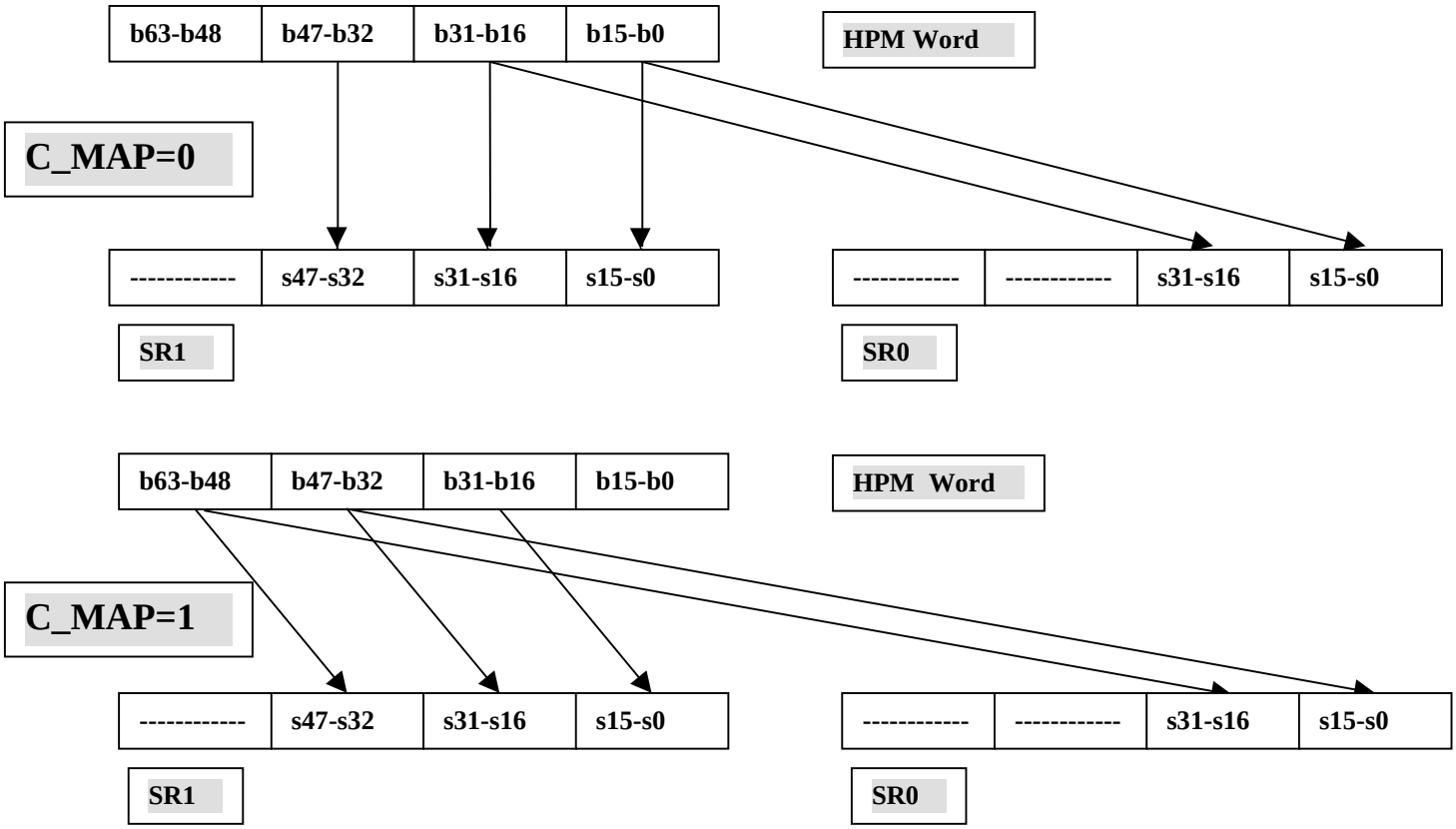
Notes:

b63-b52 CAM Index field. Updated after all compare instructions. Updated with Highest Priority Match (HPM) index when there is a match.

b51-b48 Lower 4 bits of the 16-bit device ID. Updated when device ID is written.

b47-b0 Updated after all compare operations. Reflects portion of the memory of HPM address.

Figure 4 Status Registers and RBUS Mapping



3.0 SyncCAM Internal Registers

3.1 Status Registers (SR0, SR1)

The 4K x 64 SyncCAM device has two Status Registers labeled SR0 and SR1. These registers hold the results of Compare, Read, Write or Copy operations. The RBUS outputs results after a comparison in either SR0 format or SR1 format depending on bit-6 setting in the Device Configuration Register. The user can also access the Status Registers from the CBUS by executing a "read status register" instruction. Tables 3b and 3c describe the contents of these registers after reset. Tables 3j and 3k describe the contents of these registers after all other operations.

3.2 Memory Configuration Register (MCR)

The Memory Configuration Register (MCR) is a 64-bit wide register that is used as a mask during compare instruction cycles. It provides compare masking capability in addition to the global masks. This MCR is always used during comparison as opposed to the Global Mask Registers, which may or may not be selected during comparison. After reset, all bits are '0' indicating no masking of any bits during comparison. While Global Mask Registers may be used for write and compare operations, the MCR is used only for compare operations.

3.3 Comparand Register (CR)

The Comparand Register (CR) is a 64-bit register for loading the comparand (key) data into the device for compare and other operations. For bus widths of 16 or 32 bits, the Word Enable (/WEN3-/WEN0) inputs enable the user to load data into the CR and then compare its contents with the contents of memory. This feature enables the SyncCAM to interface to buses that are 16, 32 and 64-bit wide seamlessly. This is the only register that enables the user to store and compare data with memory.

3.4 Global Mask Registers (GMR)

There are four 64-bit Global Mask Registers (GMR) that may be used either to mask compares or to mask data during memory writes. Each GMR may be selected on a cycle-by-cycle basis by specifying the GMR address in the instruction. All GMRs allow for a single bit to be shifted left or right to support proximity matching algorithms.

For compare instructions calling for a masked compare, if a mask bit is '1', the corresponding bits in the memory will not enter the compare operation. If a mask bit is '0', the corresponding bits in the memory will enter the compare operation.

For memory write instructions calling for a masked write, if a mask bit is '1', the corresponding bits in the memory will not be altered. If a mask bit is '0', the corresponding bits in the memory will be written to.

3.5 Data Translation Register (DTR)

The Data Translation Register (DTR) is a 64-bit register for performing data manipulations in the SyncCAM. These four operations are listed below:

1. 16-bit swaps
2. 32-bit swaps
3. 16-bit shifts
4. 1-bit shifts

3.6 Highest Priority Match Index Register (HPMR)

This register holds the address of the highest priority match. This register is updated after all compare operations. See table 3a.

3.7 Next Free Address Register (NFAR)

This register holds the address of next free address in the array. This is updated for all write to memory, copy to memory, and set VBITs instructions. See table 3a and Section 5.0.

3.8 Device Configuration Register (DCR)

This register holds the programmable bits for selecting modes of operation of the CAM device. This register includes a field (read only) indicating the type of device. For details, see table 3i.

3.9 Device ID Register (DIDR)

This register holds the Device ID value. This register is written into as part of initialization sequence. This register is reset only during hardware reset. Software reset instruction does not alter this register. See table 3f.

4.0 CAM Address Counter (ACR)

The CAM Address Counter (ACR) in the SyncCAM allows a user to perform read, write or copy operations continuously. The user may set the start address in the counter and program the Device Configuration Register to increment the counter after write, read or copy operations. The ACR is set to increment by setting bit b4 in the Device Configuration Register to a '1'. When the counter is set **not to Increment**, (bit b4='0'), then the counter address will not increment even for instructions that specify that the Address Counter be incremented.

When the CAM Address Counter is **set to increment** in the Device Configuration Register, the counter will be incremented after any of the following instructions are executed:

1. Copy operations to and from memory that reference the address counter.
2. Set VBITs to either Valid, Empty, Skip or RAM at the address indicated by the Address Counter.
3. Write to memory and set VBITs to Valid, Empty, Skip or RAM at the address indicated by the Address Counter.
4. Write to memory masked by Global Mask Register, set VBITs to Valid, Skip or RAM at the address indicated by the Address Counter.
5. Read memory at address indicated by the Address Counter and increment Address Counter.

The following memory operations that reference the Address Counter **do not increment** the Address Counter even if b4 in the Configuration Register is set to '1' (Increment):

1. Write to memory, no change to VBITs.
2. Write to memory masked by Global Mask Register, no change to VBITs.
3. Read memory.

These restrictions should be kept in mind when interfacing SyncCAM to buses smaller than 64-bits wide.

5.0 Next Free Address Register (NFAR)

The Next Free Address Register (NFAR) holds the address of the memory word that has its VBITs set to empty, and that is numerically closest to zero. This address is generated from the output of the priority encoder in the SyncCAM. When the CAM has no empty locations, the NFAR holds the address of the last empty location before the device became full.

The following operations will update the NFAR:

1. Write to Memory at NFAR; set VBITs to Valid, Skip or RAM.
2. Set VBITs to empty at the Address indicated by the Address Counter.
3. Set VBITs to empty at HPM address.
4. Set VBITs to empty at all matching locations.
5. Copy operations that reference the NFAR.

The NFAR will **not be updated** for the following operation:

1. Write to memory at next free address; no change to VBITs.

These restrictions should be kept in mind when interfacing SyncCAM to buses smaller than 64-bits wide or when updating memory in segments smaller than 64-bits wide.

6.0 Validity Bits

Every location in the memory array has a corresponding skip and empty bit associated with it. These are referred to as VBITs. These bits can be written to or read from just like locations in memory. These VBITs group memory words into four different categories (See table 5). Any compare instruction indicates the type of words to be searched during the cycle and only words belonging to that group participate in the search operation; all other words not belonging to the group do not participate in the match operation (indicate a no match). The Skip state allows a user to temporarily skip comparisons of certain CAM words. After hardware/software reset all words belong to the "Empty" group.

When the Skip and Empty bits are set to reflect the Valid state for a particular word, then that particular word will take part in Compare operations only when the compare operation with VBITs set to valid instruction is executed.

When the Skip and Empty bits are set to reflect the Skip state for a particular word, then that particular word will take part in compare operations only when the compare operation with VBITs set to Skip instruction is executed.

When the Skip and Empty bits are set to reflect the RAM state for a particular word, then that particular word will take part in compare operations only when the compare operation with VBITs set to RAM instruction is executed.

Option	Skip (S)	Empty (E)	Word Type
1	0	0	Valid
2	0	1	Empty
3	1	0	Skip
4	1	1	RAM

Table 5: Validity Bit (VBITs) Encoding

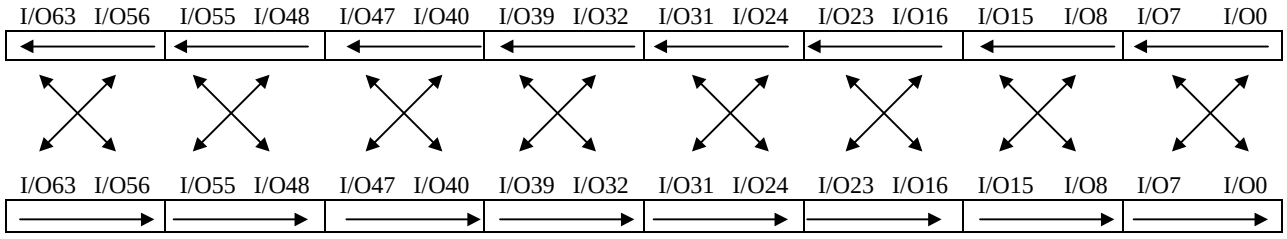
7.0 IEEE 802.3 / 802.5 Format Mapping

To support the symmetrical mapping between the address formats of IEEE 802.3 and IEEE 802.5, the SyncCAM provides a bit translation facility. The user can program bit b8 to a '1' in the Device Configuration Register to enable translation. When this bit is set to '0' it will disable translation. After reset, bit b8 is '0' indicating no translation. *This translation is applicable only for writing*.

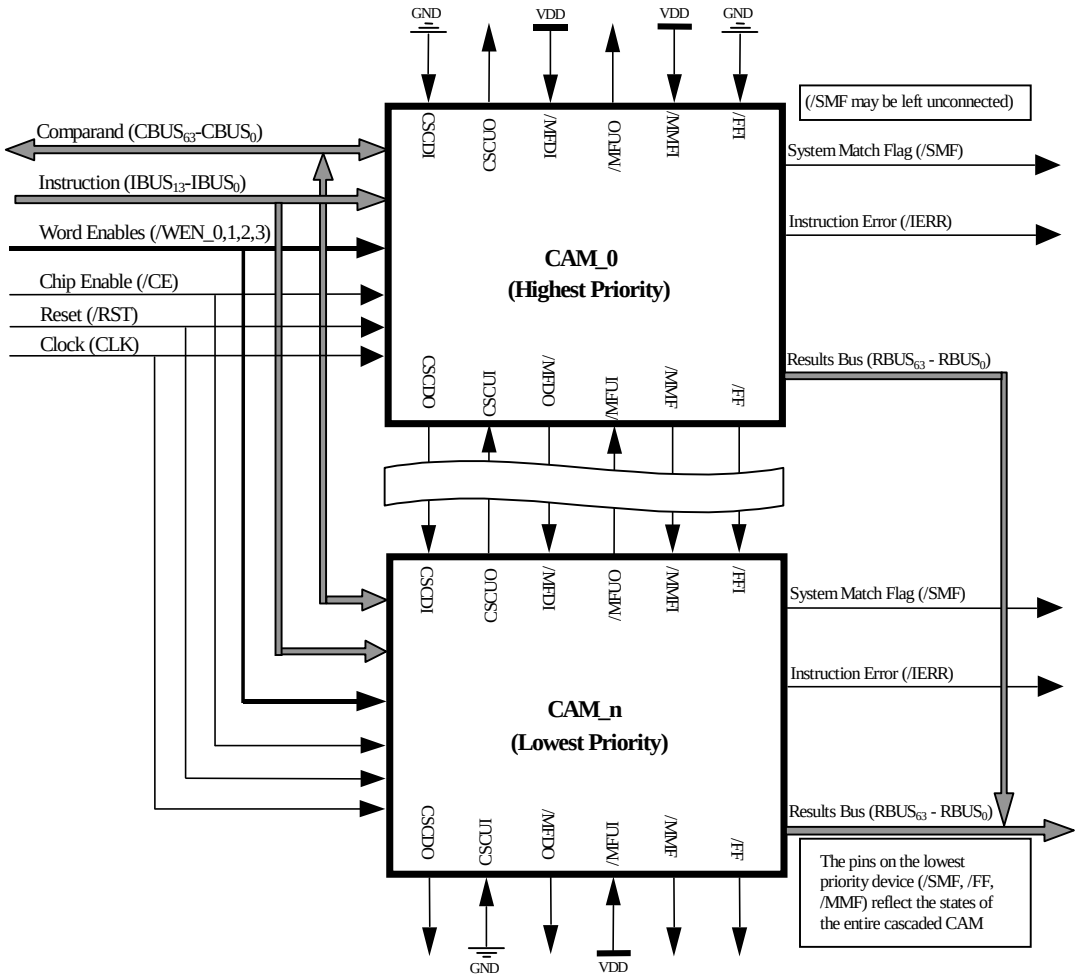
This mapping above does not apply to 16-bit registers (Address Counter, Device ID and Device Configuration).

The nth bit, D (n), maps to the xth output bit, Q (x), through the following expressions:

D(n) = Q (7-n) for 0 <= n <= 7
D(n) = Q(23-n) for 8 <= n <=15
D(n) = Q(39-n) for 16 <= n <= 23
D(n) = Q(55-n) for 24 <= n <= 31
D(n) = Q(71-n) for 32 <= n <= 39
D(n) = Q(87-n) for 40 <= n <= 47
D(n) = Q(103-n) for 48 <= n <= 55
D(n) = Q(119-n) for 56 <= n <= 63



8.0 Depth Cascading the SyncCAM



Depth cascading of the SyncCAM is accomplished by connecting them as shown above and described below.

1. Connect /FFI of the highest priority device to '0'.
2. Connect /MFDI of the highest priority device to '1'.
3. Connect /MMFI of the highest priority device to '1'.
4. Connect CSCDI of the highest priority device to '0'.
5. Connect /MFUI of the lowest priority device to '1'.
6. Connect CSCUI of the lowest priority device to '0'.
7. Connect /FF of each device to /FFI of the next lower priority device (except lowest priority device).
8. Connect /MFDO of each device to /MFDI of the next lower priority device (except lowest priority device).
9. Connect /MMF of each device to /MMFI of the next lower priority device (except lowest priority device).
10. Connect CSCDO of each device to /SCDI of the next lower priority device (except lowest priority device).
11. Connect /MFUO of each device to /MFUI of the next higher priority device (except highest priority device).
12. Connect CSCUO of each device to CSCUI of the next higher priority device (except highest priority device).

The System Match Flag (/SMF) is generated by the lowest priority device and is the logical OR of all the match flags in the cascade. The /SMF from all other devices may be left unconnected.

The System Multiple Match Flag is the Multiple Match Flag (/MMF) of the lowest priority device. This flag is asserted whenever more than one device in the cascade has a match and/or one or more devices in the cascade have a multiple match.

After compare, should a match occur in more than one device in the cascade, the device with a match that is the highest priority device will drive RBUS. The highest priority device is the one with its /MFDI high and /MFDO low.

9.0 Initializing the SyncCAM

The SyncCAM needs to be initialized after power up for proper operation. The following steps show how to initialize the SyncCAM for single device and for depth cascaded devices. Please refer to section 8 for details on depth cascading.

9.1 Single Device Initialization

1. Assert /RST pin low for a minimum of three cycles.
2. Execute NOP instruction (at least once).
3. Write to Device ID Register (any 16-bit value).
4. Select Single device mode (Device ID input on $CBUS_{15}$-$CBUS_0$).

The SyncCAM device is now ready for memory write, compare and other operations.

9.2 Depth Cascaded Devices Initialization

1. Assert /RST pin low for a minimum of three cycles.
2. Execute NOP instruction (at least once).
3. Write to Device ID Register (any 16-bit value).
4. Set Full Flag.
5. Write to Device ID Register (any 16-bit value).
6. (Repeat 4 & 5 until all devices have ID written).
7. Execute a software Reset.
8. Execute NOP instruction (at least once).

The device IDs must all be unique for proper operation. At step 3, the first device has the ID written; at step 5, the second device has the ID written and so on. The SyncCAM device is now ready for memory write, compare and other operations.

10.0 Writing to the CAM Array

After initialization, the user can write into the SyncCAM array in many ways. Two common methods of accomplishing this are described below:

10.1 Writing to Memory: Option 1

One method of writing into the CAM array is to execute "Write to memory at next free address and set VBITs to Valid, Skip or RAM" instruction repeatedly until the memory is full or all data is written into the CAMs. The write operation begins in the device with /FFI = 0 and /FF=1, continues until all locations have been written into (no EMPTY locations remain). When the last empty location has been written to, the /FF of that device will assert a '0' preventing any further "Write to memory at NFA" operations from occurring in that device. This will then enable the next lower priority device in the cascade to accept "Write to memory at NFA" operation. This continues until the last device in the chain becomes full and asserts /FF pin low, indicating that all the CAM devices are now full, and no empty locations remain.

10.2 Writing to the Memory: Option 2

Another method of writing to the CAM is to use the address from the internal address counter as opposed to the NFAR. The steps involved in this method are as follows:

1. Select Single Device Mode, with Device ID on the least significant bits of the CBUS.
2. Write to CAM word at address for ACNTR and set VBIT to valid.
3. User must either monitor the full flag for each individual device or keep an external count of the number of entries filled in each device and then enable the next CAM in a cascaded array.
4. Repeat steps 2 and 3 until all devices are full (/FF = 0 for single device or cascaded chain).
5. Select Global Device Mode.

11.0 Electrical Characteristics

11.1 Absolute Maximum Ratings (1)

Supply voltage to GND	-0.5 to +4.6V
DC output voltage (Vout)	-0.5 to VDD + 0.5V (2)
DC output current	50mA (3)
T_{BIAS} Temperature under bias	-40ºC to +85ºC
T_{STG} Storage temperature	-65ºC to +150ºC

Notes:
1. Stresses greater than ABSOLUTE MAXIMUM RATINGS will cause permanent damage to the device, resulting in functional or reliability type failures.
2. -2.0V for 10 ns, measured at the 50% point.
3. Per output, one at a time, one-second duration.

11.2 Power Supply Characteristics

			40 MHz	33 MHz	25 MHz	
Symbol	**Parameter**	**Test Conditions**	**Max**	**Max**	**Max.**	**Unit**
I_{DDO}	Operating Current	$t_{CYC} = t_{CYC}$ (min)	700	650	600	mA
I_{SB}	Idle Current	/CE = '1'	10	90	90	mA

11.3 Capacitance

Symbol	Parameter	Max.	Unit	Notes
C_{IN}	Input Capacitance	6	pF	f=1MHz, V_{IN}=0V
C_{OUT}	Output Capacitance	8	pF	f=1MHz, V_{OUT}= 0V

11.4 DC Electrical Characteristics over Operating Range (T_A = -40^{O}C - 85^{O}C, VDD = 3.3V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Max.	UNIT
V_{IH}	Input HIGH Voltage	Logic high for all Inputs	2.2	VDD + 0.5	V
V_{IL}	Input LOW Voltage	Logic low for all Inputs	-0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -4mA, VDD = Min.	2.4	-	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA, VDD = Min.	-	0.4	V
I_{LI}	Input Leakage	VDD = 3.47V; GND ≤V_{IN}≤VDD	-5	5	µA
I_{LO}	Output Leakage	GND ≤ VOUT ≤ VDD	-10	10	µA

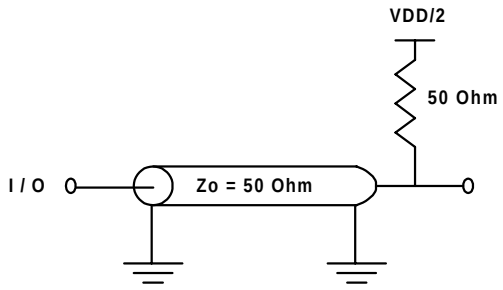
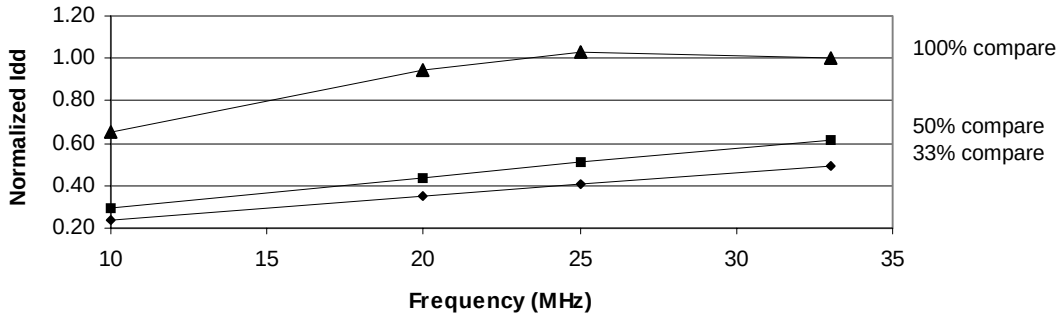


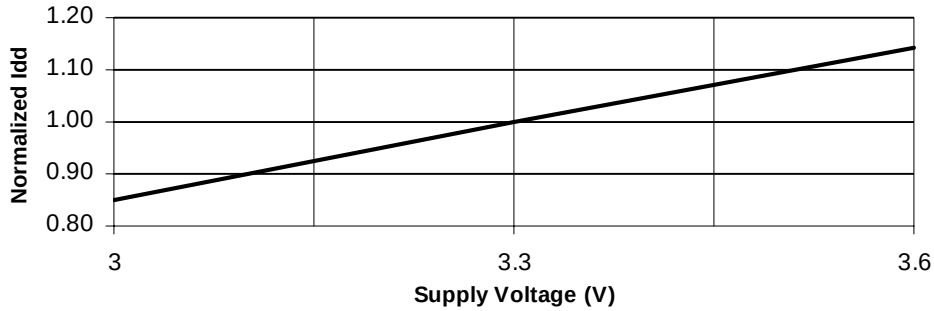
Figure 5 AC Test Conditions

11.5 Power De-rating Curves

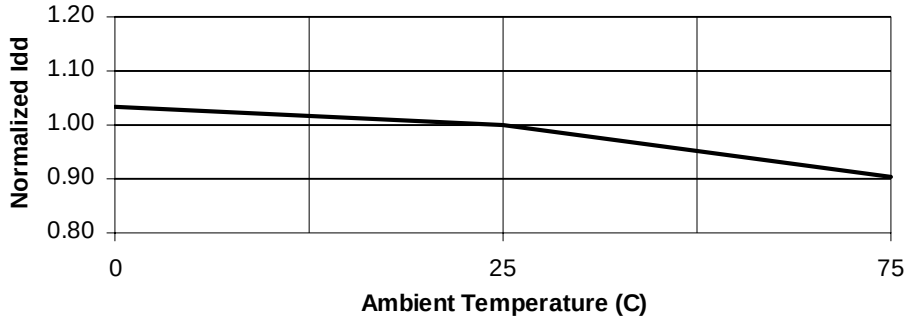
Normalized Dynamic Supply Current vs. Clock Frequency
Max Vdd=3.6V, 25 Deg C, Compare Cycles



Normalized Dynamic Supply Current vs. Supply Voltage
25 Deg C, 100% Compare



Normalized Dynamic Supply Current vs. Ambient Temp.
Vdd=3.3V, 100% Compare



12.0 AC Timing Parameters : (VDD = 3.3V ± 5%, TA= -40°C - 85°C)

#	Parameter	Type	Description	40MHz		33 MHz		25 MHz	
				Min	Max	Min	Max	Min	Max
1	t_{CYC}	IN	Cycle	25		30		40	
2	t_{CYH}	IN	Cycle high	11.5		13.5		18.5	
3	t_{CYL}	IN	Cycle low	11.5		13.5		18.5	
4	t_{CSU}	IN	Chip Enable Set-up	4		5		6	
5	t_{CHD}	IN	Chip Enable Hold	0		0		0	
6	t_{WNSU}	IN	Word Enable Set-up	4		5		6	
7	t_{WNH}	IN	Word Enable Hold	0		0		0	
8	t_{DSU}	IN	Data Setup	4		5		6	
9	t_{DHD}	IN	Data Hold	0		0		0	
10	t_{INSU}	IN	Instruction Setup	4		5		6	
11	t_{INHD}	IN	Instruction Hold	0		0		0	
12	t_{RB1}	OUT	RBUS Data Output (Pipeline Mode)		10		12		16
13	t_{RB2}	OUT	RBUS Data Output Hold (Pipeline Mode)	1		1		1	
14	t_{RB3}	OUT	RBUS Data Output (Index in Flow Through Mode)		21		25		33
15	t_{RB4}	OUT	RBUS Data Output (Memory data and flags in Flow Through Mode)	_	_		27		36
16	t_{RBH}	OUT	RBUS Data Output Hold Time (Flow Through Mode)	2		2		2	
17	t_{CDO}	OUT	CBUS Data Output		22		25		35
18	t_{CDH}	OUT	CBUS Data Output Hold	2		2		2	
19	t_{MFI}	IN	Match Flag Input Setup	4		4		4	
20	t_{MF}	OUT	Match Flag Assertion and Deassertion (/MFDO, /MFUO)	2	18	2	21	2	28
21	t_{SMF}	OUT	System Match Flag Assertion and Deassertion	2	18	2	21	2	28
22	t_{MMF}	OUT	Multiple Match Flag Assertion and Deassertion	2	21	2	25	2	33
23	t_{FFI}	IN	Full Flag Input Setup	4		4		4	
24	t_{FF1}	OUT	Full Flag Assertion and Deassertion (Write, Copy instructions)	2	23	2	26	2	36
25	t_{FF2}	OUT	Full Flag Assertion and Deassertion (VBC instructions)	2		2		2	
26	t_{IER}	OUT	Instruction Error Assertion and Deassertion	1	20	1	23	1	32

Notes:

1. **All timings are with reference to the rising edge of the clock, measured in nano seconds.**
2. **All timing numbers are for a single device (as opposed to devices in cascade).**
3. **Output hold times are guaranteed by design, but not tested in production.**
4. **t_{LEX} and t_{IER} are included for reference only. These parameters are characterized, but not tested in production.**
5. **t_{FF1}: This timing is valid for all instruction sequences except for the following : 1. Compare empty VBits, 2. Set VBITs to Valid at all matching locations.**

13.0 4K x 64 SyncCAM Instruction Set

The SyncCAM Instruction Bus is 14-bits wide. It consists of an 11-bit "Opcode field" consisting of $IBUS_{13}$-$IBUS_3$, a 2-bit global mask field "GMSK" consisting of bits $IBUS_2$-$IBUS_1$ and a 1-bit comparand field "CDS" consisting of $IBUS_0$.

Instruction Word (Opcode) Format:

IBUS13	IBUS12	IBUS11	IBUS10	IBUS09	IBUS08	IBUS07	IBUS06	IBUS05	IBUS04	IBUS03	IBUS02	IBUS01	IBUS00
fn10	fn9	fn8	fn7	fn6	fn5	fn4	fn3	fn2	fn1	fn0	x1	x0	y0
Opcode Field											GMSK		CDS

$IBUS_{13}$ -- $IBUS_{03}$: fn10.. fn0 is the Opcode field. This field determines all possible instructions. Erroneous Opcodes will result in indeterminate state in the SyncCAM.

$IBUS_{02}$ – $IBUS_{01}$: Selects between the four Global Mask Registers; designated as x1, x0.

#	x1	x0	Selects Global Mask Register
1	0	0	0
2	0	1	1
3	1	0	2
4	1	1	3

$IBUS_{00}$: Selects between Comparand/Data Translation for read/write (or) SR0/SR1 for read; designated as y0.

#	y0	Selects
1	0	SR0 for read or Comparand Register for read/write
2	1	SR1 for read or Data Translation Register read/write

Instruction: **[Opcode field]** **[GMSK]** **[CDS]**
xxxx xxxx xxx **xx** **x**

[Opcode field]: Bits 13 - 3, coded as [w2 w1 w0], w2 is bits 13-11, w1 is bits 10 - 7 and w0 is bits 6 - 3
[GMSK]: Bits 2 -1, coded as [x]
[CDS]: Bits 0, coded as [y]

14.0 SyncCAM Instruction Opcodes and Description

14.1 Compare Instructions

#	Instruction [Opcode][GMSK][CDS] [w2 w1 w0][x][y]	Instructions Explanation
1	[610] [0] [0]	Compare Valid Entries
2	[611] [0] [0]	Compare Skip Entries
3	[613] [0] [0]	Compare RAM Entries
4	[614] [x] [0]	Compare Valid Entries using Global Mask Register
5	[615] [x] [0]	Compare Skip Entries using Global Mask Register
6	[617] [x] [0]	Compare RAM Entries using Global Mask Register
7	[61D] [x] [0]	Compare Skip Entries using Global Mask; If No Match, Write Comparand to memory at NFA and set VBITs to Skip
8	[620] [0] [0]	Write to Comparand Register and Compare Valid Entries
9	[621] [0] [0]	Write to Comparand Register and Compare Skip Entries
10	[623] [0] [0]	Write to Comparand Register and Compare RAM Entries
11	[624] [x] [0]	Write to Comparand Register and Compare Valid Entries using Global Mask Register
12	[625] [x] [0]	Write to Comparand Register and Compare Skip Entries using Global Mask Register
13	[627] [x] [0]	Write to Comparand Register and Compare RAM Entries using Global Mask Register
14	[640] [0] [0]	Compare Valid VBITs
15	[641] [0] [0]	Compare Skip VBITs
16	[642] [0] [0]	Compare Empty VBITs
17	[643] [0] [0]	Compare RAM VBITs

14.2 Write Instructions

1	[000] [0] [0] H	NOP (No Operation)
2	[001] [0] [y] H	Write to Comparand or Data Translation Register
3	[002] [x] [0] H	Write to Global Mask Register
4	[003] [0] [0] H	Write to Memory at Address Register Location, No Change to VBITs
5	[004] [0] [0] H	Write to Memory at Address Register Location, Set VBITs to Valid
6	[005] [0] [0] H	Write to Memory at Address Register Location, Set VBITs to SKIP
7	[006] [0] [0] H	Write to Memory at Address Register Location, Set VBITs to RAM
8	[007] [x] [0] H	Write to Memory, masked by Global Mask Register, No Change to VBITs
9	[008] [x] [0] H	Write to Memory, masked by Global Mask Register, Set VBITs to Valid
10	[009] [x] [0] H	Write to Memory masked by Global Mask Register, Set VBITs to SKIP
11	[00A] [x] [0] H	Write to Memory masked by Global Mask Register, Set VBITs to RAM
12	[00B] [0] [0] H	Write to Memory at HPM address, No change to VBITs
13	[00C] [0] [0] H	Write to Memory at HPM address, Set VBITs to Valid
14	[00D] [0] [0] H	Write to Memory at HPM Address, Set VBITs to SKIP
15	[00E] [0] [0] H	Write to Memory at HPM Address, Set VBITs to RAM
16	[013] [0] [0] H	Write to Memory at NFA, No change to VBITs
17	[014] [0] [0] H	Write to Memory at NFA, Set VBITs to Valid
18	[015] [0] [0] H	Write to Memory at NFA, Set VBITs to Skip
19	[016] [0] [0] H	Write to Memory at NFA, Set VBITs to RAM
20	[01B] [0] [0] H	Set VBITs to Valid at Address Counter
21	[01C] [0] [0] H	Set VBITs to Empty at Address Counter
22	[01D] [0] [0] H	Set VBITs to Skip at Address Counter
23	[01E] [0] [0] H	Set VBITs to RAM at Address Counter
24	[01F] [0] [0] H	Set VBITs to Valid at HPM address
25	[020] [0] [0] H	Set VBITs to Empty, at HPM address
26	[021] [0] [0] H	Set VBITs to Skip at HPM address
27	[022] [0] [0] H	Set VBITs to RAM, at HPM address
28	[023] [0] [0] H	Set VBITs to Valid at all matching address
29	[024] [0] [0] H	Set VBITs to Empty at all matching address
30	[025] [0] [0] H	Set VBITs to Skip at all matching address
31	[026] [0] [0] H	Set VBITs to RAM at all matching address

Notes: (1) All write operations are controlled by the four Word Enables. (2) Instructions 28-31 are "VBC" instructions.

14.3 Copy Instructions

	Instruction	Instructions Explanation
32	[027] [0] [y] H	Copy Memory to Comparand Register or Data Translation Register
33	[028] [x] [y] H	Copy Memory to Comparand Register or Data Translation Register, masked by Global Mask Register
34	[029] [x] [0] H	Copy Memory to Global Mask Register
35	[02A] [x] [0] H	Copy memory at HPM Address to Global Mask Register
36	[02B] [0] [y] H	Copy Comparand Register or Data Translation Register to Memory, No change to VBITs
37	[02C] [0] [y] H	Copy Comparand Register or Data Translation Register to Memory, Set VBITs to Valid
38	[02D] [0] [y] H	Copy Comparand Register or Data Translation Register to Memory, Set VBITs to Skip
39	[02E] [0] [y] H	Copy Comparand Register or Data Translation Register to Memory, Set VBITs to RAM
40	[02F] [0] [y] H	Copy Comparand Register or Data Translation Register to memory at NFA, Set VBITs to Valid
41	[030] [0] [y] H	Copy Comparand Register or Data Translation Register to memory at NFA, Set VBITs to Skip
42	[031] [0] [y] H	Copy Comparand Register or Data Translation Register to memory at NFA, Set VBITs to RAM
43	[035] [x] [y] H	Copy Comparand Register or Data Translation Register to Global Mask Register
44	[03A] [0] [y] H	Copy Comparand or Data Translation Register to memory at HPM Address, No change to VBITs.
45	[03B] [0] [y] H	Copy Comparand or Data Translation Register to memory at HPM Address, Set VBITs Valid
46	[03C] [0] [y] H	Copy Comparand Register or Data Translation Register to memory at HPM Address, Set VBITs Skip
47	[03D] [0] [y] H	Copy Comparand or Data Translation Register to memory at HPM Address, Set VBITs to RAM
48	[042] [x] [y] H	Copy Global Mask Register to Comparand Register or Data Translation Register
49	[043] [x] [0] H	Copy Global Mask Register to Memory, Set VBITs to RAM
50	[044] [x] [0] H	Copy Global Mask Register to memory at HPM Address, Set VBITs to RAM
51	[045] [x] [0] H	Copy Global Mask Register to memory at NFA, Set VBITs to RAM

Note: All Copy instructions are 64-bit wide operations

14.4 Special Instructions

52	[046] [0] [0] H	Write to Memory Configuration Register
53	[047] [0] [0] H	Write to Device Configuration Register
54	[048] [0] [0] H	Write to Device ID Register[a]
55	[049] [0] [0] H	Copy Comparand Register to Data Translation Register
56	[04A] [0] [1] H	Copy Data Translation Register to Comparand Register
57	[04B] [0] [0] H	Set Full Flag [a]
58	[04C] [0] [0] H	Select Single Device Mode
59	[04D] [0] [0] H	Select Global Mode.
60	[04E] [0] [0] H	Software Reset [b]
61	[04F] [0] [0] H	Write Address Counter

Notes: a - This instruction will be executed in the device with /FI = 0 and /FF = 1. All other devices will treat this as NOP.
b - A Software instruction must be followed by a NOP instruction. Copy instructions are 64-bit operations; Write to Memory Configuration Register is controlled by four Word Enables.

14.5 Read Operations

1	[200] [0] [0] H	Read Address Counter [c]
2	[201] [0] [0] H	Read Memory
3	[202] [0] [0] H	Read Memory and Increment Counter
4	[203] [0] [y] H	Read Status Register
5	[204] [x] [0] H	Read Global Mask Register
6	[205] [0] [y] H	Read Comparand Register or Data Translation Register
7	[206] [0] [0] H	Read Next Free Address Register [d]
8	[207] [0] [0] H	Read Memory at HPM Address
9	[208] [0] [0] H	Read Memory Configuration Register
10	[209] [0] [0] H	Read Device Configuration Register [c]
11	[20A] [0] [0] H	Read Device ID Register [e]

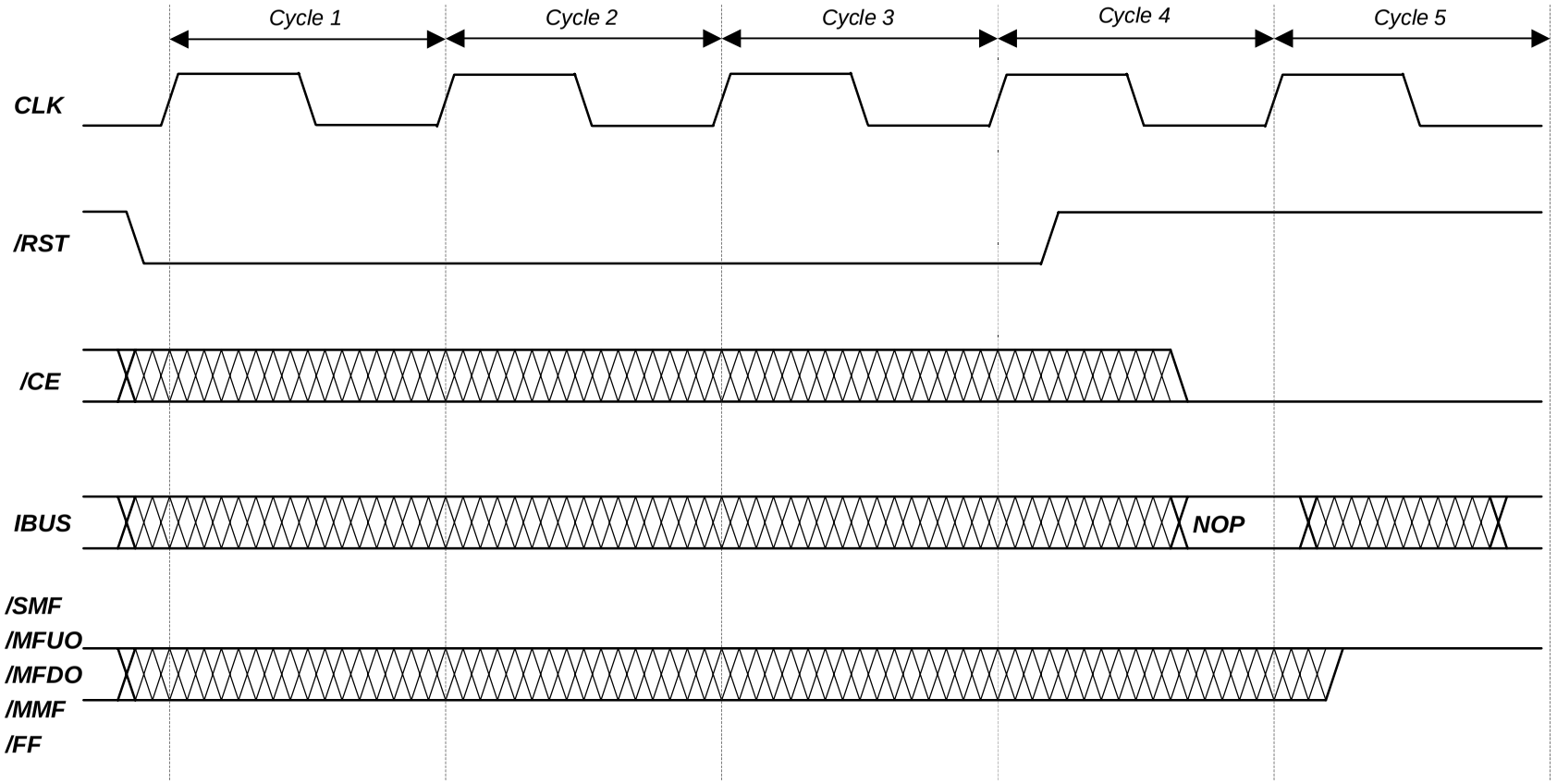
Notes: c - The data read will appear on the lower 16-bits of the Comparand Bus only.
d - The NFA will appear on bits b15-b0 of the CBUS and the Device ID will appear on bits b31 - b16.
e - The Device ID will appear on bits b31 - b16.

14.6 Data Translation Instructions

	Instruction	Instructions Explanation
1	[500] [0] [1] H	Swap Long Word 0, 1 in Data Translation Register (32-bit swap)
2	[501] [0] [1] H	Swap Word 0, 1 in Data Translation Register (16-bit swap)
3	[502] [0] [1] H	Swap Word 2, 3 in Data Translation Register (16-bit swap)
4	[503] [0] [1] H	Shift Right 16 bits in Data Translation Register (wrap around)
5	[504] [0] [1] H	Shift Left 16 bits in Data Translation Register (wrap around)
6	[505] [0] [1] H	Shift Right 1 bit in Data Translation Register (wrap around)
7	[506] [0] [1] H	Shift Left 1 bit in Data Translation Register (wrap around)
8	[507] [x] [0] H	Shift Right 1 bit in Global Mask Register (fall off to the right)
9	[508] [x] [0] H	Shift Left 1 bit in Global Mask Register (fall off to the left)

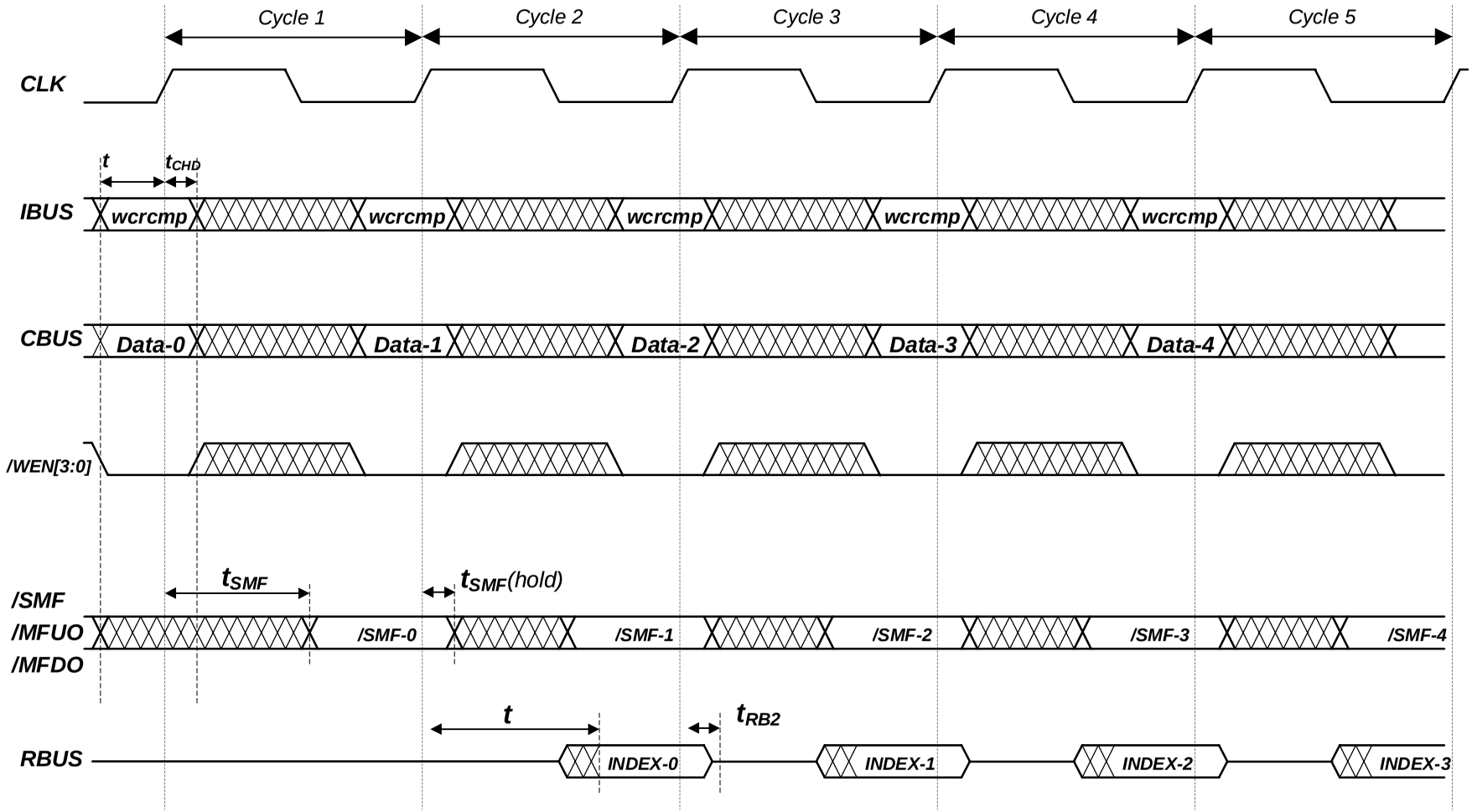
15.0 Timing Diagram

RESET CYCLE



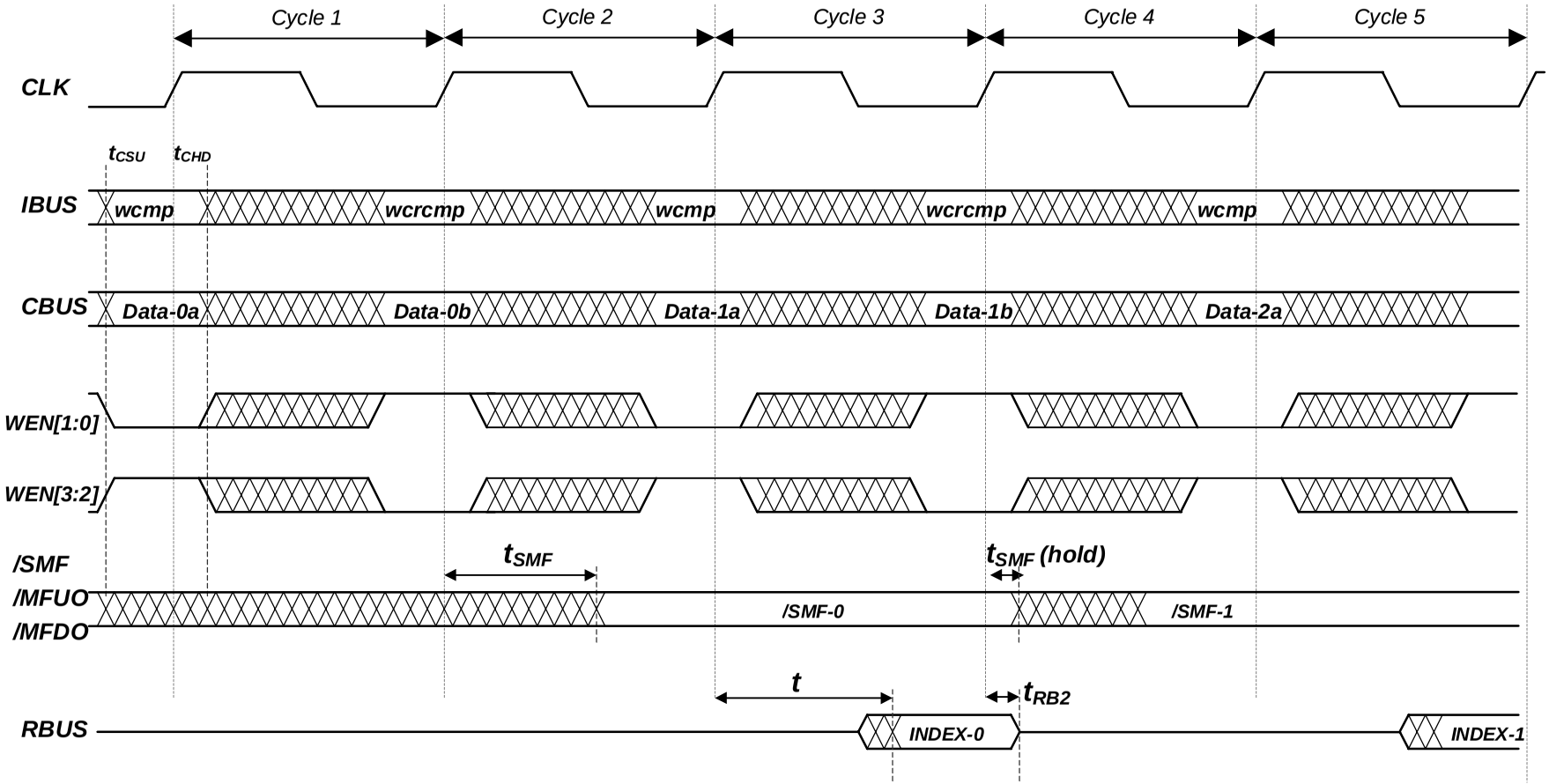
During Reset, CBUS[63:0], IBUS[13:0], and WEN[3:0] inputs are 'don't care'. RBUS is in High-Z. Reset must be followed by at least one "NOP" cycle.

64-bit Word Compare (64-bit interface, Pipelined Mode)



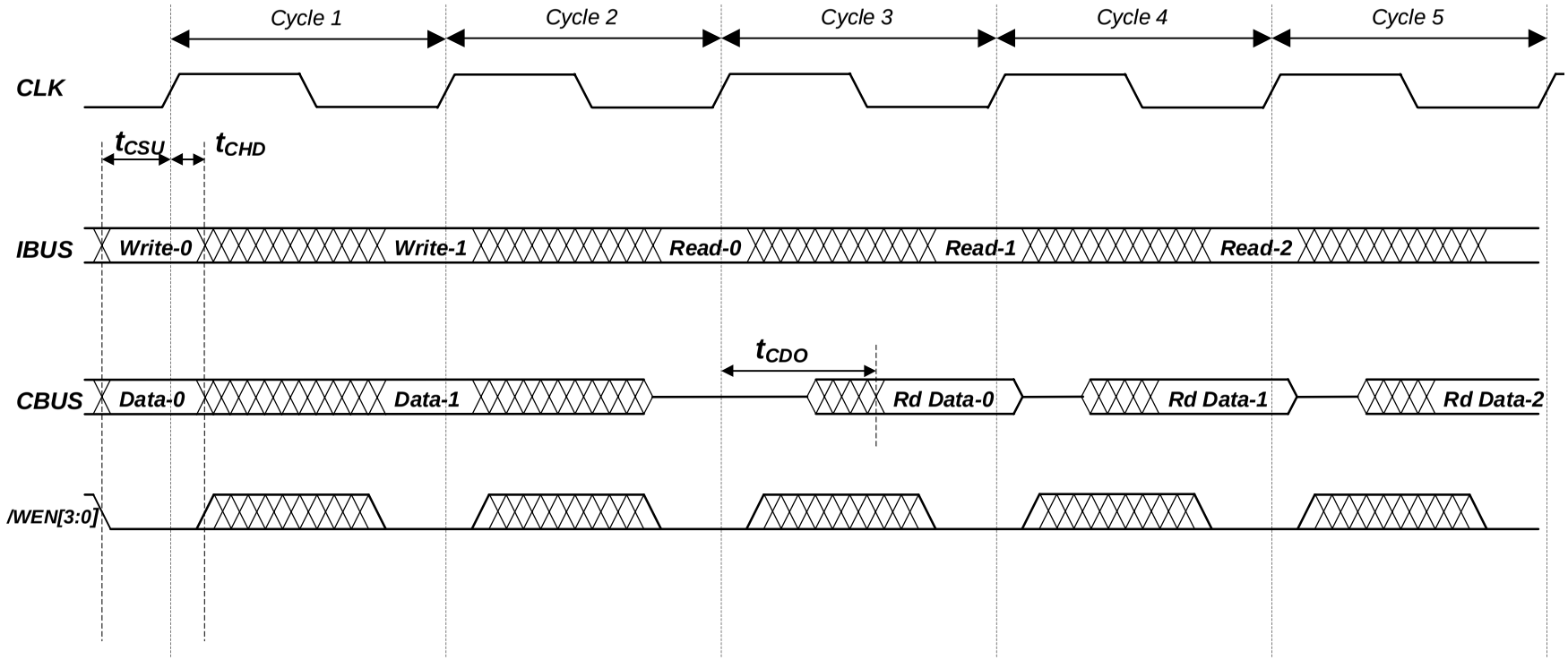
The Compare instruction is issued in the 1st cycle. The corresponding match flag is output in the 1st cycle and the RBUS output in the 2nd cycle. If a compare indicates no match (/SMF='1'), the corresponding RBUS output is High-Z. For "Flow Through" mode operation, the RBUS data is output in the same cycle as the Compare. The instruction "Write to Comparand register and Compare" is denoted as "wcrcmp". /CE = '0' during these cycles.

64-bit Word Compare (32-bit interface)



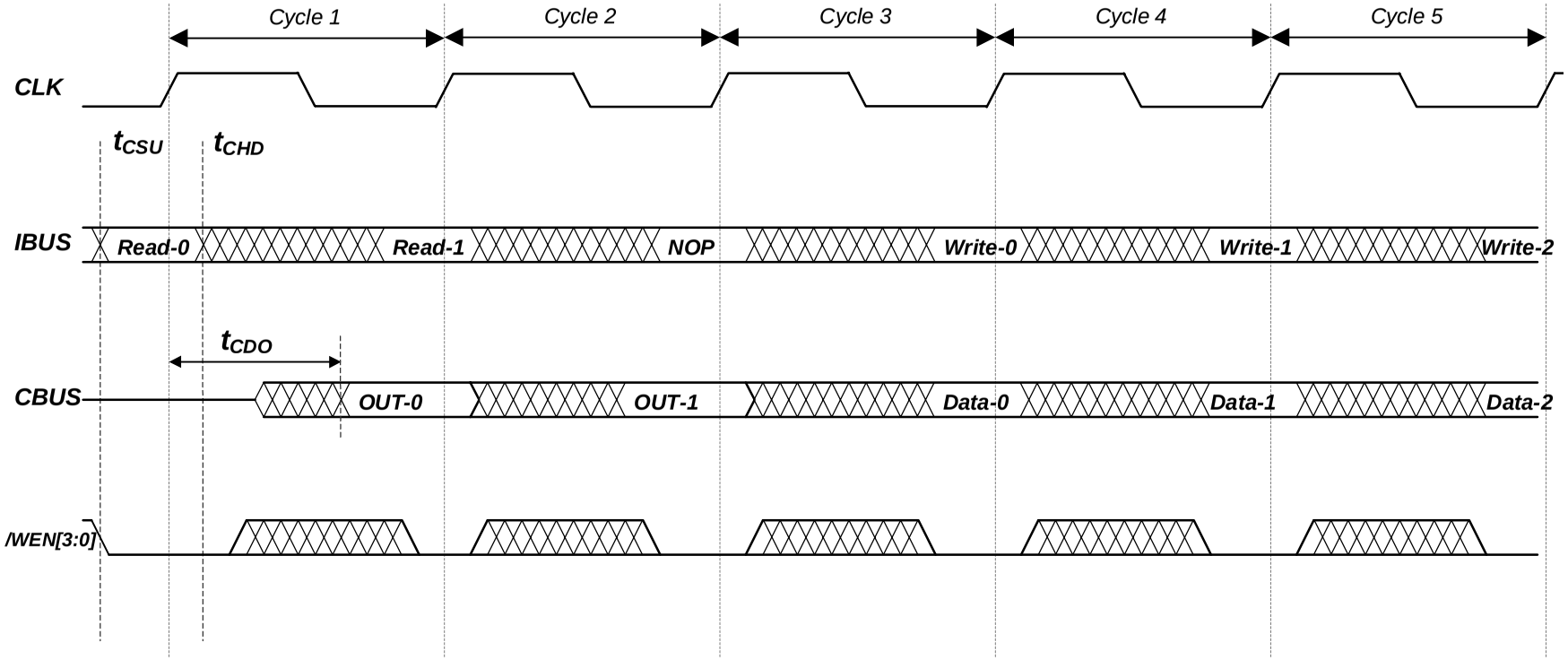
The Compare instruction is issued in the 2nd cycle. The corresponding match flag is output in the 2nd cycle and the RBUS in the 3rd cycle. If the compare instruction indicates no match (/SMF='1') the corresponding RBUS output is High-Z. The instruction "Write to Comparand" is denoted as "wcmp" and "Write to Comparand and Compare" as "wcrcmp". /CE = '0' during these cycles.

Memory Write-Memory Read Cycles (64-bit interface)



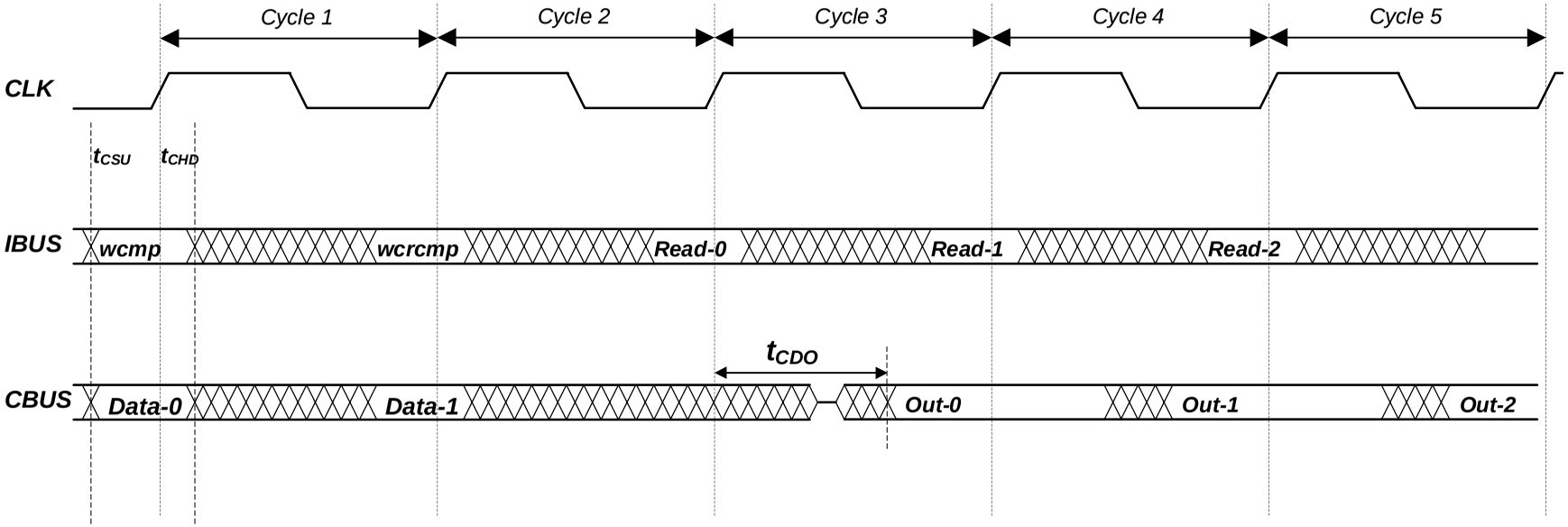
/CE = '0' during these cycles.

Memory Read-Memory Write Cycles (64-bit interface)



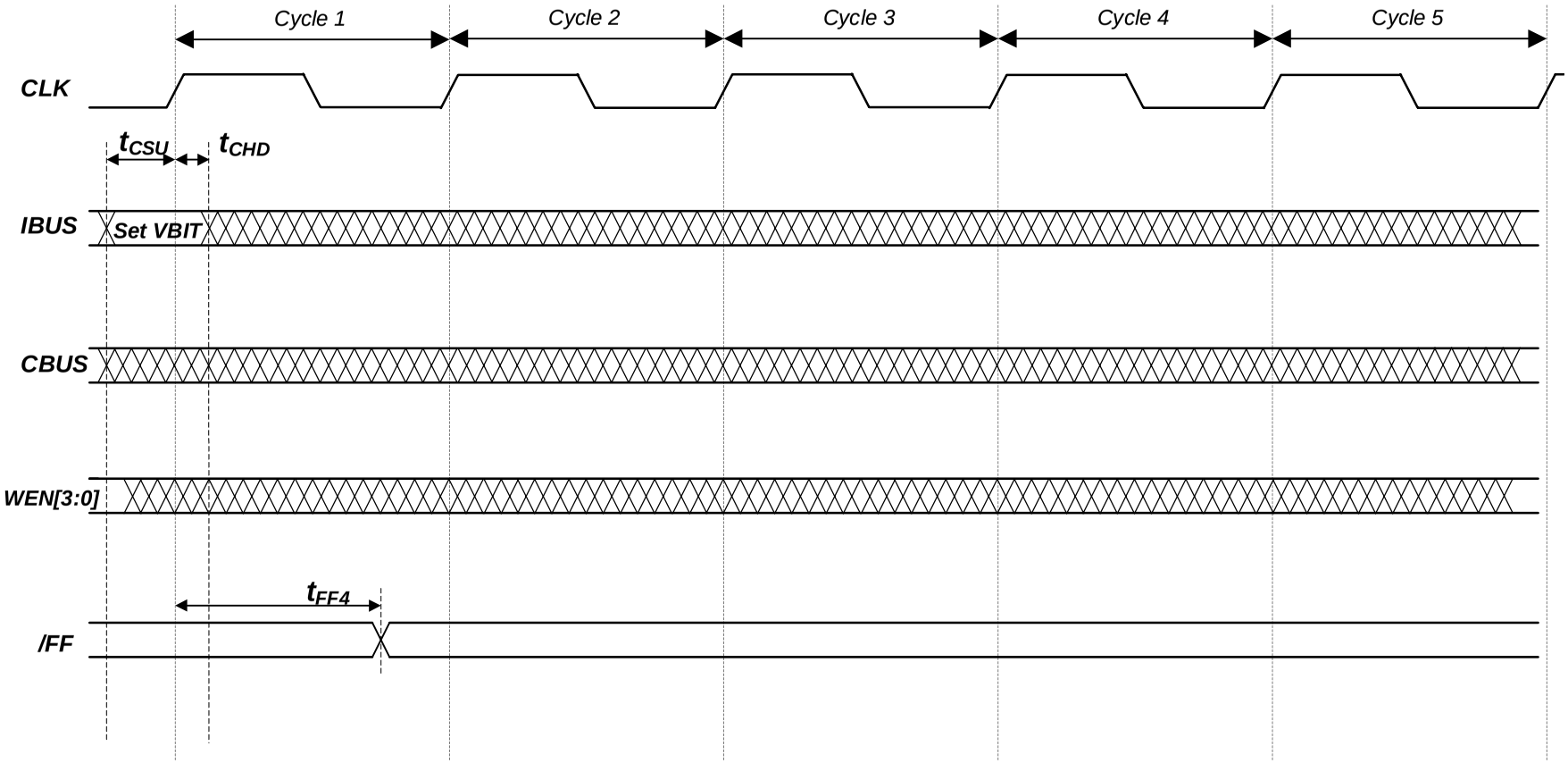
/CE = '0' during these cycles.

Compare/Memory Read Sequence



The compare instruction is issued in the 2nd cycle.The instruction "Write to Comparand" is denoted as "wcmp" and "Write to Comparand and Compare" as "wcrcmp". /CE = '0' during these cycles.

Validity Bit Operation and the Full Flag



If the device becomes full after the instruction is executed, the Full Flag is asserted; if the device was originally full and the instruction sets a location to empty, the Full Flag is de-asserted. The Full Flag assertion/Deassertion happens in the same cycle as the instruction. /CE = '0' during these cycles.

16.0 Ordering Information

Part Number	Clock Frequency	Package	Device Operating Range	Comments
NL84620-40	40MHz	292 PBGA	Commercial	Contact Factory
NL84620-33	33MHz	292 PBGA	Commercial	
NL84620-25I	25MHz	292 PBGA	Industrial	
NL84620-25			Commercial	

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