Agilent Technologies
Innovating the HP Way

Hermetically Sealed, High Speed, High CMR, Logic Gate Optocouplers

Technical Data

6N134* **5962-98001**
81028 **HCPL-268K**
HCPL-563X **HCPL-665X**
HCPL-663X **5962-90855**
HCPL-565X **HCPL-560X**

*See matrix for available extensions.

Features

- **Dual Marked with Device Part Number and DSCC Drawing Number**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and K**
- **Five Hermetically Sealed Package Configurations**
- **Performance Guaranteed over -55°C to +125°C**
- **High Speed: 10 M Bit/s**
- **CMR: > 10,000 V/µs Typical**
- **1500 Vdc Withstand Test Voltage**
- **2500 Vdc Withstand Test Voltage for HCPL-565X**
- **High Radiation Immunity**
- **6N137, HCPL-2601, HCPL-2630/-31 Function Compatibility**
- **Reliability Data**
- **TTL Circuit Compatibility**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Transportation, Medical, and Life Critical Systems**
- **Line Receiver**
- **Voltage Level Shifting**
- **Isolated Input Line Receiver**
- **Isolated Output Line Driver**
- **Logic Ground Isolation**
- **Harsh Industrial Environments**
- **Isolation for Computer, Communication, and Test Equipment Systems**

Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DSCC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DSCC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits. Quad channel devices are available by special order in the 16 pin DIP through hole packages.

Truth Table

(Positive Logic)

Multichannel Devices

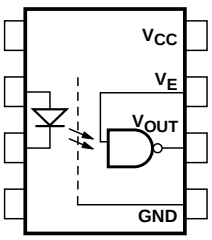
Input	Output
On (H)	L
Off (L)	H

Single Channel DIP

Input	Enable	Output
On (H)	H	L
Off (L)	H	H
On (H)	L	H
Off (L)	L	H

Functional Diagram

Multiple Channel Devices Available



The connection of a 0.1 µF bypass capacitor between V_{CC} and GND is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/µs. For Isolation Voltage applications requiring up to 2500 Vdc, the HCPL-5650 family is also available. Package styles for these parts are 8 and 16 pin DIP through hole (case outlines P and E respectively), and 16 pin surface mount DIP flat pack (case outline F), leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

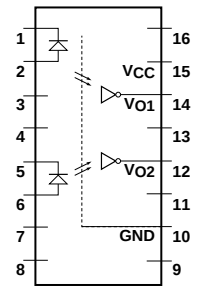
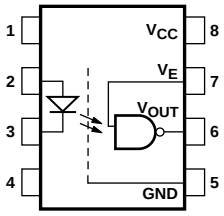
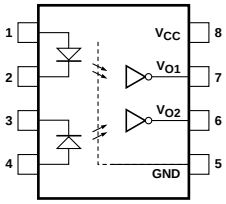
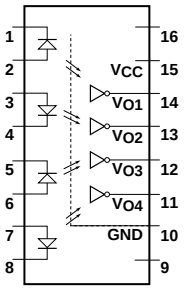
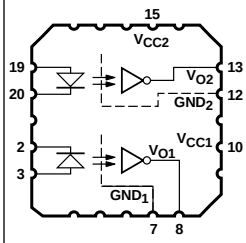
Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations, and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other parts' performance for reliability and certain limited radiation test results.

Selection Guide–Package Styles and Lead Configuration Options

Package	**16 Pin DIP**	**8 Pin DIP**	**8 Pin DIP**	**8 Pin DIP**	**16 Pin Flat Pack**	**20 Pad LCCC**
Lead Style	Through Hole	Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
Channels	2	1	2	2	4	2
Common Channel Wiring	V_{CC}, GND	None	V_{CC}, GND	V_{CC}, GND	V_{CC}, GND	None
Withstand Test Voltage	1500 Vdc	1500 Vdc	1500 Vdc	2500 Vdc	1500 Vdc	1500 Vdc
Agilent Part # & Options						
Commercial	6N134*	HCPL-5600	HCPL-5630	HCPL-5650	HCPL-6650	HCPL-6630
MIL-PRF-38534, Class H	6N134/883B	HCPL-5601	HCPL-5631	HCPL-5651	HCPL-6651	HCPL-6631
MIL-PRF-38534, Class K	HCPL-268K	HCPL-560K	HCPL-563K		HCPL-665K	HCPL-663K
Standard Lead Finish	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Gold Plate	Solder Pads
Solder Dipped	Option #200	Option #200	Option #200	Option #200		
Butt Cut/Gold Plate	Option #100	Option #100	Option #100			
Gull Wing/Soldered	Option #300	Option #300	Option #300			
Class H SMD Part #						
Prescript for all below	None	5962-	None	None	None	None
Either Gold or Solder	8102801EX	9085501HPX	8102802PX	8102805PX	8102804FX	81028032X
Gold Plate	8102801EC	9085501HPC	8102802PC	8102805PC	8102804FC	
Solder Dipped	8102801EA	9085501HPA	8102802PA	8102805PA		81028032A
Butt Cut/Gold Plate	8102801UC	9085501HYC	8102802YC			
Butt Cut/Soldered	8102801UA	9085501HYA	8102802YA			
Gull Wing/Soldered	8102801TA	9085501HXA	8102802ZA			
Class K SMD Part #						
Prescript for all below	5962-	5962-	5962-		5962-	5962-
Either Gold or Solder	9800101KEX	9085501KPX	9800102KPX		9800104KFX	9800103K2X
Gold Plate	9800101KEC	9085501KPC	9800102KPC		9800104KFC	
Solder Dipped	9800101KEA	9085501KPA	9800102KPA			9800103K2A
Butt Cut/Gold Plate	9800101KUC	9085501KYC	9800102KYC			
Butt Cut/Soldered	9800101KUA	9085501KYA	9800102KYA			
Gull Wing/Soldered	9800101KTA	9085501KXA	9800102KZA			

*JEDEC registered part.

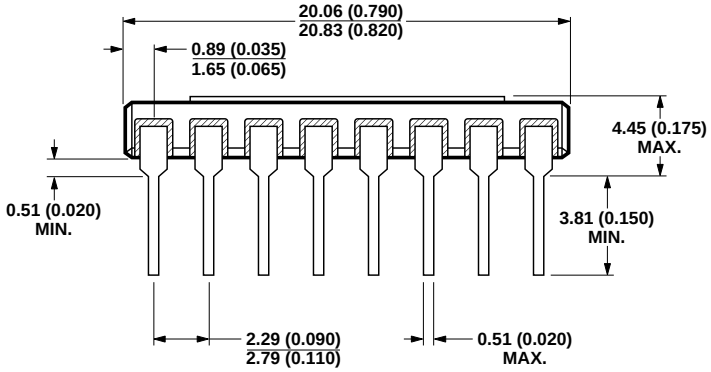
Functional Diagrams

16 Pin DIP	8 Pin DIP	8 Pin DIP	16 Pin Flat Pack	20 Pad LCCC
Through Hole	Through Hole	Through Hole	Unformed Leads	Surface Mount
2 Channels	1 Channel	2 Channels	4 Channels	2 Channels
				

Note: All DIP and flat pack devices have common V_{CC} and ground. Single channel DIP has an enable pin 7. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections. All diagrams are "top view."

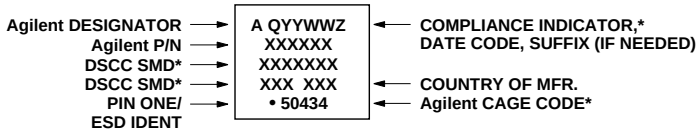
Outline Drawings

16 Pin DIP Through Hole, 2 Channels



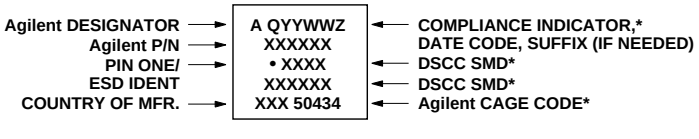
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking



* QUALIFIED PARTS ONLY

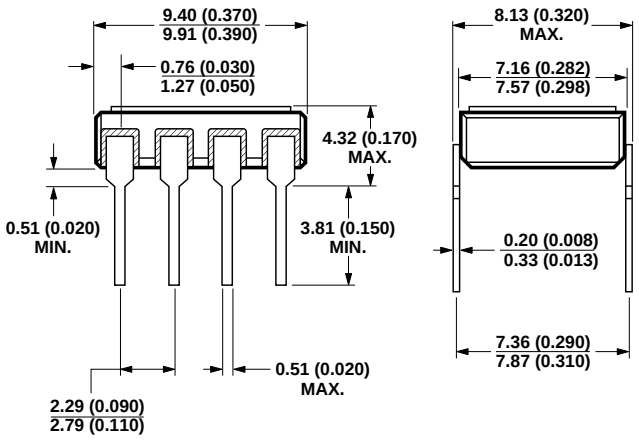
Leadless Device Marking



* QUALIFIED PARTS ONLY

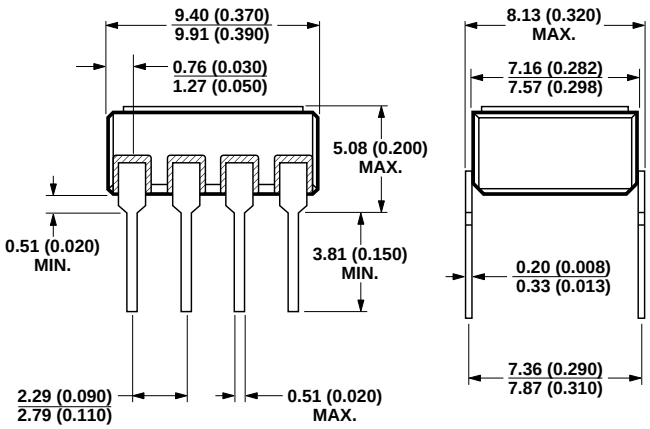
Outline Drawings (continued)

8 Pin DIP Through Hole, 1 and 2 Channels



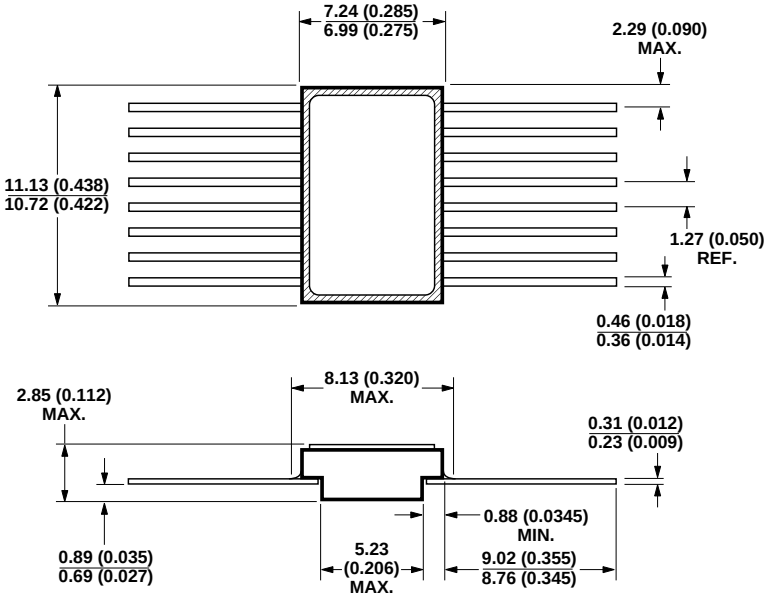
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

8 Pin DIP Through Hole, 2 Channels 2500 Vdc Withstand Test Voltage



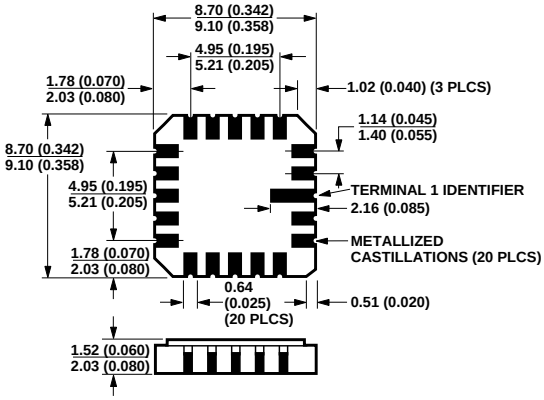
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

16 Pin Flat Pack, 4 Channels



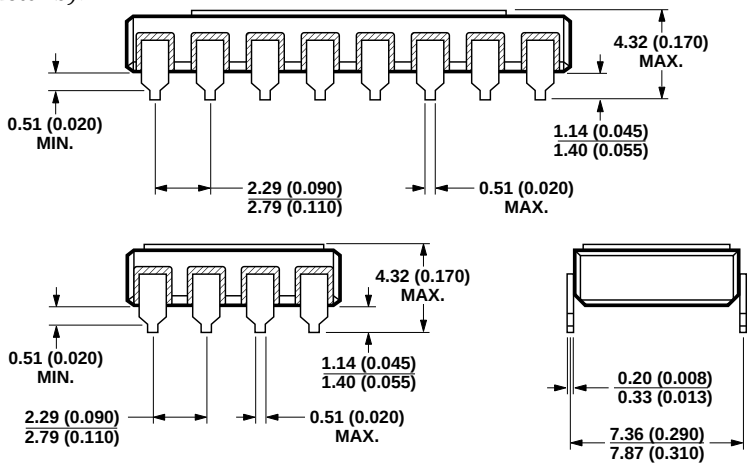
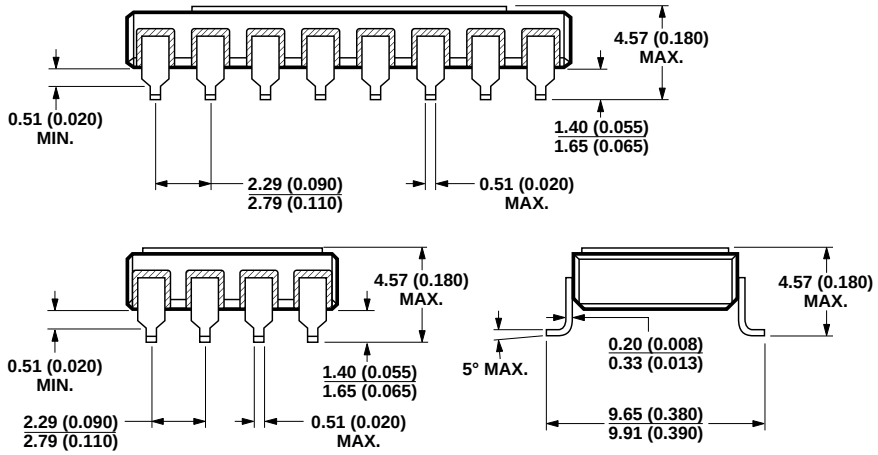
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20 Terminal LCCC Surface Mount, 2 Channels



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 and 16 pin DIP. DSCC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Absolute Maximum Ratings

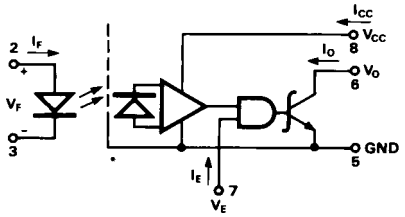
(No derating required up to +125°C)
Storage Temperature Range, T_S ..... -65°C to +150°C
Operating Temperature, T_A ..... -55°C to +125°C
Case Temperature, T_C ..... +170°C
Junction Temperature, T_J ..... +175°C
Lead Solder Temperature ..... 260°C for 10 s
Peak Forward Input Current, $I_{F\,PK}$, (each channel,
≤ 1 ms duration) ..... 40 mA
Average Input Forward Current, $I_{F\,AVG}$ (each channel) ..... 20 mA
Input Power Dissipation (each channel) ..... 35 mW
Reverse Input Voltage, V_R (each channel) ..... 5 V
Supply Voltage, V_{CC} (1 minute maximum) ..... 7 V
Output Current, I_O (each channel) ..... 25 mA
Output Power Dissipation (each channel) ..... 40 mW
Output Voltage, V_O (each channel) ..... 7 V*
Package Power Dissipation, P_D (each channel) ..... 200 mW

*Selection for higher output voltages up to 20 V is available.

Single Channel Product Only

Emitter Input Voltage, V_E ..... 5.5 V

8 Pin Ceramic DIP Single Channel Schematic



Note enable pin 7. An external 0.01 µF to 0.1 µF bypass capacitor must be connected between V_{CC} and ground for each package type.

ESD Classification

(MIL-STD-883, Method 3015)
HCPL-5600/01/0K ..... (Δ), Class 1
6N134, 6N134/883B, HCPL-5630/31/3K, HCPL-5650/51,
HCPL-6630/31/3K and HCPL-6650/51/5K ..... (Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level, Each Channel	I_{FL}	0	250	µA
Input Current, High Level, Each Channel*	I_{FH}	10	20	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	

*Meets or exceeds DSCC SMD and JEDEC requirements.

Recommended Operating Conditions (cont'd.)

Single Channel Product Only[10]

Parameter	Symbol	Min.	Max.	Units
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics (T_A = -55°C to +125°C, unless otherwise specified)

Parameter		Symbol	Test Conditions		Group A[13] Subgroups	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
High Level Output Current		I_{OH}*	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 µA		1, 2, 3		20	250	µA	1	1
Low Level Output Voltage		V_{OL}*	V_{CC} = 5.5 V, I_F = 10 mA, I_{OL} (Sinking) = 10 mA		1, 2, 3		0.3	0.6	V	2	1, 9
Current Transfer Ratio		h_F CTR	V_O = 0.6 V, I_F = 10 mA, V_{CC} = 5.5 V		1, 2, 3	100			%		1
Logic High Supply Current	Single Channel	I_{CCH}*	V_{CC} = 5.5 V, I_F = 0 mA		1, 2, 3		9	14	mA		1
	Dual Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = 0 mA				18	28	mA		6
	Quad Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = I_{F3} = I_{F4} = 0 mA				25	42	mA		
Logic Low Supply Current	Single Channel	I_{CCL}*	V_{CC} = 5.5 V, I_F = 20 mA		1, 2, 3		13	18	mA		1
	Dual Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = 20 mA				26	36	mA		6
	Quad Channel		V_{CC} = 5.5 V, I_{F1} = I_{F2} = I_{F3} = I_{F4} = 20 mA				33	50	mA		
Input Forward Voltage		V_F*	I_F = 20 mA		1, 2, 3		1.5	1.9	V	3	1, 15
					1, 2		1.55	1.75	V	3	1, 16
					3			1.85			
Input Reverse Breakdown Voltage		BV_R*	I_R = 10 µA		1, 2, 3	5			V		1
Input-Output Leakage Current		I_{I-O}*	RH = 45%, T_A = 25°C, t = 5 s	V_{I-O} = 1500 Vdc	1			1.0	µA		2, 8, 17
				V_{I-O} = 2500 Vdc	1			1.0	µA		18
Capacitance Between Input/ Output		C_{I-O}	f = 1 MHz, T_C = 25°C		4		1.0	4.0	pF		1, 3, 14

*Identified test parameters for JEDEC registered parts.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Electrical Characteristics, (Contd.) T_A = -55°C to +125°C unless otherwise specified

Parameter	Symbol	Test Conditions	Group A[13] Subgroups	Limits Min.	Limits Typ.**	Limits Max.	Units	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}*	V_{CC} = 5 V, R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA	9		60	100	ns	4, 5, 6	1, 5
			10, 11			140			
Propagation Delay Time to Low Output Level	t_{PHL}*		9		55	100	ns		
			10, 11			120			
Output Rise Time	t_{LH}	R_L = 510 Ω, C_L = 50 pF, I_F = 13 mA	9, 10, 11		35	90	ns		1
Output Fall Time	t_{HL}				35	40			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (PEAK), V_{CC} = 5 V, V_O (min.) = 2 V, R_L = 510 Ω, I_F = 0 mA	9, 10, 11	1000	>10000		V/µs	7	1, 7, 14
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (PEAK), V_{CC} = 5 V, V_O (max.) = 0.8 V, R_L = 510 kΩ, I_F = 10 mA	9, 10, 11	1000	>10000		V/µs	7	1, 7, 14

Single Channel Product Only

Low Level Enable Current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	1, 2, 3		-1.45	-2.0	mA		
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		10
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		

*Identified test parameters for JEDEC registered part.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Characteristics, T_A = 25°C, V_{CC} = 5 V

Parameter	Sym.	Typ.	Units	Test Conditions	Fig.	Note
Input Capacitance	C_{IN}	60	pF	V_F = 0 V, f = 1 MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.5	mV/°C	I_F = 20 mA		1
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V		2

Single Channel Product Only

Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	R_L = 510 Ω, C_L = 50 pF I_F = 13 mA, V_{EH} = 3 V, V_{EL} = 0 V	8, 9	1, 11
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns			1, 12

Dual and Quad Channel Product Only

Input-Input Leakage Current	I_{I-I}	0.5	nA	Relative Humidity = 45% V_{I-I} = 500 V, t = 5 s		4
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 V		4
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		4

Notes:

1. Each channel.
2. All devices are considered two-terminal devices; I_{I-O} is measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
3. Measured between each input pair shorted together and all output connections for that channel shorted together.
4. Measured between adjacent input pairs shorted together for each multichannel device.
5. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The HCPL-6630, HCPL-6631, and HCPL-663K dual channel parts function as two independent single channel units. Use the single channel parameter limits for each channel.
7. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 0.8 V). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 2.0 V).
8. This is a momentary withstand test, not an operating condition.
9. It is essential that a bypass capacitor (0.01 to 0.1 µF, ceramic) be connected from V_{CC} to ground. Total lead length between both ends of this external capacitor and the isolator connections should not exceed 20 mm.
10. No external pull up is required for a high logic state on the enable input.
11. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
12. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
13. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
14. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.
15. Not required for 6N134, 6N134/883B, 8102801, HCPL-268K and 5962-9800101 types.
16. Required for 6N134, 6N134/883B, 8102801, HCPL-268K and 5962-9800101 types.
17. Not required for HCPL-5650, HCPL-5651 and 8102805 types.
18. Required for HCPL-5650, HCPL-5651 and 8102805 types only.

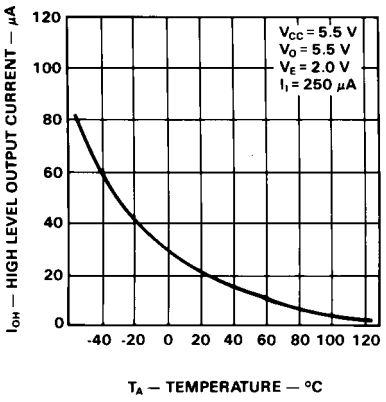


Figure 1. High Level Output Current vs. Temperature.

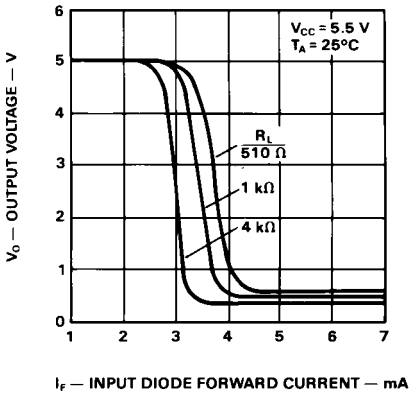


Figure 2. Input-Output Characteristics.

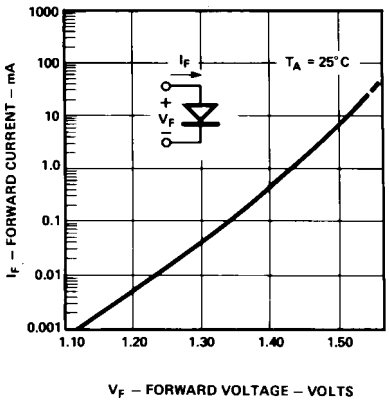
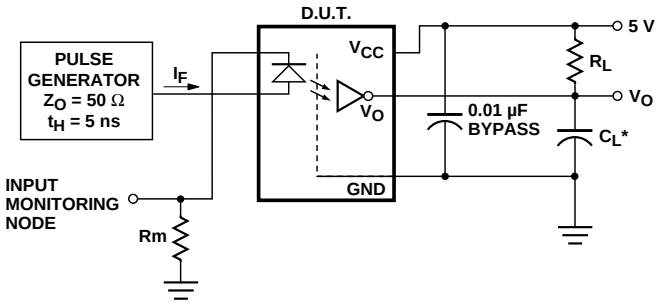


Figure 3. Input Diode Forward Characteristic.



* C_L INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

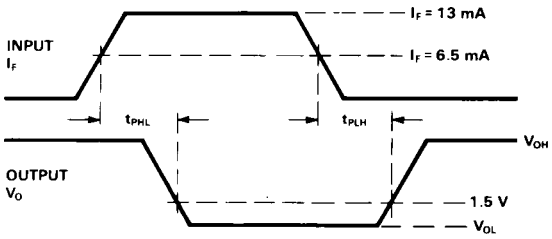


Figure 4. Test Circuit for t_{PHL} and t_{PLH}.*

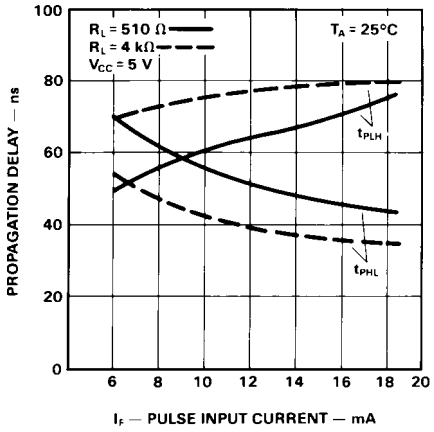


Figure 5. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

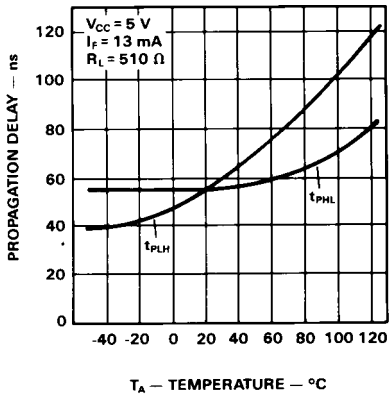


Figure 6. Propagation Delay vs. Temperature.

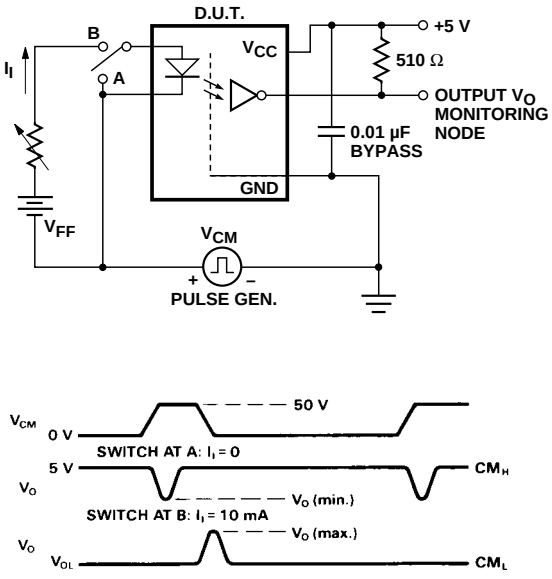


Figure 7. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

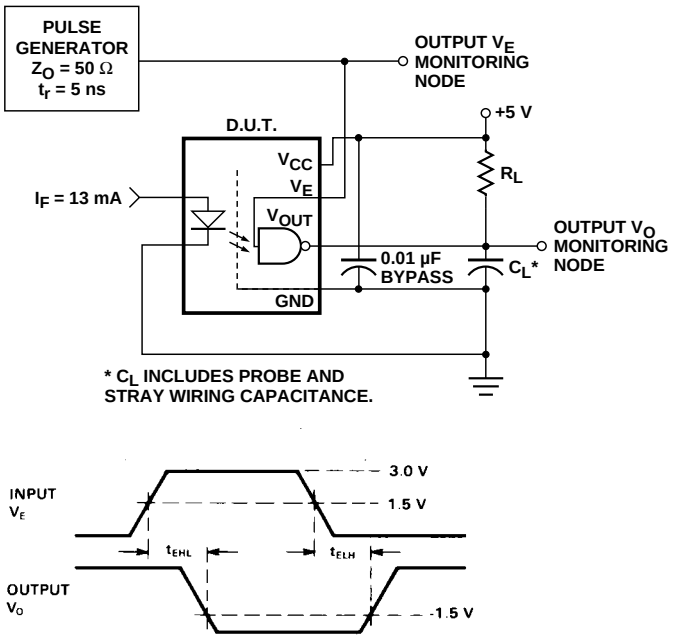


Figure 8. Test Circuit for t_{EHL} and t_{ELH}.

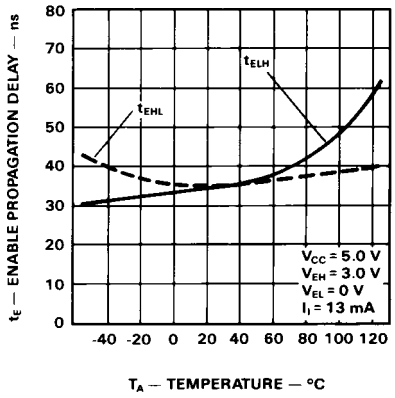


Figure 9. Enable Propagation Delay vs. Temperature.

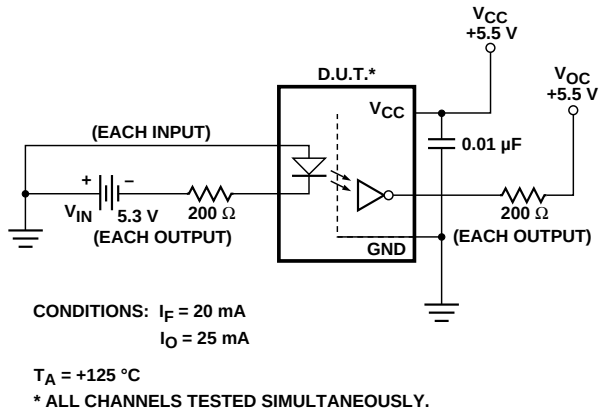
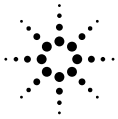


Figure 10. Operating Circuit for Burn-In and Steady State Life Tests.



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Agilent's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H and Class K devices are also in compliance with DSCC drawings 81028, 5962-90855 and 5962-98001.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

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