Features

- **8-bit Bi-directional I/O Port**
- **Individual Pull-up Resistors**
- **Data and Low-order Address Port for External Data SRAM**

Description

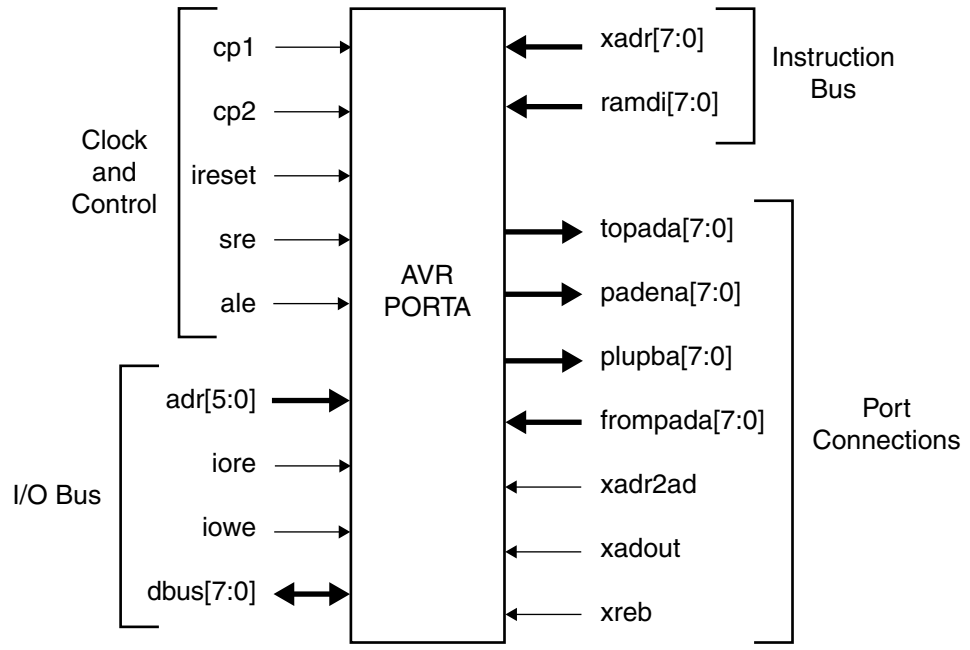
The AVRPORTA module is an 8-bit, general purpose I/O Port. It is also used to output the low-order address byte and to transfer data when accessing external data memory.

Specific Peripheral Information

The AVRPORTA peripheral is approximately 260 gates. It is designed and described in this datasheet to perform functionally identical to PORT A in the AVR® ATmega103 datasheet (literature #0945B). Any differences will be listed in the section named "Modifications to Standard Product." The peripheral was designed to function like the standard product to enable smoother transition for customers who began development and production with an AVR standard product and now wish to integrate their design into an ASIC. If the configuration of AVRPORTA does not satisfy customer requirements, it can be modified to different specifications.

This datasheet is described with a tri-state databus configuration, which is the same configuration as the AVR standard products. If desired, the AVRPORTA peripheral can be provided in a split databus configuration.

Figure 1. Physical Connections



Gate Array/ Embedded Array ASIC Macrocell

AVRPORTA

Preliminary

Rev. 1275A–07/00

Table 1. AVRPORTA Signal Descriptions

Connection Name	Description	Direction	Description
AVR Control			
cp1	System Clock (phase 1)	Input	External SRAM data is latched on cp1 positive edge.
cp2	System Clock (phase 2)	Input	Any PORT A register contents are updated only on cp2 positive edge.
ireset	Internal Reset	Input	All PORT A registers are reset to zero by reading dbus, which is driven low by the AVR.
adr[5:0]	I/O Registers Address Bus	Input	Valid only when accompanied by iore or iowe.
iore	I/O Registers Read Enable	Input	Enables a read from the I/O location addressed by adr[5:0].
iowe	I/O Registers Write Enable	Input	Enables a write to the I/O location addressed by adr[5:0].
dbus[7:0]	Data Bus	Input/Output	System data bus—can also be implemented as a split data bus.
I/O Port			
ale	Address Latch Enable	Output	Latches low-order address byte into PORT A when asserted (first access cycle). Data is latched into PORTA when de-asserted (second access cycle).
sre	External SRAM Enable	Input	When asserted, the alternate pin functions of AD0-7 on PORT A are activated.
topada[7:0]	Input to I/O Pad	Output	This 8-bit intermediate bus connects to the PORT A I/O pads at the top level of the architecture.
padena[7:0]	Output Enable to I/O Pad	Output	This 8-bit bus is the internal logic that sets up each individual port line to an input or an output.
plupba[7:0]	Pull-up Input	Output	This 8-bit bus is the internal logic that controls the MOS pull-up resistor on each individual port line.
frompada[7:0]	Directly from I/O Pad	Input	This 8-bit intermediate bus connects to the PORT A I/O pads at the top level of the architecture.
xadr2ad	External Address Enable	Input	This signal, when asserted and accompanied by sre, drives the low-order external SRAM address byte onto topada[7:0].
xadout	External Address Output Enable	Input	This signal, when asserted and accompanied by sre, drives padena[7:0] high, setting PORT A up as an output port.
xreb	External SRAM Read Enable	Input	This signal, when de-asserted and accompanied by sre, drives frompada[7:0] onto dbus[7:0], enabling a read of PORT A.
Instruction Bus			
xadr[7:0]	External SRAM Address	Input	Low-order address byte of external SRAM. This is an input to the AVRPORTA module because the address is sent back out to the PORT A I/O pads via topada[7:0].
ramdi[7:0]	External SRAM Data	Input	Data byte to/from external SRAM. This is an input to the AVRPORTA module because the address is sent back out to the PORT A I/O pads via topada[7:0].

Modifications to Standard Product

The only functional difference between the AVRPORTA peripheral and PORT A in the AVR Atmega103 is the logic associated with the SRE bit in the MCU Control Register. If the ASIC is designed with the external SRAM high-order address residing on a multi-function I/O port, the assertion of SRE disables the port from functioning as digital I/O. However, this will not be the case if the customer elects to design the ASIC with a dedicated external SRAM address bus.

Recommendations

I/O Memory Map

In an ASIC design, the AVRPORTA may be placed anywhere within the I/O memory map. However, it is recommended that the addressing scheme in Table 2 be followed due to the following reasons.

1. Any software that exists for an AVR standard product will be ported more easily to the new AVR-based ASIC.
2. New software development using AVR Studio® can be done using the built-in I/O PORT A peripheral window. If AVRPORTA is relocated within the memory map, all PORT A activity within AVR Studio may only be observed via the I/O section of the New Memory View window.

Table 2. Recommended Placement of AVRPORTA into I/O Memory Map

Address	Name	Description
$1B	PORTA	PORT A Data Register
$1A	DDRA	PORT A Data Direction Register
$19	PINA	PORT A Input Pins

Interrupt Priority

There are no interrupts associated with this implementation of AVRPORTA.

I/O-Ports

Port A

PORT A is an 8-bit, bi-directional I/O port with internal pull-ups.

Three data memory address locations are allocated for Port A, one each for the Data Register – PORTA, $1B($3B), Data Direction Register – DDRA, $1A($3A) and the Port A Input Pins – PINA, $19($39). The Port A Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The PORT A output buffers can sink 40 mA and thus drive LED displays directly. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The PORT A pins have alternate functions related to the optional external data SRAM. PORT A can be configured to be the multiplexed low-order address/data bus during accesses to the external data memory.

When PORT A is set to the alternate function by the SRE – External SRAM Enable – bit in the MCUCR – MCU Control Register, the alternate settings override the data direction register.

The PORT A Data Register - PORTA

Bit	7	6	5	4	3	2	1	0	
$1B ($3B)	**PORTA7**	**PORTA6**	**PORTA5**	**PORTA4**	**PORTA3**	**PORTA2**	**PORTA1**	**PORTA0**	**PORTA**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The PORT A Data Direction Register - DDRA

Bit	7	6	5	4	3	2	1	0	
$1A ($3A)	**DDA7**	**DDA6**	**DDA5**	**DDA4**	**DDA3**	**DDA2**	**DDA1**	**DDA0**	**DDRA**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The PORT A Input Pins Address - PINA

Bit	7	6	5	4	3	2	1	0	
$19 ($39)	**PINA7**	**PINA6**	**PINA5**	**PINA4**	**PINA3**	**PINA2**	**PINA1**	**PINA0**	**PINA**
Read/Write	R	R	R	R	R	R	R	R	
Initial value	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

The Port A Input Pins address – PINA – is not a register, and this address enables access to the physical value on each Port A pin. When reading PORTA the PORTA Data Latch is read, and when reading PINA, the logical values present on the pins are read.

PORTA as General Digital I/O

All eight bits in PORT A are equal when used as digital I/O pins.

PAn, General I/O pin: The DDAn bit in the DDRA register selects the direction of this pin, if DDAn is set (one), PAn is configured as an output pin. If DDAn is cleared (zero), PAn is configured as an input pin. If PORTAn is set (one) when the pin configured as an input pin, the MOS pull up resistor is activated. To switch the pull up resistor off, PORTAn has to be cleared (zero) or the pin has to be configured as an output pin.

Table 3. DDAn Effects on PORT A Pins

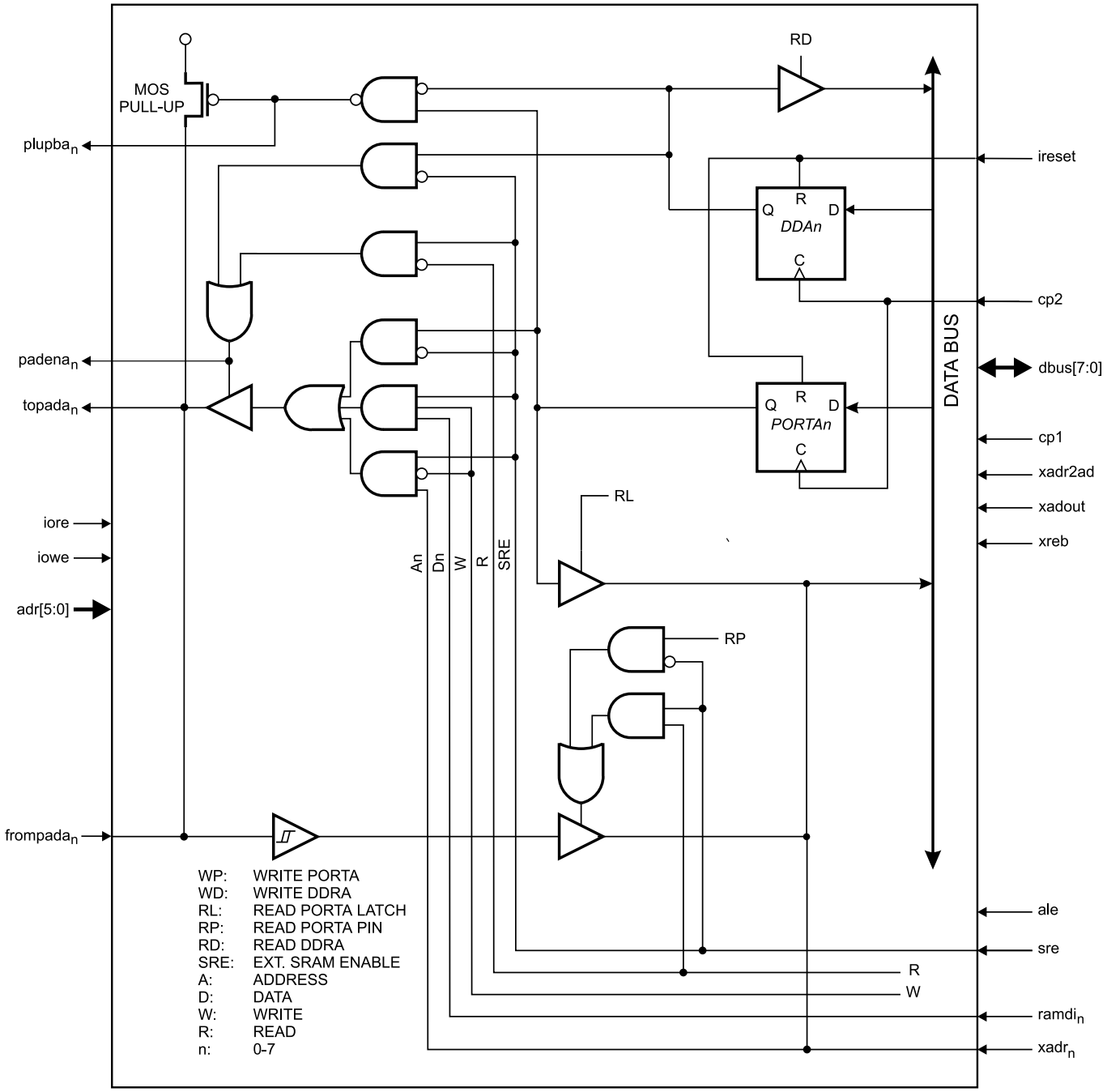
DDAn	PORTAn	I/O	Pull up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PAn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

Note: n: 7, 6...0, pin number

PORT A Schematics

Note that all port pins are synchronized. The synchronization latch is, however, not shown in the figure.

Figure 2. PORTA Schematic Diagrams (Pins PA0 - PA7)



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