AL5DS9xx9V Data Sheets

3.3V Synchronous Dual-Port SRAM

AL5DS9349V/59V/69V/79V

4K/8K/16K/32K x 18 bits

AL5DS9269/79V

16K/32K x 16 bits

AL5DS9149/59/69/79/89V

4K/8K/16K/32K/64K x 9 bits

AL5DS9069/79/89V

16K/32K/64K x 8 bits

Preliminary

Amendments (Since January 4, 2002)

02.01.04	Preliminary version 0.1
02.01.10	Preliminary version 0.2: (1) Modifies truth table and note descriptions in paragraph 7 (2) Modifies Absolute Maximum Ratings in paragraph 8.1 (3) Modifies C_{IN} and C_{OUT} DC characteristics in paragraph 8.3 (4) Modifies Bank Select Pipelined Read and Counter Rest in Pipelined Mode timing diagrams
02.04.09	Preliminary version 0.3: (1) Modifies features in paragraph 2 (2) Modifies ordering information in paragraph 4.1 (3) Modifies AC characteristics in paragraph 8.5
02.05.07	Preliminary version 0.4: (1) Modifies marking information in paragraphs 4 and 6 (2) Modifies the font type in paragraphs 6 and 9
02.09.25	Preliminary version 0.5: (1) Split the datasheets to two parts: AL5DS9389V/9289V/9199V/9099V for 1M bit density and other parts for less than 1M bit density (2) Modifies the pin-out diagram in paragraph 6 (3) Modifies the truth table of address control in paragraph 7
02.11.01	Preliminary version 0.6: Modifies the DC characteristics in paragraph 8.3

THE INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE WIHOUT NOTICE.

AL5DS9XX9V 3.3V Synchronous Dual-Port SRAM

Contents:

1 General Description

A Dual-port RAM is a static RAM with a dual-ported cell. There are separate address, data and control signals for each port to access a common SRAM array. A dual-port RAM is generally classified with FIFOs as a "specialty" memory. They are most commonly used in communications that include the exchange of data between processors, processes and systems.

Each port contains an internal counter for fast memory access applications. The initial address of the internal counter is loaded with the port's Address Strobe (/ADS). It also allows the Counter Enable (/CNTEN) to increment the internal counter on each Low to High transition of that port's clock signal. The counter can address the entire memory array and will loop back to start (address 0). The internal counter will be reset to zero while asserting Counter Reset (/CNTRST).

The AL5DS9xx9V is a high speed, 3.3V, synchronous, CMOS, dual-ported SRAM series. The AL5DS9389V is configured as 64K x 18-bit, AL5DS9289V as 64K x 16-bit, AL5DS9199V as 128K x 9-bit and AL5DS9099V as 128K x 8-bit. All these parts support both Pipelined and Flow-Through modes that are selected via the Pipe/FT pin. In the Pipelined mode, two cycles are required to reactivate the data outputs. The AL5DS9xx9V series features dual Chip Enables that allow simple depth and width expansion without external control logic.

All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages. AL5DS9289V and AL5DS9389V are also available in 128-pin TQFP packages.

2 Features

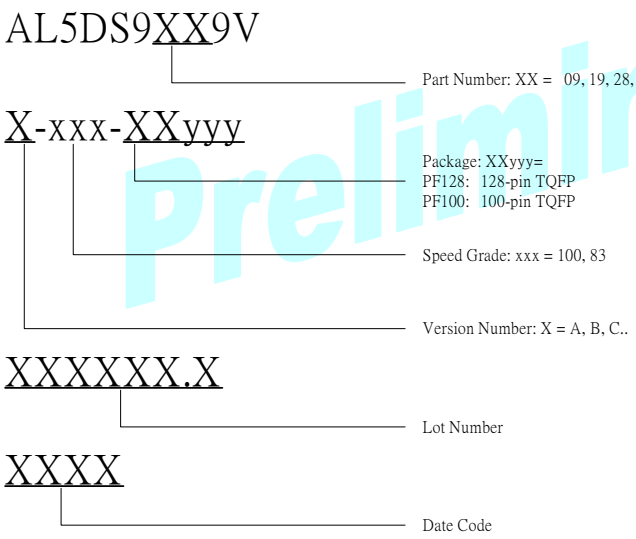
- True dual ported memory cells
- 4 Flow-Through/Pipelined devices:
  -- 64K x 18-bit organization (AL5DS9389V)
  -- 64K x 16-bit organization (AL5DS9289V)
  -- 128K x 9-bit organization (AL5DS9199V)
  -- 128K x 8-bit organization (AL5DS9099V)
- Supports byte write/read for 16/18 bit devices
- Separate upper-byte and lower-byte controls for bus matching (only for 16/18 bit devices)
- 3 modes supported:
  -Pipelined
  -Flow-Through
  -Burst
- Counter enable and reset
- Fast 100-MHz operation on both ports in Pipelined output mode
- Supports depth and width expansion
- 0.25-micron CMOS for optimum speed/power
- High speed clock to data access
- 3.3V low operating power
- Pin-compatible and functionally equivalent to IDT or Cypress
- Available in 100 or 128 pin TQFP

3 Applications

- Cellular Base Stations
- Cellular Phones
- Multi-protocol Routers
- LAN/WAN Switches
- PBXs
- RAIDs (Storage Networks)
- Set-top Boxes
- Audio/Video Editing
- Graphics Accelerators
- Satellite Encoders
- Cable Modems
- Flight Simulators
- High-end Printing Servers
- Ultrasound Imaging

4 Chip Information

4.1 Marking Information



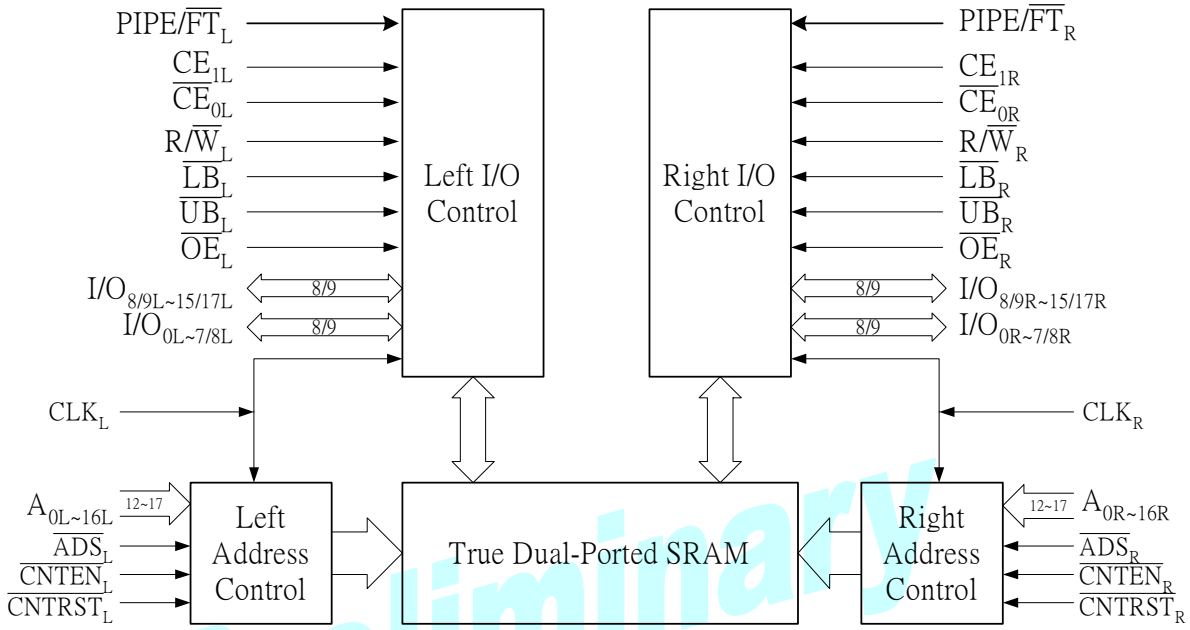
4.2 Ordering Information

Two packages are available for AL5DS9xx9V series Synchronous Dual-Port SRAM.

Part number	Speed (MHz)	Package	Power Supply	Word Length	Bus Width
AL5DS9069V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	16K	8 bits
AL5DS9069V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	16K	8 bits
AL5DS9079V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	32K	8 bits
AL5DS9079V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	32K	8 bits
AL5DS9089V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	64K	8 bits
AL5DS9089V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	64K	8 bits
AL5DS9149V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	4K	9 bits
AL5DS9149V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	4K	9 bits
AL5DS9159V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	8K	9 bits

Part number	Speed (MHz)	Package	Power Supply	Word Length	Bus Width
AL5DS9159V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	8K	9 bits
AL5DS9169V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	16K	9 bits
AL5DS9169V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	16K	9 bits
AL5DS9179V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	32K	9 bits
AL5DS9179V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	32K	9 bits
AL5DS9189V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	64K	9 bits
AL5DS9189V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	64K	9 bits
AL5DS9269V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	16K	16 bits
AL5DS9269V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	16K	16 bits
AL5DS9279V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	32K	16 bits
AL5DS9279V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	32K	16 bits
AL5DS9269V (A-100-PF128)	100	128 pin TQFP	3.3V±10%	16K	16 bits
AL5DS9269V (A-83-PF128)	83	128 pin TQFP	3.3V±10%	16K	16 bits
AL5DS9279V (A-100-PF128)	100	128 pin TQFP	3.3V±10%	32K	16 bits
AL5DS9279V (A-83-PF128)	83	128 pin TQFP	3.3V±10%	32K	16 bits
AL5DS9349V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	4K	18 bits
AL5DS9349V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	4K	18 bits
AL5DS9359V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	8K	18 bits
AL5DS9359V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	8K	18 bits
AL5DS9369V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	16K	18 bits
AL5DS9369V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	16K	18 bits
AL5DS9379V (A-100-PF100)	100	100 pin TQFP	3.3V±10%	32K	18 bits
AL5DS9379V (A-83-PF100)	83	100 pin TQFP	3.3V±10%	32K	18 bits
AL5DS9379V (A-100-PF128)	100	128 pin TQFP	3.3V±10%	32K	18 bits
AL5DS9379V (A-83-PF128)	83	128 pin TQFP	3.3V±10%	32K	18 bits

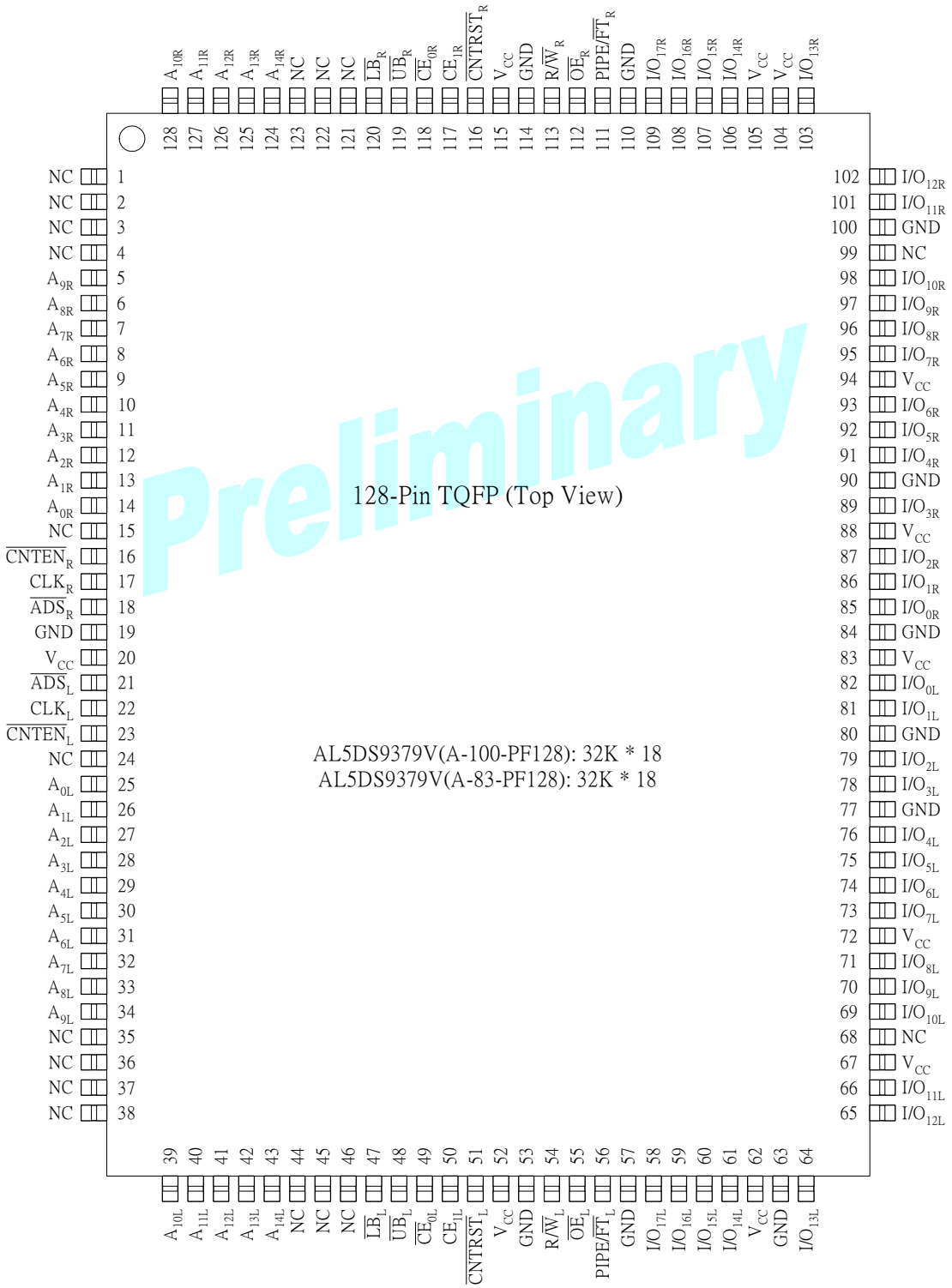
5 Function Block Diagram



Note 1: $\overline{LB}_R$ and $\overline{UB}_R$ are for 16/18 bit devices only.
Note 2: $I/O_{0\sim7}$ for 8/16 bit devices, $I/O_{0\sim8}$ for 9/18 bit devices, $I/O_{8\sim15}$ for 16 bit devices, and $I/O_{9\sim17}$ for 18 bit devices.
Note 3: $A_{0\sim15}$ for 64K, and $A_{0\sim16}$ for 128K devices

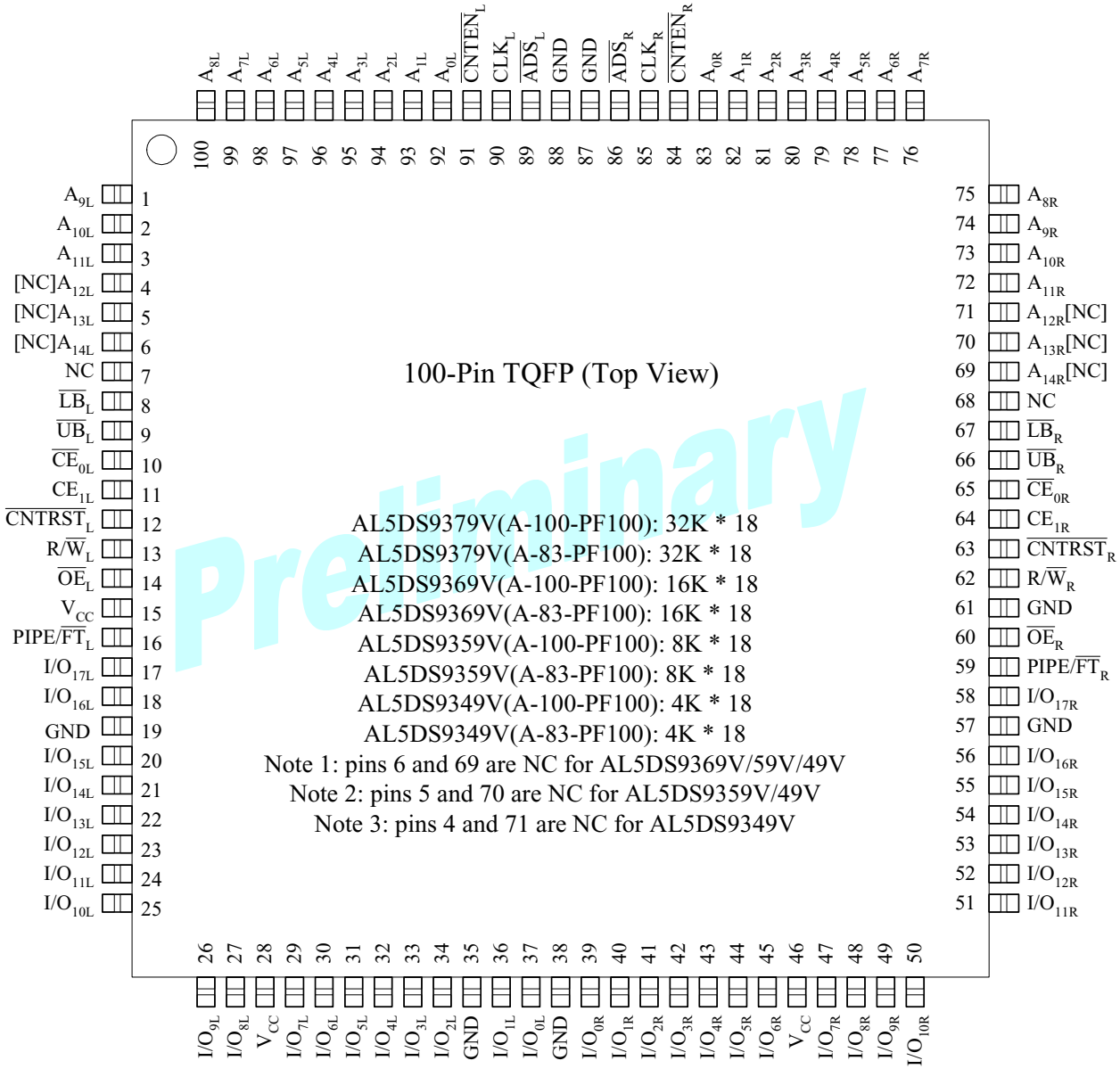
6 Pin-out Diagram

128 pin 14mm*20mm*1.4mm TQFP package-1:

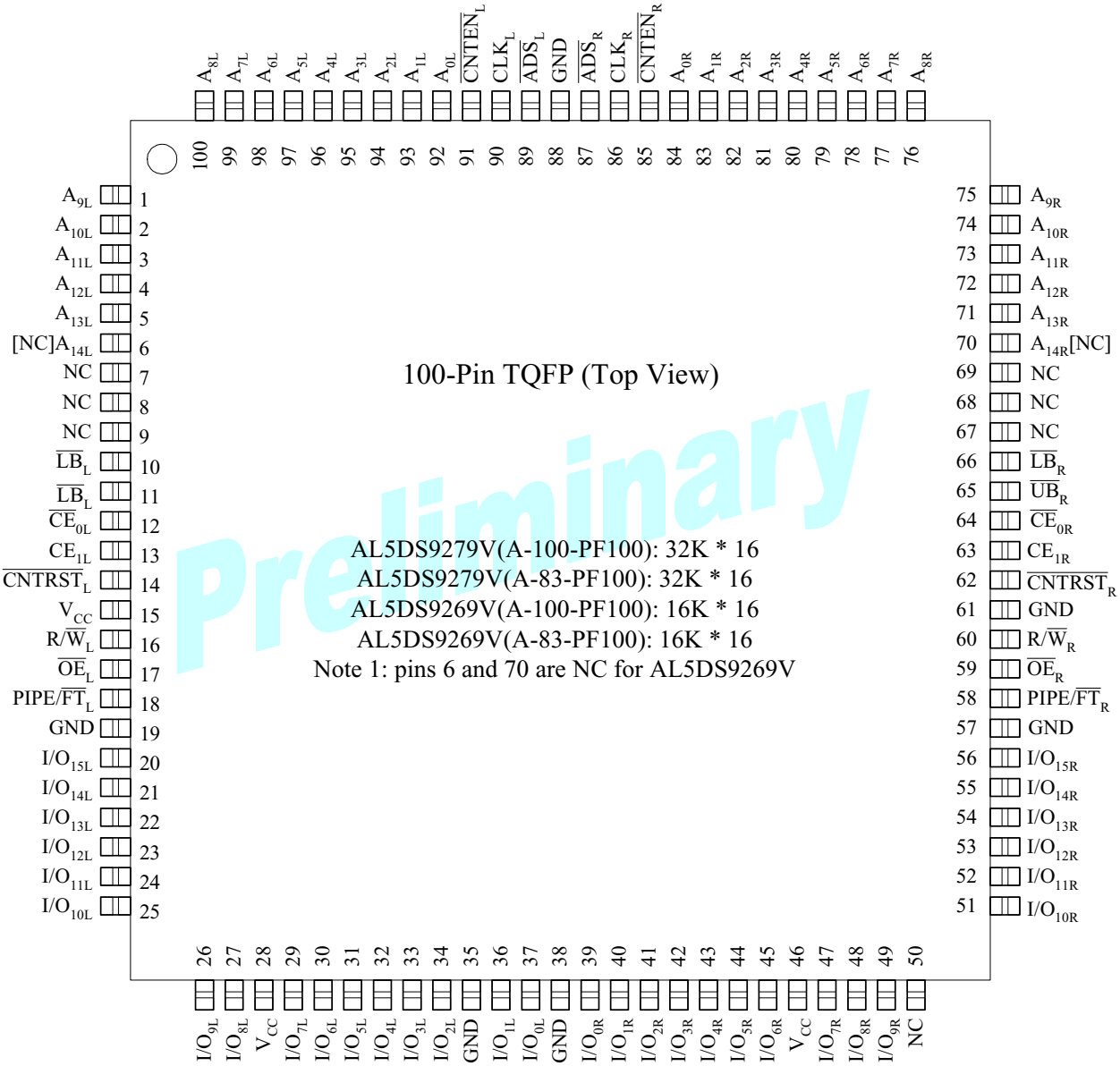


128 pin 14mm*20mm*1.4mm TQFP package-2:

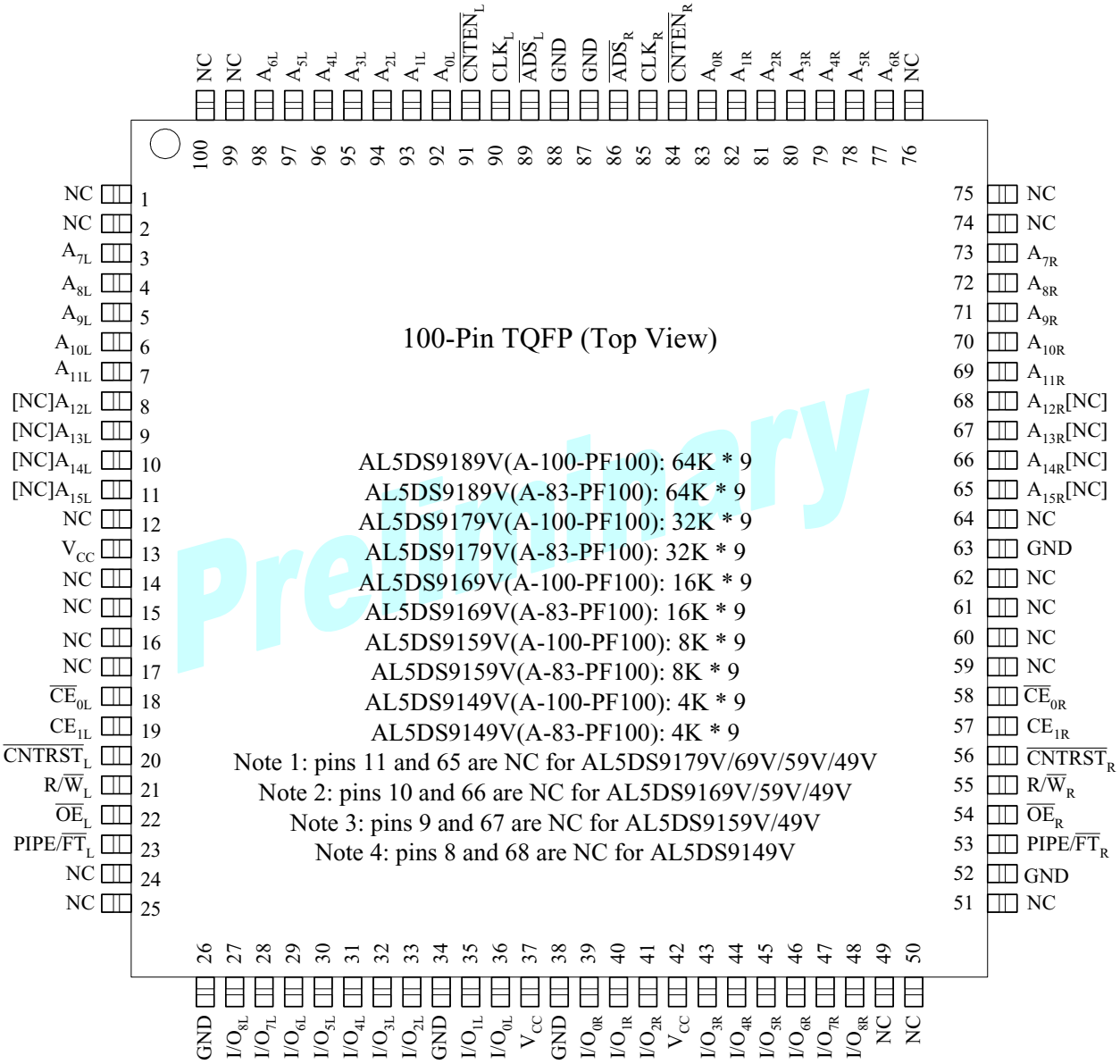
100 pin 14mm*14mm*1.4mm TQFP package-1:



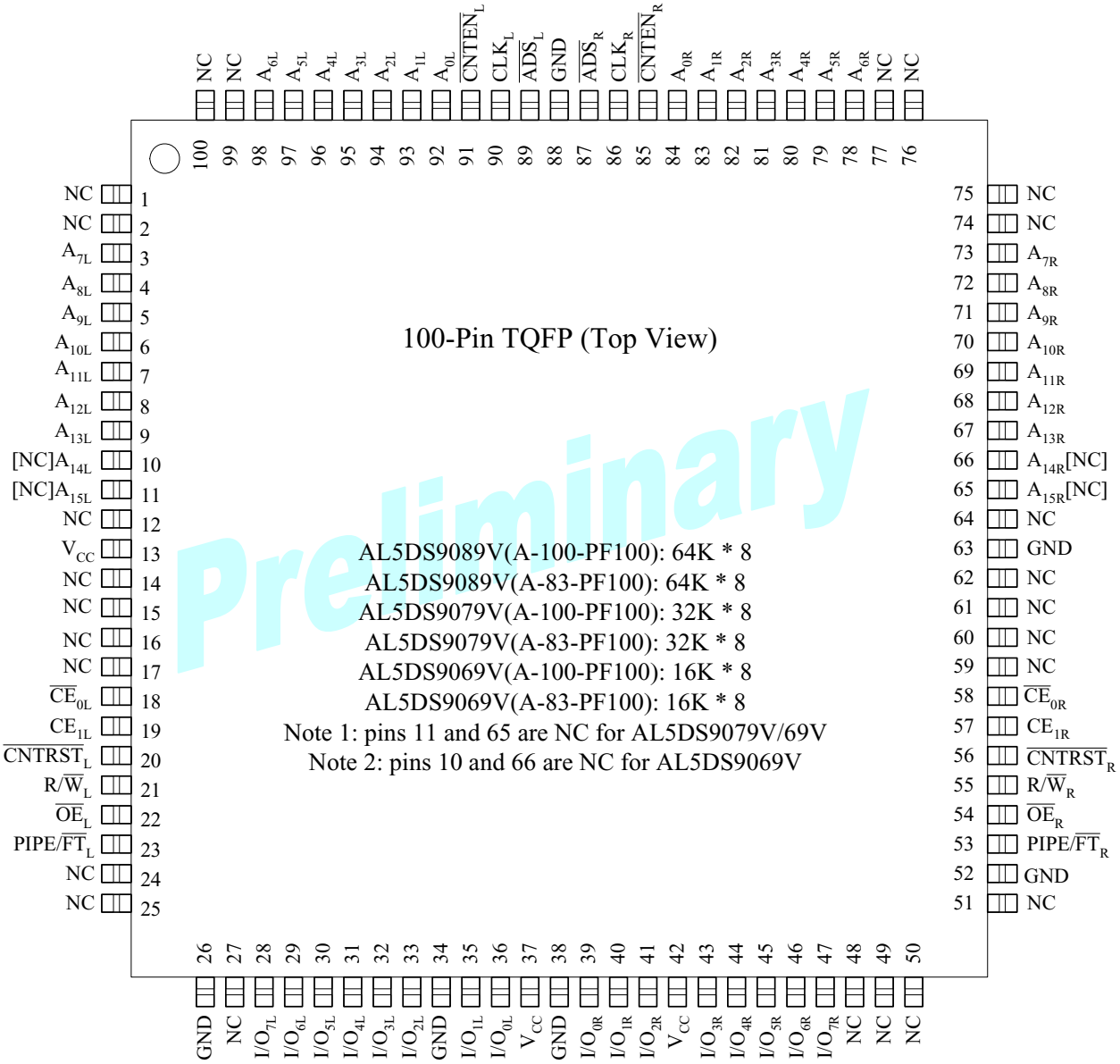
100 pin 14mm*14mm*1.4mm TQFP package-2:



100 pin 14mm*14mm*1.4mm TQFP package-3:



100 pin 14mm*14mm*1.4mm TQFP package-4:



7 Pin Definition and Description

The pin-out definitions are described as follows:

Left Port	Right Port	I/O type	Description
A_{0L}~A_{16L}	A_{0R}~A_{16R}	I	Address bus.
/ADS_L	/ADS_R	I	Address Strobe. Low active. Asserting this signal LOW while using an external address will access the port. /ADS is only dependent of /CNTRST control signal.
/$CNTEN_L$	/$CNTEN_R$	I	Counter Enable. Low active. When counter is enabled, the internal address counter increments one on each rising edge of CLK regardless of Chip Enable and Lower Byte or Upper Byte Selects.
/$CNTRST_L$	/$CNTRST_R$	I	Counter Reset. Low active. Resets the internal address counter to zero. This signal is independent of all other control signals.
/CE_{0L}, CE_{1L}	/CE_{0R}, CE_{1R}	I	Chip Enable. Low active for Chip Enable 0 and High active for Chip Enable 1.
CLK_L	CLK_R	I	Clock input.
I/O_{0L}~I/O_{17L}	I/O_{0R}~I/O_{17R}	I/O	Data bus.
/LB_L	/LB_R	I	Lower Byte Select. Low active. Enables the read and write operations to the lower byte (I/O_0-I/O_8 for 18 bit devices, I/O_0-I/O_7 for 16 bit devices) while asserting this signal Low. Not available for 8/9 bit devices.
/UB_L	/UB_R	I	Upper Byte Select. Low active. Enables the read and write operations to the upper byte (I/O_9-I/O_{17} for 18 bit devices, I/O_8-I/O_{15} for 16 bit devices) while asserting this signal Low. Not available for 8/9 bit devices.
/OE_L	/OE_R	I	Output Enable. Low active. Asynchronous input signal.
R/W_L	R/W_R	I	Read/Write Enable. High active for read operations and Low active for write operations.
$PIPE/FT_L$	$PIPE/FT_R$	I	Pipelined and Flow-Through Mode Select. High active for Pipelined mode and Low active for Flow-Through mode.
NC		-	No connection
Digital Power			
V_{CC}		DP	Digital power
GND		DP	Digital ground

Note: For I/O type, I, O, and DP indicate input, output, and digital power respectively.

For 18 or 16 bit devices, the truth table of read/write and enable control is as follows:

/CE0	CE1	CLK	R/W	/UB	/LB	/OE	Upper byte	Lower byte	Note
X	X	X	X	X	X	H	High-Z	High-Z	Outputs disabled
L	H	↑	H	H	L	L	High-Z	Data output	Read Lower byte only
L	H	↑	H	L	H	L	Data output	High-Z	Read Upper byte only
L	H	↑	H	L	L	L	Data output	Data output	Read both bytes
L	H	↑	L	H	L	X	High-Z	Data input	Write to Lower byte
L	H	↑	L	L	H	X	Data input	High-Z	Write to Upper byte
L	H	↑	L	L	L	X	Data input	Data input	Write to both bytes
X	X	↑	X	H	H	X	High-Z	High-Z	Both bytes disabled
H	X	↑	X	X	X	X	High-Z	High-Z	Chip disabled (Note 2)
X	L	↑	X	X	X	X	High-Z	High-Z	Chip disabled (Note 2)

Note 1: H, L, X, and ↑ denote V_{IH}, V_{IL}, Don't Care and Rising-Edge Trigger, respectively.

Note 2: For Pipelined mode, chip is disabled on the following clock cycle if /CE changes state.

For 9 or 8 bit devices, the truth table of read/write and enable control is as follows:

/CE0	CE1	CLK	R/W	/OE	Data I/O	Note
X	X	X	X	H	High-Z	Outputs disabled
L	H	↑	H	L	Data output	Read operation
L	H	↑	L	X	Data input	Write operation
H	X	↑	X	X	High-Z	Chip disabled (Note 2)
X	L	↑	X	X	High-Z	Chip disabled (Note 2)

Note 1: H, L, X, and ↑ denote V_{IH}, V_{IL}, Don't Care and Rising-Edge Trigger, respectively.

Note 2: For Pipelined mode, chip is disabled on the following clock cycle if /CE changes state.

The truth table of address counter control is as follows:

/CNTRST	/ADS	/CNTEN	CLK	Address input	Previous address	Internal address	Data I/O	Note
L	X	X	↑	X	X	0	Q_0	Reset internal address counter to 0
H	L	X	↑	A_n	X	A_n	Q_n	Load external address into internal address counter
H	H	L	↑	X	A_P	A_{P+1}	Q_{P+1}	Enable internal address counter
H	H	L	↑	X	A_{max}	A_0	Q_0	Enable internal address counter (Note 4)
H	H	H	↑	X	A_P	A_P	Q_P	Disable internal address counter

Note 1: H, L, X, and ↑ denote V_{IH}, V_{IL}, Don't Care and Rising-Edge Trigger, respectively.

Note 2: Assuming $/CE_0$, /UB, /LB, and /OE = V_{IL} and assuming CE_1 and R/W = V_{IH}.

Note 3: Data I/O is configured in Flow-Through mode. For Pipelined mode, the data output will be delayed by one cycle.

Note 4: Because the internal address counter will be larger than the maximum memory address, it will not reset the internal address counter to 0 on the next clock cycle when the previous internal address has encountered the maximum memory address. Therefore, the application software should remember to load a new address into the internal address counter or to invoke the /CNTRST signal to reset the internal address counter to 0 if the internal address has encountered the maximum memory address.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

(Exceeding the rating can be harmful to product life. These are only user guidelines and are not tested.)

Parameter		3.3V Rating	Unit
V_{CC}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Input Pin Voltage	-0.3 ~ +(V_{CC}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage Temperature	-40 ~ +125	°C
T_{VSOL}	Vapor Phase Soldering Temperature (15 Sec.)	220	°C

8.2 Recommended Operating Conditions

Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
V_{CC}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{CC}	V
T_{AMB}	Ambient Op. Temperature	0		+70	°C

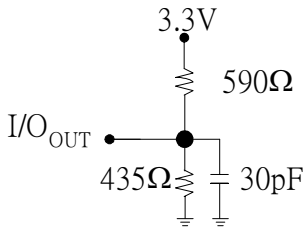
8.3 DC Characteristics

(V_{CC} = 3.3V, GND=0V. T_{AMB} = 0 to 70°C) Note: Some parameters are guaranteed by design only and are not production tested.

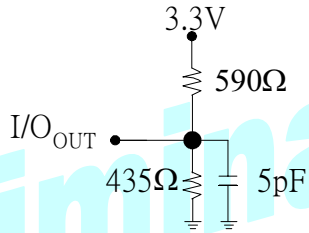
Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
V_{IH}	Hi-level Input Voltage	0.7 V_{CC}	-	V_{CC}	V
V_{IL}	Lo-level Input Voltage	0		0.3 V_{CC}	V
V_{OH}	Hi-level Output Voltage (V_{CC} = Min., I_{OH} = -4 mA)	2.4	-	V_{CC}	V
V_{OL}	Lo-level Output Voltage (V_{CC} = Min., I_{OH} = +4 mA)	-	-	+0.4	V
C_{IN}	Input Capacitance at V_{CC}=3.3V, T_A=25°C and f=1MHz			10	pF
C_{OUT}	Output Capacitance at V_{CC}=3.3V, T_A=25°C and f=1MHz			10	pF
I_{LI}	Input Leakage Current (V_{CC} = 3.6V, V_{IN} = 0V~ V_{CC})			+5	µA
I_{LO}	Output Leakage Current (CE_1 = V_{IL}, V_{OUT} = 0V~ V_{CC})			+5	µA
I_{OZ}	3-state Current (/OE = V_{IH})		TBD		µA
I_{CC}	Operating Current (V_{CC} = Max., I_{OUT} = 0 mA, outputs disabled)		TBD	TBD	mA
I_{SB1}	Standby Current (Both ports are TTL level inputs)		TBD	TBD	mA
I_{SB2}	Standby Current (One port is TTL level inputs)		TBD	TBD	mA
I_{SB3}	Standby Current (Both ports are CMOS level inputs)		TBD	TBD	µA
I_{SB4}	Standby Current (One port is CMOS level inputs)		TBD	TBD	mA

8.4 AC Test Loads

8.4.1 Normal Load (Load 1)



8.4.2 3-State Load (Load 2)



8.5 AC Characteristics

(V_{CC} = 3.3V, GND=0V, T_{AMB} = 0 to 70°C) Note: Some parameters are guaranteed by design only and are not production tested.

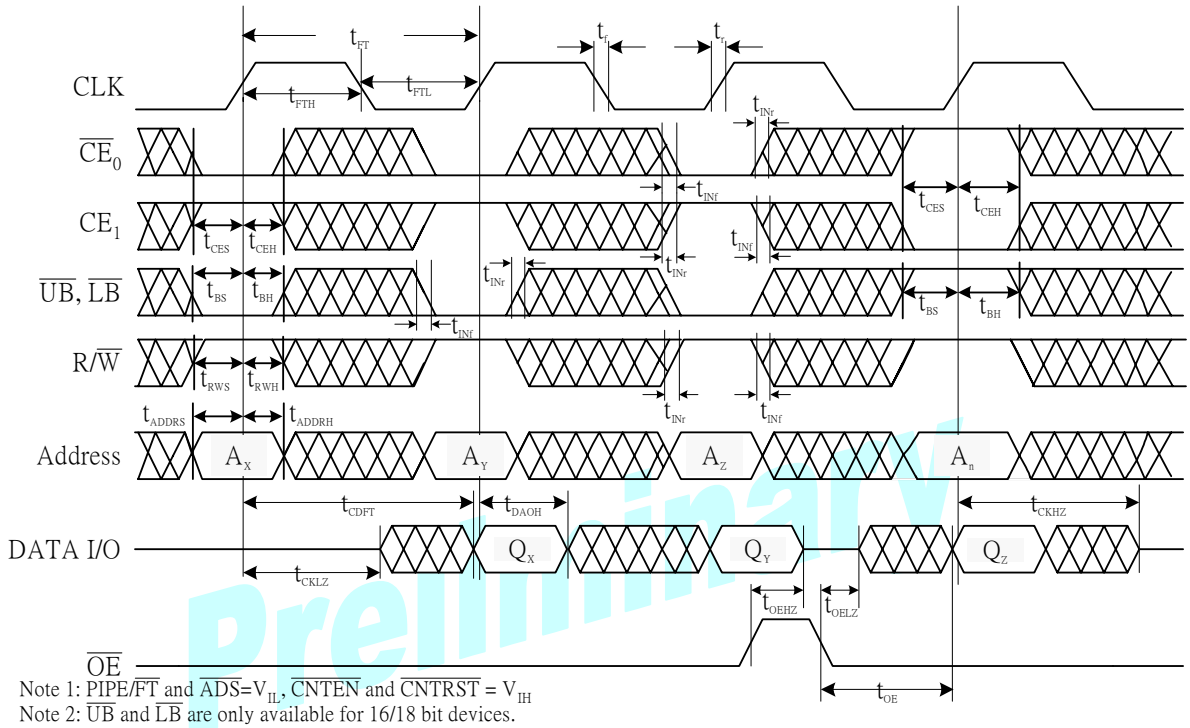
Parameter		3.3V Rating				Unit
		-100		-83		
		Min	Max	Min	Max	
Address Control						
t_{ADDRS}	Setup time for Address	3.5		4		ns
t_{ADDRH}	Hold time for Address	0		0		ns
t_{INr}	Rising time for all control inputs		3		3	ns
t_{INf}	Falling time for all control inputs		3		3	ns
t_{ADSS}	Setup time for /ADS	3.5		4		ns
t_{ADSH}	Hold time for /ADS	0		0		ns
t_{CENS}	Setup time for /CNTEN	3.5		4.5		ns
t_{CENH}	Hold time for /CNTEN	0		0		ns
t_{CRSTS}	Setup time for /CNTRST	3.5		4		ns
t_{CRSTH}	Hold time for /CNTRST	0		0		ns

Parameter		3.3V Rating				Unit
		-100		-83		
		Min	Max	Min	Max	
I/O Control						
t_{INr}	Rising time for all control inputs		3		3	ns
t_{INf}	Falling time for all control inputs		3		3	ns
t_{CES}	Setup time for Chip Enable	3.5		4		ns
t_{CEH}	Hold time for Chip Enable	0		0		ns
t_{RWS}	Setup time for R/W	3.5		4		ns
t_{RWH}	Hold time for R/W	0		0		ns
t_{BS}	Setup time for /UB and /LB (not for 8/9 bit devices)	3.5		4		ns
t_{BH}	Hold time for /UB and /LB (not for 8/9 bit devices)	0		0		ns
t_{DAIS}	Setup time for input data	3.5		4		ns
t_{DAIH}	Hold time for input data	0		0		ns
t_{OE}	Output Enable to data valid		8		9	ns
t_{OELZ}	Output Enable to Low Z [1]	2		2		ns
t_{OEHZ}	Output Enable to High Z [1]	1	7	1	7	ns
t_{CDFT}	Clock to data valid of Flow-Through		15		18	ns
t_{CDPIPE}	Clock to data valid of Pipelined		6.5		7.5	ns
t_{CKLZ}	Clock High to Low Z [1]	2		2		ns
t_{CKHZ}	Clock High to High Z [1]	2	9	2	9	ns
t_{DAOH}	Data output hold time after Clock High	2		2		ns
t_{CWDD}	Write port Clock High to Read data delay		28		30	ns
Clock						
f_{FT}	Frequency of Flow-Through		53		45	MHz
t_{FT}	Clock cycle time of Flow-Through	19		22		ns
δ_{FT}	Duty Factor for Flow-Through (t_{FTH} * f_{FT})	40	60	40	60	%
f_{PIPE}	Frequency of Pipelined		100		83	MHz
t_{PIPE}	Clock cycle time of Pipelined	10		12		ns

Parameter		3.3V Rating				Unit
		-100		-83		
		Min	Max	Min	Max	
δ_{PIPE}	Duty Factor for Pipelined (t_{PIPEH} * f_{PIPE})	40	60	40	60	%
t_r	Rising time for Clock		3		3	ns
t_f	Falling time for Clock		3		3	ns
t_{CCS}	Setup time for Clock to Clock		9		10	ns

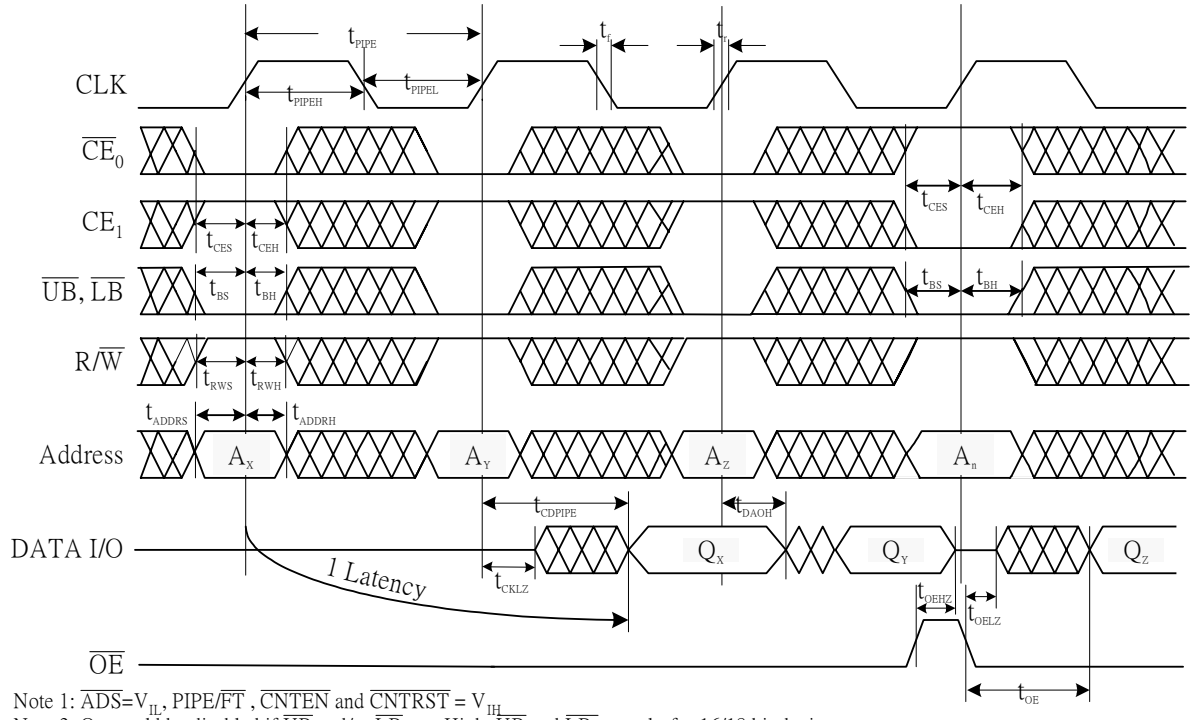
Note 1: The above parameters that use 3-State load (load 2) under test conditions are guaranteed by design only.

9 Timing Diagrams



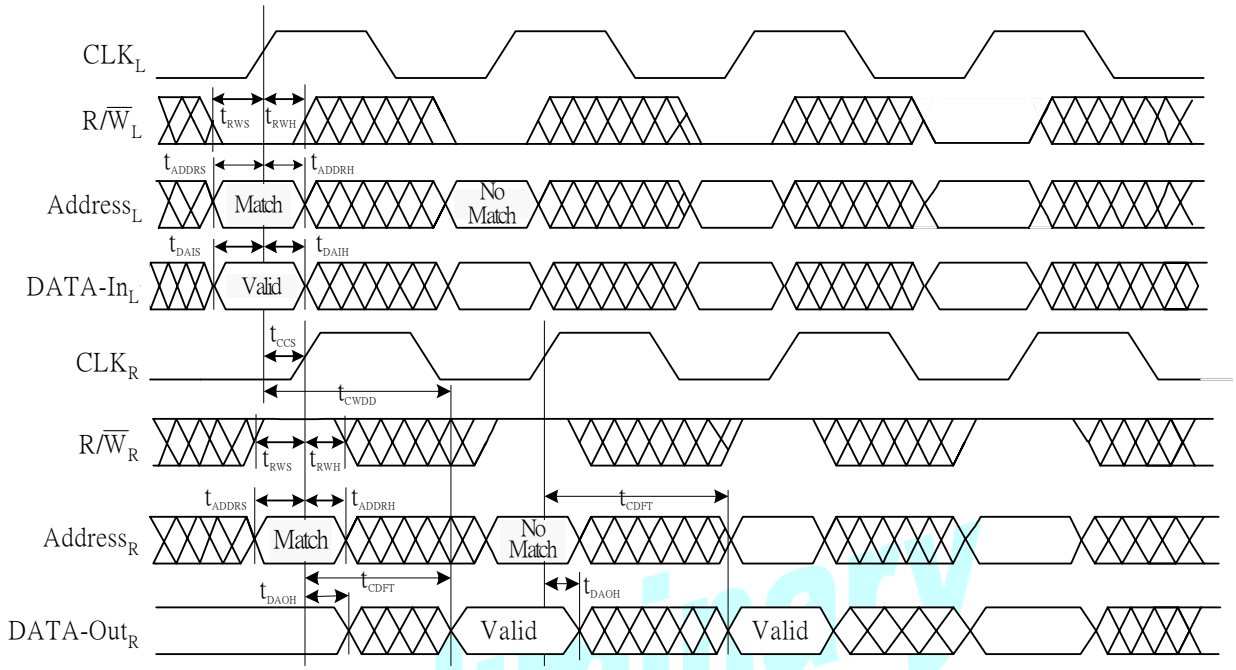
Note 1: PIPE/$\overline{FT}$ and $\overline{ADS}$=V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}
Note 2: $\overline{UB}$ and $\overline{LB}$ are only available for 16/18 bit devices.

Read Cycle for Flow-Through Mode



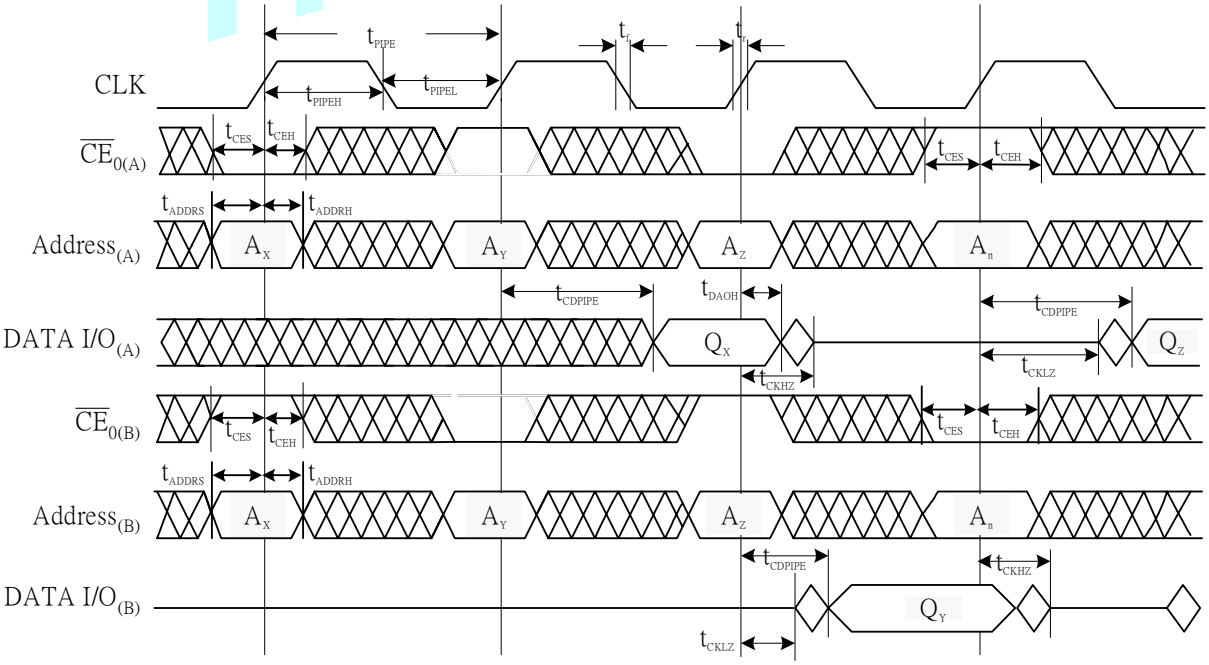
Note 1: $\overline{ADS}$=V_{IL}, PIPE/$\overline{FT}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}
Note 2: Q_Z would be disabled if $\overline{UB}$ and/or $\overline{LB}$ was High. $\overline{UB}$ and $\overline{LB}$ are only for 16/18 bit devices.

Read Cycle for Pipelined Mode



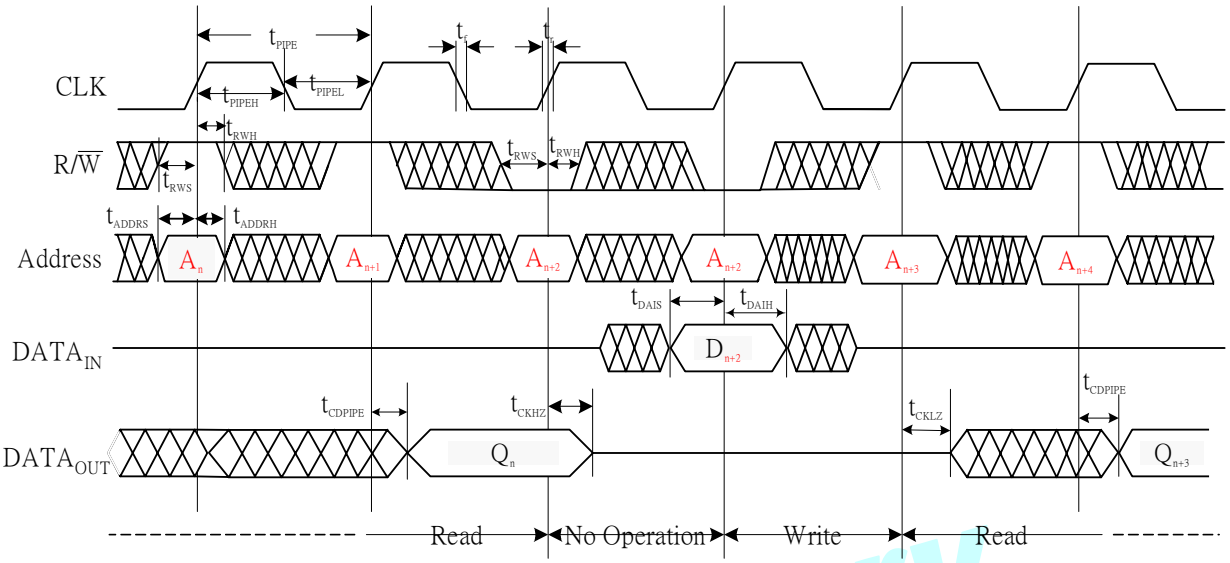
Note1: If T_{CCS} > maximum specified, then data is not valid until $T_{CCS}+T_{CDFT}$ and ignores T_{CWDD}.
Note2: $\overline{OE}_R$, $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, PIPE/$\overline{FT}$ and $\overline{ADS}$=V_{IL}, $\overline{OE}_L$, CE_1, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}

Left Port Write to Flow-Through Right Port Read



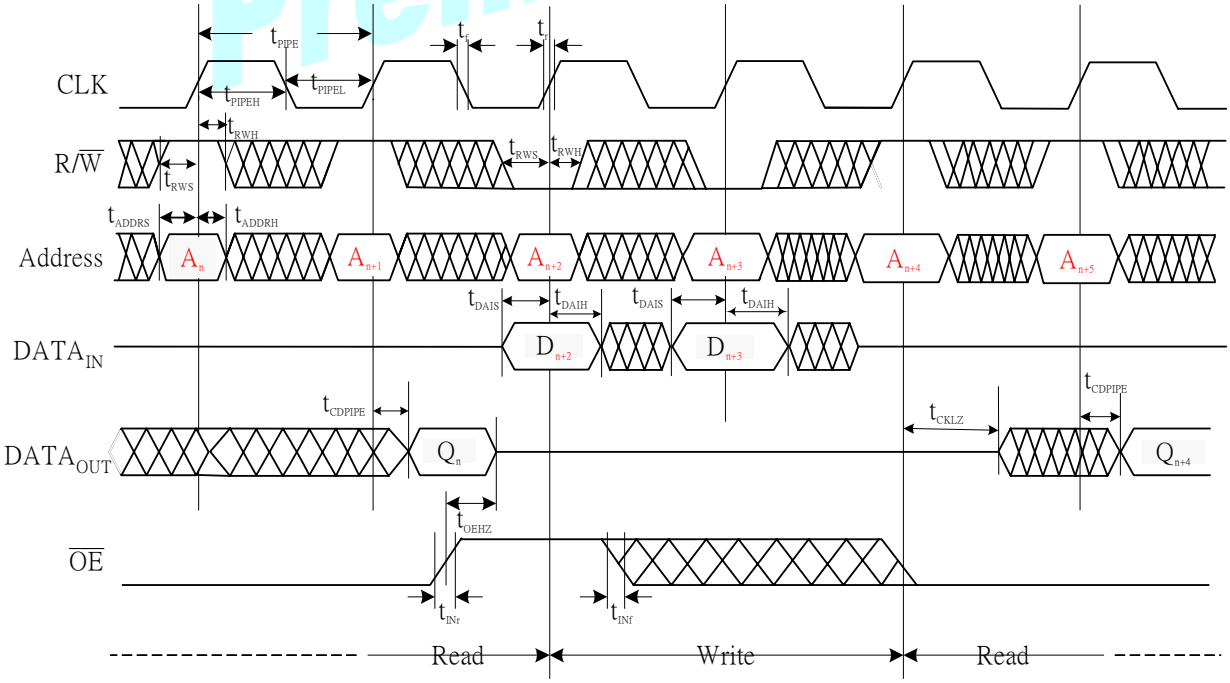
Note 1: $\overline{UB}$, $\overline{LB}$, $\overline{OE}$ and $\overline{ADS}$=V_{IL}, $CE_{1(A)}$, $CE_{1(B)}$, R/$\overline{W}$, PIPE/$\overline{FT}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}
Note 2: Each bank consists of one AverLogic dual port SRAM for this waveform. $Address_{(A)}$ = $Address_{(B)}$

Bank Select Pipelined Read



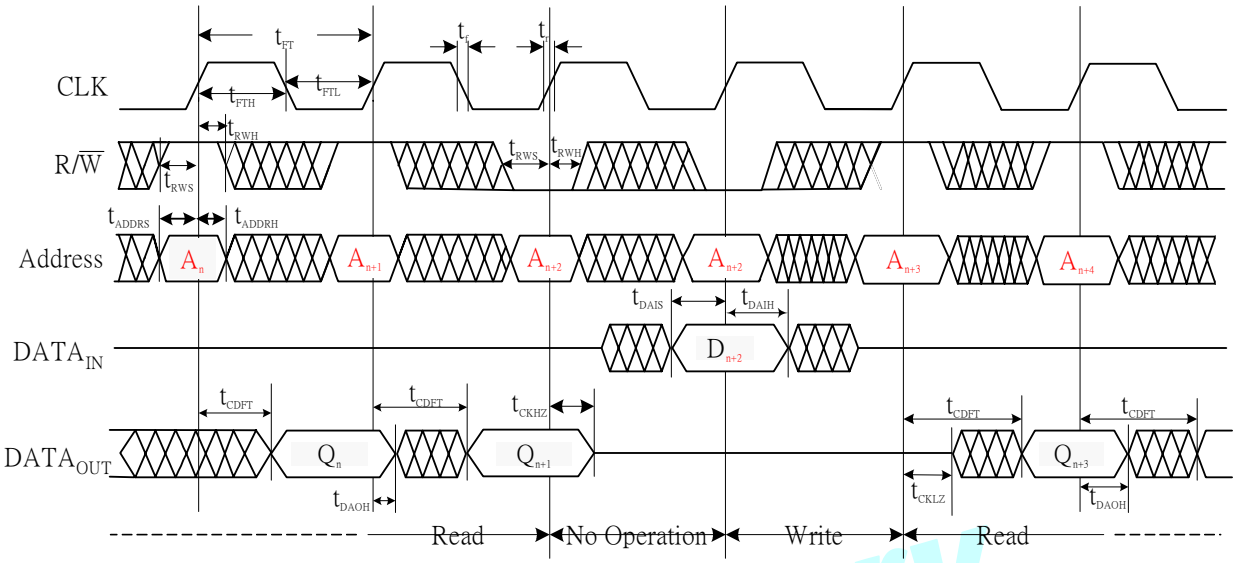
Note 1: $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ and $\overline{ADS}$=V_{IL}, CE_1, PIPE/$\overline{FT}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}
Note 2: Output state is determined by the previous cycle control signals.
Note 3: Data in memory at the selected address should be re-written to ensure data integrity during No Operation cycle.

Pipelined Read-to-Write-to-Read Mode ($\overline{OE}$ = V_{IL})



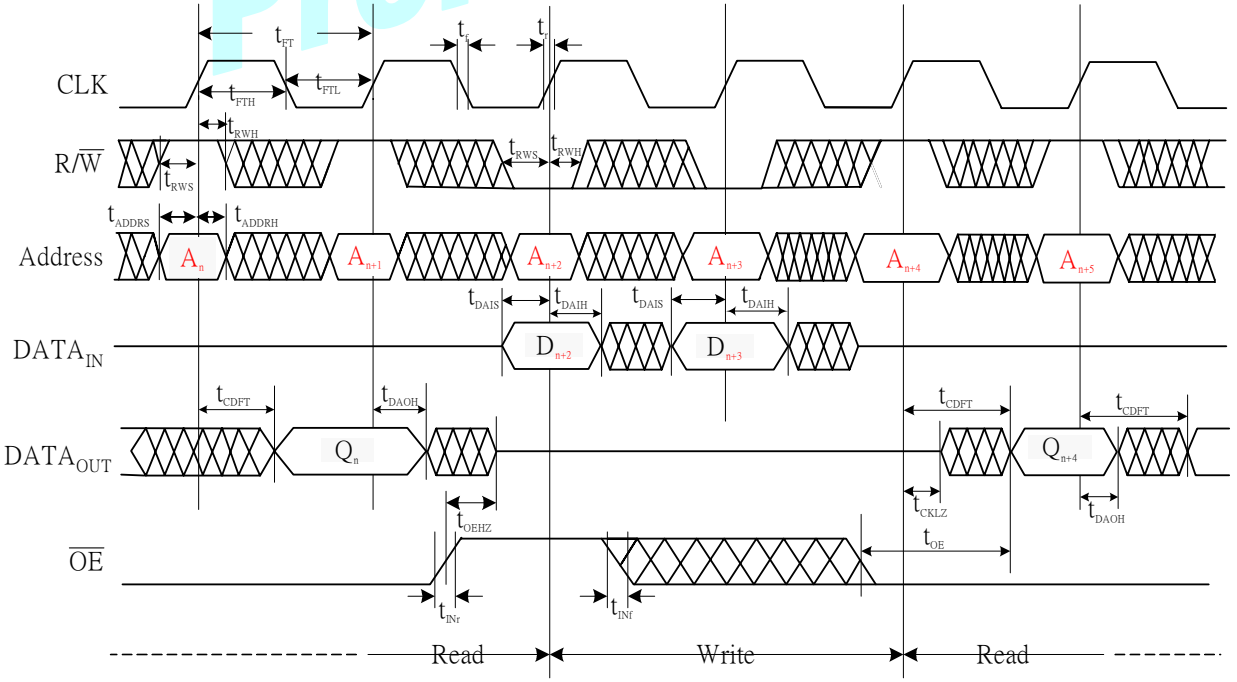
Note 1: $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ and $\overline{ADS}$=V_{IL}, CE_1, PIPE/$\overline{FT}$, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}
Note 2: Output state is determined by the previous cycle control signals.

Pipelined Read-to-Write-to-Read Mode ($\overline{OE}$ controlled)



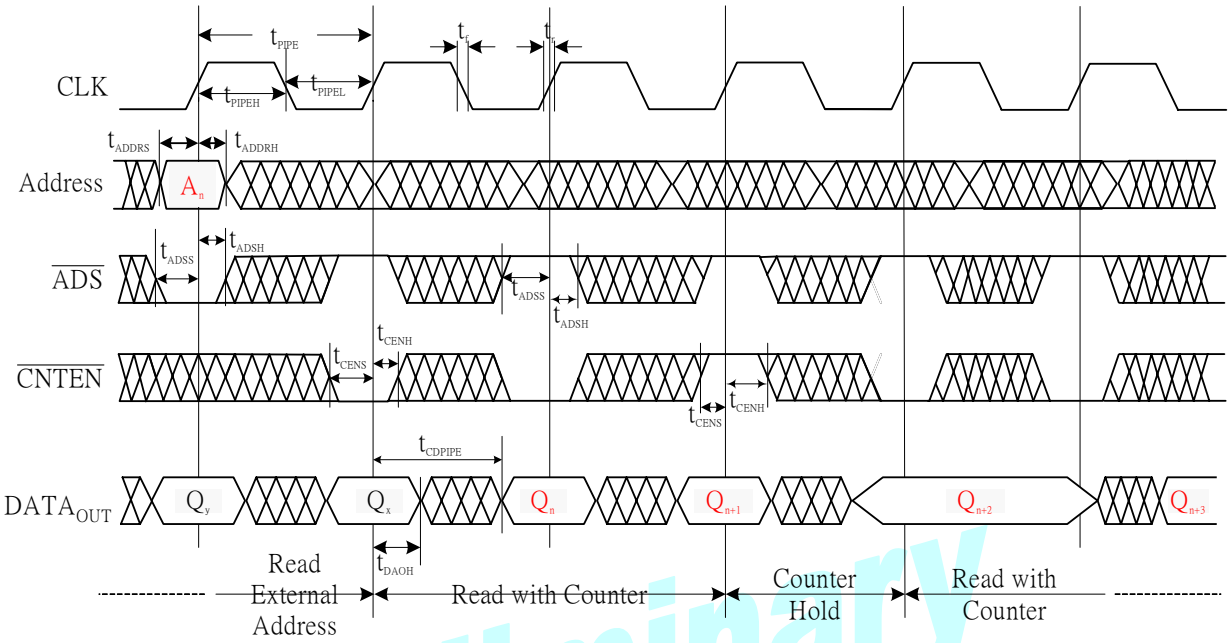
Note 1: $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, PIPE/$\overline{FT}$, and $\overline{ADS}$=V_{IL}, CE_1, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}
Note 2: Output state is determined by the previous cycle control signals.
Note 3: Data in memory at the selected address should be re-written to ensure data integrity during No Operation cycle.

Flow-Through Read-to-Write-to-Read Mode ($\overline{OE}$ = V_{IL})



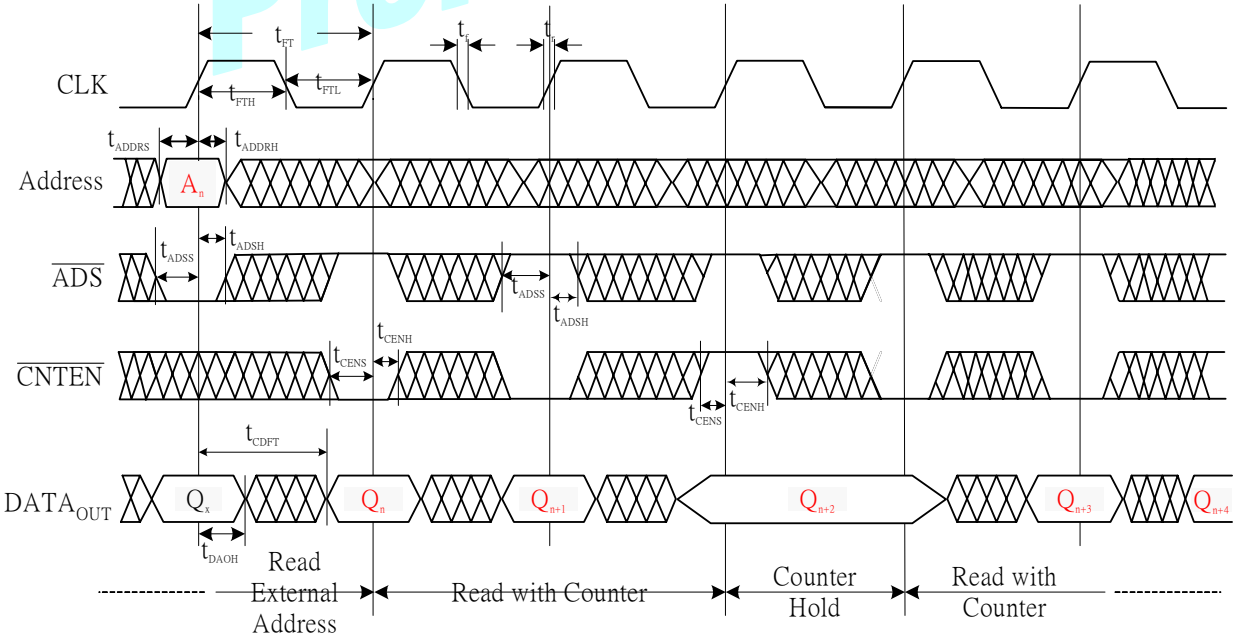
Note 1: $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, PIPE/$\overline{FT}$ and $\overline{ADS}$=V_{IL}, CE_1, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}
Note 2: Output state is determined by the previous cycle control signals.

Flow-Through Read-to-Write-to-Read Mode ($\overline{OE}$ controlled)



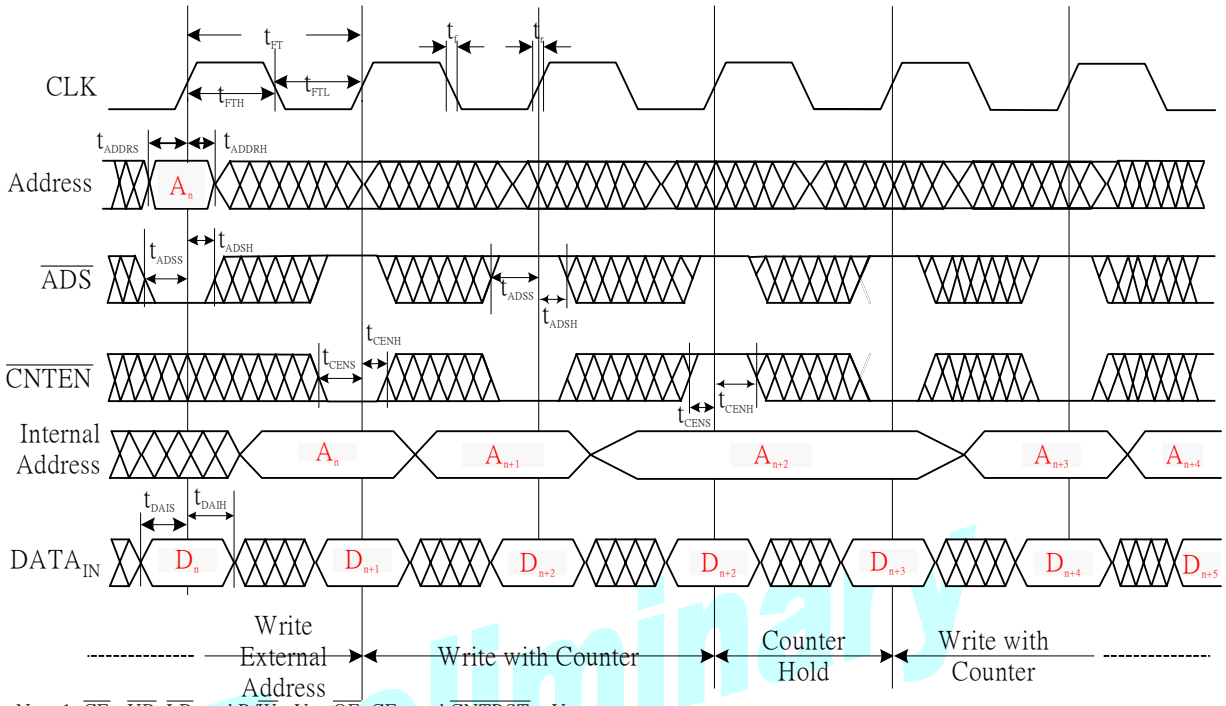
Note 1: $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$ and $\overline{OE}$=V_{IL}, CE_1, PIPE/$\overline{FT}$, R/$\overline{W}$ and $\overline{CNTRST}$ = V_{IH}

Pipelined Read with Internal Address Counter Enable



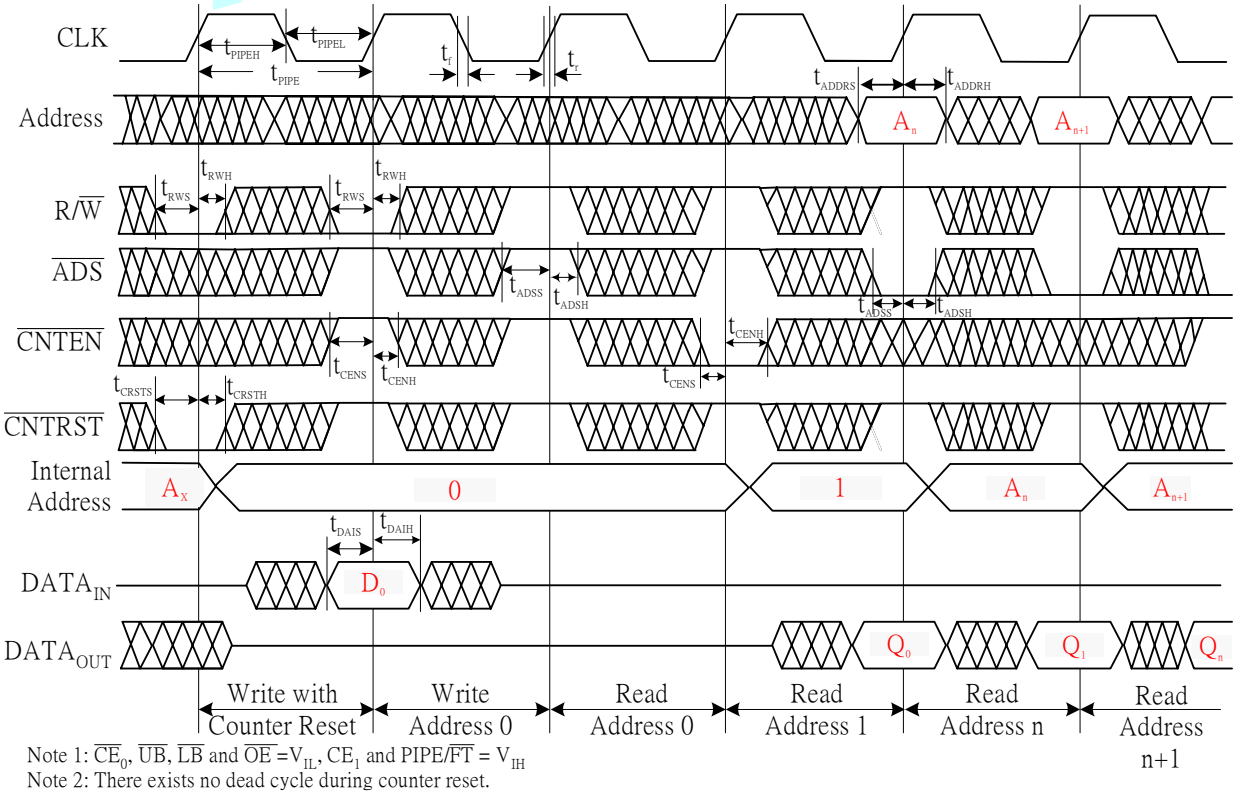
Note 1: $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, PIPE/$\overline{FT}$ and $\overline{OE}$=V_{IL}, CE_1, R/$\overline{W}$ and $\overline{CNTRST}$ = V_{IH}

Flow-Through Read with Internal Address Counter Enable



Note 1: $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ =V_{IL}, $\overline{OE}$, CE_1, and $\overline{CNTRST}$ = V_{IH}
Note 2: Pipelined mode is the same as Flow-Through mode.

Pipelined/Flow-Through Write with Internal Address Counter Enable

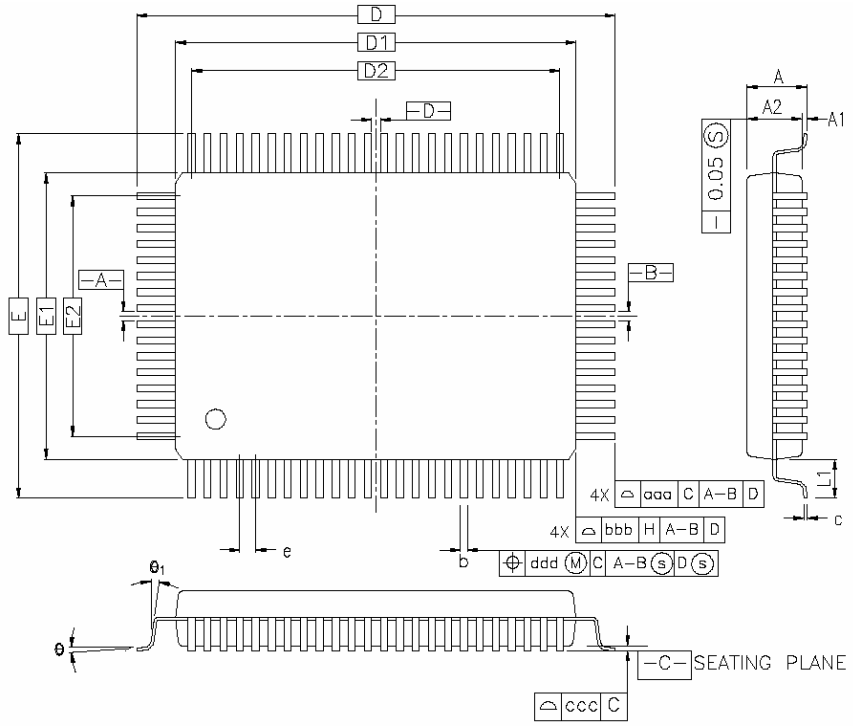


Note 1: $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$ and $\overline{OE}$ =V_{IL}, CE_1 and PIPE/$\overline{FT}$ = V_{IH}
Note 2: There exists no dead cycle during counter reset.

Counter Reset in Pipelined Mode

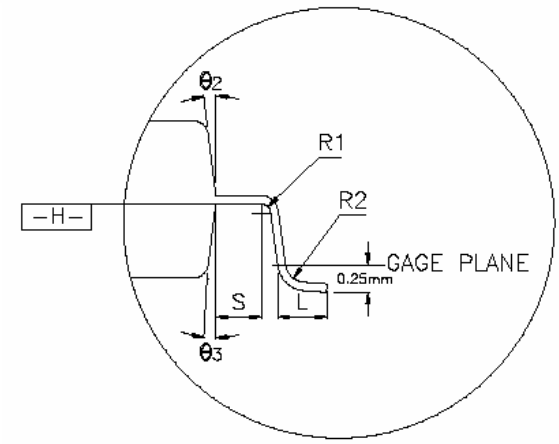
10 Mechanical Drawing

128 PIN 14mm*20mm*1.4mm TQFP:



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D1	20.00 BSC.			0.787 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

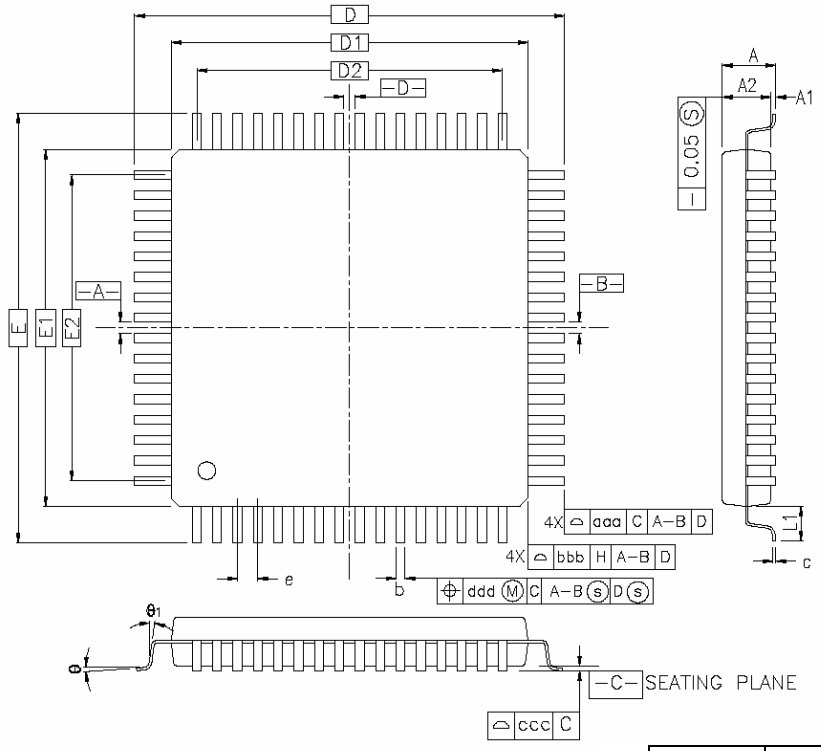


SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES:

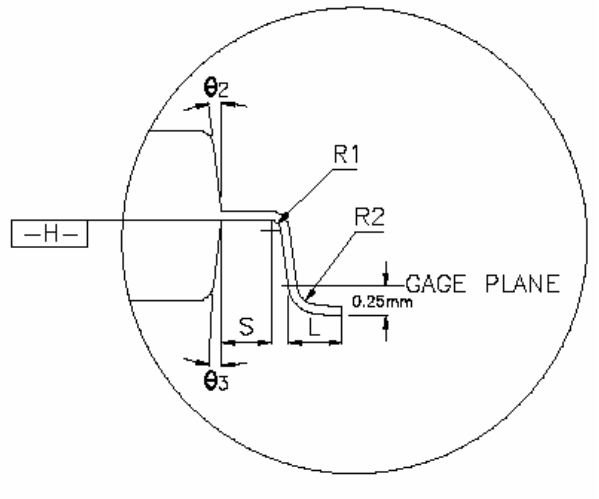
1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions that include mold mismatch.
2. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm (for 0.4mm and 0.5mm pitch packages).

100 PIN 14mm*14mm*1.4mm TQFP:



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES:

1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions that include mold mismatch.
2. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm (for 0.4mm and 0.5mm pitch packages).

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