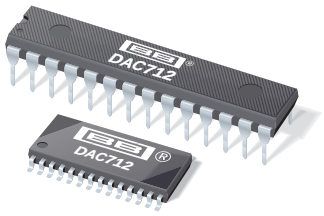
BURR-BROWN®



DAC712

16-BIT DIGITAL-TO-ANALOG CONVERTER With 16-Bit Bus Interface

FEATURES

- HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: ±10V
- 13-, 14-, AND 15-BIT LINEARITY GRADES
- 16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)
- POWER DISSIPATION: 600mW max
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- 28-LEAD DIP AND SOIC PACKAGES

DESCRIPTION

DAC712 is a complete 16-bit resolution D/A converter with 16 bits of monotonicity over temperature.

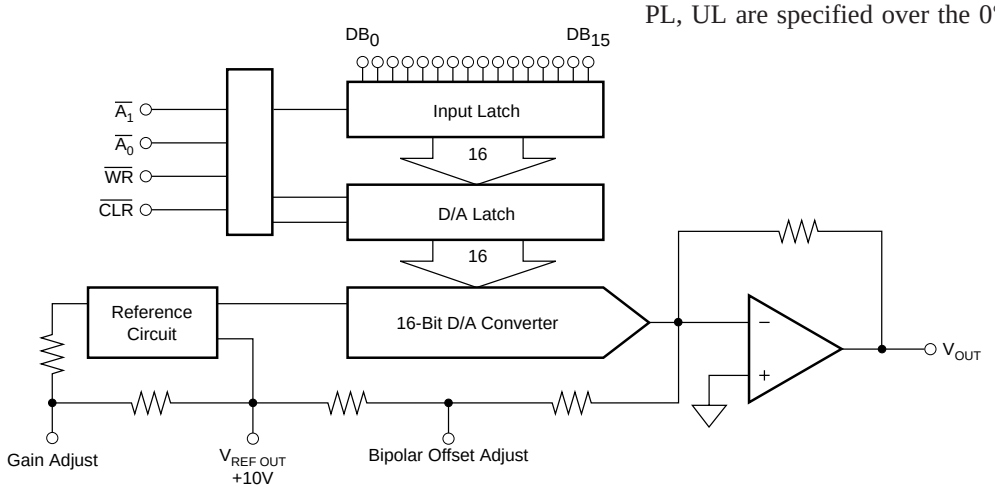
DAC712 has a precision +10V temperature compensated voltage reference, ±10V output amplifier and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a CLEAR function that resets the analog output to bipolar zero.

GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

DAC712 is available in two linearity error performance grades: ±4LSB and ±2LSB and three differential linearity grades: ±4LSB, ±2LSB, and ±1LSB. The DAC712 is specified at power supply voltages of ±12V and ±15V.

DAC712 is packaged in a 28-pin 0.3" wide plastic DIP and in a 28-lead wide-body plastic SOIC. The DAC712P, U, PB, UB, are specified over the –40°C to +85°C temperature range and the DAC712PK, UK, PL, UL are specified over the 0°C to +70°C range.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1164G
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SPECIFICATIONS

ELECTRICAL

At T_A = 25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = –12V and –15V, unless otherwise noted.

PARAMETER	DAC712P, U MIN	DAC712P, U TYP	DAC712P, U MAX	DAC712PB, UB MIN	DAC712PB, UB TYP	DAC712PB, UB MAX	UNITS
INPUT							
RESOLUTION		16			*		Bits
DIGITAL INPUTS							
Input Code		Binary Two's Complement			*		
Logic Levels[1]							
V_{IH}	+2.0		$+V_{CC}$ – 1.4	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Differential Linearity Error			±4			±2	LSB
T_{MIN} to T_{MAX}			±8			±4	LSB
Monotonicity Over Temp	13			14			Bits
Gain Error[3]			±0.1			±0.1	%
T_{MIN} to T_{MAX}			±0.2			±0.15	%
Bipolar Zero Error[3]			±0.1			*	% FSR[2]
			±20			*	mV
T_{MIN} to T_{MAX}			±0.2			±0.15	% FSR
			±40			±30	mV
Power Supply Sensitivity Of Full Scale:			±0.003			*	% FSR/% V_{CC}
			±30			*	ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE							
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)[4]							
20V Output Step		6			*	10	µs
1 LSB Output Step[5]		4			*		µs
Output Slew Rate		10			*		V/µs
Total Harmonic Distortion + Noise							
0dB, 1001Hz, f_S = 100kHz		0.005			*		%
–20dB, 1001Hz, f_S = 100kHz		0.03			*		%
–60dB, 1001Hz, f_S = 100kHz		3.0			*		%
SINAD							
1001Hz, f_S = 100kHz		87			*		dB
Digital Feedthrough[5]		2			*		nV-s
Digital-to-Analog Glitch Impulse[5]		15			*		nV-s
Output Noise Voltage (Includes Reference)		120			*		nV/$\sqrt{Hz}$
ANALOG OUTPUT							
Output Voltage Range							
$+V_{CC}$, $-V_{CC}$ = ±11.4V	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short Circuit to ACOM, Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+9.975	+10.000	+10.025	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	V
Output Resistance		1			*		Ω
Source Current	2			*			mA
Short Circuit to ACOM, Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	V
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	V
Current (No Load, ±15V Supplies)							
$+V_{CC}$		13	15		*	*	mA
$-V_{CC}$		22	25		*	*	mA
Power Dissipation[6]		525	600		*	*	mW
TEMPERATURE RANGES							
Specification							
All Grades	–40		+85	*		*	°C
Storage	–60		+150	*		*	°C
Thermal Coefficient θ_{JA}							
DIP Package		75			*		°C/W
SOIC Package		75			*		°C/W

* Specifications are the same as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = –12V and –15V, unless otherwise noted.

PARAMETER	DAC712PK, UK MIN	DAC712PK, UK TYP	DAC712PK, UK MAX	DAC712PL, UL MIN	DAC712PL, UL TYP	DAC712PL, UL MAX	UNITS
INPUT							
RESOLUTION		16			*		Bits
DIGITAL INPUTS							
Input Code		Binary Two's Complement			*		
Logic Levels[1]							
V_{IH}	+2.0		$+V_{CC}$ – 1.4	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±2			±2	LSB
T_{MIN} to T_{MAX}			±2			±2	LSB
Differential Linearity Error			±2			±1	LSB
T_{MIN} to T_{MAX}			±2			±1	LSB
Monotonicity Over Temp	15			16			Bits
Gain Error[3]			±0.1			*	%
T_{MIN} to T_{MAX}			±0.15			±0.02	%
Bipolar Zero Error[3]			±0.1			*	% FSR[2]
			±20			*	mV
T_{MIN} to T_{MAX}			±0.15			±0.15	% FSR
			±30			*	mV
Power Supply Sensitivity of Full Scale			±0.003			*	%FSR/% V_{CC}
			±30			*	ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE							
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)[4]							
20V Output Step		6	10		*	10	µs
1LSB Output Step[5]		4			*		µs
Output Slew Rate		10			*		V/µs
Total Harmonic Distortion + Noise							
0dB, 1001Hz, f_S = 100kHz		0.005			*		%
–20dB, 1001Hz, f_S = 100kHz		0.03			*		%
–60dB, 1001Hz, f_S = 100kHz		3.0			*		%
SINAD							
1001Hz, f_S = 100kHz		87			*		dB
Digital Feedthrough[5]		2			*		nV–s
Digital-to-Analog Glitch Impulse[5]		15			*		nV–s
Output Noise Voltage (includes reference)		120			*		nV/$\sqrt{Hz}$
ANALOG OUTPUT							
Output Voltage Range							
$+V_{CC}$, $-V_{CC}$ = ±11.4V	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short Circuit to ACOM, Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+9.975	+10.000	+10.025	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	V
Output Resistance		1			*		Ω
Source Current	2			*			mA
Short Circuit to ACOM, Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	V
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	V
Current (No Load, ±15V Supplies)							
$+V_{CC}$		13	15		*	*	mA
$-V_{CC}$		22	25		*	*	mA
Power Dissipation[6]		525	600			*	mW
TEMPERATURE RANGES							
Specification							
All Grades	0		+70	*		*	°C
Storage	–60		+150	*		*	°C
Thermal Coefficient, θ_{JA}							
DIP Package		75			*		°C/W
SOIC Package		75			*		°C/W

* Same specification as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V, +17V
$-V_{CC}$ to COMMON	0V, –17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	–1V to $+V_{CC}$ –0.7V
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

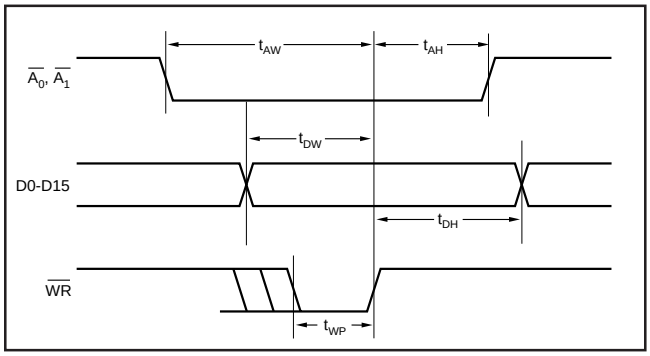
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC712P	Plastic DIP	246
DAC712U	Plastic SOIC	217
DAC712PB	Plastic DIP	246
DAC712UB	Plastic SOIC	217
DAC712PK	Plastic DIP	246
DAC712UK	Plastic SOIC	217
DAC712PL	Plastic DIP	246
DAC712UL	Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	TEMPERATURE RANGE	LINEARITY ERROR MAX at +25°C	DIFFERENTIAL LINEARITY ERROR MAX at +25°C
DAC712P	–40°C to +85°C	±4LSB	±4LSB
DAC712U	–40°C to +85°C	±4LSB	±4LSB
DAC712PB	–40°C to +85°C	±2LSB	±2LSB
DAC712UB	–40°C to +85°C	±2LSB	±2LSB
DAC712PK	0°C to +70°C	±2LSB	±2LSB
DAC712UK	0°C to +70°C	±2LSB	±2LSB
DAC712PL	0°C to +70°C	±2LSB	±1LSB
DAC712UL	0°C to +70°C	±2LSB	±1LSB

TIMING DIAGRAM



TIMING SPECIFICATIONS

T_A = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	50		ns
t_{AW}	$\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$	50		ns
t_{AH}	$\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$	10		ns
t_{DH}	Data Hold after end of $\overline{WR}$	10		ns
t_{WP}(1)	Write Pulse Width	50		ns
t_{CP}	CLEAR Pulse Width	200		ns

NOTES: (1) For single-buffered operation, t_{WP} is 80ns min. Refer to page 10.

TRUTH TABLE

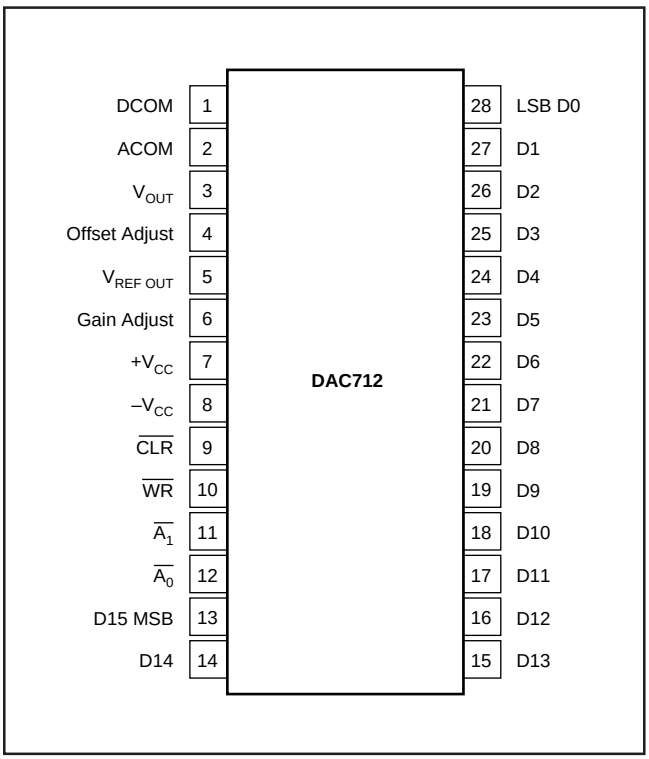
$\overline{A_0}$	$\overline{A_1}$	$\overline{WR}$	$\overline{CLR}$	DESCRIPTION
0	1	$1 \rightarrow 0 \rightarrow 1$	1	Load Input Latch
1	0	$1 \rightarrow 0 \rightarrow 1$	1	Load D/A Latch
1	1	$1 \rightarrow 0 \rightarrow 1$	1	No Change
0	0	0	1	Latches Transparent
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN CONFIGURATION



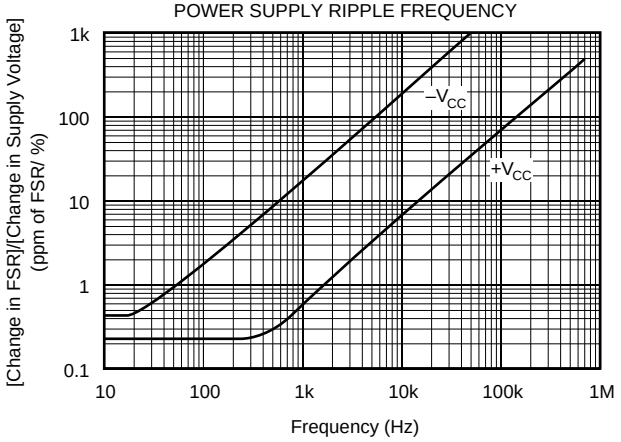
PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DCOM	Power Supply return for digital currents.
2	ACOM	Analog Supply Return.
3	V_{OUT}	±10V D/A Output.
4	Off Adj	Offset Adjust (Bipolar).
5	$V_{REF\ OUT}$	Voltage Reference Output.
6	Gain Adj	Gain Adjust.
7	$+V_{CC}$	+12V to +15V Supply.
8	$-V_{CC}$	–12V to –15V Supply.
9	$\overline{CLR}$	CLEAR. Sets D/A output to BIPOLAR ZERO (Active Low).
10	$\overline{WR}$	Write (Active Low).
11	$\overline{A_1}$	Enable for D/A latch (Active Low).
12	$\overline{A_0}$	Enable for Input latch (Active Low).
13	D15	Data Bit 15 (Most Significant Bit).
14	D14	Data Bit 14.
15	D13	Data Bit 13.
16	D12	Data Bit 12.
17	D11	Data Bit 11.
18	D10	Data Bit 10.
19	D9	Data Bit 9.
20	D8	Data Bit 8.
21	D7	Data Bit 7.
22	D6	Data Bit 6.
23	D5	Data Bit 5.
24	D4	Data Bit 4.
25	D3	Data Bit 3.
26	D2	Data Bit 2.
27	D1	Data Bit 1.
28	D0	Data Bit 0 (Least Significant Bit).

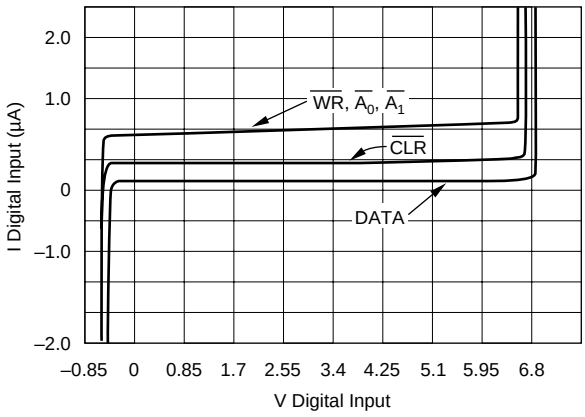
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

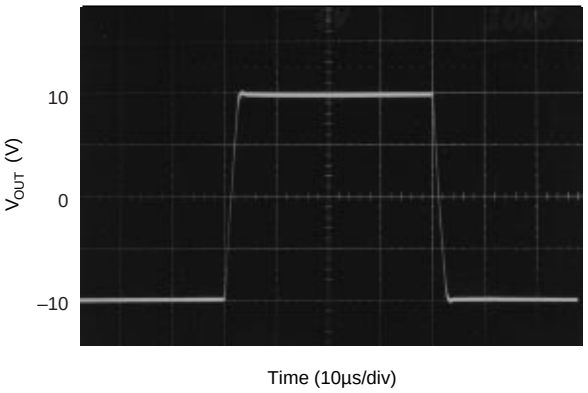
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



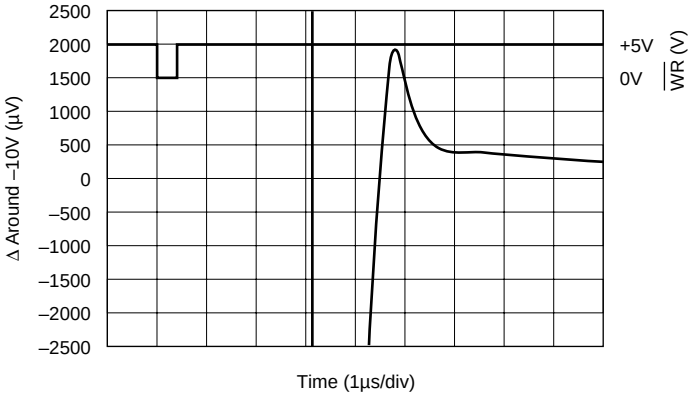
LOGIC vs V LEVEL



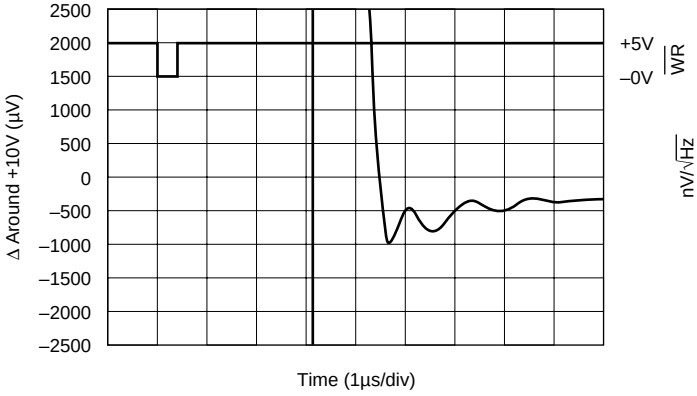
± FULL SCALE OUTPUT SWING



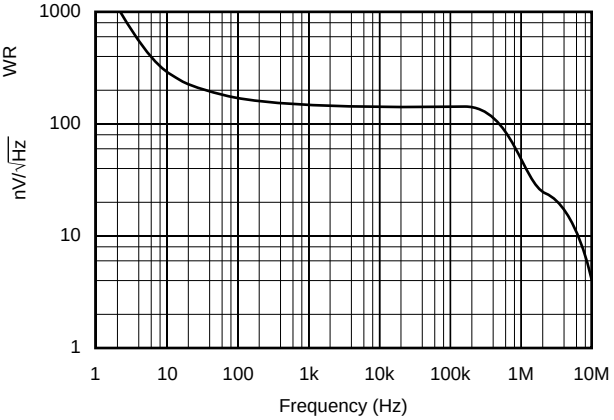
SETTLING TIME, +10V TO –10V



SETTLING TIME, –10V TO +10V



Spectral Noise Density



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC712 is guaranteed over the specification temperature range to 13, 14, 15, and 16 bits for performance grades DAC712P/U, DAC712PB/UB, DAC712PK/UK, and DAC712PL/UL respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry ($FFFF_{HEX}$ to 0000_{HEX}, and 0000_{HEX} to $FFFF_{HEX}$: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from $7FFF_{HEX}$ to 8000_{HEX}.

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

DAC712 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface.

INTERFACE LOGIC

DAC712 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic “0” will enter the latch. When the enable inputs return to logic “1”, the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a bipolar zero output.

LOGIC INPUT COMPATIBILITY

DAC712 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic “0” and control inputs will float to logic “0” if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

DAC712 is designed to accept positive-true binary two’s complement (BTC) input codes which are compatible with bipolar analog output operation. For bipolar analog output configuration, a digital input of $7FFF_{HEX}$ gives a plus full scale output, 8000_{HEX} gives a minus full scale output, and 0000_{HEX} gives bipolar zero output.

INTERNAL REFERENCE

DAC712 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.

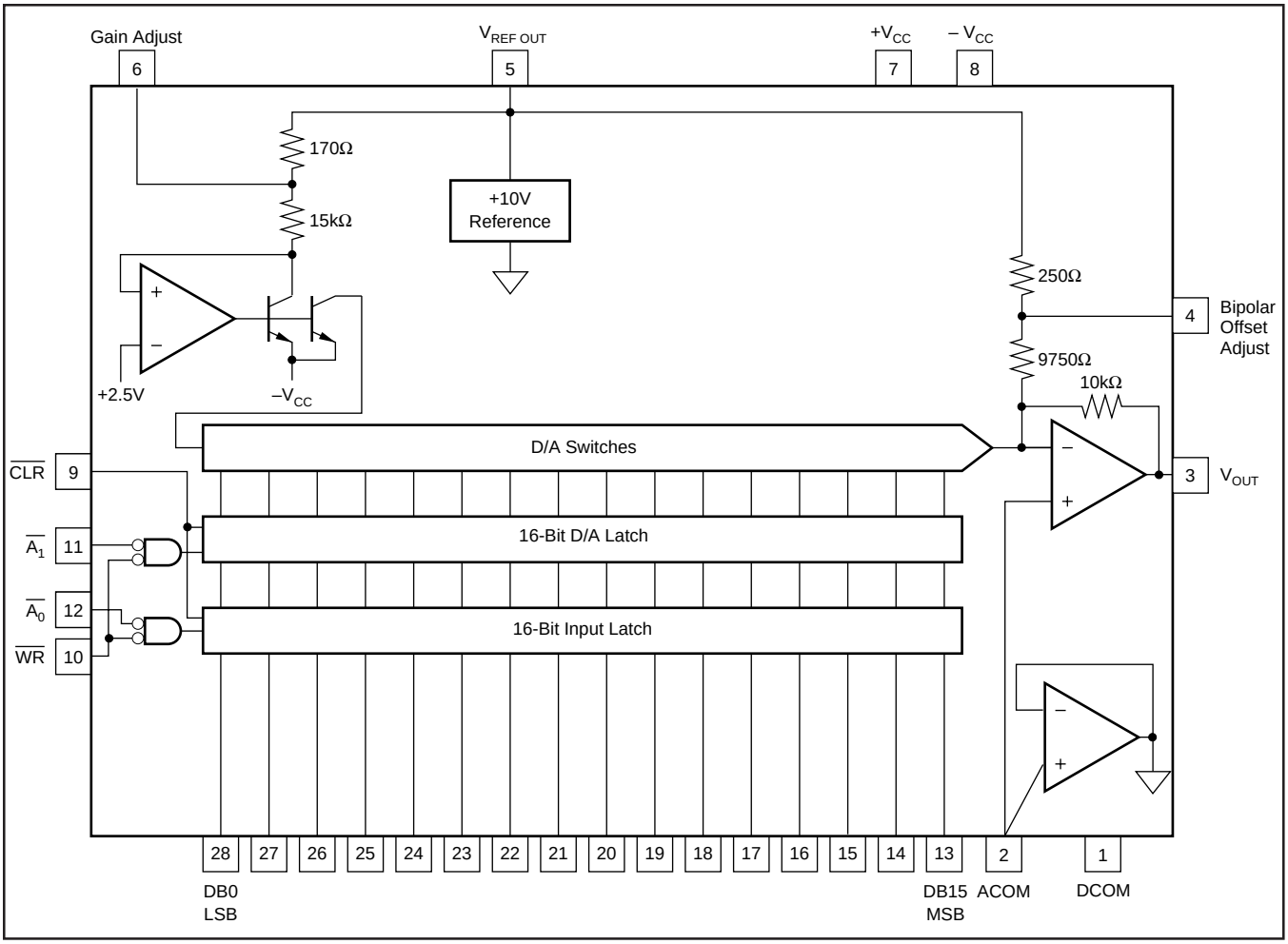


FIGURE 1. DAC712 Block Diagram.

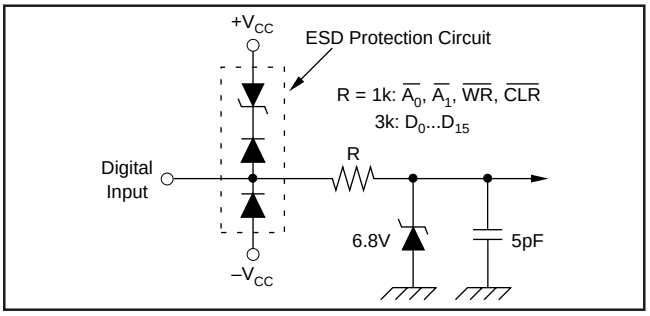


FIGURE 2. Equivalent Circuit of Digital Inputs.

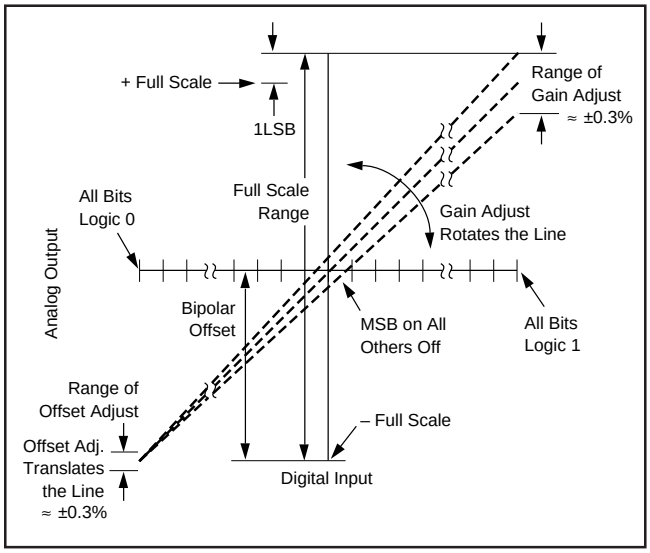


FIGURE 3. Relationship of Offset and Gain Adjustments.

OUTPUT VOLTAGE SWING

The output amplifier of DAC712 is committed to a ±10V output range. DAC712 will provide a ±10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

Offset Adjustment

Apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for –10V.

DAC712 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 305µV		
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG OUTPUT (V)	DESCRIPTION
$7FFF_H$	+9.999695	+ Full Scale –1LSB
|		
4000_H	+5.000000	3/4 Scale
|		
0001_H	+0.000305	BPZ + 1LSB
0000_H	0.000000	Bipolar Zero (BPZ)
$FFFF_H$	–0.000305	BPZ – 1LSB
|		
$C000_H$	–5.000000	1/4 Scale
|		
8000_H	–10.00000	Minus Full Scale

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milli-inch wide printed circuit conductor 60 milli-inches long will result in a voltage drop of 150µV.

The analog output of DAC712 has an LSB size of 305µV (–96dB). The noise floor of the D/A must remain below this level in the frequency range of interest. The DAC712's noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

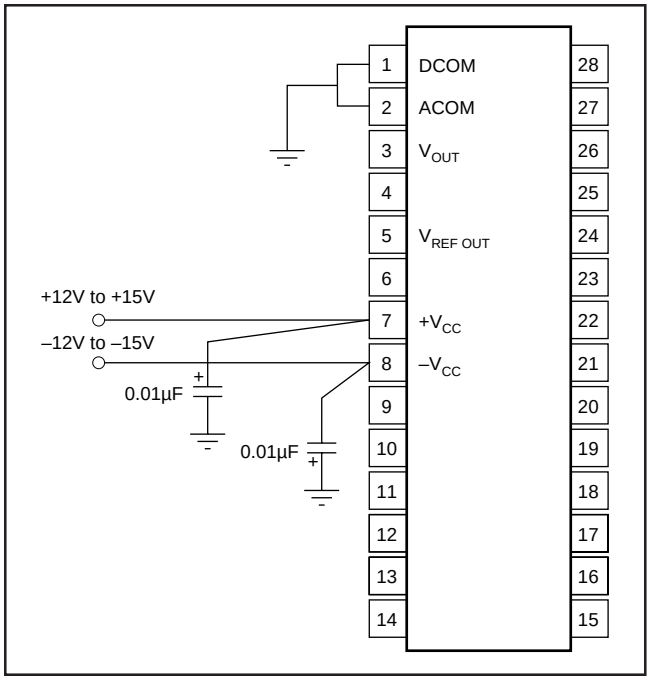


FIGURE 4. Power Supply Connections.

DAC712 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC712s are used or if DAC712 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because

there is no change in DAC712 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC712 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, +5V.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC712 output amplifier is connected internally for the ±10V bipolar (20V) output range. That is, the bipolar offset resistor is connected to an internal reference voltage and the 20V range resistor is connected internally to V_{OUT}. DAC712 cannot be connected by the user for unipolar operation.

DIGITAL INTERFACE

BUS INTERFACE

DAC712 has 16-bit double-buffered data bus interface with control lines for easy interface to interface to a 16-bit bus. The double-buffered feature permits update of several D/As simultaneously.

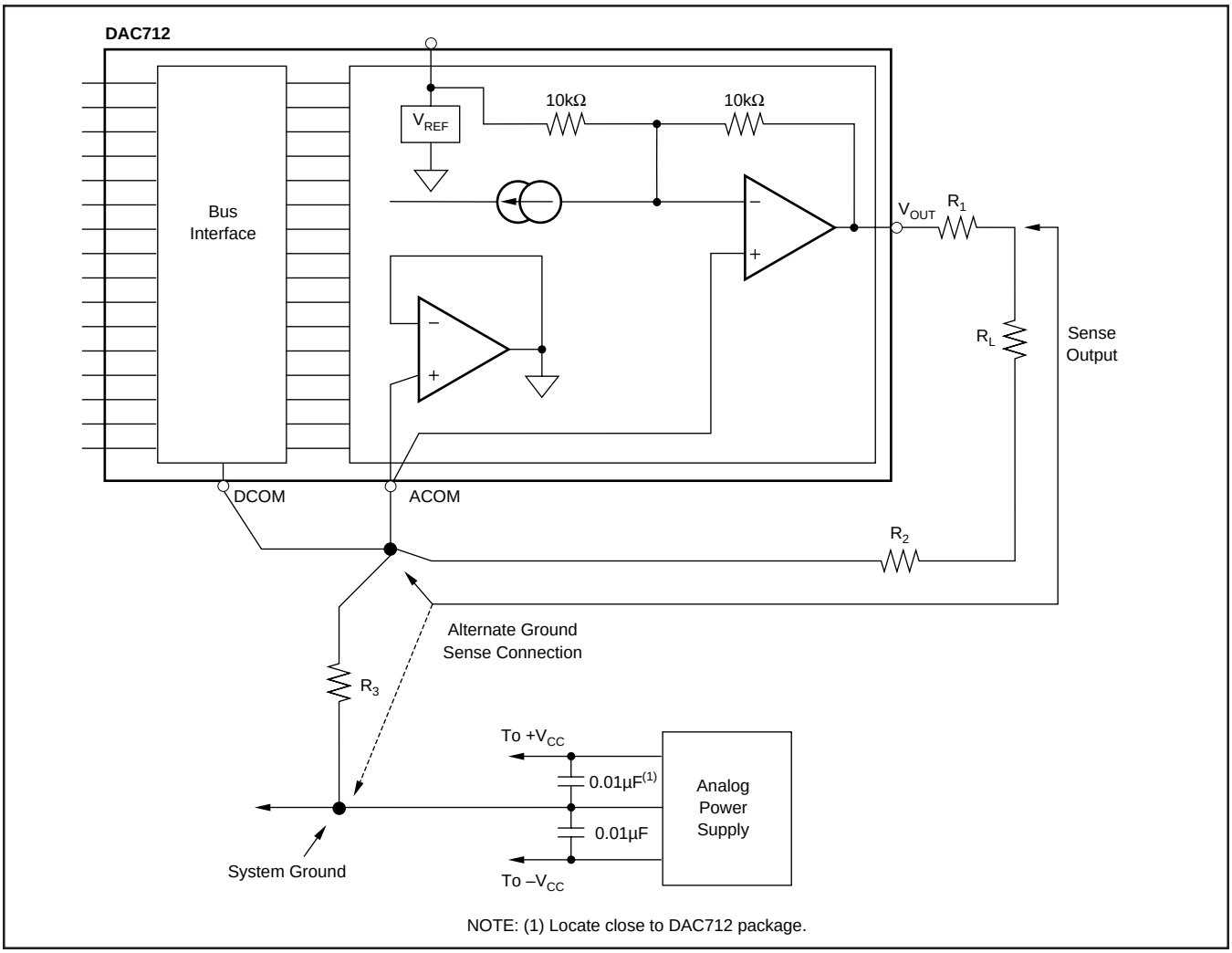


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

$\overline{A_0}$ is the enable control for the DATA INPUT LATCH. $\overline{A_1}$ is the enable for the D/A LATCH. $\overline{WR}$ is used to strobe data into latches enabled by $\overline{A_0}$, and $\overline{A_1}$. Refer to the block diagram of Figure 1 and to Timing Diagram on page 3.

$\overline{CLR}$ sets the INPUT DATA LATCH to all zero and the D/A LATCH to a code that gives bipolar 0V at the D/A output.

SINGLE-BUFFERED OPERATION

To operate the DAC712 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting $\overline{A_0}$ to DCOM. If $\overline{A_1}$ is not used to enable the D/A, it should be connected to DCOM also. For this mode of operation, the width of $\overline{WR}$ will need to be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

TRANSPARENT INTERFACE

The digital interface of the DAC712 can be made transparent by asserting $\overline{A_0}$, $\overline{A_1}$, and $\overline{WR}$ LOW, and asserting $\overline{CLR}$ HIGH.

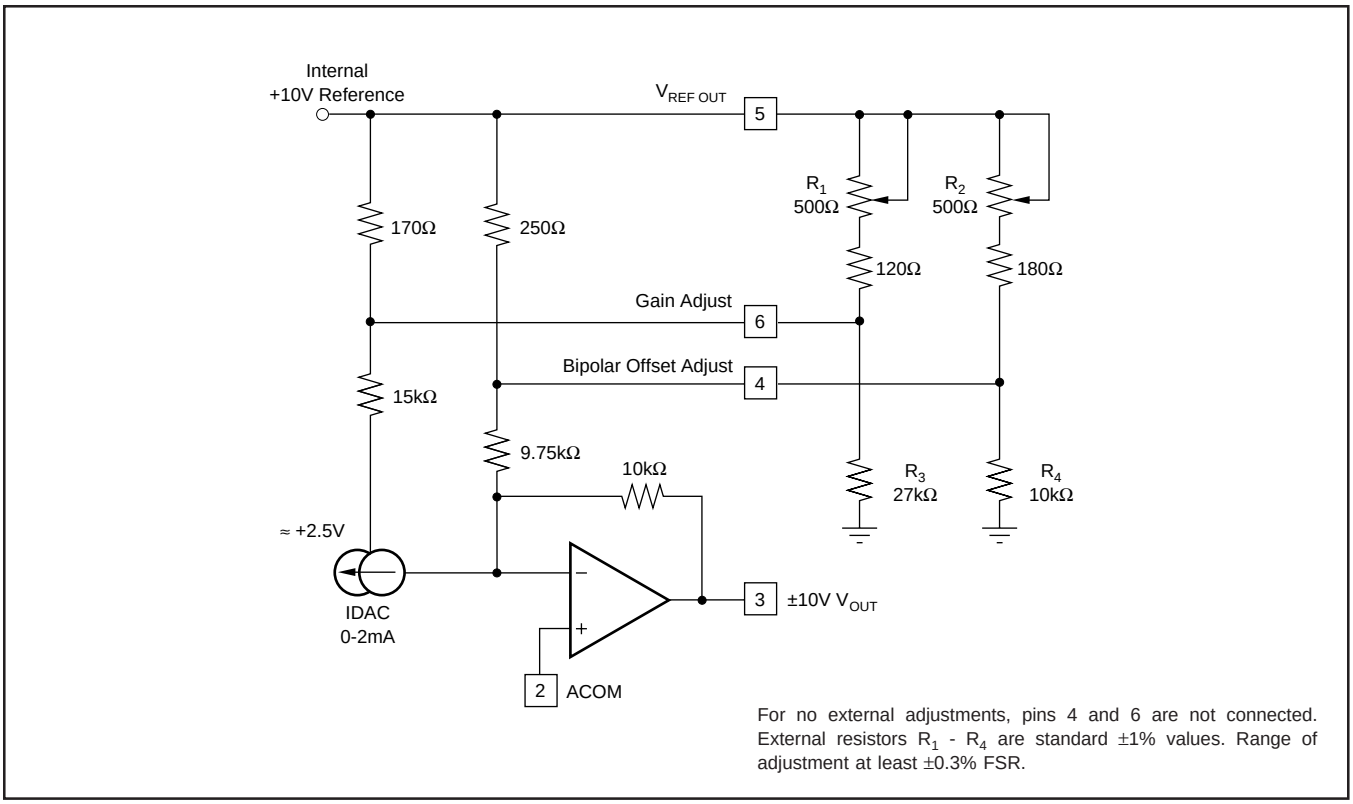
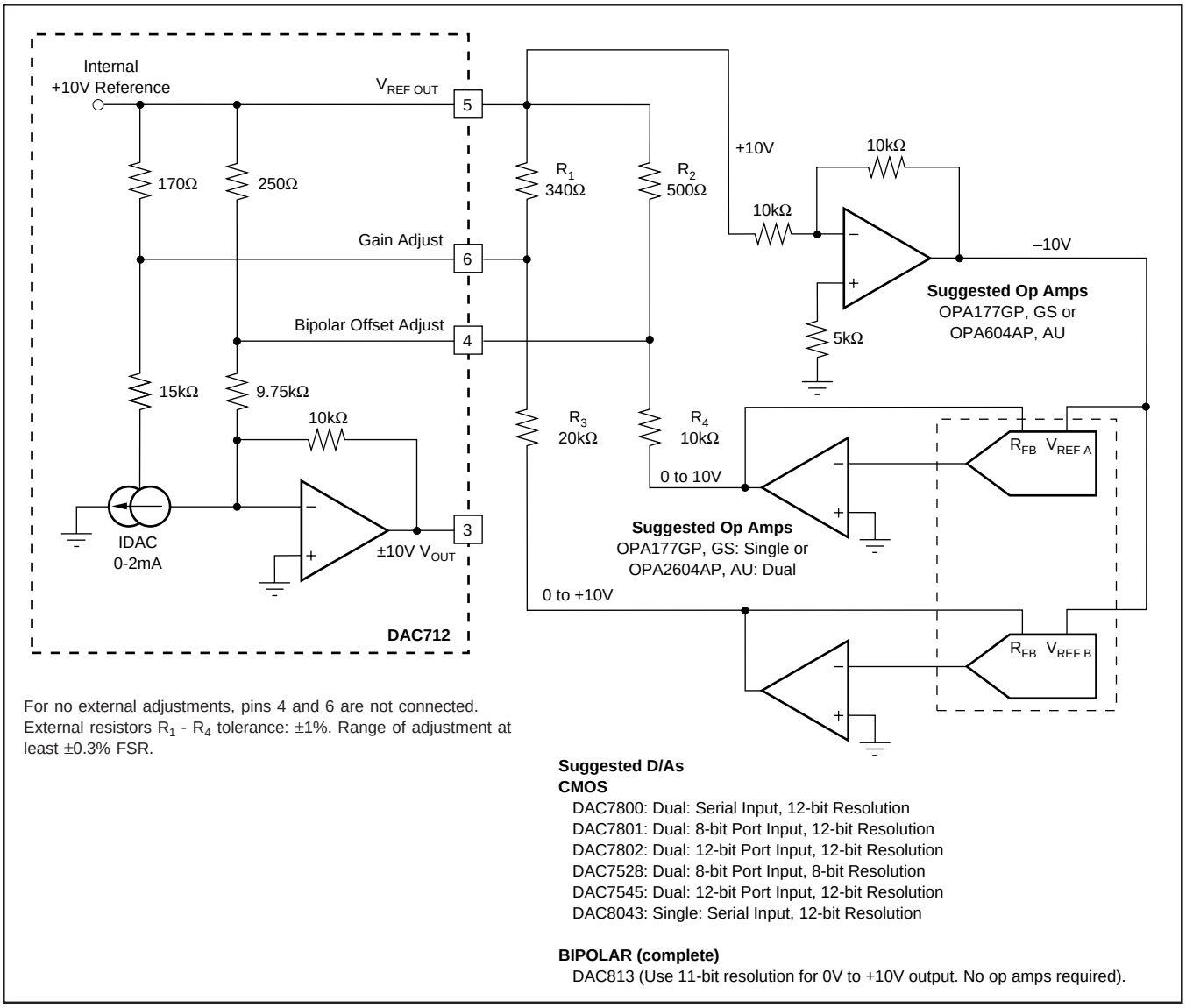


FIGURE 6. Manual Offset and Gain Adjust Circuits.



For no external adjustments, pins 4 and 6 are not connected. External resistors R_1 - R_4 tolerance: ±1%. Range of adjustment at least ±0.3% FSR.

Suggested D/As

CMOS

DAC7800: Dual: Serial Input, 12-bit Resolution
DAC7801: Dual: 8-bit Port Input, 12-bit Resolution
DAC7802: Dual: 12-bit Port Input, 12-bit Resolution
DAC7528: Dual: 8-bit Port Input, 8-bit Resolution
DAC7545: Dual: 12-bit Port Input, 12-bit Resolution
DAC8043: Single: Serial Input, 12-bit Resolution

BIPOLAR (complete)

DAC813 (Use 11-bit resolution for 0V to +10V output. No op amps required).

FIGURE 7. Gain and Offset Adjustment Using D/A Converters.