SRAM 256K x 16 Bit

SUPER LOW POWER/VOLTAGE CMOS SRAM

Features

- Operating voltage: 2.7V to 3.6V
- Access times: 55 / 70 ns (max.)
- Wide operating temperature range :
  - Industrial grade : -40°C to + 85°C
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 1.5V (min.)
- Available in 48-ball 6x8mm Mini-BGA packages

Ordering Information

- 44-pin 400mil TSOP (Type II)
- 48-ball 6x8mm Mini-BGA

Product No.	Operating Voltage	Operating Temperature	Operating Current Icc1 (max.)	Standby Current Isb1 (max.)	Packing Type
M23L416256A – 55 SB[*1] M23L416256A – 70 SB[*1]	+2.7V ~ +3.6V	-40°C ~ +85°C	45 mA	10 uA	6 x 8 mm Mini-BGA
M23L416256A – 55 LB[*1] M23L416256A – 70 LB[*1]				40 uA	

Notes *1 : S means Super Low Power , L means Low Power.

General Description

The M23L416256A is a low operating current 4,194,304-bit static random access memory organized as 262,144 words by 16 bits and operates on low power voltage from 2.7V to 3.6V. It is built using high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

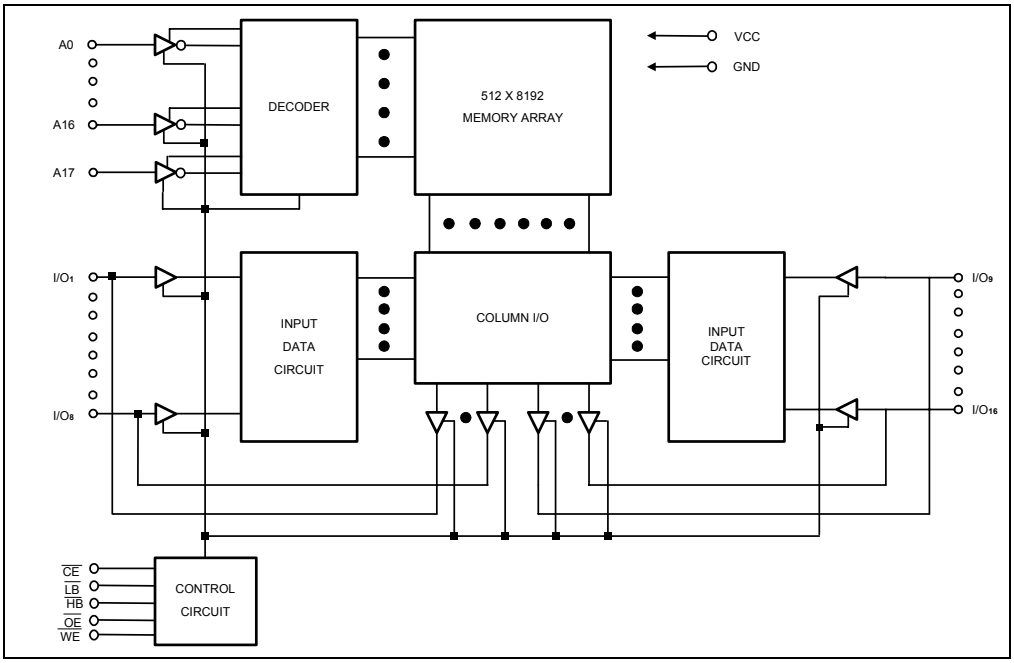
The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 1.5V.

Pin Configurations

Mini-BGA 48-ball Top View

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O_9	$\overline{HB}$	A3	A4	$\overline{CE}$	I/O_1
C	I/O_{10}	I/O_{11}	A5	A6	I/O_2	I/O_3
D	GND	I/O_{12}	A17	A7	I/O_4	VCC
E	VCC	I/O_{13}	NC	A16	I/O_5	GND
F	I/O_{15}	I/O_{14}	A14	A15	I/O_6	I/O_7
G	I/O_{16}	NC	A12	A13	$\overline{WE}$	I/O_8
H	NC	A8	A9	A10	A11	NC

Block Diagram



Pin Description

Symbol	Description	Symbol	Description
A0 - A17	Address Inputs	$\overline{HB}$	Higher Byte Enable Input (I/O_9 - I/O_{16})
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
I/O_1 - I/O_{16}	Data Input / Output	VCC	Power Supply
$\overline{WE}$	Write Enable Input	GND	Ground
$\overline{LB}$	Low Byte Enable Input (I/O_1 – I/O_8)	NC	No Connection

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_1 to I/O_8 Mode	I/O_9 to I/O_{16} Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I_{SB1}, I_{SB}
X	X	X	H	H	High – Z	High – Z	I_{SB1}, I_{SB}
L	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Read	High – Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	High – Z	Read	I_{CC1}, I_{CC2}, I_{CC}
L	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Write	High – Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	High – Z	Write	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	X	X	High – Z	High – Z	I_{CC1}, I_{CC2}, I_{CC}

Note: X = H or L

Recommended DC Operating Conditions (T_A = -40°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Min.	Max.	Unit
C_{IN}*	Input Capacitance	V_{IN} = 0V		6	pF
$C_{I/O}$*	Input / Output Capacitance	$V_{I/O}$ = 0V		8	pF

* These parameters are sampled and not 100% tested.

Absolute Maximum Ratings*

VCC to GND ..... -0.5V to +4.6V
IN, IN/OUT Volt to GND ..... -0.5V to VCC + 0.5V
Operating Temperature, Topr ..... -40°C to +85°C
Storage Temperature, Tstg ..... -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time ..... 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = -40°C to + 85°C, VCC = 2.7 V to 3.6V)

Symbol	Parameter	Conditions		M23L416256A-55/70			Unit
				Min.	Typ.	Max.	
I_{LI}	Input Leakage Current	V_{IN} = GND to VCC		-	-	1	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IH} $V_{I/O}$ = GND to VCC		-	-	1	μA
I_{CC1}	Operating Current	Min. Cycle, Duty = 100%, V_{IN} = V_{IL} or V_{IN} = V_{IH} $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA, V_{DD} = 3.3V		-	-	45	mA
I_{CC2}		$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0 mA V_{IN} ≥ Vcc-0.2 or V_{IN} ≤ 0.2V, f = 1MHz, Duty = 100%,		-	-	5	mA
I_{SB}	TTL Standby Current	$\overline{CE}$ = V_{IH}		-	-	1.0	mA
I_{SB1}	CMOS Standby Current	$\overline{CE}$ ≥ VCC - 0.2V, V_{IN} ≥ 0V	L*1	-	-	40	μA
			S*1			10	μA
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA		2.4		-	V

Notes *1 : L means Low power , S means Super Low Power.

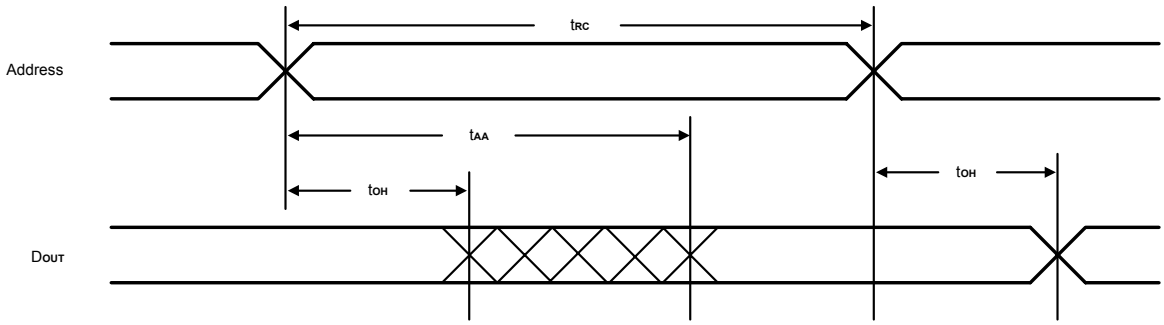
AC Characteristics (T_A = -40°C to +85°C, VCC = 2.7V to 3.6V)

Symbol	Parameter	M23L416256A-55		M23L416256A-70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
T_{RC}	Read Cycle Time	55	-	70	-	ns
T_{AA}	Address Access Time	-	55	-	70	ns
T_{ACE}	Chip Enable Access Time	-	55	-	70	ns
T_{BE}	Byte Enable Access Time	-	55	-	70	ns
T_{OE}	Output Enable to Output Valid	-	25	-	35	ns
T_{CLZ}	Chip Enable to Output in Low Z	10	-	10	-	ns
T_{BLZ}	Byte Enable to Output in Low Z	10	-	10	-	ns
T_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
T_{CHZ}	Chip Disable to Output in High Z	-	20	-	25	ns
T_{BHZ}	Byte Disable to Output in High Z	-	20	-	25	ns
T_{OHZ}	Output Disable to Output in High Z	-	20	-	25	ns
T_{OH}	Output Hold from Address Change	10	-	10	-	ns
WRITE CYCLE						
T_{WC}	Write Cycle Time	55	-	70	-	ns
T_{CW}	Chip Enable to End of Write	45	-	60	-	ns
T_{BW}	Byte Enable to End of Write	45	-	60	-	ns
T_{AS}	Address Setup Time	0	-	0	-	ns
T_{AW}	Address Valid to End of Write	50	-	60	-	ns
T_{WP}	Write Pulse Width	40	-	50	-	ns
T_{WR}	Write Recovery Time	0	-	0	-	ns
T_{WHZ}	Write to Output in High Z	-	20	-	20	ns
T_{DW}	Data to Write Time Overlap	25	-	30	-	ns
T_{DH}	Data Hold from Write Time	0	-	0	-	ns
T_{OW}	Output Active from End of Write	5	-	5	-	ns

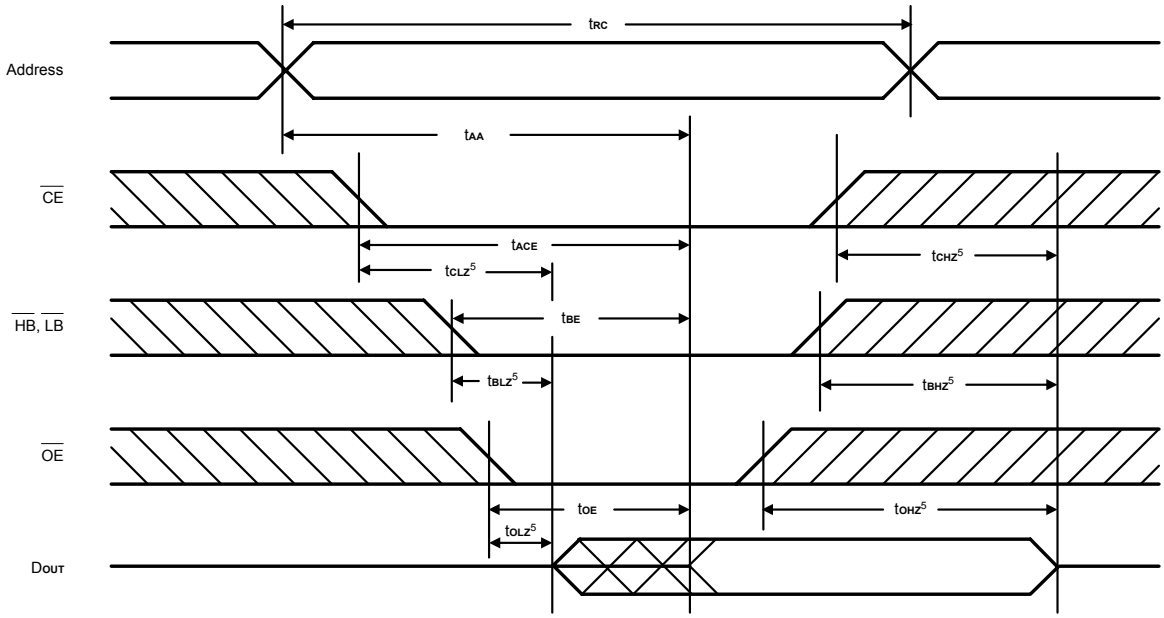
Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit Condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1[1, 2, 4]



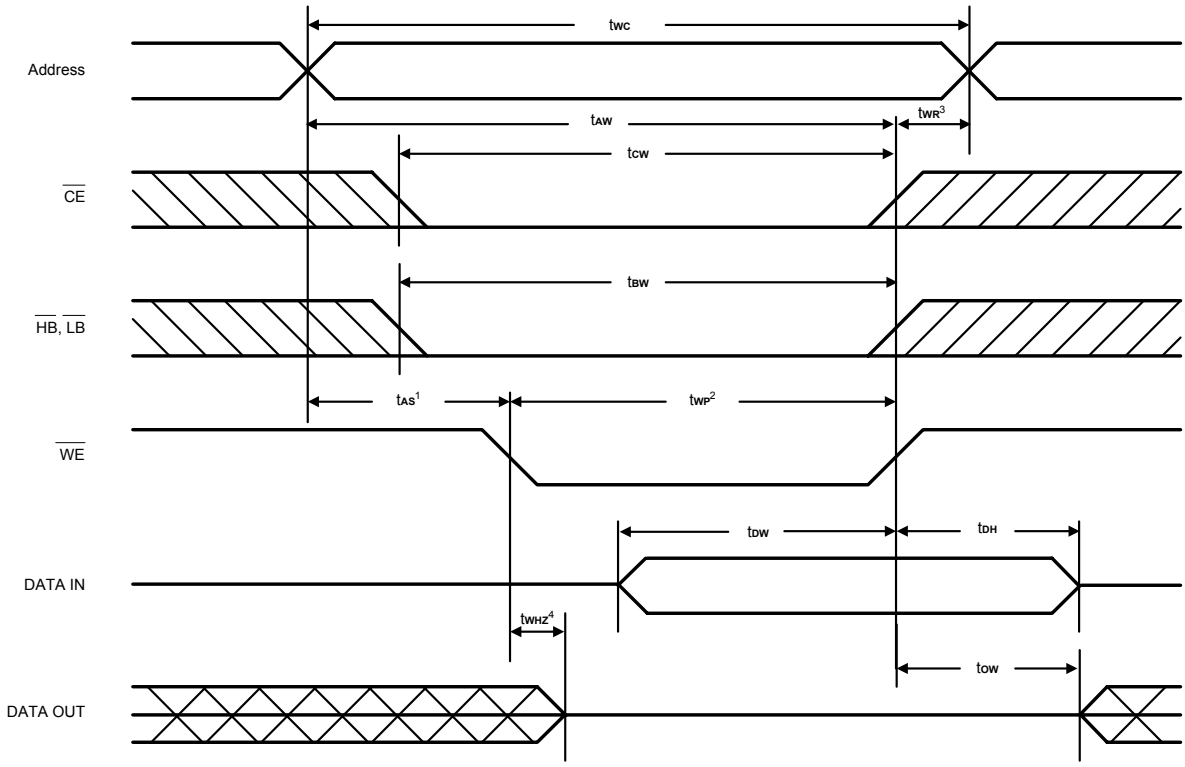
Read Cycle 2[1, 2, 3]



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE}$ = V_{IL}, $\overline{HB}$ = V_{IL} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

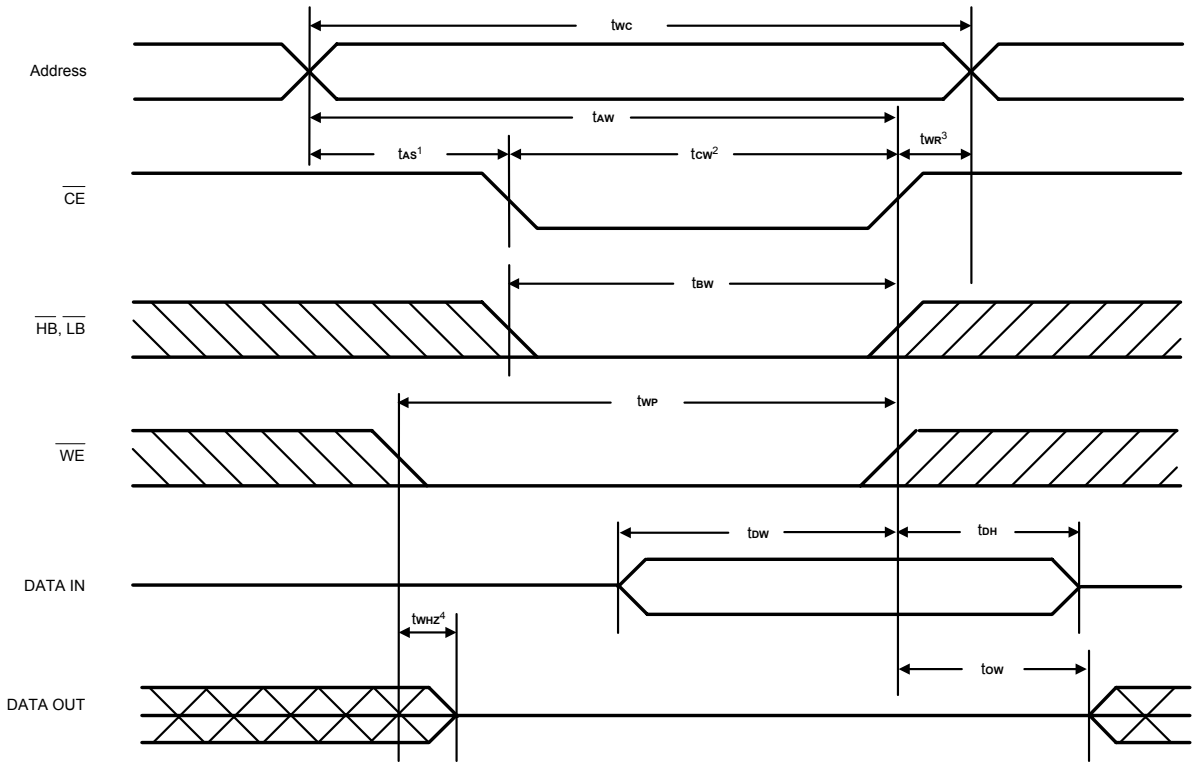
Timing Waveforms (continued)

Write Cycle 1
(Write Enable Controlled)



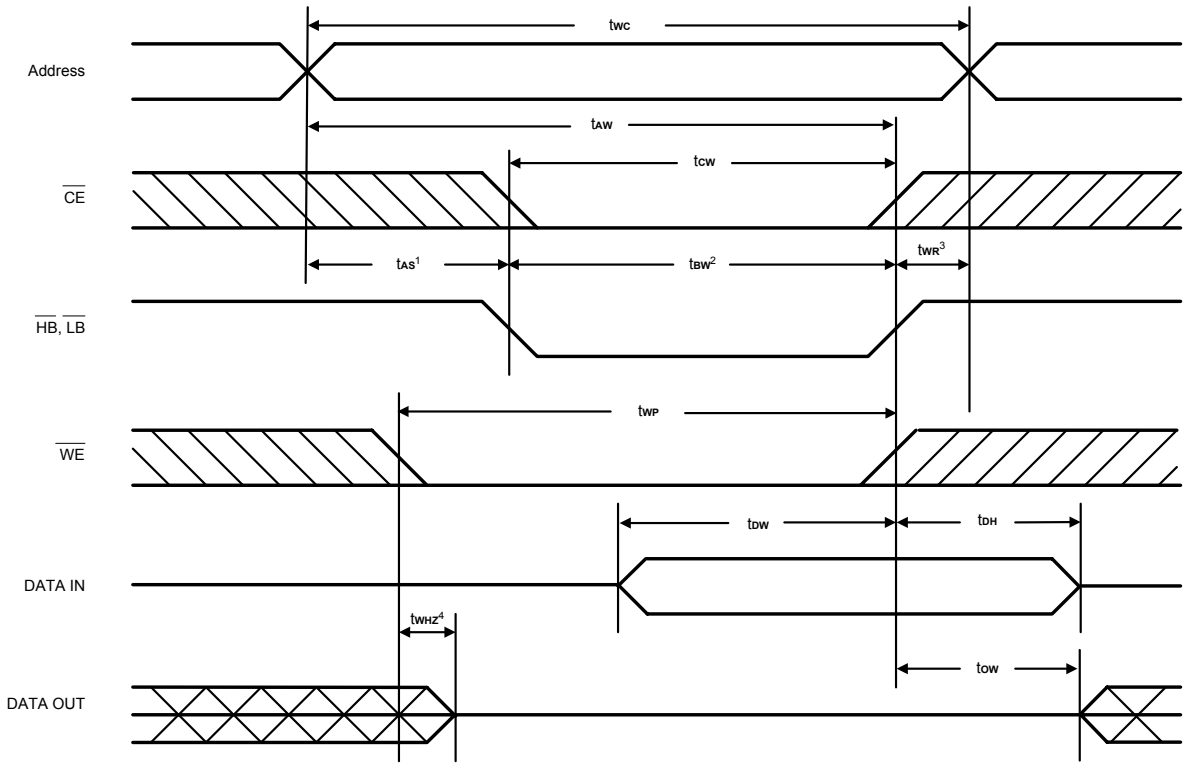
Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CE}$, $\overline{WE}$ and ($\overline{HB}$ and , or $\overline{LB}$).
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ or ($\overline{HB}$ and , or $\overline{LB}$) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions (T_A = -40°C to 85°C)

Input Pulse Levels	0.4V to 2.2V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

NOTES : FIGURE 1A \ 1B shown the maximum \ minimum testing loading.

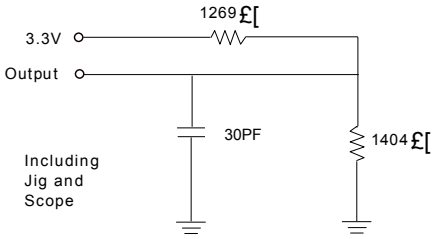


FIGURE 1A

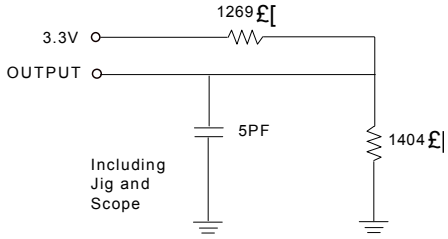
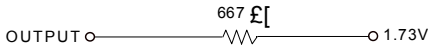


FIGURE 1B

Thevenin equivalent



All input pulses

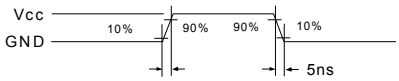
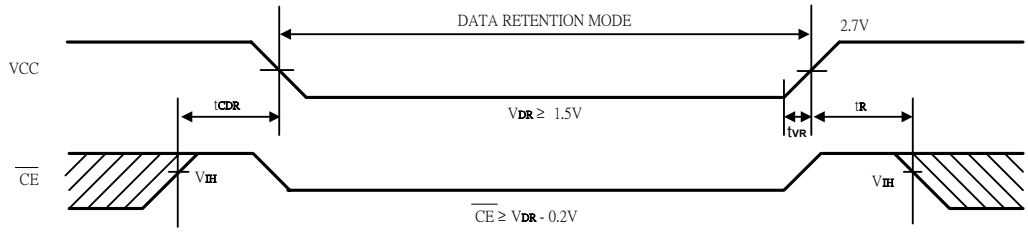


FIGURE 2

Data Retention Characteristics (T_A = -40°C to + 85°C)

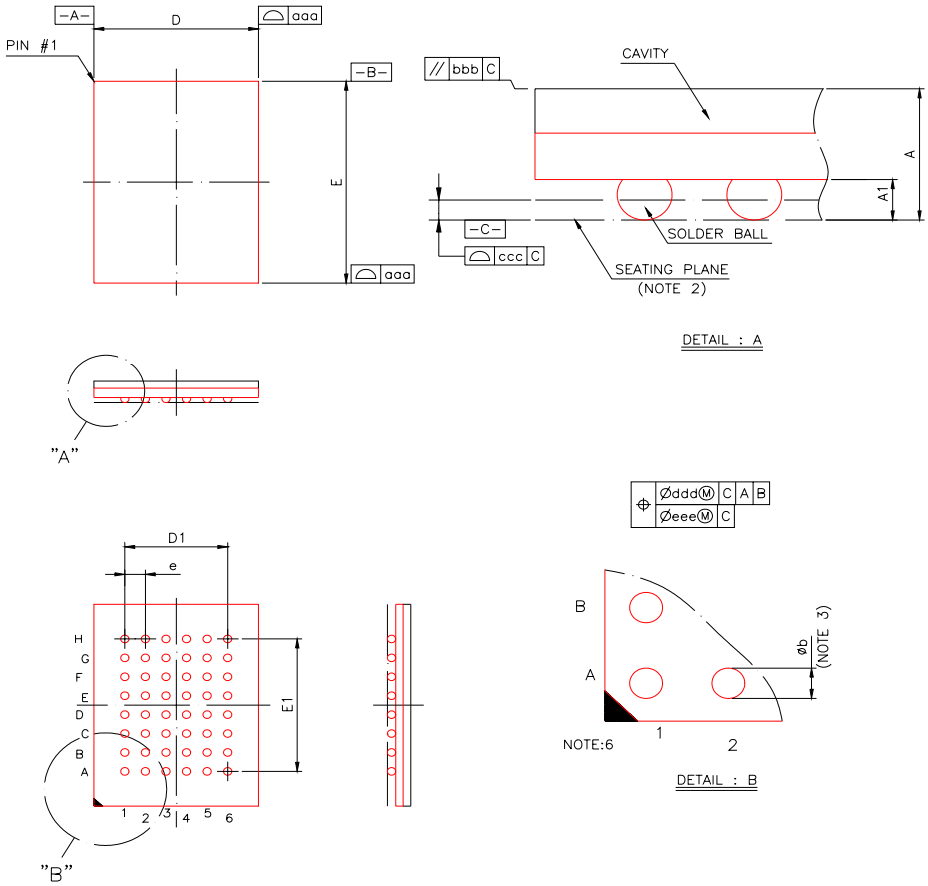
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DR}	VCC for Data Retention	$\overline{CE} \geq$ VCC - 0.2V	1.5	3	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq$ VCC - 0.2V or $\overline{LB} = \overline{HB} \geq$ VCC - 0.2V	-	10	µA
T_{CDR}	Chip Disable to Data Retention Time	See Retention Waveform	0	-	ns
t_R	Operation Recovery Time		T_{RC}	-	ns

Low VCC Data Retention Waveform



PACKING DIMENSIONS

48/48-BALL Mini-BGA (6x8mm) Outline Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	1.14	----------	1.40	0.049	----------	0.055
A_1	0.20	0.25	0.30	0.008	0.010	0.012
Φb	0.30	0.35	0.40	0.012	0.014	0.016
D	5.90	6.00	6.10	0.232	0.236	0.240
D_1	----------	3.75	----------	----------	0.148	----------
E	7.90	8.00	8.10	0.311	0.315	0.319
E_1	----------	5.25	----------	----------	0.207	----------
e	----------	0.75	----------	----------	0.030	----------
aaa	0.10			0.004		
bbb	0.08			0.003		
ccc	0.10			0.004		
ddd	0.20			0.008		
eee	0.10			0.004		

NOTE :

1. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. REFERENCE DOCUMENT : JEDEC MO-207.