SRAM 512K x 16 Bit

PSEUDO SRAM

Features

- 1T SRAM Memory Cell
- Operating voltage: 2.7V to 3.3V
- Access times: 70 / 85 ns (max.)
- 512Kx16 bit Organization
- Wide operating temperature range :
  - Standard grade : -25°C to + 85°C
  - Industrial grade : -40°C to + 85°C
- Data mask function by /LB, /HB
- Common I/O using three-state output
- Available in 48-ball 6x8mm Mini-BGA packages
- All inputs and outputs are directly TTL-compatible

Ordering Information

- 48-ball 6x8mm Mini-BGA

Product No.	Operating Voltage	Operating Temperature	Operating Current Icc1 (max.)	Standby Current Isb1 (max.)	Packing Type
M24L816512A – 70B M24L816512A – 85B	+2.7V ~ +3.3V	-25°C ~ +85°C	25 mA	100 uA	6 x 8 mm Mini-BGA
M24L816512A – 70BI M24L816512A – 85BI		-40°C ~ +85°C			

General Description

The M24L816512A is a low operating current 8,388,608 bit static random access memory organized as 524,288 words by 16 bits and operates on low power voltage from 2.7V to 3.3V. It is built using high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.

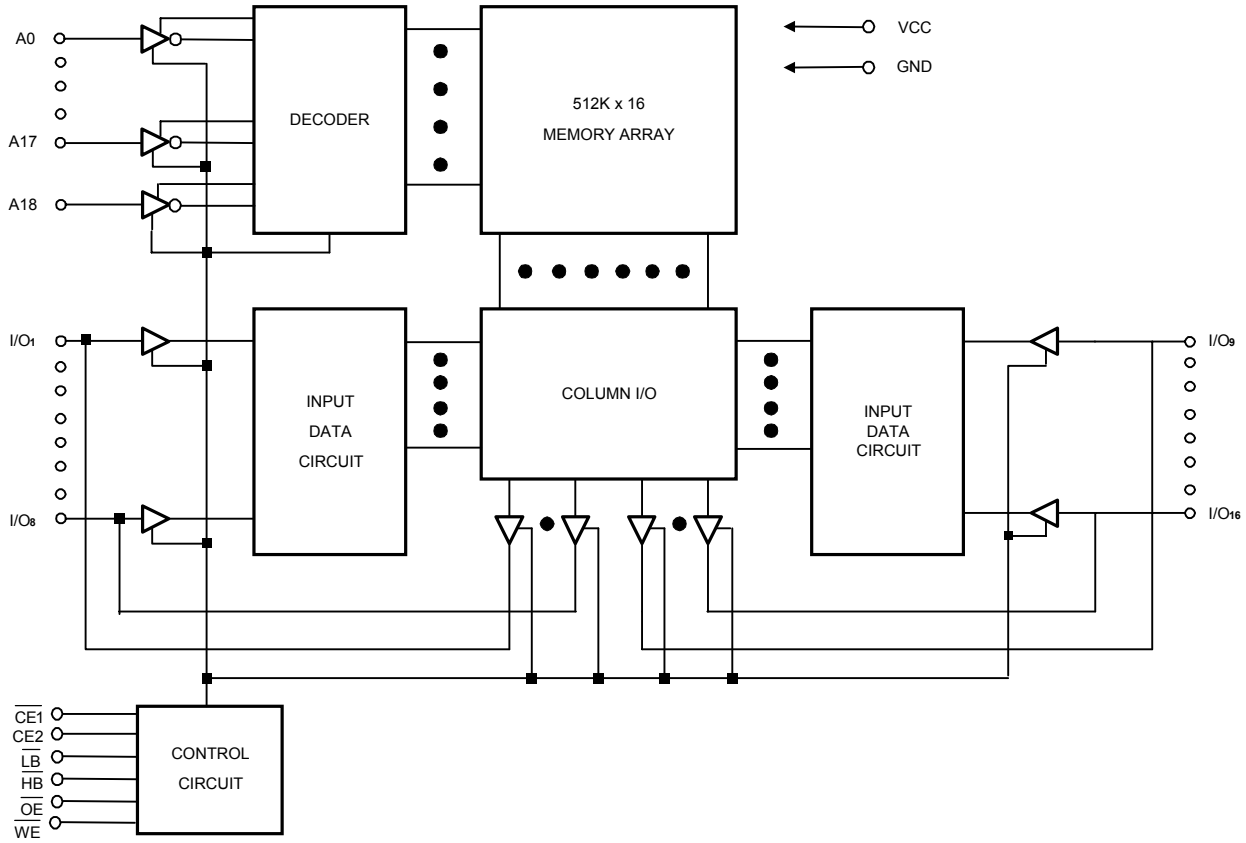
Pin Configurations

Mini-BGA 48-ball Top View

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O_9	$\overline{HB}$	A3	A4	$\overline{CE1}$	I/O_1
C	I/O_{10}	I/O_{11}	A5	A6	I/O_2	I/O_3
D	GND	I/O_{12}	A17	A7	I/O_4	VCC
E	VCC	I/O_{13}	DNU	A16	I/O_5	GND
F	I/O_{15}	I/O_{14}	A14	A15	I/O_6	I/O_7
G	I/O_{16}	DNU	A12	A13	$\overline{WE}$	I/O_8
H	A18	A8	A9	A10	A11	DNU

Note : DNU pins are to be connected to Vss or left open.

Block Diagram



Pin Description

Symbol	Description	Symbol	Description
A0 - A18	Address Inputs	$\overline{HB}$	Higher Byte Enable Input (I/O_9 - I/O_{16})
$\overline{CE1}$	Chip Enable	$\overline{OE}$	Output Enable
CE2	Deep Power Down	V_{CC}	Power Supply
I/O_1 - I/O_{16}	Data Input / Output	GND	Ground
$\overline{WE}$	Write Enable Input	DNU	Do Not Use
$\overline{LB}$	Low Byte Enable Input (I/O_1 – I/O_8)	-	-

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O1 to I/O8	I/O9 to I/O16	Mode	Power
H	H	X	X	X	X	High – Z	High – Z	Deselect	Standby
X	L	X	X	X	X	High – Z	High – Z	Deselect	Deep Power Down
L	H	X	X	H	H	High – Z	High – Z	Deselect	Standby
L	H	H	H	L	X	High – Z	High – Z	Output Disable	Active
L	H	H	H	X	L	High – Z	High – Z	Output Disable	Active
L	H	L	H	L	H	D-out	High – Z	Lower byte Read	Active
L	H	L	H	H	L	High – Z	D-out	Upper Byte Read	Active
L	H	L	H	L	L	D-out	D-out	Word Read	Active
L	H	X	L	L	H	D-in	High – Z	Lower Byte Write	Active
L	H	X	L	H	L	High – Z	D-in	Upper Byte Write	Active
L	H	X	L	L	L	D-in	D-in	Word Write	Active

Note: X = H or L

Recommended DC Operating Conditions (T_A = -25°C to + 85°C (Standard), T_A = -40°C to + 85°C (Industrial))

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3	3.3	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.2	V
V_{IL}	Input Low Voltage	-0.2	-	+0.6	V

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Min.	Max.	Unit
C_{IN}*	Input Capacitance	V_{IN} = 0V	-	8	pF
$C_{I/O}$*	Input / Output Capacitance	$V_{I/O}$ = 0V	-	10	pF

* These parameters are sampled and not 100% tested.

Absolute Maximum Ratings*

V_{CC} to GND .....-0.2V to +3.3V
IN, IN/OUT Volt to GND ..... -0.2V to V_{CC} + 0.3V
Operating Temperature, Topr .....-25°C to +85°C (Standard)
Operating Temperature, Topr .....-40°C to +85°C (Industrial)
Storage Temperature, Tstg.....-65°C to +125°C
Power Dissipation, P_T..... 1W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics : (T_A = -25°C to + 85°C (Standard), T_A = -40°C to + 85°C (Industrial), V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Conditions	M24L816512A-70/85			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-1	-	1	μA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	-1	-	1	μA
I_{CC1}	Operating Current	Min. Cycle, Duty = 100%, V_{IN} = V_{IL} or V_{IH}, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0mA, V_{DD} = 3.3V	-	-	25	mA
I_{CC2}		f = 1MHz, Duty = 100%, $V_{IN} \geq V_{CC}$-0.2 or $V_{IN} \leq$ 0.2V, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA	-	-	5	mA
I_{SB1}	CMOS Standby Current	$\overline{CE1} \geq V_{CC}$ - 0.2V, $V_{IN} \geq$ 0V	-	-	100	μA
I_{SBD}	Deep Power Down	CE2 $\leqq$ 0.2V, Other inputs = V_{SS}~V_{CC}	-	-	10	
V_{OL}	Output Low Voltage	I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0 mA	2.4	-	-	V

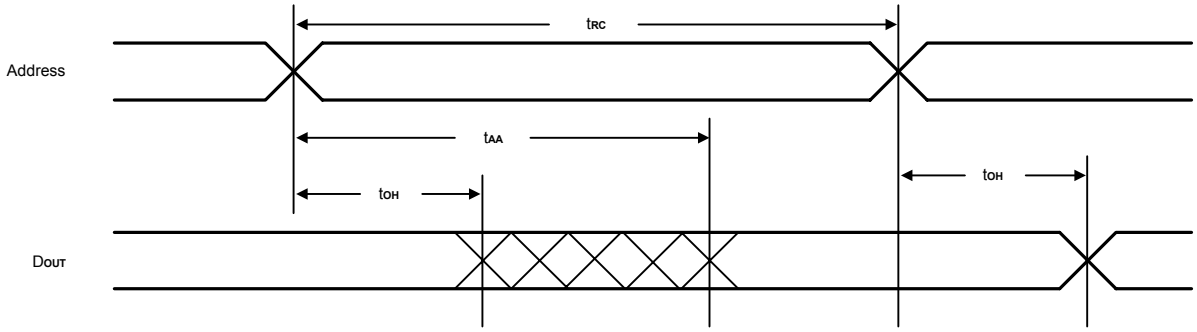
AC Characteristics (T_A = -25°C to + 85°C (Standard), T_A = -40°C to + 85°C (Industrial), V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	M24L816512A -70		M24L816512A –85		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
T_{RC}	Read Cycle Time	70	-	85	-	ns
T_{AA}	Address Access Time	-	70	-	85	ns
T_{ACE1}	Chip Enable ($\overline{CE1}$)Access Time	-	70	-	85	ns
T_{ACE2}	Chip Enable (CE2)Access Time	-	70	-	85	ns
T_{OE}	Output Enable to Output Valid	-	35	-	40	ns
T_{BE}	Byte Enable Access Time	-	70		85	ns
T_{CLZ}	Chip Enable to Output in Low Z	10	-	10	-	ns
T_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
T_{BLZ}	Byte Enable to Output in Low Z	10	-	10		ns
T_{HZ}	Chip Disable to Output in High Z	-	25	-	35	ns
T_{OHZ}	Output Disable to Output in High Z	-	25	-	35	ns
T_{BHZ}	Byte Disable to Output in High Z	-	25	-	35	ns
T_{OH}	Output Hold from Address Change	10	-	10	-	ns
WRITE CYCLE						
T_{WC}	Write Cycle Time	70	-	85	-	ns
T_{WP}	Write Pulse Width	50	-	60	-	ns
T_{AW}	Address Valid to End of Write	60	-	70	-	ns
T_{CW}	Chip Enable to End of Write	60	-	70	-	ns
T_{BW}	Byte Enable to End of Write	60	-	70	-	ns
T_{AS}	Address Setup Time	0	-	0	-	ns
T_{WR}	Write Recovery Time	0	-	0	-	ns
T_{WHZ}	Write to Output in High Z	-	20	-	30	ns
T_{OW}	Output Active to End of Write	5	-	5	-	ns
T_{DW}	Data to Write Time Overlap	30	-	30	-	ns
T_{DH}	Data Hold from Write Time	0	-	0	-	ns

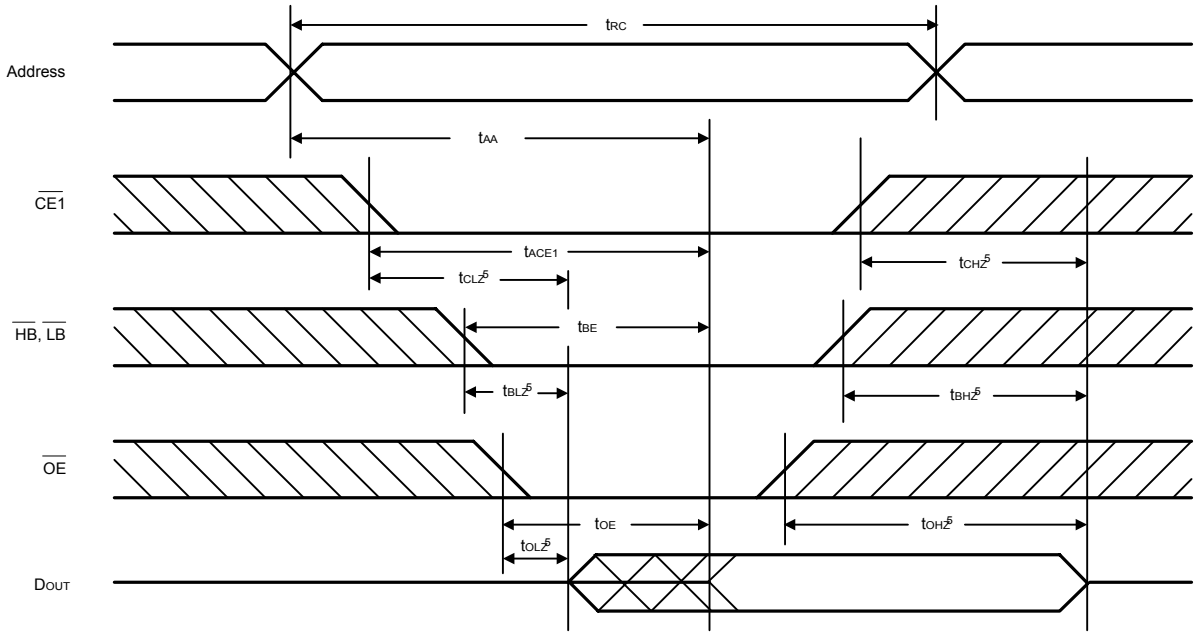
Note: T_{HZ}, T_{OHZ} and T_{BHZ} and T_{WHZ} are defined as the time at which the outputs achieve the open circuit Condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle - Addressed Controlled



Read Cycle - $\overline{CE1}$ Controlled

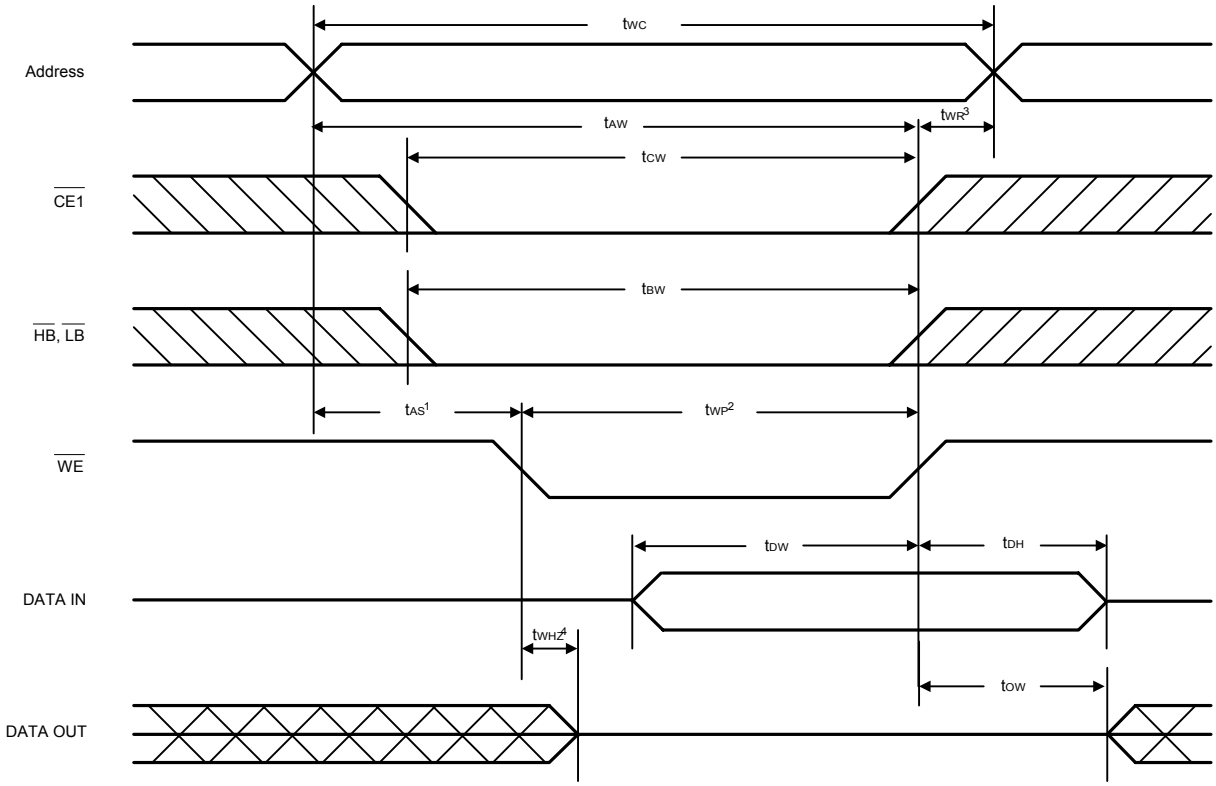


Notes: 1. $\overline{WE}$ is high for Read Cycle.

2. Device is continuously enabled $\overline{CE1}$ = V_{IL}, $\overline{HB}$ = V_{IL} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE1}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

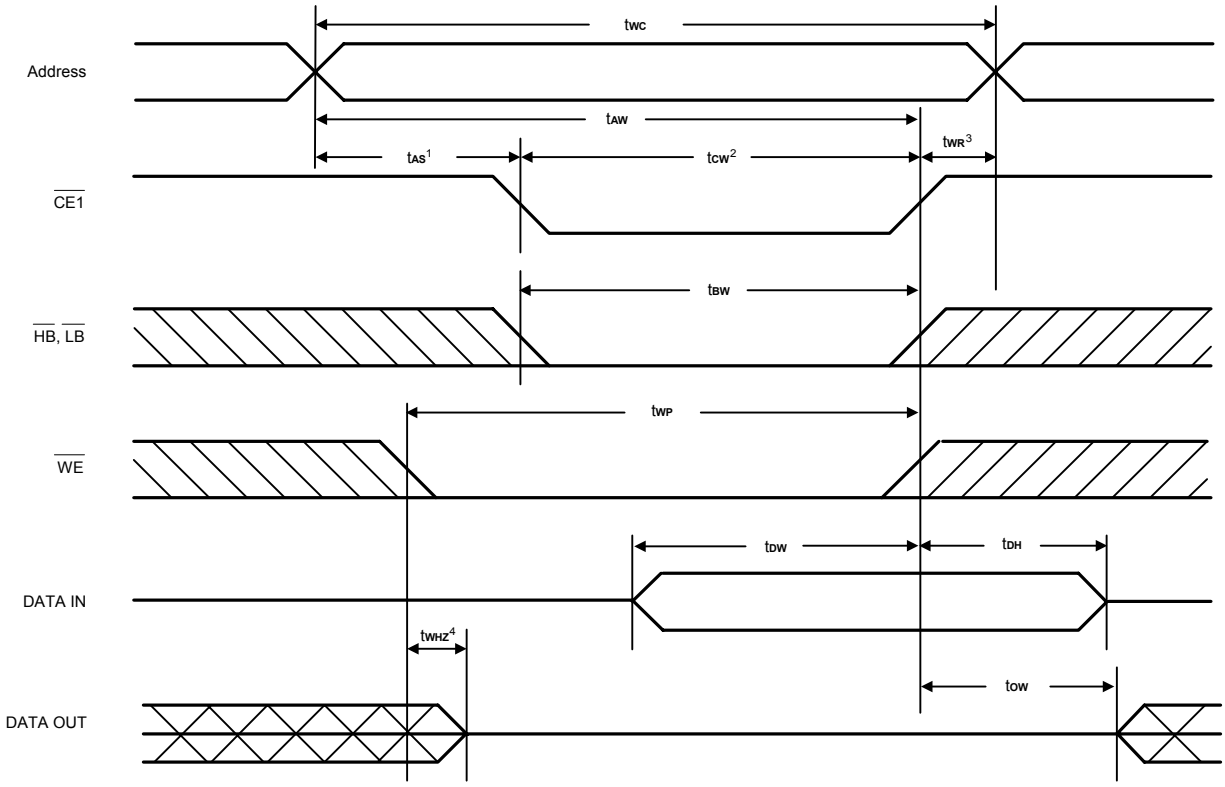
Timing Waveforms (continued)

Write Cycle 1
($\overline{WE}$ **Controlled)**



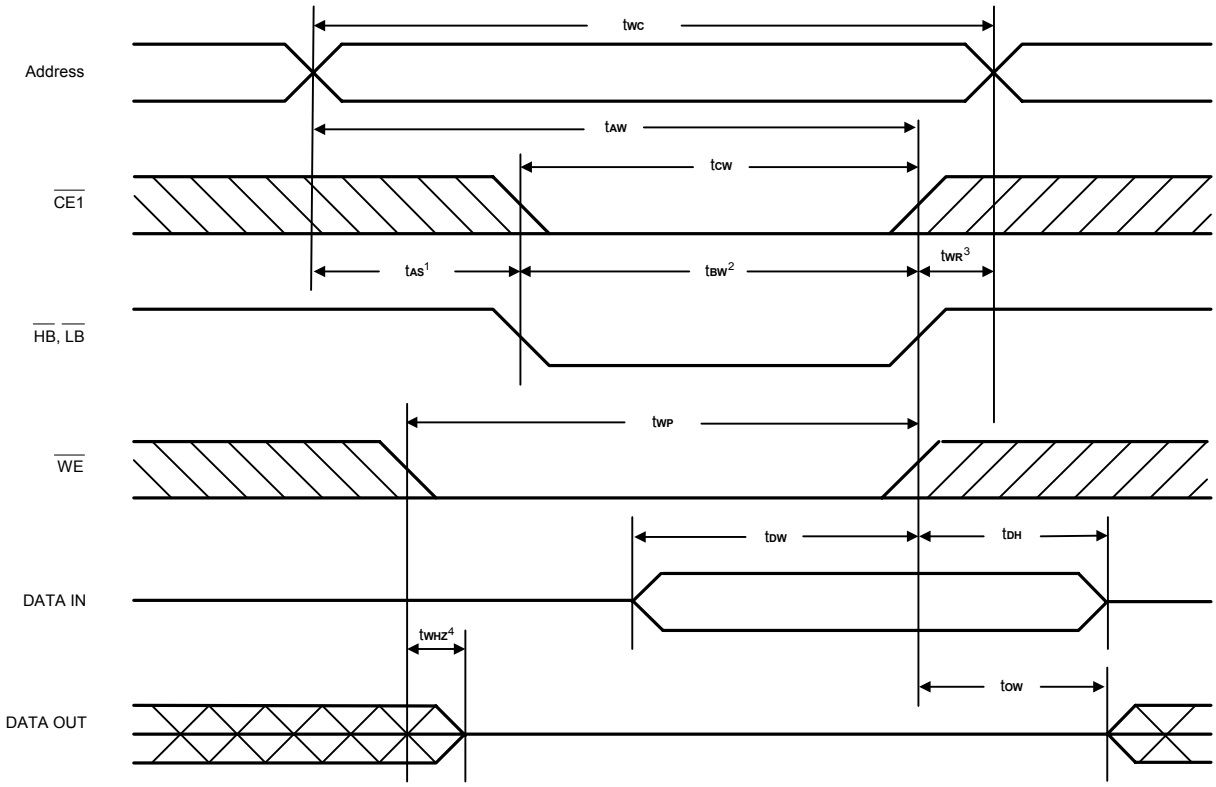
Timing Waveforms (continued)

Write Cycle 2
($\overline{CE1}$ Controlled)



Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)

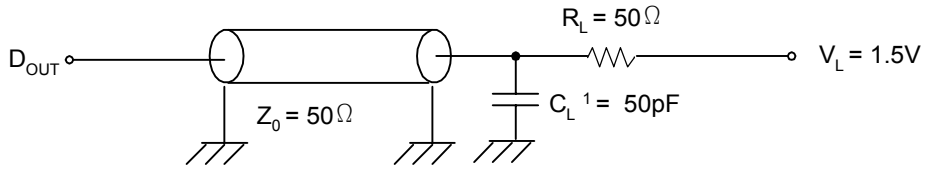


Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CE1}$, $\overline{WE}$ and ($\overline{HB}$ and , or $\overline{LB}$).
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ or ($\overline{HB}$ and , or $\overline{LB}$) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions (T_A = -25°C to + 85°C (Standard), T_A = -40°C to + 85°C (Industrial))

Input Pulse Levels	0.4V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC Test Loads



Note :
1. Including scope and jig capacitance.

Power-Up Sequence

1. Supply power.
2. Maintain stable power for longer than 200 μs.

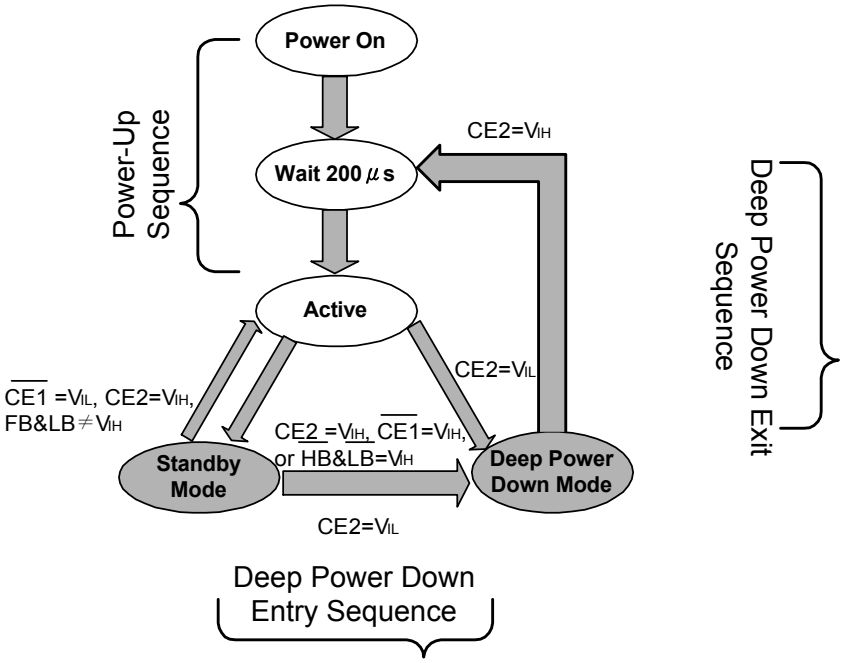
Deep Power Entry Sequence

1. Keep CE2 low state.
Deep power down mode is maintained while CE2 is low state.

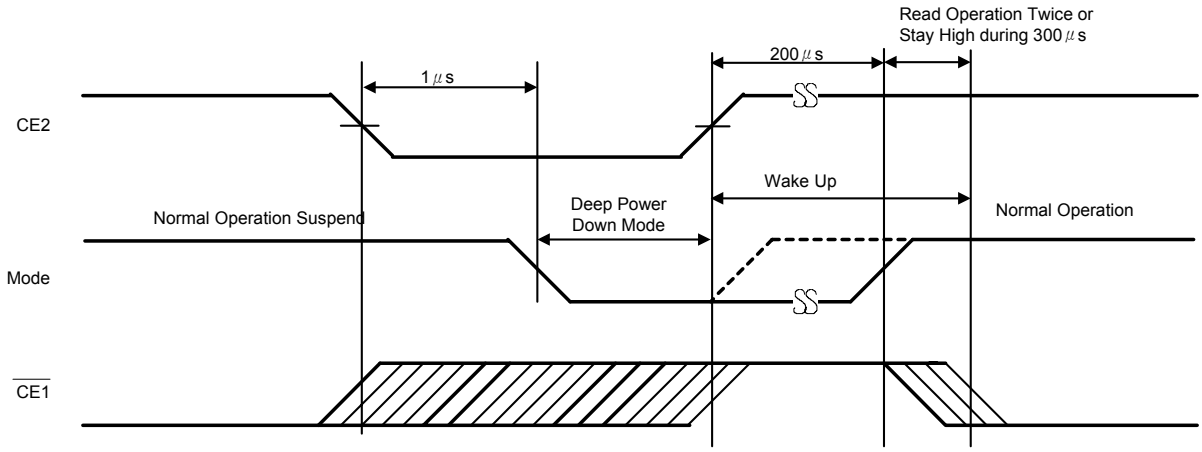
Deep Power Exit Sequence

1. Keep CE2 high state.
2. Maintained stable power for longer than 200 μs.

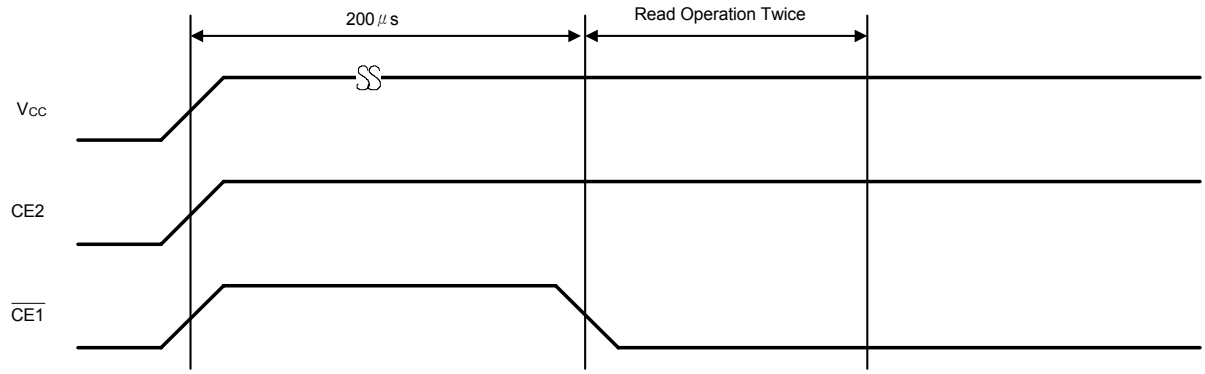
State Diagram



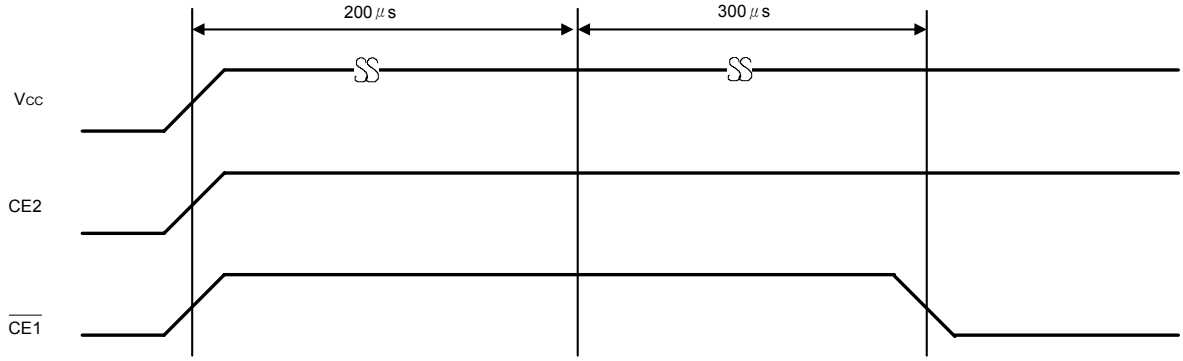
Deep Power Down Mode



Power Up1



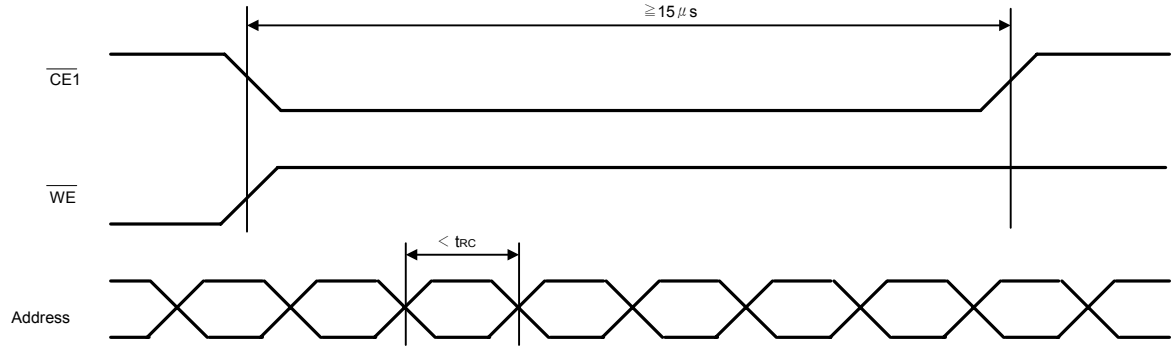
Power Up2 (No Dummy Cycle)



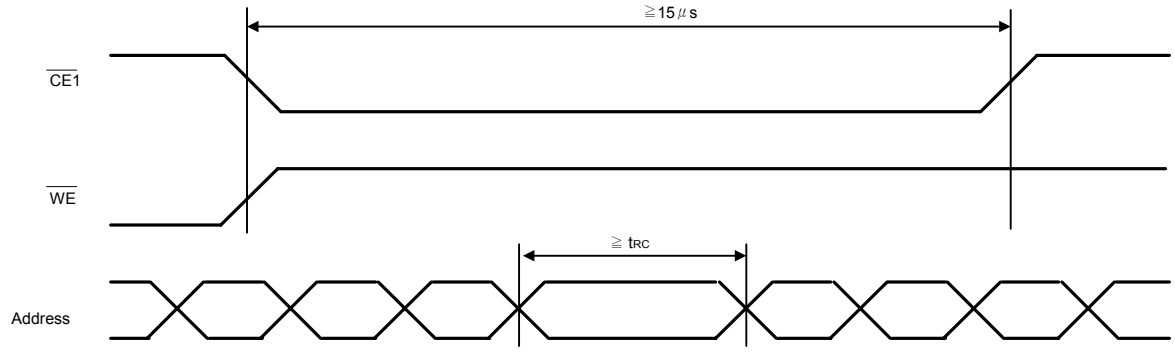
Avoid Timing

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than t_{RC} during over 15 μs at read operation shown as in Abnormal Timing, it requires a normal read timing at leat during 15 μs shown as in Avoidable timing 1 or toggle $\overline{CE1}$ to high ($\geqq t_{RC}$) one time at least shown as in Avoidable Timing 2.

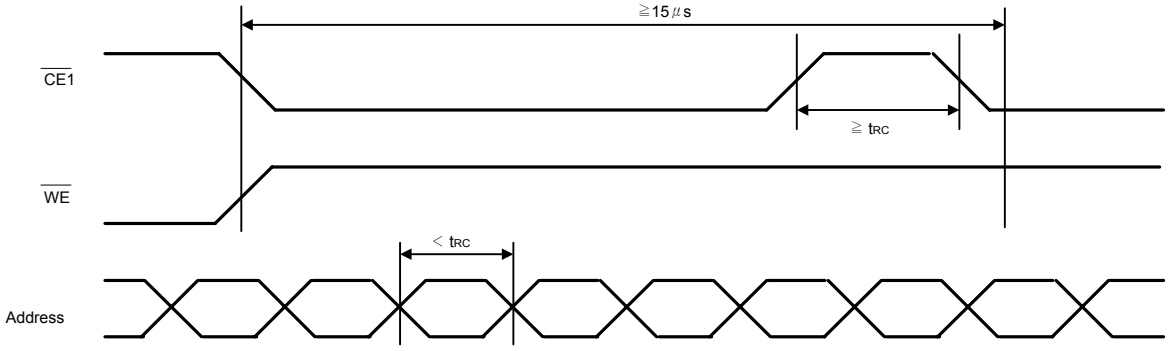
Abnormal Timing



Avoidable Timing 1

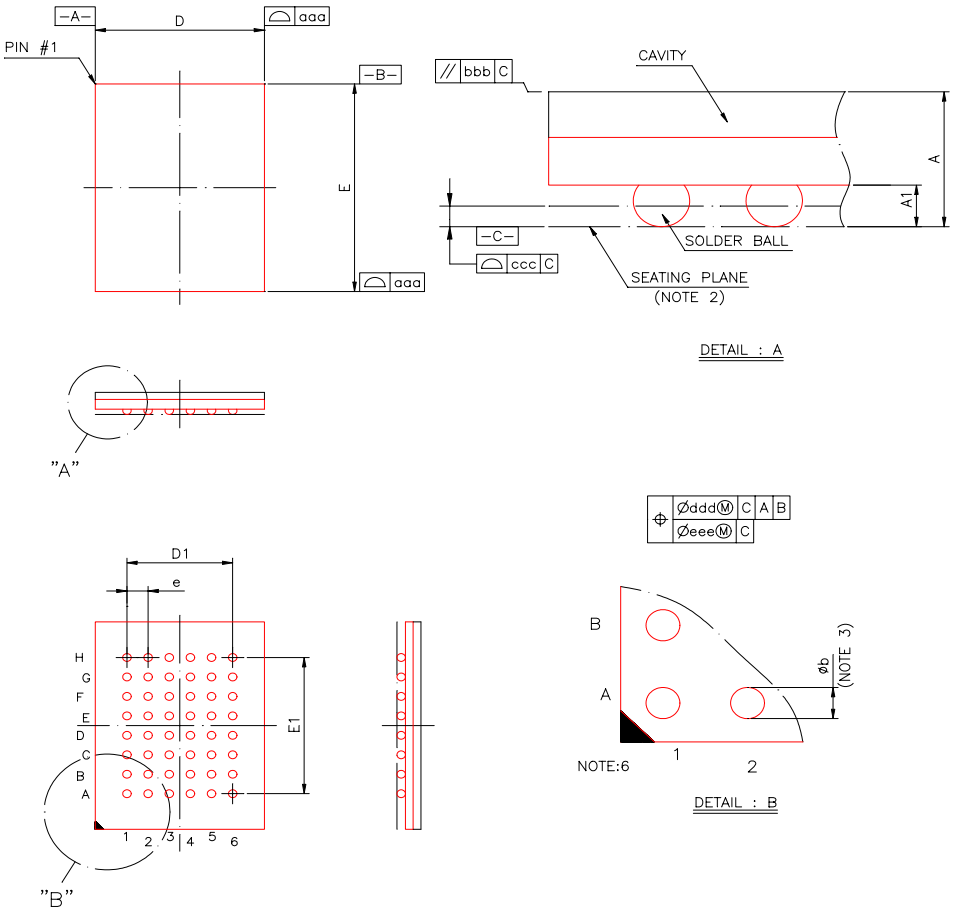


Avoidable Timing 2



PACKING DIMENSIONS

48/48-BALL Mini-BGA (6x8mm) Outline Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	1.14	----------	1.40	0.049	----------	0.055
A_1	0.20	0.25	0.30	0.008	0.010	0.012
Φb	0.30	0.35	0.40	0.012	0.014	0.016
D	5.90	6.00	6.10	0.232	0.236	0.240
D_1	----------	3.75	----------	----------	0.148	----------
E	7.90	8.00	8.10	0.311	0.315	0.319
E_1	----------	5.25	----------	----------	0.207	----------
e	----------	0.75	----------	----------	0.030	----------
aaa	0.10			0.004		
bbb	0.08			0.003		
ccc	0.10			0.004		
ddd	0.20			0.008		
eee	0.10			0.004		

NOTE :

1. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. REFERENCE DOCUMENT : JEDEC MO-207.

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