BAE SYSTEMS

128K x 16 Radiation Hardened Static RAM MCM – 3.3 V

209A542

Features

Product Description

Radiation

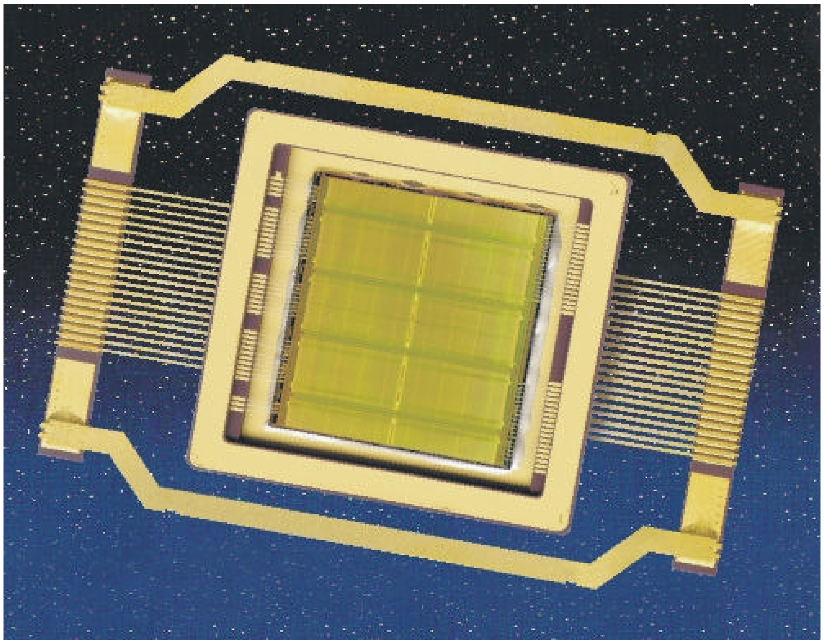
- Fabricated with Bulk CMOS 0.5 µm Process
- Total Dose Hardness through $1x10^6$ rad(Si)
- Neutron Hardness through $1x10^{14}$ N/cm^2
- Dynamic and Static Transient Upset Hardness through $1x10^9$ rad(Si)/s
- Soft Error Rate of < $1x10^{-11}$ Upsets/Bit-Day
- Latchup Free

Other

- Read/Write Cycle Times ≤30 ns (-55 °C to 125°C)
- SMD Number Pending
- Asynchronous Operation
- CMOS or TTL Compatible I/O
- Single 3.3 V ±5% Power Supply
- Low Operating Power
- Packaging Options
  - 40-Lead Dual Flat Pack (0.855” x 0.710”)

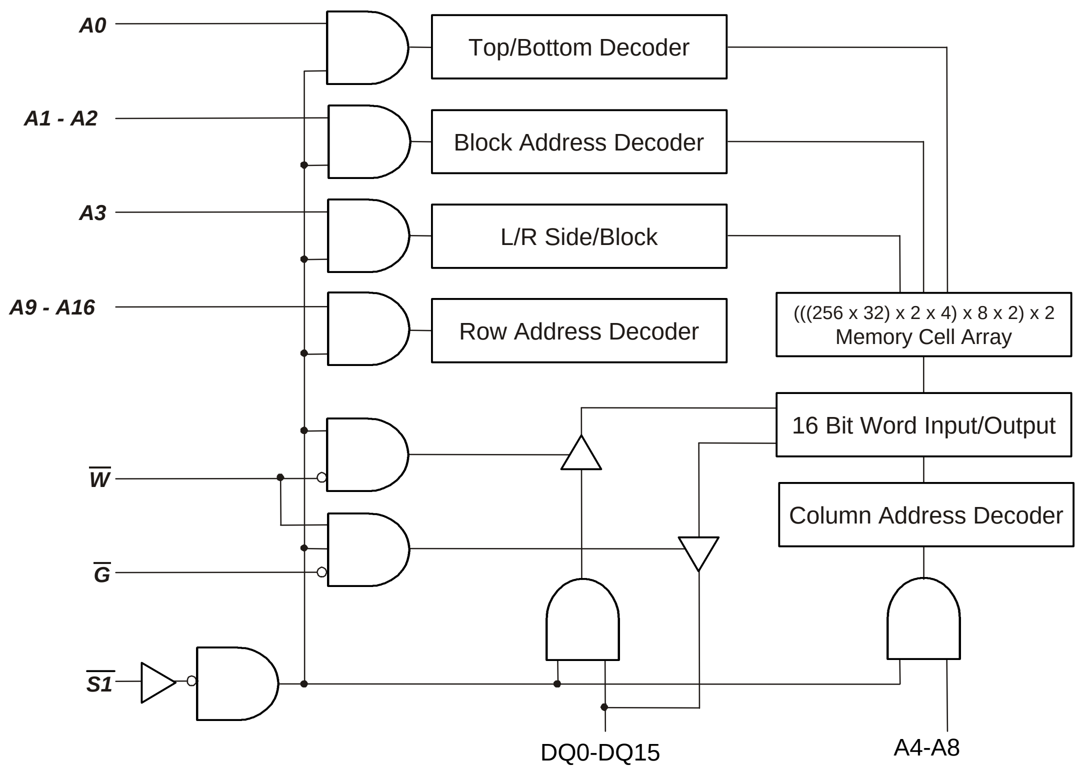
General Description

The 128K x 16 radiation hardened static RAM is composed of two 128K x 8 SRAM memory die assembled in a double-sided ceramic substrate. Each die is a high performance 131,072 word x 8-bit static random access memory with industry-standard functionality. It is fabricated with BAE SYSTEMS’ radiation hardened technology and is designed for use in systems operating in radiation environments. The RAM operates over the full military temperature range and requires a single 3.3 V ±5% power supply. The RAM is available with CMOS compatible I/O. Power consumption is typically less than 40 mW/MHz in operation, and less than 20 mW in the low power disabled mode. The RAM read operation is fully asynchronous, with an associated typical access time of 19 nanoseconds.



BAE SYSTEMS’ enhanced bulk CMOS technology is radiation hardened through the use of advanced and proprietary design, layout, and process hardening techniques.

Functional Diagram



Signal Definitions

A: 0-16 – Address input pins that select a particular 16-bit word within the memory array.

DQ: 0-15 – Bi-directional data pins that serve as data outputs during a read operation and as data inputs during a write operation.

$\overline{S1}$ – Negative chip select, when at a low level, allows normal read or write operation. When at a high level, $\overline{S1}$ forces the SRAM to a precharge condition, holds the data output drivers in a high impedance state and disables the data input buffers only. If this signal is not used, it must be connected to GND.

$\overline{W}$ – Negative write enable, when at a low level, activates a write operation and holds the data output drivers in a high impedance state. When at a high level, $\overline{W}$ allows normal read operation.

$\overline{G}$ – Negative output enable, when at a high level holds the data output drivers in a high impedance state. When at a low level, the data output driver state is defined by $\overline{S1}$ and $\overline{W}$. If this signal is not used it must be connected to GND.

Truth Table

Mode	Inputs(1),(2)				Power
	$\overline{S1}$	$\overline{W}$	$\overline{G}$	I/O	
Write	Low	Low	X	Data-In	Active
Read	Low	High	Low	Data-Out	Active
Standby	X	X	X	High-Z	Standby
Standby(3)	High	X	X	High-Z	Standby

Notes:

1) V_{IN} for don't care (X) inputs = V_{IL} or V_{IH}.

2) When $\overline{G}$ = high, I/O is high-Z.

3) To dissipate the minimum amount of standby power when in standby mode: $\overline{S1}$ = V_{DD}. All other input levels may float.

Absolute Maximum Ratings

Applied Conditions[(1)]	*Minimum*	*Maximum*
Storage Temperature Range (Ambient)	-65°C	+150°C
Operating Temperature Range T_{CASE}	-55°C	+125°C
Positive Supply Voltage	-0.5 V	+5.5 V
Input Voltage[(2)]	-0.5 V	V_{DD}+ 0.5 V
Output Voltage[(2)]	-0.5 V	V_{DD}+ 0.5 V
Power Dissipation[(3)]		1.25 W
Lead Temperature (Soldering 5 sec)		+230°C
Electrostatic Discharge Sensitivity[(4)]	(Class II)	

Notes:

1) Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. All voltages are with reference to the module ground leads.

2) Maximum applied voltage shall not exceed +5.5 V.

3) Guaranteed by design; not tested.

4) Class as defined in MIL-STD-883, Method 3015.

Recommended Operating Conditions

Symbol	*Parameters*[(1)]	*Minimum*	*Maximum*	*Units*
V_{DD}	Supply Voltage	+3.14	+3.46	Volt
GND	Supply Voltage Reference	0.0	0.0	Volt
T_C	Case Temperature	-55	+125	Celsius
V_{IL}	Input Logic “Low”	-0.3	+0.8	Volt
V_{IH}	Input Logic “High”	+2.0	V_{DD}	Volt

Note:

1)All voltages referenced to GND.

Power Sequencing

Power shall be applied to the device only in the following sequences to prevent damage due to excessive currents:

- Power-Up Sequence: GND, V_{DD}, Inputs
- Power-Down Sequence: Inputs, V_{DD}, GND

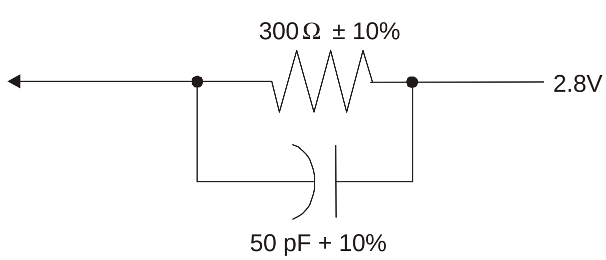
DC Electrical Characteristics

Test	Symbol	Test Conditions[1]	Device Type	Limits Minimum	Limits Maximum	Units
Supply Current (Cycling Selected)	I_{DD1}	$F = F_{MAX} = 1/t_{AVAV(min)}$ $\overline{S1}$ = GND No Output Load	All		360	mA
Supply Current (Cycling De-Selected)	I_{DD2}	$F = F_{MAX} = 1/t_{AVAV(min)}$ $\overline{S1} = V_{DD}$	All		6.0	mA
Supply Current (Standby)	I_{DD3}	F = 0 MHz $\overline{S1} = V_{DD}$	All		6.0	mA
Data Retention Current	I_{DR}	V_{DD}= 2.5 V	All		4.0	mA
High Level Output Voltage	V_{OH}	I_{OH}= -4 mA I_{OH} = -200 µA	All	4.0 V_{DD} - 0.5 V		V
Low Level Output Voltage	V_{OL}	I_{OL}= 8 mA I_{OL} = 200 µA	All		0.4 0.05	V
High Level Input Voltage	V_{IH}		All	2.0		V
Low Level Input Voltage	V_{IL}		All		0.8	V
Input Leakage	I_{ILK}	$0 V \le V_{IN} \le 5.5 V$	All	-20	20	µA
Output Leakage	I_{OLK}	$0 V \le V_{OUT} \le 5.5 V$	All	-20	20	µA
C_{in}	(2)	By Design/ Verified By Characterization	All		6	pF
C_{out}	(2)	By Design/ Verified By Characterization	All		9	pF

Note:

1) Typical operating conditions:
-55°C £ T_{case} £ +125°C; 3.14 V £ V_{DD} £ 3.46 V; unless otherwise specified.
2) Guaranteed by design and verified by periodic characterization.

Output Load Circuit



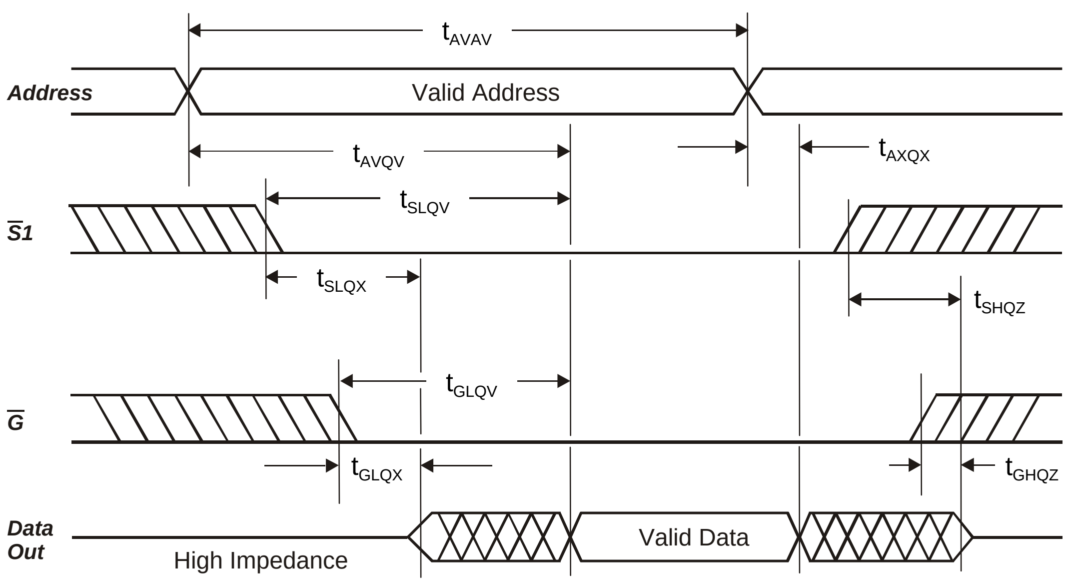
Read Cycle AC Timing Characteristics[1]

Test	***Symbol***	***Minimum or Maximum***	***Device Type***	***Limits***	***Units***
Read Cycle Time	t_{AVAV} [2]	Minimum	All	30	ns
Address Access Time	t_{AVQV}	Maximum	All	30	ns
Chip Select Access Time	t_{SLQV}	Maximum	All	30	ns
Output Enable Access Time	t_{GLQV}	Maximum	All	15	ns
Chip Select to Output Active	t_{SLQX}	Minimum	All	0	ns
Output Enable to Output Active	t_{GLQX}	Minimum	All	0	ns
Output Hold After Address Change	t_{AXQX}	Minimum	All	0	ns
Chip Select to Output Disable	t_{SHQZ}	Maximum	All	15	ns
Output Enable to Output Disable	t_{GHQZ}	Maximum	All	15	ns

Notes:

1)Test conditions: input switching levels V_{IL}/V_{IH} = 0.5 V/V_{DD} -0.5 V (CMOS), input rise and fall times < 5 ns, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading C_L = 50 pF. For C_L > 50 pF, derate access times by 0.02 ns/pF (typical). -55°C £ T_{case} £ +125°C; 3.14 V £ V_{DD} £ 3.46 V; unless otherwise specified.
2) Cycle time per individual die.

Read Cycle Timing Diagram



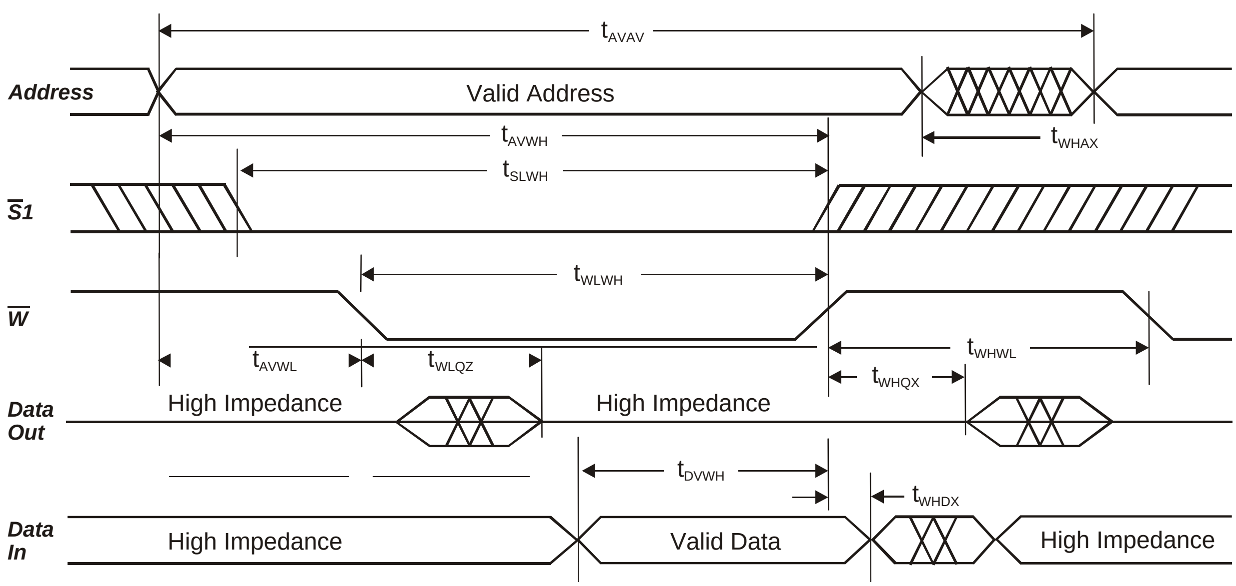
Write Cycle AC Timing Characteristics(1)

Test	Symbol	Minimum or Maximum	Device Type	Limits	Units
Write Cycle Time	t_{AVAV}	Minimum	All	40	ns
Write Pulse Width Access Time	t_{WLWH}	Minimum	All	25	ns
Chip Select to End of Write	t_{SLWH}	Minimum	All	35	ns
Data Setup to End of Write	t_{DVWH}	Minimum	All	35	ns
Address Setup to End of Write	t_{AVWH}	Minimum	All	35	ns
Data Hold After End of Write	t_{WHDX}	Minimum	All	5	ns
Address Setup to Start of Write	t_{AVWL}	Minimum	All	0	ns
Address Hold After End of Write	t_{WHAX}	Minimum	All	0	ns
Write Enable to Output Disable	t_{WLQZ}	Maximum	All	18	ns
Output Active After End of Write	t_{WHQX}	Minimum	All	1	ns
Write Disable Pulse Width	t_{WHWL}	Minimum	All	15	ns

Note:

1) Test conditions: input switching levels V_{IL}/V_{IH} = 0.5 V/V_{DD} - 0.5 V (CMOS), input rise and fall times < 5 ns, input and output timing reference levels shown in the Tester AC Timing Characteristics table, capacitive output loading = 50 pF. -55°C £ T_{case} £ +125°C; 3.14 V £ V_{DD} £ 3.46 V; unless otherwise specified.

Write Cycle Timing Diagram



Dynamic Electrical Characteristics

Read Cycle

The RAM is asynchronous in operation, allowing the read cycle to be controlled by address, chip select ($\overline{S1}$) (refer to Read Cycle Timing diagram). To perform a valid read operation, both chip select and output enable ($\overline{G}$) must be low and chip enable and write enable ($\overline{W}$) must be high. The output drivers can be controlled independently by the $\overline{G}$ signal. Consecutive read cycles can be executed with $\overline{S1}$ held continuously low, and toggling the addresses.

For an address-activated read cycle, $\overline{S1}$ must be valid prior to or coincident with the activating address edge transition(s). Any amount of toggling or skew between address edge transitions is permissible; however, data outputs will become valid t_{AVQV} time following the latest occurring address edge transition. The minimum address activated read cycle time is t_{AVAV} . When the RAM is operated at the minimum address-activated read cycle time, the data outputs will remain valid on the RAM I/O until t_{AXQX} time following the next sequential address transition.

To control a read cycle with $\overline{S1}$, all addresses must be valid prior to or coincident with the enabling $\overline{S1}$ edge transition. Address transitions can occur later than the specified setup times to $\overline{S1}$; however, the valid data access time will be delayed. Any address edge transition, that occurs during the time when $\overline{S1}$ is low, will initiate a new read access, and data outputs will not become valid until t_{AVQV} time following the address edge transition. Data outputs will enter a high impedance state t_{SHQZ} time following a disabling $\overline{S1}$ edge transition.

Write Cycle

The write operation is synchronous with respect to the address bits, and control is governed by write enable ($\overline{W}$), chip select ($\overline{S1}$) edge transitions (refer to Write Cycle Timing diagrams). To perform a write operation, both $\overline{W}$ and $\overline{S1}$ must be low. Consecutive write cycles can be performed with $\overline{W}$ or $\overline{S1}$ held continuously low. At least one of the control signals must transition to the opposite state between consecutive write operations.

The write mode can be controlled via two different control signals: $\overline{W}$ and $\overline{S1}$. Both modes of control are similar except the $\overline{S1}$ controlled mode actually disables the RAM during the write recovery pulse. Only the $\overline{W}$ controlled mode is shown in the table and diagram on the previous page for simplicity. However, each mode of control provides the same write cycle timing characteristics. Thus, some of the parameter names referenced below are not shown in the write cycle table or diagram, but indicate which control pin is in control as it switches high or low.

To write data into the RAM, $\overline{W}$ and $\overline{S1}$ must be held low for at least t_{WLWH} /t_{SLSH} time. Any amount of edge skew between the signals can be tolerated and any one of the control signals can initiate or terminate the write operation. For consecutive write operations, write pulses must be separated by the minimum specified t_{WHWL} /t_{SLSH} time. Address inputs must be valid at least t_{AVWL} /t_{AVSL} time before the enabling $\overline{W}$/$\overline{S1}$ edge transition, and must remain valid during the entire write time. A valid data overlap of write pulse width time of t_{DVWH} /t_{DVSH}, and an address valid to end of write time of t_{AVWH} /t_{AVSH} also must be provided for during the write operation. Hold times for address inputs and data inputs with respect to the disabling $\overline{W}$/$\overline{S1}$ edge transition must be a minimum of t_{WHAX} /t_{SHAX} time and t_{WHDX} /t_{SHDX} time, respectively. The minimum write cycle time is t_{AVAV}.

Radiation Characteristics

Total Ionizing Radiation Dose

The SRAM will meet all stated functional and electrical specifications over the entire operating temperature range after a total ionizing radiation dose of $1x10^6$ rad(Si). All electrical and timing performance parameters will remain within specifications after rebound at V_{DD} = 3.3 V and T = 125°C extrapolated to ten years of operation. Total dose hardness is assured by wafer level testing of process monitor transistors and RAM product using 10 keV X-ray and Co60 radiation sources. Transistor gate threshold shift correlations have been made between 10 keV X-rays applied at a dose rate of $1x10^5$ rad(Si)/min at T = 25°C and gamma rays (Cobalt 60 source) to ensure that wafer level X-ray testing is consistent with standard military radiation test environments.

Transient Pulse Ionizing Radiation

The SRAM is capable of writing, reading, and retaining stored data during and after exposure to a transient ionizing radiation pulse of ≤ 50 ns duration up to $1x10^9$ rad(Si)/s, when applied under recommended operating conditions. To ensure validity of all specified performance parameters before, during, and after radiation (timing degradation during transient pulse radiation is ≤ 10%), stiffening capacitance can be placed on the package between the package (chip) V_{DD} and GND with the inductance between the package (chip) and stiffening capacitance kept to a minimum. If there are no operate-through or valid stored data requirements, typical de-coupling capacitors should be mounted on the circuit board as close as possible to each device.

The SRAM will meet any functional or electrical specification after exposure to a radiation pulse of ≤ 50 ns duration up to $1x10^{12}$ rad(Si)/s, when applied under recommended operating conditions. Note that the current conducted during the pulse by the RAM inputs, outputs, and power supply may significantly exceed the normal operating levels. The application design must accommodate these effects.

Neutron Radiation

The SRAM will meet any functional or timing specification after a total neutron fluence of up to $1x10^{14}$ cm^{-2} applied under recommended operating or storage conditions. This assumes an equivalent neutron energy of 1 MeV.

Soft Error Rate

The SRAM has a soft error rate (SER) performance of $<1x10^{-11}$ upsets/bit-day, under recommended operating conditions. This hardness level is defined by the Adams 90% worst case cosmic ray environment.

Latchup

The SRAM will not latch up due to any of the above radiation exposure conditions when applied under recommended operating conditions.

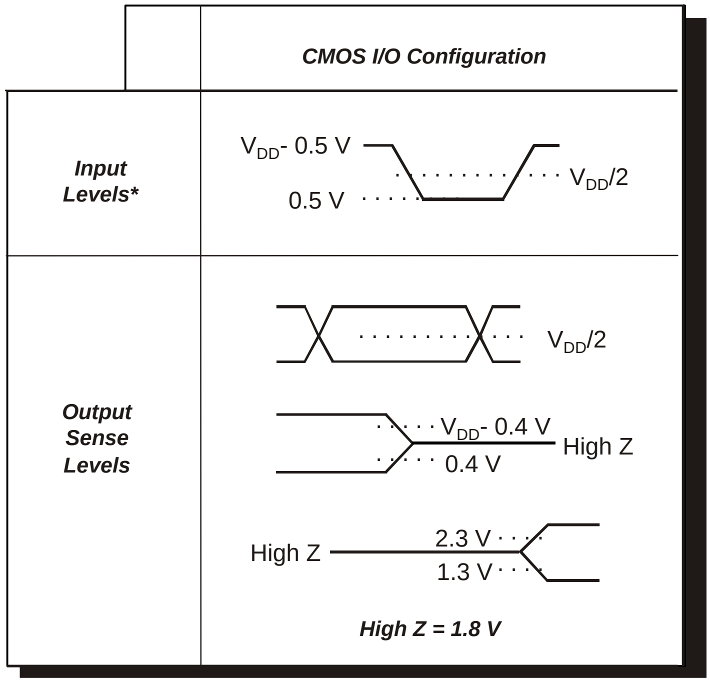
Radiation Hardness Ratings (1),(2)

Symbol	*Characteristics*	*Conditions*	*Minimum*	*Maximum*	*Units*
RTD	Total Dose		1E + 06		rad(Si)
SEU1	Single Event Upset(3)	-55°C ≤ T_{case} ≤ 80°C		1E - 11	Upsets/Bit-Day
SEU2	Single Event Upset (3)	-55°C ≤ T_{case} ≤ 125°C		1E - 10	Upsets/Bit-Day
RNF	Neutron Fluence		1E + 14		N/cm^2
SEU1	Single Event Induced Latchup (4)	-55°C ≤ T_{case} ≤ 125°C			MeV
SEL	Single Event Induced Latchup (4)	-55°C ≤ T_{case} ≤ 125°C V_{DD} = 3.46 V			Immune

Notes:

1) Measured at room temperature unless otherwise stated. Verification test per TRB approved test plan.
2) Device electrical characteristics are guaranteed for post irradiation levels at 25°C.
3) 90% worst case particle environment, geosynchronous orbit, 0.025'' of aluminum shielding. Specification set using the CREME code upset rate calculation method with a 2 µm epi thickness.
4) Immune for LET £ 120 $MeV/mg/cm^2$.

Tester AC Timing Characteristics



*Input rise and fall times <5 ns

Radiation Hardness Assurance

BAE SYSTEMS provides a superior quality level of radiation hardness assurance for our products. The excellent product quality is sustained via the use of our qualified QML operation which requires process control with statistical process control, radiation hardness assurance procedures and a rigid computer controlled manufacturing operation monitoring and tracking system.

The BAE SYSTEMS technology is built with resistance to radiation effects. Our product is designed to exhibit $< 1e^{-11}$ fails/bit-day in a 90% worst case geosynchronous orbit under worst case operating conditions. Total dose hardness is assured by irradiating test structures on every lot and total dose exposure with Cobalt 60 testing performed quarterly on TCI lots to assure the product is meeting the QML radiation hardness requirements.

Screening Levels

BAE SYSTEMS has two QML screen levels (Q and V) to meet full compliant space applications. For limited performance and evaluation situations, BAE SYSTEMS offers an engineering screen level.

Reliability

BAE SYSTEMS' reliability starts with an overall product assurance system that utilizes a quality system involving all employees including operators, process engineers and product assurance personnel. An extensive wafer lot acceptance methodology, using in-line electrical data as well as physical data, assures product quality prior to assembly. A continuous reliability monitoring program evaluates every lot at the wafer level, utilizing test structures as well as product testing. Test structures are placed on every wafer, allowing correlation and checks within-wafer, wafer-to-wafer, and from lot-to-lot.

Reliability attributes of the CMOS process are characterized by testing both irradiated and non-irradiated test structures. The evaluations allow design model and process changes to be incorporated for specific failure mechanisms, i.e., hot carriers, electromigration, and time dependent dielectric breakdown. These enhancements to the operation create a more reliable product.

The process reliability is further enhanced by accelerated dynamic life tests of both irradiated and non-irradiated test structures. Screening and testing procedures from the customer are followed to qualify the product.

A final periodic verification of the quality and reliability of the product is validated by a TCI (Technology Conformance Inspection).

Standard Screening Procedure

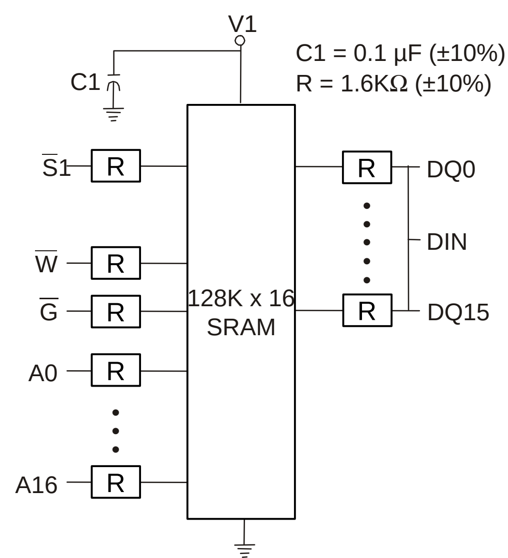
Flow	*QML Level*		*Comments*
	Q	*V*	
Wafer Lot Acceptance	X	X	Alternate Method Used
Serialization	X	X	Die Traceability
Destructive Bond Pull	Sample	Sample	
Internal Visual	X	X	MIL-STD-883, TM 2010
Temperature Cycle	X	X	
Constant Acceleration	X	X	
PIND	X	X	
Radiography		X	
Electrical Test	X	X	
Dynamic Burn-In	X	X	
Electrical Test		X	
Static Burn-In		X	3.46 V, 125°C, 144 Hours
Final Electrical	X	X	Meets Group A
PDA	X	X	< 5% Fallout
Fine and Gross Leak	X	X	
External Visual	X	X	MIL-STD-883, TM 2009

Burn-In Circuit

Stress Methodology

There are two methods of burn-in defined. For “Static” burn-in, all possible addresses are written with a logic “1” for half of the burn-in duration and a logic “0” for the remaining half. For “Dynamic” burn-in, all possible addresses are written with alternating high and low data.

All I/O pins specified in the static and dynamic burn-in pin lists are driven through individual series resistors (1.6K Ω ±10%). The burn-in circuit diagram is shown at right.



Voltage Levels

- Vin(0): 0.0 V to + 0.4 V
  - V_{IL} = Low level for all programmed signals
- Vin(1): + 3.3 V to + 3.7 V
  - V_{IH} = High level for all programmed signals
- V1: + 3.45 V (-0% / +10%)
  - All V_{DD} pins are tied to this level
- Vsx: Float or GND
  - All GND pins are tied to this level

Pin Listing

The dynamic burn-in pin listing is shown at right.
F = square wave, 100 KHz to 1.0 MHz.

Input	*Signal*	*Input*	*Signal*	*Input*	*Signal*
A0	F/2	A5	F/64	A10	F/2048
A1	F/4	A6	F/128	A11	F/4096
A2	F/8	A7	F/256	A12	F/8192
A3	F/16	A8	F/512	A13	F/16384
A4	F/32	A9	F/1024	A14	F/32768

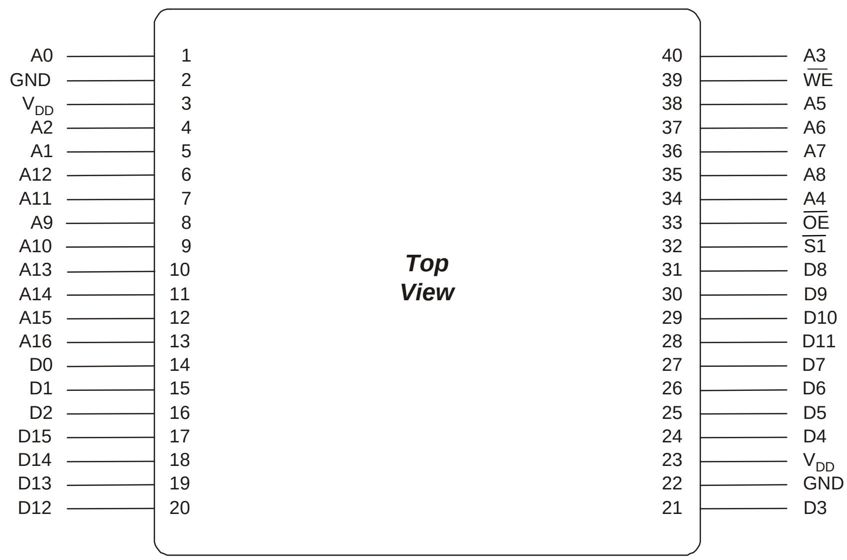
Input	*Signal*
A15	F/65536
A16	F/131072
$\overline{W}$	F/262144
D_{IN}	F/524288
$\overline{S}1$	F/1048578
$\overline{G}$	V_{IL}

Packaging

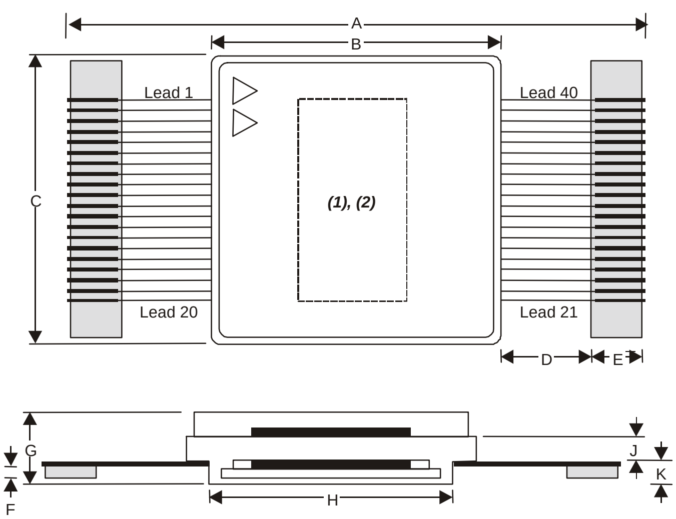
The 128K x 16 SRAM is offered in a custom 40-lead dual FP. All packages are constructed of multilayer ceramic (Al_2O_3) and feature internal power and ground planes.

Optional capacitors can be mounted to the package to maximize supply noise decoupling and increase board packing density. These capacitors attach directly to the internal package power and ground planes. This design minimizes resistance and inductance of the bond wire and package, both of which are critical in a transient radiation environment. All NC pins must be connected to either V_{DD}, GND or an active driver to prevent charge build up in the radiation environment. (NC = no connect.)

40-Lead Dual Flat Pack Pinout



40-Lead Dual Flat Pack



A=1.635	F=.030
B=.885 ± .008	G=.164
C=.710 ± .010	H=.775
D=.245 ± .015	J=.048
E=.135	K=.045

Notes:

1) Part mark per device specification.

2) ‘‘QML’’ may not be required per device specification.

3) Dimensions are in inches.

4) Lead width: .008 ± .002.

5) Lead height: .006 ± .002.

6) Unless otherwise specified, all tolerances are ± .005”.

Ordering Information

128K x 16 CMOS Memory Device - MCM (3.3 V)
•Part Number 209A542

X ***Package Designation***	***Y*** ***Speed Designation***	***Z*** ***Screen Designation***
1=40-Lead FP	3 = 30 ns 4 = 40 ns	1=QML VV 3=Engineering 4=QML VQ 5=QML QQ 7=Customer Specific

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