

FAN7311

LCD Backlight Inverter Drive IC

Features

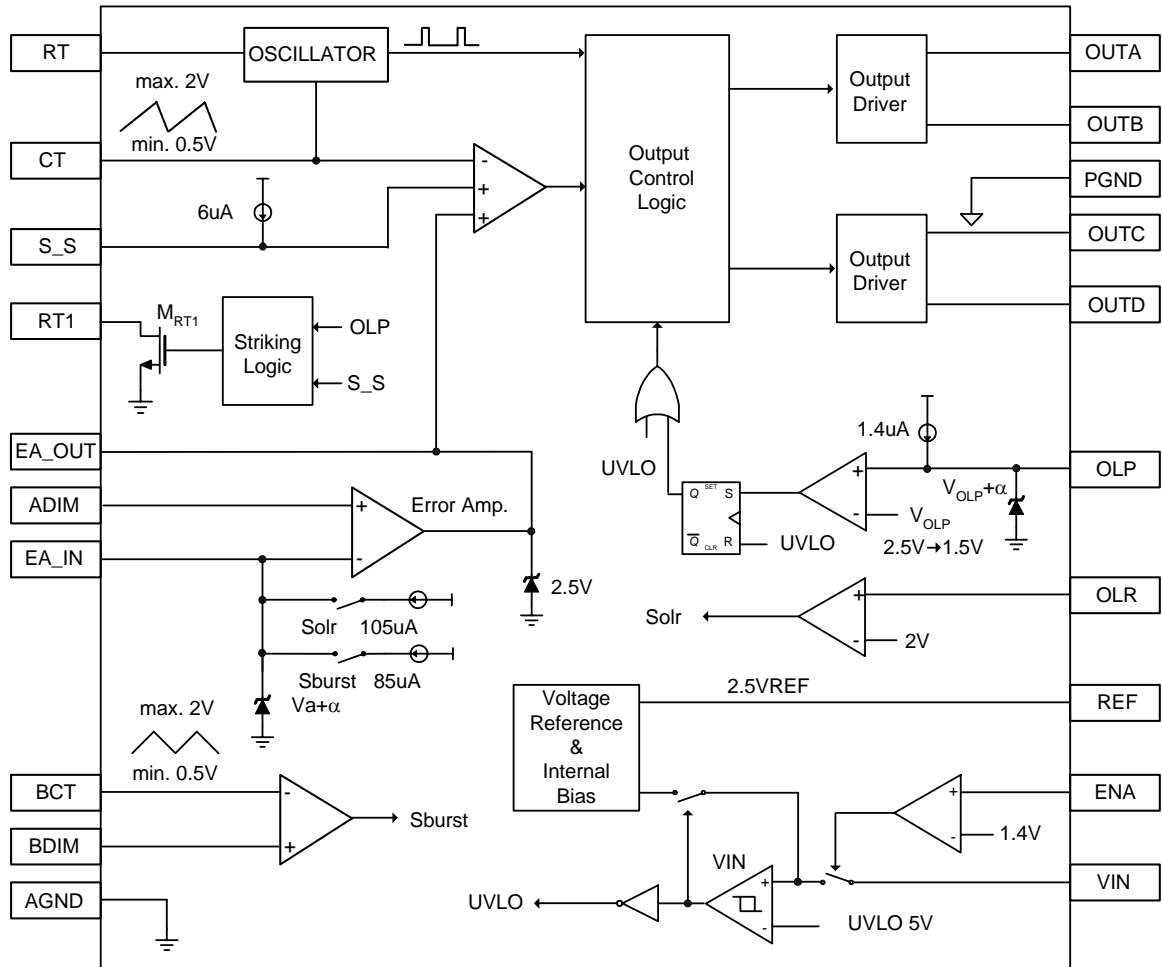
- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range : 5V to 25.5V
- Back Light Lamp Ballast and Soft Dimming
- Reduces Number of Required External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS Full-Bridge Topology
- Soft Start
- PWM Control at Fixed Frequency
- Analog and Burst Dimming Function
- Programmable Striking Frequency
- Open Lamp Protection
- Open Lamp Regulation
- 20-Pin SSOP

Description

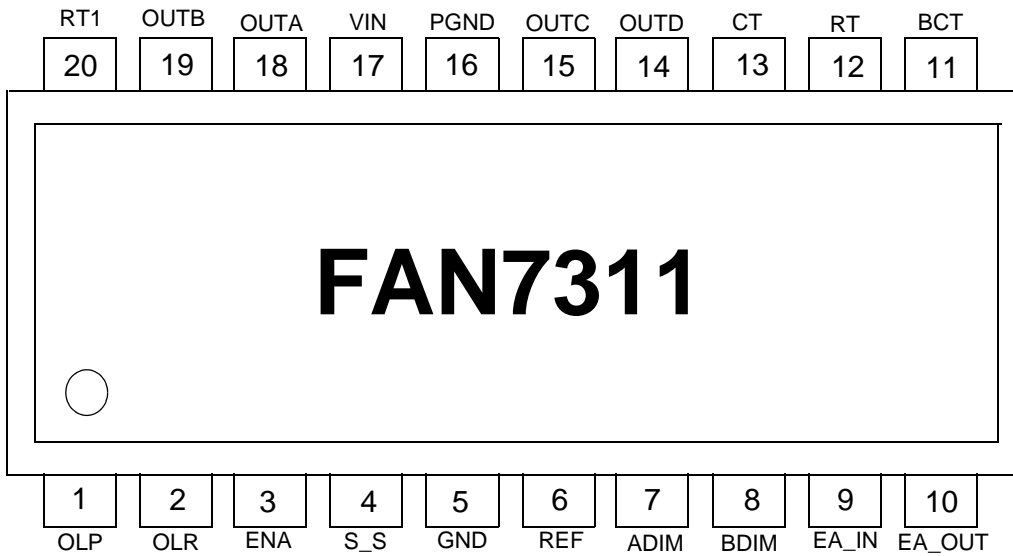
The FAN7311 provides all the control functions for a series parallel resonant converter as well as a pulse width modulation (PWM) controller to develop a supply voltage. Typical operating frequency range is between 30kHz and 250kHz, depending on the CCFL and the transformer's characteristics. The FAN7311 uses a new patent-pending phase-shift control.



Internal Block Diagram



Pin Assignments



Pin Definitions

No	Name	Function/Description	No	Name	Function/Description
1	OLP	Open Lamp Protection	11	BCT	Burst Dimming Timing Capacitor
2	OLR	Open Lamp Regulation	12	RT	Timing Resistor
3	ENA	Enable Input	13	CT	Timing Capacitor
4	S_S	Soft Start	14	OUTD	NMOSFET Drive Output D
5	GND	Analog Ground	15	OUTC	PMOSFET Drive Output C
6	REF	2.5V Reference Voltage	16	PGND	Power Ground
7	ADIM	Analog Dimming Input	17	VIN	Supply Voltage
8	BDIM	Burst Dimming Input	18	OUTA	PMOSFET Drive Output A
9	EA_IN	Error Amplifier Input	19	OUTB	NMOSFET Drive Output B
10	EA_OUT	Error Amplifier Output	20	RT1	Striking Frequency Resistor

Absolute Maximum Ratings

For typical values $T_a=25^{\circ}\text{C}$, $V_{CC}=12\text{V}$ and for min/max values T_a is the operating ambient temperature range with $-25^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $5\text{V} \leq V_{CC} \leq 25.5\text{V}$, unless otherwise specified.

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	5 ~ 25.5	V
Operating Temperature Range	T_{opr}	-25 ~ 85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 ~ 150	$^{\circ}\text{C}$
Thermal Resistance Junction-Air (Note1,2)	$R_{\theta JA}$	112	$^{\circ}\text{C}/\text{W}$
Power Dissipation	P_d	1.1	W

Note:

- Thermal resistance test board
Size: 76.2mm * 114.3mm * 1.6mm(1S0P)
JEDEC standard: JESD51-3, JESD51-7
- Assume no ambient airflow

Electrical Characteristics

For typical values $T_a=25^{\circ}\text{C}$, $V_{CC}=12\text{V}$ and for min/max values T_a is the operating ambient temperature range with $-25^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $5\text{V} \leq V_{CC} \leq 25.5\text{V}$, unless otherwise specified.

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION (Recommend X7R Capacitor)						
Line Regulation	ΔV_{ref}	$5 \leq V_{CC} \leq 25.5\text{V}$	-	2	25	mV
2.5V Regulation Voltage	V_{25}	-	2.45	2.5	2.55	V
OSCILLATOR SECTION(MAIN)						
Oscillation Frequency	fosc	$T_a = 25^{\circ}\text{C}$, $C_t = 270\text{pF}$ $R_t = 18\text{k}$	108	115	122	kHz
		$C_t = 270\text{pF}$, $R_t = 18\text{k}$	106	115	124	
CT High Voltage	V_{cth}	-	-	2.0	-	V
CT Low Voltage	V_{ctl}	-	-	0.5	-	V
OSCILLATOR SECTION(BURST)						
Oscillation Frequency	foscB	$C_{tb} = 10\text{nF}$, $R_t=18\text{k}$	195	225	255	Hz
BCT High Voltage	V_{bcth}	-	-	2	-	V
BCT Low Voltage	V_{bctl}	-	-	0.5	-	V
ERROR AMP SECTION						
Open Loop Gain		-	-	80	-	dB
Unit Gain Bandwidth		-	-	1.5	-	MHz
Feedback Output High Voltage	V_{eh}	$EA_IN = 0\text{V}$	2.0	2.27	2.54	V
Output Sink Current	I_{sin}	$EA_OUT = 1.5\text{V}$	-	-	-1	mA
Output Source Current	I_{sur}	$EA_OUT = 1.5\text{V}$	1	-	-	mA
EA_IN Driving Current On OLR	I_{olr}	-	75	105	135	μA
EA_IN Driving Current On Burst Dimming	I_{burst}	-	61	85	109	μA
Feedback High Voltage On Burst Dimming	V_{fbh}	$R(EA_IN) = 60\text{k}\Omega$	$V_a+0.1$	$V_a+0.4$	$V_a+0.7$	V
SOFT START SECTION						
Soft Start Current	I_{SS}	$S_S=2\text{V}$	4	6	8	μA
Soft Start Clamping Voltage	V_{ssh}	-	-	5	-	V
PROTECTION SECTION						
Open Lamp Protection Voltage 0	V_{olp0}	Start at open lamp	2.2	2.5	2.8	V
Open Lamp Protection Voltage 1	V_{olp1}	Normal -> open lamp	1.3	1.5	1.7	V
Open Lamp Regulation Voltage	V_{olr}	-	1.75	2	2.25	V
Open Lamp Protection Charging Current	I_{olp}	-	0.7	1.4	2.1	μA
UNDER VOLTAGE LOCK OUT SECTION						
Start Threshold Voltage	V_{th}	-	-	-	5	V
Start Up Current	I_{st}	$V_{CC} = V_{th}-0.2$	-	130	180	μA
Operating Supply Current	I_{op}	$V_{CC} = 12\text{V}$	-	1.5	4	mA
Stand-by Current	I_{sb}	$V_{CC} = 12\text{V}$	-	200	370	μA
ON/OFF SECTION						
On State Input Voltage	V_{on}	-	2	-	5	V
Off Stage Input Voltage	V_{off}	-	-	-	0.7	V

Electrical Characteristics (Continued)

For typical values $T_a=25^{\circ}\text{C}$, $V_{CC}=12\text{V}$ and for min/max values T_a is the operating ambient temperature range with $-25^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$ and $5\text{V} \leq V_{CC} \leq 25.5\text{V}$, unless otherwise specified.

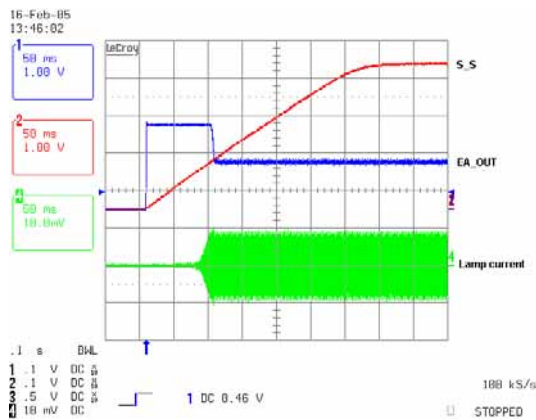
Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT SECTION						
PMOS Gate High Voltage	Vpdhv	$V_{CC} = 12\text{V}$	-	V_{CC}	-	V
PMOS Gate Low Voltage	Vphlv	$V_{CC} = 12\text{V}$	$V_{CC}-10.5$	$V_{CC}-8.5$	$V_{CC}-6.5$	V
NMOS Gate Drive Volgate	Vndhv	$V_{CC} = 12\text{V}$	6.5	8.5	10.5	V
NMOS Gate Drive Volgate	Vndhv	$V_{CC} = 12\text{V}$	-	0	-	V
PMOS Gate Voltage With UVLO Activated	Vpuv	$V_{CC} = V_{th}-0.2$	$V_{CC}-0.3$	-	-	V
NMOS Gate Voltage With UVLO Activated	Vnuv	$V_{CC} = V_{th}-0.2$	-	-	0.3	V
Rising Time	Tr	$V_{CC} = 12\text{V}$, Cload=2nF	-	200	500	ns
Falling Time	Tf	$V_{CC} = 12\text{V}$, Cload=2nF	-	200	500	ns
MAX./MIN OVERLAP						
Min. Overlap between diagonal switches		fosc=100KHz	-	0	-	%
Max. Overlap between diagonal switches		fosc=100KHz	-	100	-	%
DELAY TIME						
PDR_A/NDR_B		Rt=18k	-	450	-	ns
PDR_C/NDR_D		Rt=18k	-	450	-	ns

Function Description

UVLO: The under voltage lockout circuit guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the Vin value. The UVLO circuit turns on the control circuit when Vin exceeds 5V. When Vin is lower than 5V, the IC's standby current is less than 200uA.

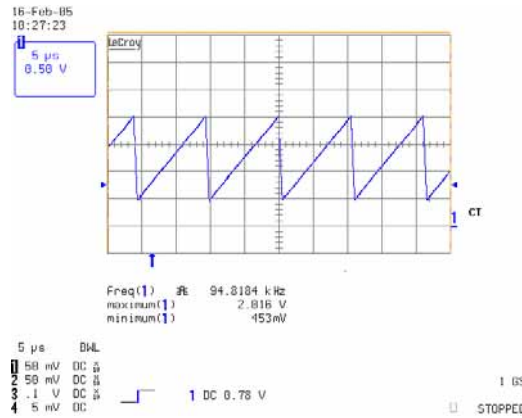
ENA: Applying voltage higher than 2V to the ENA pin enables the operation of the IC. Applying voltage lower than 0.7V to the ENA pin will disable the operation of the inverter.

Soft start: The soft start function requires that the S_S pin is connected through a capacitor to GND. A soft start circuit ensures a gradual increase in the input and output power. The capacitor connected to the S_S pin determines the rate at which the duty ratio rises. It is charged by a 6uA current source.



Main oscillator: The timing capacitors (CTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next, the timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed by adjusting the Rt and CT values. The main frequency can be calculated as shown below.

$$f_{op} = \frac{19}{32 R_T C_T}$$

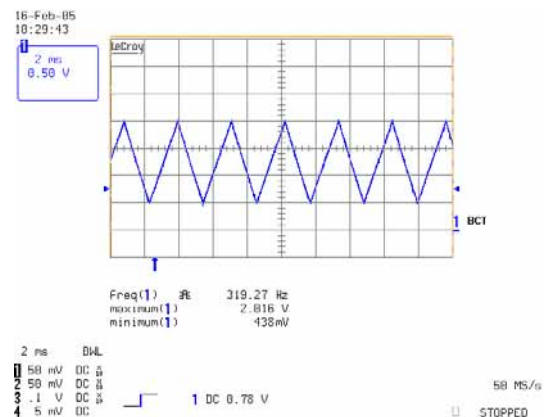


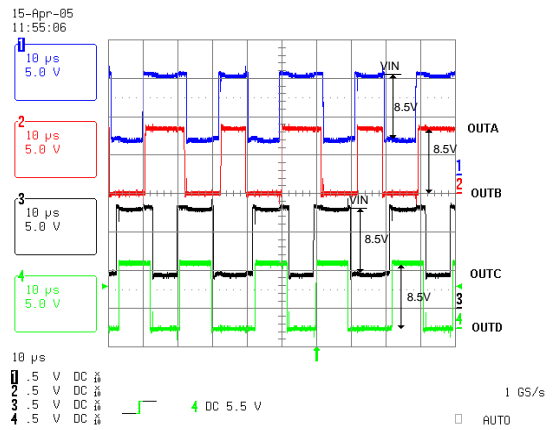
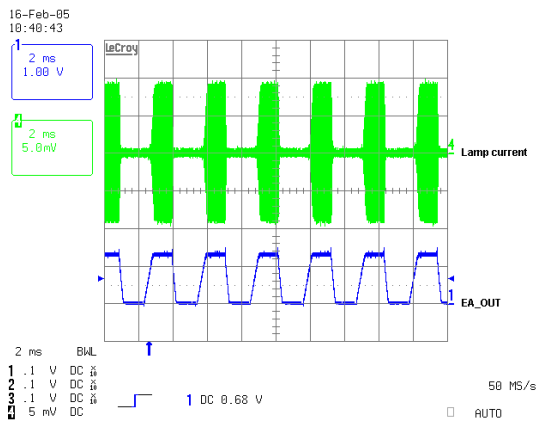
Burst oscillator & burst dimming: The timing capacitors (BCTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next the timing capacitors start charging again and a new switching cycle begins. The burst dimming frequency can be programmed by adjusting the Rt and BCT values. The burst dimming frequency can be calculated as shown below.

$$f_{burst} = \frac{3.75}{64 R_T BCT}$$

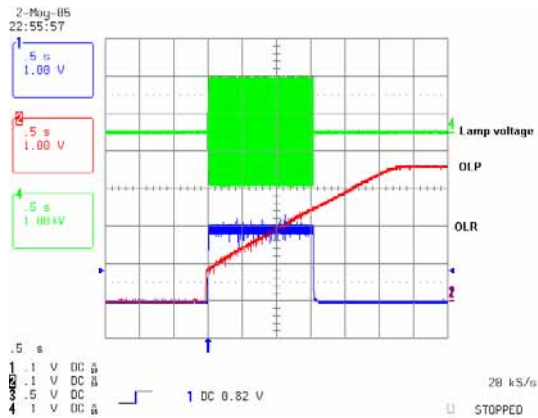
To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.

What does the following sentence mean? Please rewrite. To compare the input of BDIM pin with the 0.5~2V triangular wave of burst oscillator makes the PWM pulse for burst dimming. The PWM pulse controls EA_OUT's voltage by summing 85uA into the EA_IN pin.





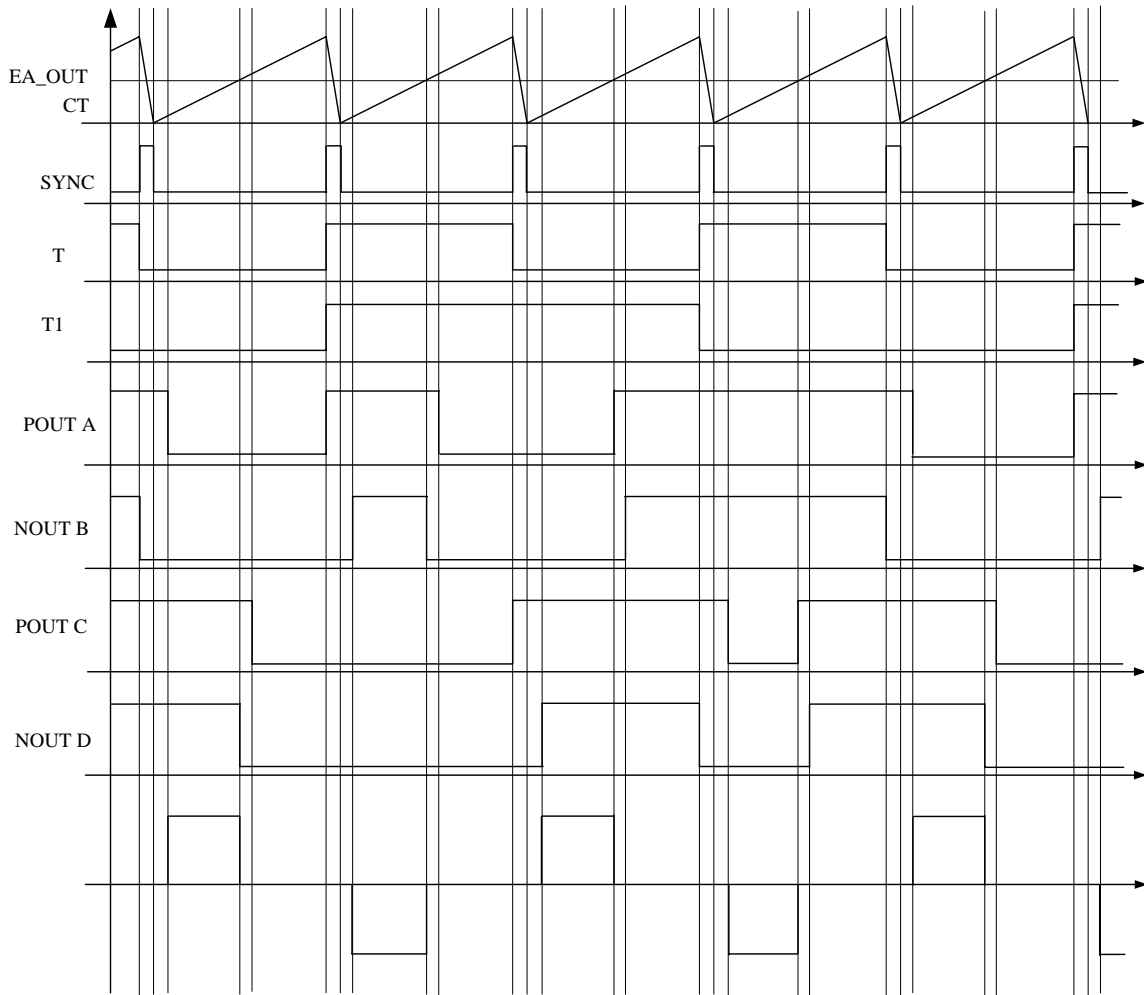
Open lamp regulation & open lamp protection: It is necessary to suspend power stage operation if an open lamp occurs, because the power stage has high gain. When a voltage higher than 2V is applied to the OLR pin, the part enters regulation mode and controls the EA_OUT voltage. This limits the lamp voltage by summing 105uA into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 1.4uA internal current source. Once it reaches 2.5V, the IC enters shut down where all the output is high.



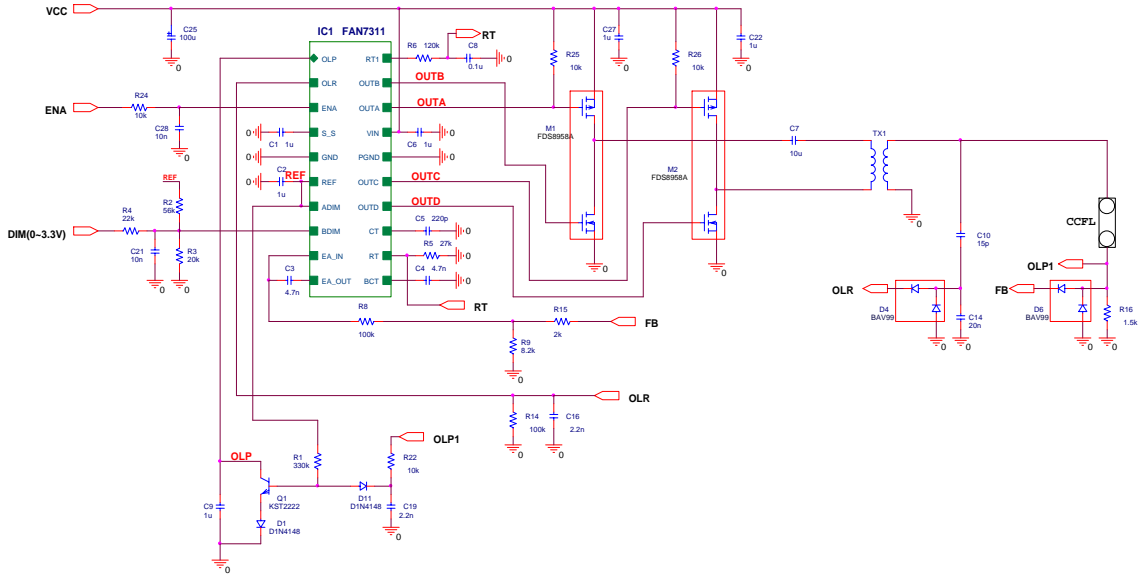
Output Drives: The four output drives are designed so that switches A and B, C and D never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair will drive the other half-bridge.

Timing Diagram

The FAN7311 uses the improved phase-shift control full-bridge to drive CCFL. As a result, the temperature difference between the left and the right leg is almost zero. The detail timing is shown below.



Typical Application Circuits



Ordering Information

Product number	Package	Operating Temperature
FAN7311G	20-SSOP	-25°C ~ 85°C
FAN7311GX		

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT Quiet Series™	ISOPLANAR™	POP™	SuperFET™
ActiveArray™	FAST®	LittleFET™	Power247™	SuperSOT™-3
Bottomless™	FASTr™	MICROCOUPLER™	PowerTrench®	SuperSOT™-6
CoolFET™	FPS™	MicroFET™	QFET®	SuperSOT™-8
CROSSVOLT™	FRFET™	MicroPak™	QST™	SyncFET™
DOME™	GlobalOptoisolator™	MICROWIRE™	QT Optoelectronics™	TinyLogic®
EcoSPARK™	GTO™	MSX™	Quiet Series™	TINYOPTO™
E ² CMOS™	HiSeC™	MSXPro™	RapidConfigure™	TruTranslation™
EnSigna™	I ² C™	OCX™	RapidConnect™	UHC™
FACT™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	UltraFET®
Across the board. Around the world.™	OPTOLOGIC®	SMART START™	SPM™	VCX™
The Power Franchise™	OPTOPLANAR™	Stealth™		
Programmable Active Droop™	PACMAN™			

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- | | |
|---|---|
| <p>1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.</p> | <p>2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.</p> |
|---|---|

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. 17