

FDS6975

Dual P-Channel, Logic Level, PowerTrench™ MOSFET

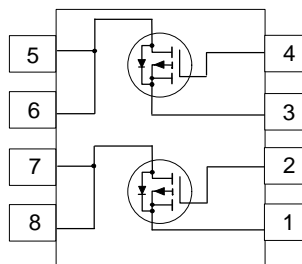
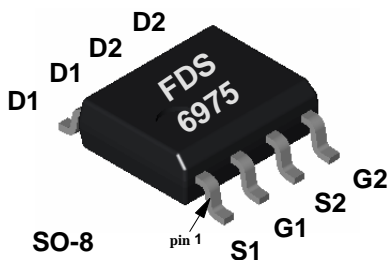
General Description

These P-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- -6 A, -30 V. $R_{DS(ON)} = 0.032 \Omega$ @ $V_{GS} = -10$ V,
 $R_{DS(ON)} = 0.045 \Omega$ @ $V_{GS} = -4.5$ V.
- Low gate charge (14.5nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

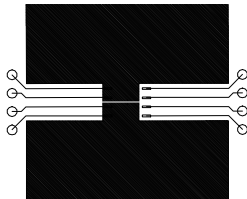
Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	-6	A
	- Pulsed	-20	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

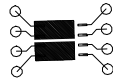
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-30			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = -250 μA, Referenced to 25 °C		-21		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μA
		T _J = 55°C			-10	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-1	-1.7	-3	V
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C		4		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -6 A		0.025	0.032	Ω
		T _J = 125°C		0.033	0.051	
		V _{GS} = -4.5 V, I _D = -5 A		0.034	0.045	
I _{D(on)}	On-State Drain Current	V _{GS} = -10 V, V _{DS} = -5 V	-20			A
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -6 A		16		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz		1540		pF
C _{oss}	Output Capacitance			400		pF
C _{rss}	Reverse Transfer Capacitance			170		pF
SWITCHING CHARACTERISTICS (Note 2)						
t _{D(on)}	Turn - On Delay Time	V _{DS} = -15 V, I _D = -1 A		13	24	ns
t _r	Turn - On Rise Time	V _{GEN} = -10 V, R _{GEN} = 6 Ω		22	35	ns
t _{D(off)}	Turn - Off Delay Time			47	75	ns
t _f	Turn - Off Fall Time			18	30	ns
Q _g	Total Gate Charge	V _{DS} = -10 V, I _D = -6 A,		14.5	20	nC
Q _{gs}	Gate-Source Charge	V _{GS} = -5 V		4		nC
Q _{gd}	Gate-Drain Charge			5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -1.3 A (Note 2)		-0.73	-1.2	V

Notes:

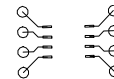
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

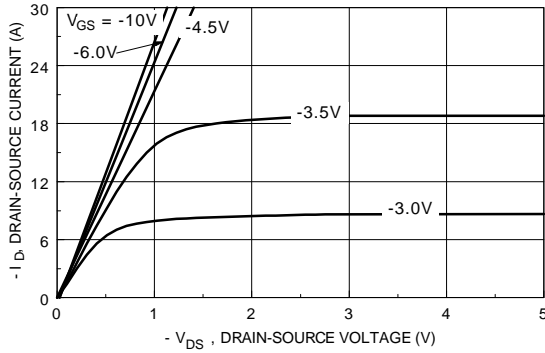


Figure 1. On-Region Characteristics.

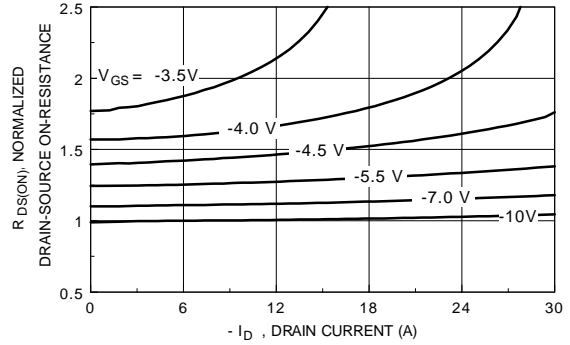


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

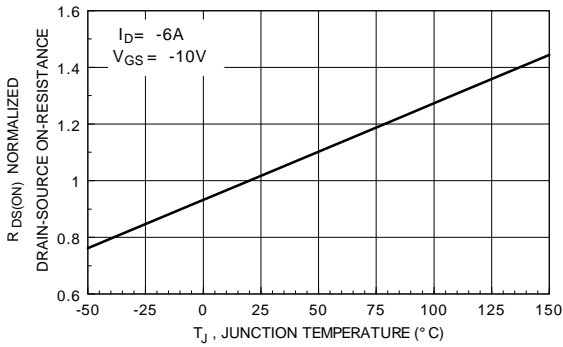


Figure 3. On-Resistance Variation with Temperature.

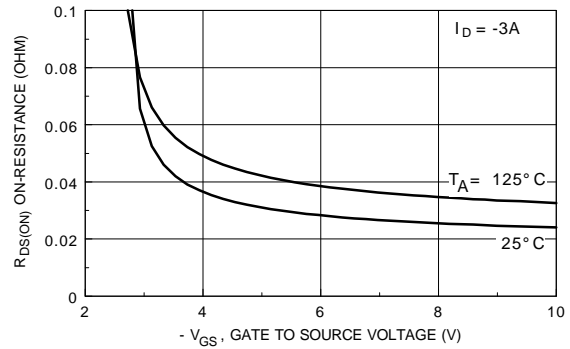


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

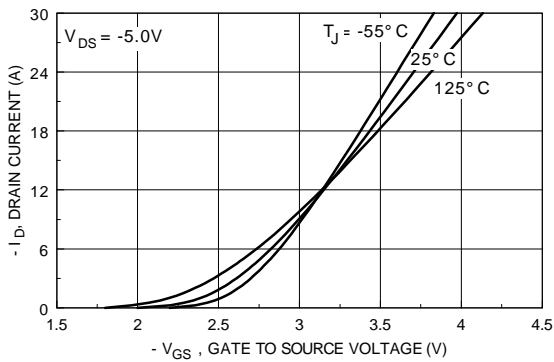


Figure 5. Transfer Characteristics.

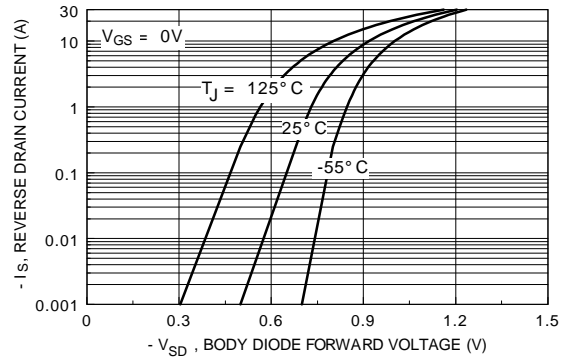


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

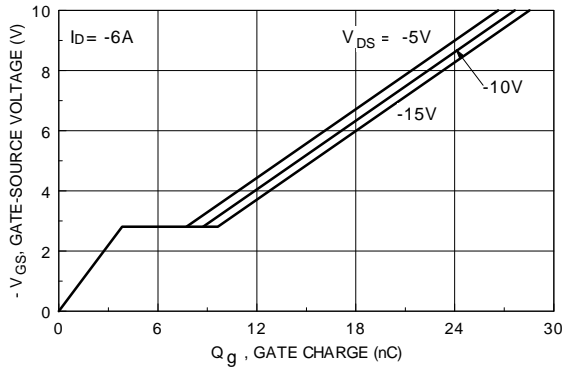


Figure 7. Gate Charge Characteristics.

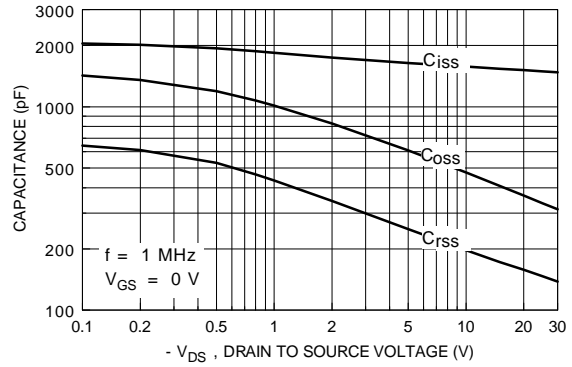


Figure 8. Capacitance Characteristics.

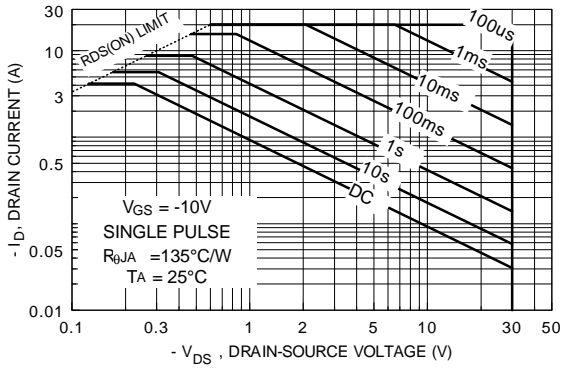


Figure 9. Maximum Safe Operating Area.

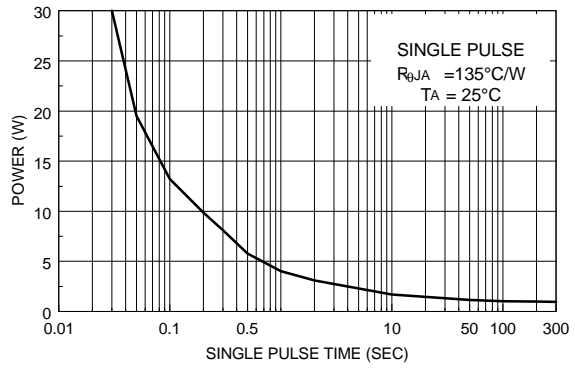


Figure 10. Single Pulse Maximum Power Dissipation.

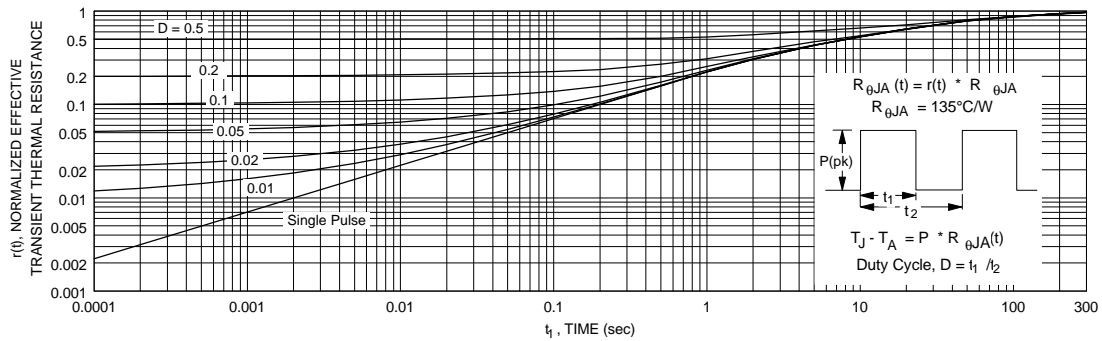


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

SO-8 Tape and Reel Data and Package Dimensions



SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

F63TNR Label sample



SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0



Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7\"/>								
12mm	13\"/>								

SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MINIMUM
LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	ISOPANAR™	TinyLogic™
CoolFET™	MICROWIRE™	UHC™
CROSSVOLT™	POP™	VCX™
E ² CMOS™	PowerTrench™	
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	
HiSeC™	SuperSOT™-8	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.