GENNUM

# GS4901B/GS4900B
# SD Clock and Timing Generator with GENLOCK

**GS4901B/GS4900B Preliminary Data Sheet**

## Key Features

### Video Clock Synthesis

- Pre-programmed for 4 video clock periods (14.32 MHz, 27 MHz, 36 MHz, and 54 MHz)
- Accuracy of free-running clock frequency limited only by crystal reference
- One differential and two single-ended video clock outputs
- Each clock may be individually delayed for skew control
- Video output clock may be directly connected to Gennum's serializers for a SMPTE-compliant SDI output

### Audio Clock Synthesis (GS4901B only)

- Three audio clock outputs
- Generates any audio clock up to 512*96kHz
- Pre-programmed for 7 audio clocks

### Timing Generation

- Generates up to 8 timing signals at a time
- Choose from 9 pre-programmed timing signals: H and V sync and blanking, F Sync, F Digital, AFS (GS4901B only), Display Enable, 10FID, and up to 4 user-defined timing signals
- Pre-programmed to generate timing for 9 different video formats

### Genlock Capability

- Clocks may be free-running or genlocked to an input reference with a variable offset step size of 100-200ps (depending on exact clock frequency)
- Variable timing offset step size of 100-200ps up to one frame
- Output may be cross-locked to a different input reference
- Freeze operation on loss of reference
- Optional crash or drift lock on application of reference
- Automatic input format detection

### General Features

- Reduces design complexity and saves board space - 9mm x 9mm package plus crystal reference replaces multiple VCXOs, PLLs and timing generators
- Pb-free and RoHS Compliant
- Low power operation typically 300mW
- 1.8V core and 1.8V or 3.3V I/O power supplies
- 64-PIN QFN package

### Applications

- Video cameras; Digital audio and/or video recording/play back devices; Digital audio and/or video processing devices; Computer/video displays; DVD/MPEG devices; Digital Set top boxes; Video projectors; High definition video systems; Multi-media PC applications

## Description

The GS4901B is a highly flexible, digitally controlled clock synthesis circuit and timing generator with genlock capability. It can be used to generate video and audio clocks and timing signals, and allows multiple devices to be genlocked to an input reference.

The GS4900B includes all the features of the GS4901B, but does not offer audio clocks or AFS pulse generation.

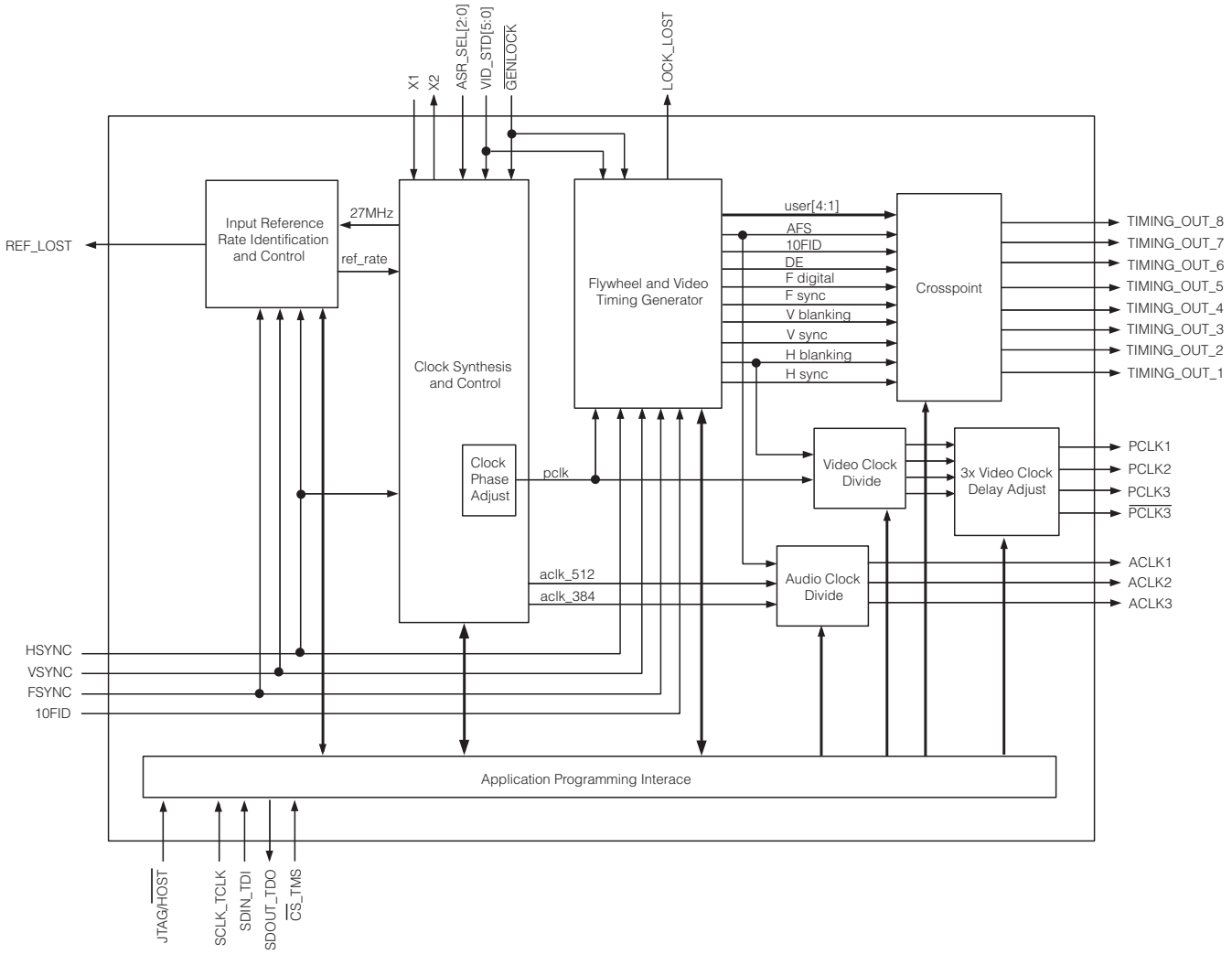
The GS4901B/GS4900B will recognize input reference signals conforming to 36 different video standards, and will genlock the output timing information to the incoming reference. The GS4901B/GS4900B supports cross-locking, allowing the output to be genlocked to an incoming reference that is different from the output video standard selected.

The user may select to output one of 4 different video sample clock rates. The chosen clock frequency can be further divided using internal dividers, and is available on two video clock outputs and one LVDS video clock output pair. The video clocks are frequency and phased-locked to the horizontal timing reference, and can be individually delayed with respect to the timing outputs for clock skew control.

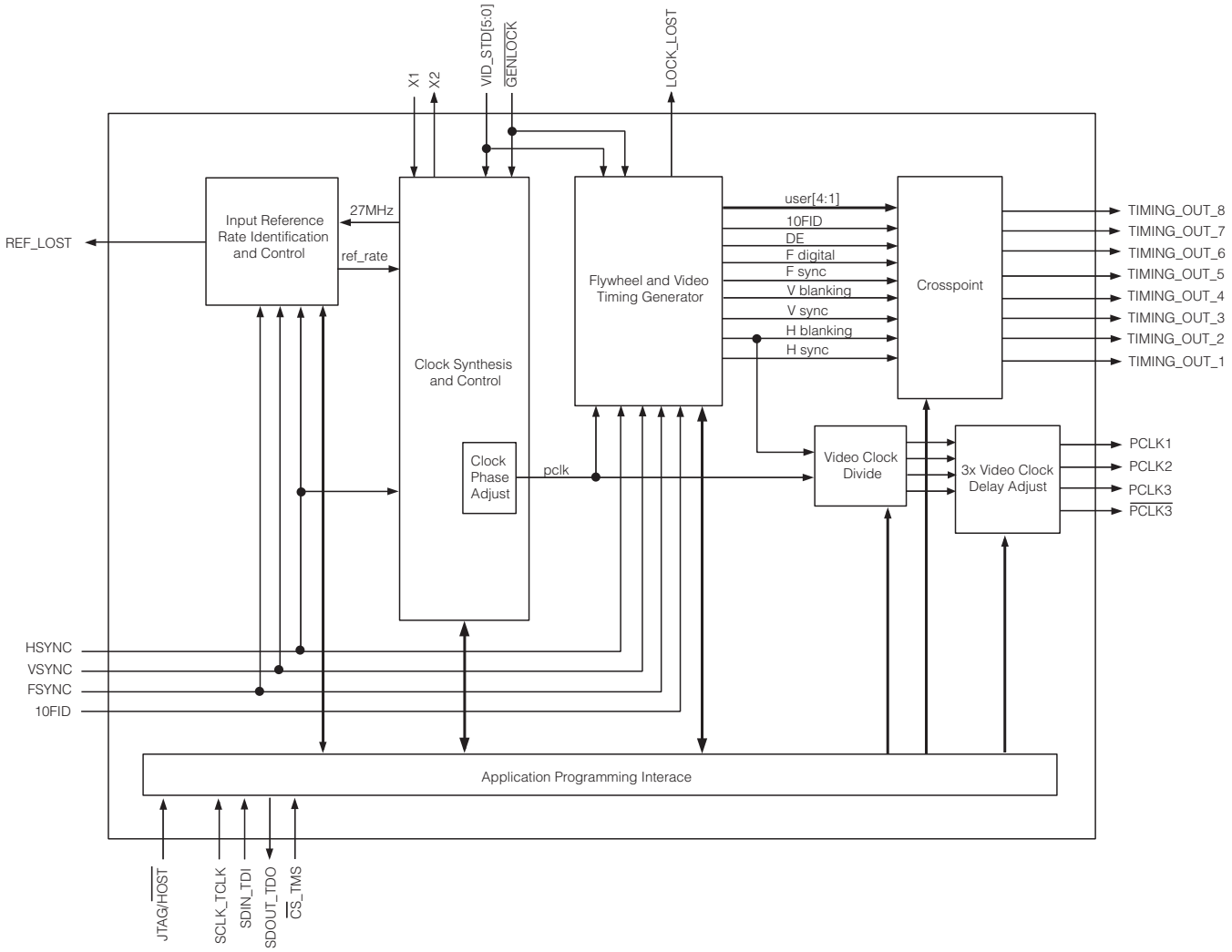
Eight user-selectable timing outputs are provided that can automatically produce the following timing signals for 9 different video formats: HSync, Hblanking, VSync, Vblanking, F sync, F digital, AFS (GS4901B only), DE, and 10FID. These timing outputs may be locked to the input reference signal for genlock timing and may be phase adjusted via internal registers.

In addition, the GS4901B provides three audio sample clock outputs that can produce audio clocks up to 512fs with fs ranging from 9.7kHz to 96kHz. Audio to video phasing is accomplished by an external 10FID input reference, a 10FID signal specified via internal registers, or a user-programmed audio frame sequence.

The GS4901B/GS4900B is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS Compliant).




**GS4901B Functional Block Diagram**




**GS4900B Functional Block Diagram**

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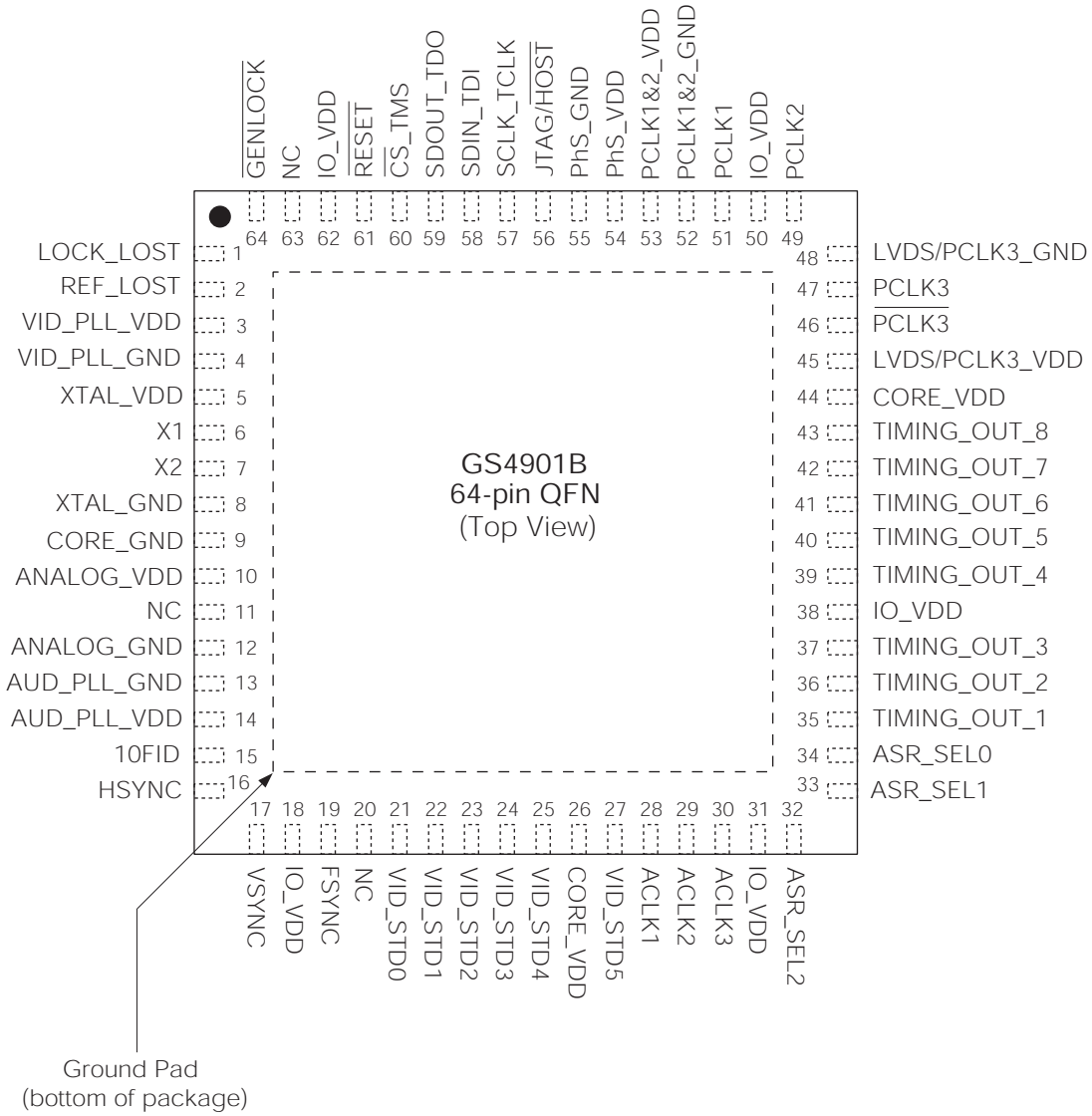
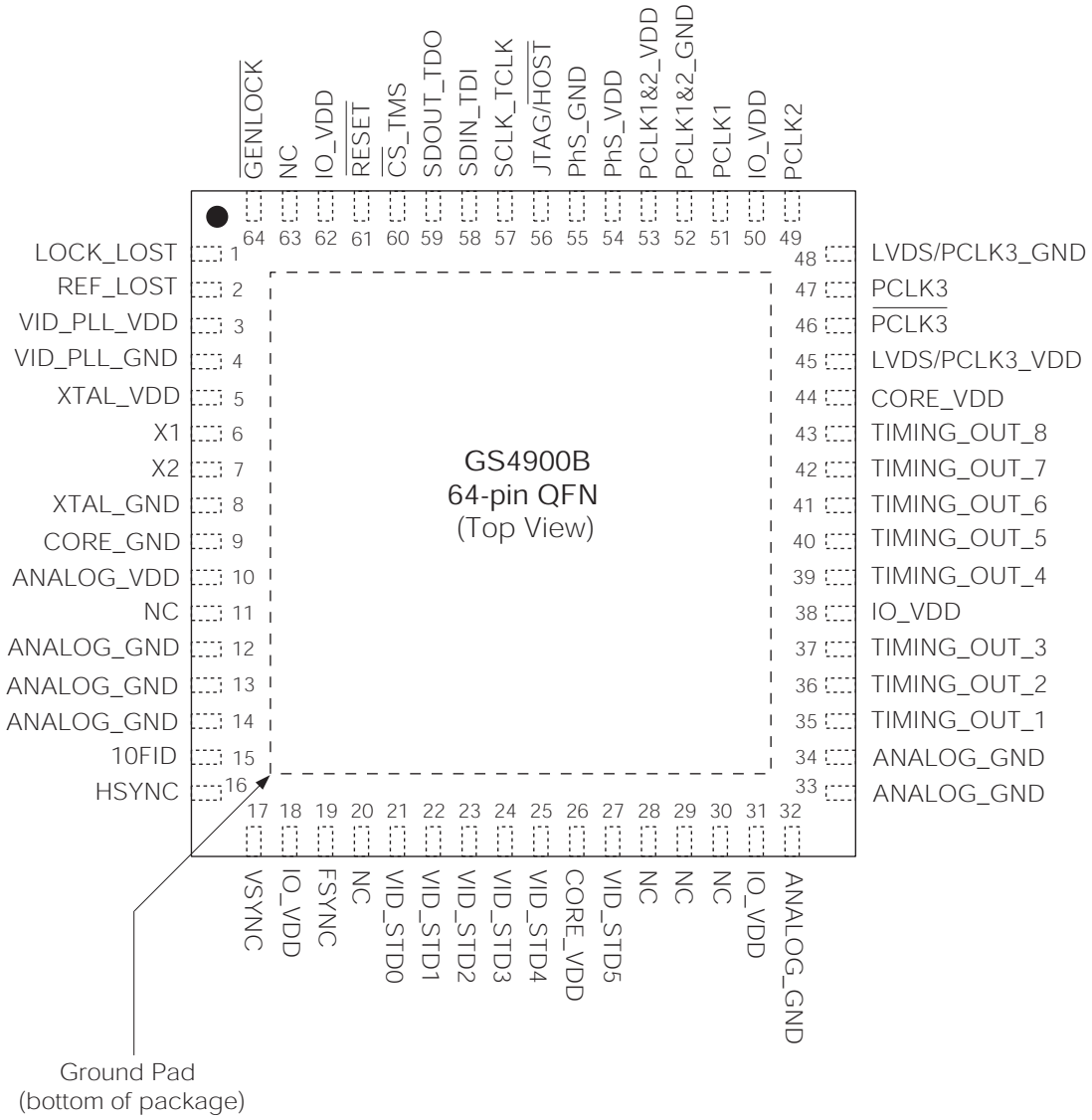
# 1. Pin Out

## 1.1 GS4901B Pin Assignment



## 1.2 GS4900B Pin Assignment



# 1.3 Pin Descriptions

**Table 1-1: Pin Descriptions**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 1 | LOCK_LOST | Non Synchronous | Output | STATUS SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>This pin will be HIGH if the output is not genlocked to the input.<br>The GS4901B/GS4900B monitors the output pixel/line counters, as well as the internal lock status from the genlock block and asserts LOCK_LOST HIGH if it is determined that the output is not genlocked to the input. This pin will be LOW if the device successfully genlocks the output clock and timing signals to the input reference.<br>If LOCK_LOST is LOW, the reference timing generator outputs will be phase locked to the detected reference signal, producing an output in accordance with the video standard selected by the VID_STD[5:0] pins. |
| 2 | REF_LOST | Non Synchronous | Output | STATUS SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>This pin will be HIGH if:<br>• No input reference signal is applied to the device; or<br>• The input reference applied does not meet the minimum/maximum timing requirements described in Section 3.5.2 on page 43.<br>This pin will be LOW otherwise.<br>If the reference signal is removed when the device is in Genlock mode, REF_LOST will go HIGH and the GS4901B/GS4900B will enter Freeze mode (see Section 3.2.1.2 on page 38). |
| 3 | VID_PLL_VDD | – | Power Supply | Most positive power supply connection for the video clock synthesis internal block. Connect to +1.8V DC. |
| 4 | VID_PLL_GND | – | Power Supply | Ground connection for the video clock synthesis internal block. Connect to GND. |
| 5 | XTAL_VDD | – | Power Supply | Most positive power supply connection for the crystal buffer. Connect to either +1.8V DC or +3.3V DC.<br>NOTE: Connect to +3.3V for minimum output PCLK jitter. |
| 6 | X1 | Non Synchronous | Input | ANALOG SIGNAL INPUT<br>Connect to a 27MHz crystal or a 27MHz external clock source. See Figure 1-1. |
| 7 | X2 | Non Synchronous | Output | ANALOG SIGNAL OUTPUT<br>Connect to a 27MHz crystal, or leave this pin open circuit if an external clock source is applied to pin 6. See Figure 1-1. |
| 8 | XTAL_GND | – | Power Supply | Ground connection for the crystal buffer. Connect to GND. |
| 9 | CORE_GND | – | Power Supply | Ground connection for core and I/O. Solder to the ground plane of the application board.<br>NOTE: The CORE_GND pin should be soldered to the same main ground plane as the exposed ground pad on the bottom of the device. |
| 10 | ANALOG_VDD | – | Power Supply | Most positive power supply connection for the analog input block. Connect to +1.8V DC. |
| 11, 20, 63 | NC | – | – | Do not connect. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 12 | ANALOG_GND | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 13 | AUD_PLL_GND (GS4901B only) | – | Power Supply | Ground connection for the audio clock synthesis internal block. Connect to GND. |
| | ANALOG_GND (GS4900B only) | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 14 | AUD_PLL_VDD (GS4901B only) | – | Power Supply | Most positive power supply connection for the audio clock synthesis internal block. Connect to +1.8V DC. |
| | ANALOG_GND (GS4900B only) | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 15 | 10FID | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The 10FID external reference signal is applied to this pin by the application layer. 10FID defines the field in which the video and audio clock phase relationship is defined according to SMPTE 318-M. It is also used to define a 3:2 video cadence.<br>NOTE: If the input reference format does not include a 10 Field ID signal, this pin should be held LOW. See Section 3.4.2 on page 41. |
| 16 | HSYNC | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The HSYNC external reference signal is applied to this pin by the application layer. When the GS4901B/GS4900B is operating in Genlock mode, the device senses the polarity of the HSYNC input automatically, and references to the leading edge.<br>This signal must adhere to one of the 36 defined video standards supported by the device. In this mode of operation, the HSYNC input provides a horizontal scanning reference signal.<br>The HSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 20 describes the 36 video formats recognized by the GS4901B/GS4900B. |
| 17 | VSYNC | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The VSYNC external reference signal is applied to this pin by the application layer. When the GS4901B/GS4900B is operating in Genlock mode, the device senses the polarity of the VSYNC input automatically, and references to the leading edge.<br>This signal must adhere to one of the 36 defined video standards supported by the device. In this mode of operation, the VSYNC input provides a vertical scanning reference signal.<br>The VSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 20 describes the 36 video formats recognized by the GS4901B/GS4900B. |
| 18, 31, 38, 50, 62 | IO_VDD | – | Power Supply | Most positive power supply connection for the digital I/O signals. Connect to either +1.8V DC or +3.3V DC.<br>NOTE: All five IO_VDD pins must be powered by the same voltage. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 19 | FSYNC | Non Synchronous | Input | REFERENCE SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>The FSYNC external reference signal is applied to this pin by the application layer.<br>The first field is defined as the field in which the first broad pulse (also known as serration) is in the first half of a line. The FSYNC signal should be set HIGH during the first field for sync-based references.<br>Then this signal must adhere to one of the 36 defined video standards supported by the device. In this mode of operation, the FSYNC input provides an odd/even field input reference.<br>The FSYNC signal may have analog timing, such as from a sync separator, or may be digital such as from an SDI deserializer. Section 1.4 on page 20 describes the 36 video formats recognized by the GS4901B/GS4900B.<br>For blanking-based references, the FSYNC signal should be set HIGH during the second field.<br>NOTE: If the input reference format does not include an F sync signal, this pin should be held LOW. |
| 27, 25, 24, 23, 22, 21 | VID_STD[5:0] | Non Synchronous | Input | CONTROL SIGNAL INPUTS<br>Signal levels are LVCMOS/LVTTL compatible.<br>Video Standard Select.<br>Used to select the desired video format for video clock and timing signal generation.<br>4 different video sample clocks, as well as 9 different video format timing signal outputs may be selected using these pins.<br>NOTE: The VID_STD[5:4] pins should be grounded by the application layer since these pins are not required to select output video standards 1 to 10.<br>For details on the supported video standards and video clock frequency selection, please see Section 1.4 on page 20. |
| 26, 44 | CORE_VDD | – | Power Supply | Most positive power supply connection for the digital core. Connect to +1.8V DC. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 28, 29, 30 | ACLK1<br>ACLK2<br>ACLK3<br>(GS4901B only) | – | Output | CLOCK SIGNAL OUTPUTS<br>Signal levels are LVCMOS/LVTTL compatible.<br>Audio output clock signals.<br>ACLK1, ACLK2, and ACLK3 present audio sample rate clock outputs to the application layer.<br>By default, after system reset, the audio clock output pins of the device provide clock signals as follows:<br>ACLK1 = 256fs<br>ACLK2 = 64fs<br>ACLK3 = fs, where fs is the fundamental sampling frequency.<br>The fundamental sampling frequency is selected using ASR_SEL[2:0]. Additional sampling frequencies may be programmed in the host interface.<br>It is also possible to select different division ratios for each of the audio clock outputs by programming designated registers in the host interface. Clock outputs of 512fs, 384fs, 256fs, 192fs, 128fs, 64fs, fs and z bit are selectable on a pin-by-pin basis.<br>NOTE: ACLK1-3 will have a 50% duty cycle, unless fs is selected as 96kHz and the host interface is configured such that one of the three ACLK pins is set to output a clock signal at 192fs or 384fs. If this is the case, then a 512fs clock will have a 33% duty cycle.<br>These signals will be high impedance when ASR_SEL[2:0] = 000b. |
| | NC<br>(GS4900B only) | – | – | Do not connect. |
| 32, 33, 34 | ASR_SEL[2:0]<br>(GS4901B only) | Non Synchronous | Input | CONTROL SIGNAL INPUTS<br>Signal levels are LVCMOS/LVTTL compatible.<br>Audio Sample Rate Select.<br>Used to select the fundamental sampling frequency, fs, of the audio clock outputs. See Table 3-7.<br>When ASR_SEL[2:0] = 000b, audio clock generation will be disabled and the ACLK1 to ACLK3 pins will be high impedance. In this case, AUD_PLL_VDD (pin 14) may be connected to GND to minimize noise and power consumption. |
| | ANALOG_GND<br>(GS4900B only) | – | Power Supply | Ground connection for the analog input block. Connect to GND. |
| 35 | TIMING_OUT_1 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is H Sync.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 36 | TIMING_OUT_2 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is H blanking.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 37 | TIMING_OUT_3 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is V Sync.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 39 | TIMING_OUT_4 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is V blanking.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 40 | TIMING_OUT_5 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is F Sync.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 41 | TIMING_OUT_6 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is F digital.<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 42 | TIMING_OUT_7 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is 10 Field ID (10FID).<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 43 | TIMING_OUT_8 | Synchronous with PCLK1 ~ PCLK3 | Output | TIMING SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selectable timing output.<br>Selectable from: H sync; H blanking; V sync; V blanking; F sync; F digital; Display Enable; 10 field ID (film cadence); AFS video/audio timing (GS4901B only); USER_1~4.<br>See Section 1.5 on page 24 for signal descriptions.<br>NOTE: Default output is Display Enable (DE).<br>The current drive capability of this pin may be set high or low via designated registers in the host interface. By default, the current drive will be low.<br>This signal will be high impedance when VID_STD[5:0] = 00h. |
| 45 | LVDS/PCLK3_VDD | – | Power Supply | Most positive power supply connection for PCLK3 output circuitry and LVDS driver. Connect to +1.8V DC. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 46, 47 | $\overline{\text{PCLK3}}$, PCLK3 | – | Output | CLOCK SIGNAL OUTPUTS<br>Signal levels are LVDS compatible.<br>Differential video clock output signal.<br>PCLK3/$\overline{\text{PCLK3}}$ present a differential video sample rate clock output to the application layer.<br>By default, after system reset, this output will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface.<br>It is also possible to select different division ratios for the PCLK3/$\overline{\text{PCLK3}}$ outputs by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected.<br>The PCLK3/$\overline{\text{PCLK3}}$ outputs will be high impedance when VID_STD[5:0] = 00h. |
| 48 | LVDS/PCLK3_GND | – | Power Supply | Ground connection for PCLK3 output circuitry and LVDS driver. Connect to GND. |
| 49 | PCLK2 | – | Output | CLOCK SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Video clock output signal.<br>PCLK2 presents a video sample rate clock output to the application layer.<br>By default, after system reset, the PCLK2 output pin will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface.<br>It is also possible to select different division ratios for the PCLK2 output by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected.<br>By setting designated registers in the host interface, the current drive capability of this pin may be set high or low. By default, the current drive will be low.<br>The PCLK2 output will be held LOW when VID_STD[5:0] = 00h. |

**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 51 | PCLK1 | – | Output | CLOCK SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Video clock output signal.<br>PCLK1 presents a video sample rate clock output to the application layer.<br>By default, after system reset, the PCLK1 output pin will operate at the fundamental frequency determined by the setting of the VID_STD[5:0] pins. It is possible to define other non-standard fundamental clock rates using the host interface.<br>It is also possible to select different division ratios for the PCLK1 output by programming designated registers in the host interface. A clock output of the fundamental rate, fundamental rate ÷2, or fundamental rate ÷4 may be selected.<br>By setting designated registers in the host interface, the current drive capability of this pin may be set high or low. By default, the current drive will be low.<br>The PCLK1 output will be held LOW when VID_STD[5:0] = 00h. |
| 52 | PCLK1&2_GND | – | Power Supply | Ground connection for PCLK1&2 circuitry. Connect to GND. |
| 53 | PCLK1&2_VDD | – | Power Supply | Most positive power supply connection for PCLK1&2 circuitry. Connect to +1.8V DC. |
| 54 | PhS_VDD | – | Power Supply | Most positive power supply connection for the video clock phase shift internal block. Connect to +1.8V DC. |
| 55 | PhS_GND | – | Power Supply | Ground connection for the video clock phase shift internal block. Connect to GND. |
| 56 | JTAG/$\overline{\text{HOST}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to select JTAG Test Mode or Host Interface Mode.<br>When set HIGH, $\overline{\text{CS}}$_TMS, SCLK_TCLK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing.<br>When set LOW, $\overline{\text{CS}}$_TMS, SCLK_TCLK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation. |
| 57 | SCLK_TCLK | Non Synchronous | Input | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Clock / Test Clock.<br>All JTAG / Host Interface address and data are shifted into/out of the device synchronously with this clock.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>SCLK_TCLK operates as the host interface serial data clock, SCLK.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>SCLK_TCLK operates as the JTAG test clock, TCLK. |

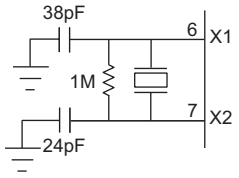
**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 58 | SDIN_TDI | Synchronous with SCLK_TCLK | Input | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Input / Test Data Input.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>SDIN_TDI operates as the JTAG test data input, TDI. |
| 59 | SDOUT_TDO | Synchronous with SCLK_TCLK | Output | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Output / Test Data Output.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>SDOUT_TDO operates as the JTAG test data output, TDO. |
| 60 | $\overline{\text{CS}}$_TMS | Synchronous with SCLK_TCLK | Input | SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Chip Select / Test Mode Select.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>$\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>$\overline{\text{CS}}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH. |
| 61 | $\overline{\text{RESET}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to reset the internal operating conditions to their default settings or to reset the JTAG test sequence.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW):<br>When asserted LOW, all host registers and functional blocks will be set to their default conditions. All input and output signals will become high impedance, except PCLK1 and PCLK2, which will be set LOW.<br>When set HIGH, normal operation of the device will resume.<br>The user must hold this pin LOW during power-up and for a minimum of 500 uS after the last supply has reached its operating voltage.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH):<br>When asserted LOW, all host registers and functional blocks will be set to their default conditions and the JTAG test sequence will be held in reset.<br>When set HIGH, normal operation of the JTAG test sequence will resume. |

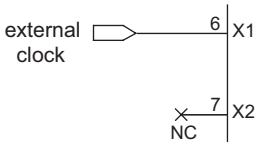
**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 64 | $\overline{\text{GENLOCK}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Selects Genlock mode or Free Run mode.<br>When this pin is set LOW and the device has successfully genlocked the output to the input reference, the device will enter Genlock mode. The video clock and timing outputs will be frequency and phase locked to the detected reference signal.<br>When this pin is set HIGH, the video clock and the reference-timing generator will free-run.<br>By default, the GS4901B's audio clocks will be genlocked to the output video clock regardless of the setting of this pin.<br>NOTE: The user must apply a reference to the input of the device prior to setting $\overline{\text{GENLOCK}}$ = LOW. If the $\overline{\text{GENLOCK}}$ pin is set LOW and no reference signal is present, the generated clock and timing outputs of the device may correspond to the internal default settings of the chip until a reference is applied. |
| – | Ground Pad | – | – | Ground pad on bottom of package must be soldered to main ground plane of PCB. |

External Crystal Connection




External Clock Source Connection




Notes:

1. Capacitor values listed represent the total capacitance, including discrete capacitance and parasitic board capacitance.

2. X1 serves as an input, which may alternatively accept a 27MHz clock source. To accomodate this, mismatched capacitor values are recommended.

**Figure 1-1: XTAL1 and XTAL2 Reference Circuits**

## 1.4 Pre-Programmed Recognized Video Standards

Table 1-2 describes the video standards recognized by the GS4901B/GS4900B. The device will automatically recognize VID_STD[5:0] = 1 to 10. In order to enable the device to recognize and lock to any of the HD reference formats defined by VID_STD[5:0] = 11 to 38, the user must set the corresponding bit LOW in the Reference_Standard_Disable register, located at address 11h-13h of the host interface. In addition, the user must set the HD_Reference_Enable bit of register 82h[7] HIGH.

Please see the descriptions of the Reference_Standard_Disable and HD_Reference_Enable registers in Section 3.10.3 on page 66.

If an HD reference format is left disabled in the Reference_Standard_Disable register, or if the HD_Reference_Enable bit is not set HIGH in register 82h, the device will NOT recognize this format should it be applied to the input of the device.

**The user may select VID_STD[5:0] = 1 or 3-10 ONLY as output formats.**

If desired, the external VID_STD[5:0] pins may be ignored by setting bit 1 of the Video_Control register, and the video standard may instead be selected via the VID_STD[5:0] register of the host interface (see Section 3.10.3 on page 66). Although the external VID_STD[5:0] pins will be ignored in this case, they should not be left floating.

NOTE: VID_STD[5:4] should always be set LOW by the application layer since these pins are not required to select output video standards 1 to 10.

**Table 1-2: Recognized Video Standards**

| VID_STD [5:0] | System Nomenclature | Video PCLK Frequency (MHz) | PCLKS / Total Line | Total Lines / Frame | PCLKS / Active Line | H Sync Width (Clocks) | H Sync Polarity | V Sync Width (Lines) | V Sync Polarity | Active Lines / Frame | Scan Format Standard |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | PCLK1&2 =LOW. PCLK3/PCLK3 = High Impedance | – | – | – | – | – | – | – | – | – | – |
| 1 | 4fsc 525 / 2:1 interlace | 14.32 | 910 | 525 | 768 | 67 | negative | 3 | negative | 486 | SMPTE 244M |
| 2* | Composite PAL 625 / 2:1 interlace / 25 | – | – | 625 | – | – | negative | 2.5 | negative | 576 | – |
| 3 | 601 525 / 2:1 interlace | 27 | 1716 | 525 | 1440 | 127 | negative | 3 | negative | 486 | SMPTE 125M/267M |
| 4‡ | 601 625 / 2:1 interlace | 27 | 1728 | 625 | 1440 | 127 | negative | 2.5 | negative | 576 | ITU-R BT.601-5 |
| 5 | 601 – 18MHz 525 / 2:1 interlace | 36 | 2288 | 525 | 1920 | 169 | negative | 3 | negative | 486 | SMPTE 267M |
| 6‡ | 601 – 18 MHz 625 / 2:1 interlace | 36 | 2304 | 625 | 1920 | 169 | negative | 2.5 | negative | 576 | ITU-R BT.601-5 |
| 7 | 720x486/59.94/2:1 interlace | 54 | 3432 | 525 | 2880 | 252 | negative | 3 | negative | 486 | SMPTE RP174 / SMPTE 347M |
| 8‡ | 720x576/50/2:1 interlace | 54 | 3456 | 625 | 2880 | 252 | negative | 2.5 | negative | 576 | ITU-R BT.799 / SMPTE 347M |
| 9 | 720x483/59.94/1:1 progressive | 54 | 1716 | 525 | 1440 | 127 | negative | 6 | negative | 483 | SMPTE 293M / SMPTE 347M |
| 10 | 720x576/50/1:1 progressive | 54 | 1728 | 625 | 1440 | 127 | negative | 5 | negative | 576 | ITU-R BT.1358 / SMPTE 347M |
| 11* | 1280x720/60/1:1 progressive | 74.25 | 1650 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 12* | 1280x720/59.94/1:1 progressive | 74.175 | 1650 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 13* | 1280/720/50/1:1 progressive | 74.25 | 1980 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |

**Table 1-2: Recognized Video Standards (Continued)**

| VID_STD [5:0] | System Nomenclature | Video PCLK Frequency (MHz) | PCLKS / Total Line | Total Lines / Frame | PCLKS / Active Line | H Sync Width (Clocks) | H Sync Polarity | V Sync Width (Lines) | V Sync Polarity | Active Lines / Frame | Scan Format Standard |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 14* | 1280x720/30/1:1 progressive | 74.25 | 3300 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 15* | 1280x720/29.97/1:1 progressive | 74.175 | 3300 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 16* | 1280x720/25/1:1 progressive | 74.25 | 3960 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 17* | 1280x720/24/1:1 progressive | 74.25 | 4125 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 18* | 1280x720/23.98/1:1 progressive | 74.175 | 4125 | 750 | 1280 | 80 | tri | 5 | negative | 720 | SMPTE 296M |
| 19* | 1920x1035/60/2:1 interlace | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1035 | SMPTE 260M |
| 20* | 1920x1035/59.94/2:1 interlace | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1035 | SMPTE 260M |
| 21* | 1920x1080/60/1:1 progressive | 148.5 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 22* | 1920x1080/59.94/1:1 progressive | 148.35 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 23* | 1920x1080/50/1:1 progressive | 148.5 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 24* | Reserved | – | – | – | – | – | – | – | – | – | – |
| 25* | 1920x1080/60/2:1 interlace | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 26* | 1920x1080/59.94/2:1 interlace | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 27* | 1920x1080/50/2:1 interlace | 74.25 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 28* | Reserved | – | – | – | – | – | – | – | – | – | – |

**Table 1-2: Recognized Video Standards (Continued)**

| VID_STD [5:0] | System Nomenclature | Video PCLK Frequency (MHz) | PCLKS / Total Line | Total Lines / Frame | PCLKS / Active Line | H Sync Width (Clocks) | H Sync Polarity | V Sync Width (Lines) | V Sync Polarity | Active Lines / Frame | Scan Format Standard |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 29* | 1920x1080/30/1:1 progressive | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 30* | 1920x1080/30/PsF | 74.25 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 31* | 1920x1080/29.97/1:1 progressive | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 32* | 1920x1080/29.97/PsF | 74.175 | 2200 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 33* | 1920x1080/25/1:1 progressive | 74.25 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 34* | 1920x1080/25/PsF | 74.25 | 2640 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 35* | 1920x1080/24/1:1 progressive | 74.25 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 36* | 1920x1080/24/PsF | 74.25 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |
| 37* | 1920x1080/23.98/1:1 progressive | 74.175 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE 274M |
| 38* | 1920x1080/23.98/PsF | 74.175 | 2750 | 1125 | 1920 | 80 | tri | 5 | negative | 1080 | SMPTE RP 211 |

* VID_STD[5:0] = 2 and 11-38 are recognized as input references only. In addition, VID_STD[5:0] = 11-38 must be enabled in the Reference_Standard_Disable register and the HD_Reference_Enable bit of register 82h[7] must be set HIGH before they will be recognized by the device.

‡ When VID_STD = 4, 6, or 8, the Vblanking output pulse width is 2 lines too long for field 1 and 1 line too short for field 2 when compared to the digital timing defined in ITU-R BT.656 and ITU-R BT.799.

# 1.5 Output Timing Signals

Table 1-3 describes the output timing signals available to the user via pins TIMING_OUT_1 to TIMING_OUT_8. The user may output any of the signals listed below on each pin by programming the Output_Select registers beginning at address 43h of the host interface.

**Table 1-3: Output Timing Signals**

| Signal Name | Description | Default Output Pin |
|---|---|---|
| H Sync | The H Sync signal has a leading edge at the start of the horizontal sync pulse. Its width is determined by the selected video standard (see Table 1-2).<br>In Genlock mode the leading edge of the output H Sync signal is nominally simultaneous with the half amplitude point of the reference HSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 35).<br>By default, after system reset, the polarity of the H Sync signal output will be active LOW. The polarity may be selected as active HIGH by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66). | TIMING_OUT_1 |
| H Blanking | The H Blanking signal is used to indicate the portion of the video line not containing active video data.<br>The H Blanking signal will be LOW (default polarity) for the portion of the video line containing valid video samples. The signal will be LOW at the first valid pixel of the line, and HIGH after the last valid pixel of the line.<br>The H Blanking signal remains HIGH throughout the horizontal blanking period.<br>The width of this signal will be determined by the selected video standard (see Table 1-2).<br>When in Genlock mode, the output H Blanking signal will be phase locked to the reference HSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 35).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66). | TIMING_OUT_2 |
| V Sync | The V Sync timing signal has a leading edge at the start of the vertical sync pulse. Its width is determined by the selected video standard (see Table 1-2).<br>The leading edge of V Sync is nominally simultaneous with the leading edge of the first broad pulse.<br>When in Genlock mode, the output V Sync signal will be phase locked to the reference VSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 35).<br>By default, after system reset, the polarity of the V Sync signal output will be active LOW. The polarity may be selected as active HIGH by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66). | TIMING_OUT_3 |

**Table 1-3: Output Timing Signals (Continued)**

| Signal Name | Description | Default Output Pin |
|---|---|---|
| V Blanking | The V Blanking signal is used to indicate the portion of the video field/frame not containing active video lines.<br>The V Blanking signal will be LOW (default polarity) for the portion of the field/frame containing valid video data, and will be HIGH throughout the vertical blanking period.<br>The width of this signal will be determined by the selected video standard (see Table 1-2).<br>When in Genlock mode, the output V Blanking signal will be phase locked to the reference VSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 35).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66).<br>NOTE: When VID_STD = 4, 6, or 8, the Vblanking output pulse width is 2 lines too long for field 1 and 1 line too short for field 2 when compared to the digital timing defined in ITU-R BT.656 and ITU-R BT.799. | TIMING_OUT_4 |
| F Sync | The F Sync signal is used to indicate field 1 and field 2 for interlaced video formats.<br>The F Sync signal will be HIGH (default polarity) for the entire period of field 1. It will be LOW for all lines in field 2 and for all lines in progressive scan systems.<br>The width and timing of this signal will be determined by the V Sync parameters of the selected video standard (see Table 1-2). The F Sync signal always changes state on the leading edge of V Sync.<br>When in Genlock mode, the output F Sync signal will be phase locked to the reference FSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 35).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66). | TIMING_OUT_5 |
| F Digital | F Digital is used in digital interlaced standards to indicate field 1 and field 2.<br>The F Digital changes state at the leading edge of every V Blanking pulse. It will be LOW (default polarity) for the entire period of field 1 and for all lines in progressive scan systems. It will be HIGH for all lines in field 2 .<br>The width and timing of this signal will be determined by the timing parameters of the selected video standard (see Table 1-2).<br>When in Genlock mode, the output F Digital signal will be phase locked to the reference FSYNC input. This timing may be offset using the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 35).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66). | TIMING_OUT_6 |

**Table 1-3: Output Timing Signals (Continued)**

| Signal Name | Description | Default Output Pin |
|---|---|---|
| 10 Field Identification | The 10 Field Identification (10FID) signal is used to indicate the 10-field sequence for 29.97Hz, 30Hz, 59.94Hz and 60Hz video standards. It will be LOW for output standards with other frame rates.<br>The sequence defines the phase relationship between film frames and video frames, so that cadence may be maintained in mixed format environments.<br>The 10FID signal will be HIGH (default polarity) for one line at the start of the 10-field sequence. It will be LOW for all other lines. The signal's rising and falling edges will be simultaneous with the leading edge of the H Sync output signal.<br>Alternatively, by setting bit 4 of the Video_Control register (see Section 3.10.3 on page 66), the 10FID output signal may be configured to go HIGH (default polarity) on the leading edge of the H Sync output on line 1 of the first field in the 10 field sequence, and be reset LOW on the leading edge of the H Sync pulse of the first line of the second field in the 10 field sequence.<br>When in Genlock mode, the output 10FID signal will be phase locked to the 10FID reference input. If a 10FID input is not provided to the device, the user must configure the 10FID output using register 1Ah of the host interface (see Section 3.8.1 on page 57).<br>For applications involving audio, this signal may be used in place of the AFS signal if the format selected is appropriate for a 10 field AFS repetition rate, and the desired phase relationship of audio to video clock phasing coincides with the desired film frame cadence.<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66).<br>Please see Section 3.8.1 on page 57 for more detail on the 10FID output signal. | TIMING_OUT_7 |
| Display Enable | The Display Enable (DE) signal is used to indicate the display enable for graphic display interfaces.<br>This signal will be HIGH (default polarity) whenever pixel information is to be displayed on the display device (i.e. whenever both H Blanking and V Blanking are in the active video state)<br>The width and timing of this signal will be determined by the timing parameters of the selected video standard (see Table 1-2).<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3 on page 66). | TIMING_OUT_8 |
| Audio Frame Sync<br>(GS4901B only) | The Audio Frame Sync (AFS) signal is HIGH (default polarity) for the duration of the first line of the n'th video frame to indicate that the ACLK dividers are reset at the start of line 1 of that frame. It is defined according to the frame rate of the video format and the selected audio sample rate programmed via the VID_STD[5:0] and ASR_SEL[2:0] pins or the host interface.<br>For example, if the video format is based on a 59.94Hz frame rate and the audio sample rate clock is 48kHz, then n=5, and the AFS signal will be identical to the 10FID signal.<br>By default, the AFS signal is reset by the 10 Field Identification (10FID) reference input. This feature may be disabled using the Audio_Control register at address 31h of the host interface (see Section 3.10.3 on page 66). The AFS signal may also be reset using register 1Ah of the host interface. With no reference, the frame divide by "n" controlling the AFS signal will free-run at an arbitrary phase.<br>The default polarity of this signal may be inverted by programming the Polarity register at address 56h of the host interface (see Section 3.10.3).<br>Please see Section 3.8.2 on page 58 for more detail on the AFS output signal. | – |

**Table 1-3: Output Timing Signals (Continued)**

| Signal Name | Description | Default Output Pin |
|---|---|---|
| USER_1~4 | The GS4901B/GS4900B offers four user programmable output signals. Each USER signal is controlled by four timing registers and a polarity select bit. The timing registers define the start and stop times in H pixels and V lines and begin at address 57h of the host interface (see Section 3.10.3 on page 66).<br>Each user signal is individually programmable and the polarity, position, and width of each output may be defined with respect to the H, V, and F output timings of the device. Each output signal may be programmed in both the horizontal and vertical dimensions relative to the leading edges of H and V Sync. If desired, the pulses produced may then be combined with a logical AND, OR, or XOR function to produce a composite signal (for example, a horizontal back porch pulse during active lines only, or the active part of lines 15 through 20 for vertical information retrieval). Each output has selectable polarity.<br>Please see Section 3.8.3 on page 59 for more detail on the USER_1~4 output signals. | – |

# 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

| Parameter | Conditions | Value/Units |
|---|---|---|
| Supply Voltage Core and Analog (CORE_VDD, VID_PLL_VDD, AUD_PLL_VDD, PhS_VDD, ANALOG_VDD) | – | -0.3V to +2.1V |
| Supply Voltage I/O (IO_VDD, XTAL_VDD) | – | -0.3V to +3.6V |
| Input Voltage Range (any input) | IO_VDD = +3.3V | -0.3V to +5.5V |
| | IO_VDD = +1.8V | -0.3V to +3.6V |
| Operating Temperature | – | $-20°C \leq T_A \leq 85°C$ |
| Storage Temperature | – | $-50°C \leq T_{STG} \leq 125°C$ |
| Soldering Temperature | – | 260°C |
| ESD protection on all pins | – | 1 kV |

## 2.2 DC Electrical Characteristics

**Table 2-1: DC Electrical Characteristics**

$V_{DD}$ = 1.8V, $T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **System** | | | | | | | |
| Operating Temperature Range | $T_A$ | – | 0 | 25 | 70 | °C | 1 |
| Core power supply voltage | CORE_VDD | – | 1.71 | 1.8 | 1.89 | V | – |
| Digital I/O Buffer Power Supply Voltage | IO_VDD | 1.8V Operation | 1.71 | 1.8 | 1.89 | V | – |
| | IO_VDD | 3.3V Operation | 3.135 | 3.3 | 3.465 | V | – |
| Video PLL Power Supply Voltage | VID_PLL_VDD | – | 1.71 | 1.8 | 1.89 | V | – |
| Audio PLL Power Supply Voltage (GS4901B only) | AUD_PLL_VDD | – | 1.71 | 1.8 | 1.89 | V | – |
| Analog Power Supply Voltage | ANALOG_VDD | – | 1.71 | 1.8 | 1.89 | V | – |
| Crystal Buffer Power Supply Voltage | XTAL_VDD | 1.8V Operation | 1.71 | 1.8 | 1.89 | V | – |
| | XTAL_VDD | 3.3V Operation | 3.135 | 3.3 | 3.465 | V | – |
| Video Clock Phase Shift Supply Voltage | PhS_VDD | – | 1.71 | 1.8 | 1.89 | V | – |

**Table 2-1: DC Electrical Characteristics (Continued)**

$V_{DD}$ = 1.8V, $T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| System Power | $P_D$ | GS4901B<br>CORE_VDD = Max<br>IO_VDD = Max<br>T = 70°C<br>unloaded, max PCLK frequency | – | – | 415 | mW | – |
| | $P_D$ | GS4901B<br>CORE_VDD = 1.8V<br>IO_VDD = 3.3V<br>T = 25°C<br>unloaded,<br>PCLK = 27 MHz | – | 265 | – | mW | – |
| | $P_D$ | GS4900B<br>CORE_VDD = Max<br>IO_VDD = Max<br>T = 70°C<br>unloaded, max PCLK frequency | – | – | 365 | mW | – |
| | $P_D$ | GS4900B<br>CORE_VDD = 1.8V<br>IO_VDD = 3.3V<br>T = 25°C<br>unloaded<br>PCLK = 27 MHz | – | 215 | – | mW | – |
| **Digital I/O** | | | | | | | |
| Input Voltage, Logic LOW | $V_{IL}$ | 1.8V Operation | – | – | 0.35 x VDD | V | – |
| | $V_{IL}$ | 3.3V Operation | – | – | 0.8 | V | – |
| Input Voltage, Logic HIGH | $V_{IH}$ | 1.8V Operation | 0.65 x IO_VDD | – | 3.6 | V | – |
| | $V_{IH}$ | 3.3V Operation | 2.145 | – | 5.25 | V | – |
| Output Voltage, Logic LOW | $V_{OL}$ | current drive = HIGH or LOW as selected | – | – | 0.4 | V | 2 |
| Output Voltage, Logic HIGH | $V_{OH}$ | current drive = HIGH or LOW as selected | 0.65 x IO_VDD | – | – | V | 2 |
| **Digital Output Currents** | | | | | | | |
| Timing Output Drive Current | – | IO_VDD = 1.8V<br>current drive = LOW | – | 5 | – | mA | – |
| | – | IO_VDD = 3.3V<br>current drive = LOW | – | 10 | – | mA | – |
| | – | IO_VDD = 1.8V<br>current drive = HIGH | – | 7 | – | mA | – |
| | – | IO_VDD = 3.3V<br>current drive = HIGH | – | 12 | – | mA | – |

**Table 2-1: DC Electrical Characteristics (Continued)**

$V_{DD}$ = 1.8V, $T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Clock Output Drive Current | – | IO_VDD = 1.8V current drive = LOW | – | 5 | – | mA | – |
| | – | IO_VDD = 3.3V current drive = LOW | – | 7 | – | mA | – |
| | – | IO_VDD = 1.8V current drive = HIGH | – | 7 | – | mA | – |
| | – | IO_VDD = 3.3V current drive = HIGH | – | 10 | – | mA | – |
| Output Voltage LVDS, Common Mode | $V_{OCM}$ | – | 1.125 | 1.25 | 1.375 | V | 3 |
| Output Voltage LVDS, Differential | $V_{ODIFF}$ | – | – | 350 | – | mV | 3 |
| LVDS High-impedance Leakage Current | – | To 1.8V or GND | – | – | 1.4 | uA | – |

NOTES

1. All DC and AC electrical parameters within specification.
2. Assuming that the current being sourced or sinked is less than the Timing Output Drive Current specified.
3. Into a 100Ω termination connected between PCLK3 and $\overline{\text{PCLK3}}$.

# 2.3 AC Electrical Characteristics

**Table 2-2: AC Electrical Characteristics**

$V_{DD}$ = 1.8V, $T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **System** | | | | | | | |
| Reference Detection Time | – | from when the reference input is first present | – | 2 | 4 | frames | – |
| **Digital I/O** | | | | | | | |
| PCLK Output Frequency | – | – | 3.375 | – | 54 | MHz | – |
| PCLK Jitter | – | XTAL_VDD = 3.3V | – | 300 | – | ps | 1, 2 |
| PCLK Duty Cycle | – | – | 40 | – | 60 | % | – |
| PCLK1 & PCLK2 Rise/Fall Times 15pF load 20% - 80% | – | IO_VDD = 1.8V current drive = LOW | – | – | 1.7 | ns | – |
| | – | IO_VDD = 3.3V current drive = LOW | – | – | 1.5 | ns | – |
| | – | IO_VDD = 1.8V current drive = HIGH | – | – | 1.1 | ns | – |
| | – | IO_VDD = 3.3V current drive = HIGH | – | – | 0.9 | ns | – |

**Table 2-2: AC Electrical Characteristics (Continued)**

$V_{DD}$ = 1.8V, $T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| PCLK3 Rise/Fall Time<br>20% - 80% | – | 100Ω differential load<br>10pF to ground per pin | – | – | 850 | ps | – |
| PCLK Outputs Relative Timing Skew | – | default PCLK phase delay of zero | -3 | – | 3 | ns | 3 |
| ACLK Frequency<br>(GS4901B only) | – | – | 0.0097 | – | 49.152 | MHz | – |
| ACLK Duty Cycle<br>(GS4901B only) | – | – | 40 | – | 60 | % | 4 |
| ACLK1-3 Rise/Fall Times<br>15pF load<br>20% - 80%<br>(GS4901B only) | – | IO_VDD = 1.8V<br>current drive = LOW | – | – | 3.0 | ns | – |
| | – | IO_VDD = 3.3V<br>current drive = LOW | – | – | 1.5 | ns | – |
| | – | IO_VDD = 1.8V<br>current drive = HIGH | – | – | 2.5 | ns | – |
| | – | IO_VDD = 3.3V<br>current drive = HIGH | – | – | 1.4 | ns | – |
| ACLK Outputs Relative Timing Skew<br>(GS4901B only) | – | – | -3 | – | 3 | ns | 3 |
| Digital Timing Output Delay Time | $t_{OD}$ | – | – | – | 4.3 | ns | 5 |
| Digital Timing Output Hold Time | $t_{OH}$ | – | 1 | – | – | ns | 5 |
| Digital Timing Output Rise/Fall Times<br>15pF load<br>20% - 80% | – | IO_VDD = 1.8V<br>current drive = LOW | – | – | 3.0 | ns | – |
| | – | IO_VDD = 3.3V<br>current drive = LOW | – | – | 1.5 | ns | – |
| | – | IO_VDD = 1.8V<br>current drive = HIGH | – | – | 2.5 | ns | – |
| | – | IO_VDD = 3.3V<br>current drive = HIGH | – | – | 1.4 | ns | – |
| **GSPI** | | | | | | | |
| GSPI Input Clock Frequency | $f_{GSPI}$ | – | – | – | 10.0 | MHz | 6 |
| GSPI Clock Duty Cycle | $DC_{GSPI}$ | – | 40 | – | 60 | % | 6 |
| GSPI Input Setup Time | $t_3$ in Figure 3-15 | – | 1.5 | – | – | ns | 6 |

### Table 2-2: AC Electrical Characteristics (Continued)

$V_{DD}$ = 1.8V, $T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Condition | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| GSPI Input Hold Time | $t_8$ in Figure 3-15 | – | 1.5 | – | – | ns | 6 |

NOTES

1. The video output clock may be directly connected to Gennum's GS9062 serializer for a SMPTE-compliant SDI output with output jitter below 0.2UI.
2. All output standards EXCEPT VID_STD[5:0] = 1 (450ps typ.) and VID_STD[5:0] = 5 or 6 (500ps typ.)
3. Timings from any CLK output to any other CLK output.
4. If fs=96kHz and ACLK is configured to output a clock signal at 192fs or 384fs, a 512fs clock will typically have a 33% duty cycle distortion. See Section 3.7.2 on page 53.
5. With PCLK phasing delay set to nominal (zero offset), each increment of the clock phasing adjustment decreases output hold time and delay time by a nominal 700ps. The times $t_{OD}$ and $t_{OH}$ are defined in Figure 2-1.
6. For detailed GSPI timing parameters, please refer to Table 3-12.

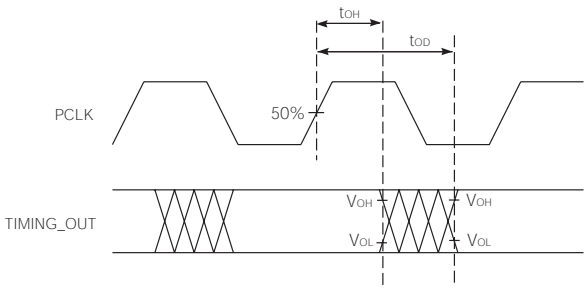



**Figure 2-1: PCLK to TIMING_OUT Signal Output Timing**

### Table 2-3: Suggested External Crystal Specification

| |
|---|
| 27.000000 MHz |
| AT Cut |
| Nominal Dissipation = 50 uW |
| Frequency accuracy at 25°C = +/- 10ppm |
| Frequency variation 0-70°C = +/- 10ppm |
| ASR = 50 +/- 20Ω |
| NOTE: The user may select an appropriate crystal accuracy for their application. If the device is operating in Free Run mode, the output clock and timing signals will have the same accuracy as the crystal. However, if operating in Genlock mode, all output signals are based on the input reference, and therefore a less accurate crystal may be sufficient. See Section 3.2 on page 34. |

## 2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-2. The recommended standard Pb reflow profile is shown in Figure 2-3.

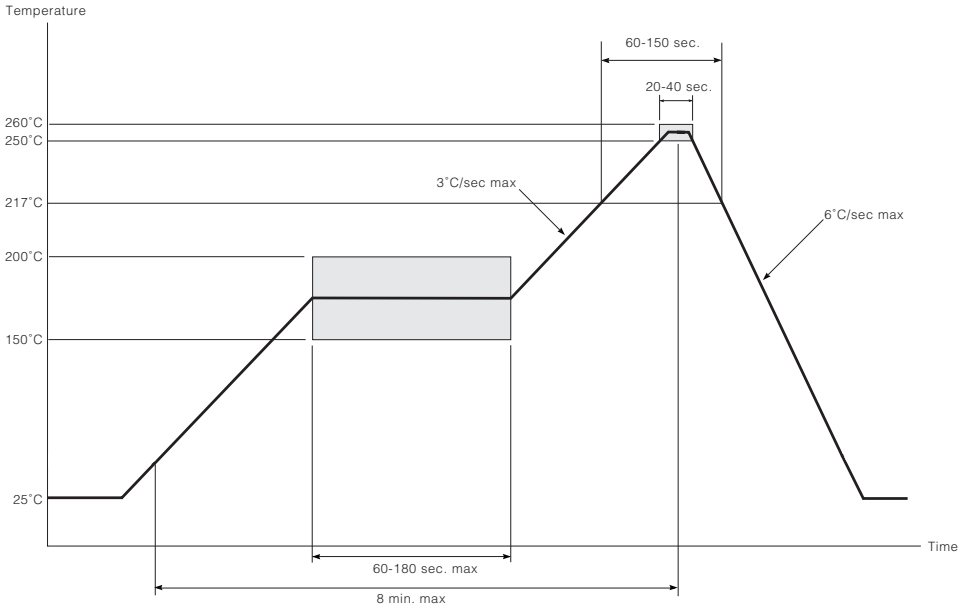



**Figure 2-2: Maximum Pb-free Solder Reflow Profile (preferred)**

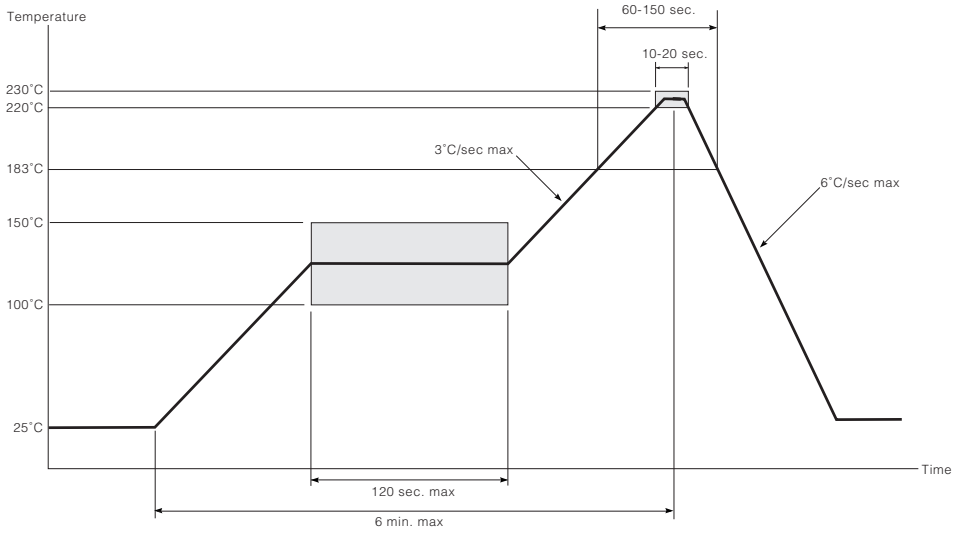



**Figure 2-3: Standard Pb Solder Reflow Profile**

# 3. Detailed Description

## 3.1 Functional Overview

The GS4901B/GS4900B is a highly flexible, digitally controlled clock synthesis circuit and timing generator with genlock capability.

The device has two main modes of operation: Genlock mode and Free Run mode. In Genlock mode, the video clock and timing outputs, will be frequency and phase locked to the detected reference input signal. In Free Run mode, the occurrence of all frequencies is based on a 27MHz external crystal reference.

The GS4901B/GS4900B will recognize input reference signals conforming to 36 different video standards. It supports cross-locking, allowing the output to be genlocked to an incoming reference that is different from the output video standard selected.

When the device is in Genlock mode and the input reference is removed, the GS4901B/GS4900B will enter Freeze mode. In this mode, the output clock and timing signals will maintain their previously genlocked phase and frequency to within +/- 2ppm.

The user may select to output one of 4 different video sample clock rates. The chosen clock frequency may be further internally divided, and is available on two video clock outputs and one LVDS video clock output pair. The video clocks may also be individually phase delayed with respect to the timing outputs for clock skew control.

Eight user-selectable timing outputs are provided that can automatically produce the following timing signals for 9 different video formats: HSync, Hblanking, VSync, Vblanking, F sync, F digital, AFS (GS4901B only), DE, and 10FID.

In addition, the GS4901B provides three audio sample clock outputs that can produce audio clocks up to 512fs with fs ranging from 9.7kHz to 96kHz. Audio to video phasing is accomplished by either an external 10FID input reference, a 10FID signal specified via internal registers, or a user-programmed audio frame sequence.

## 3.2 Modes of Operation

The GS4901B/GS4900B will operate in either Genlock mode or Free Run mode depending on the setting of the $\overline{\text{GENLOCK}}$ pin. These two modes are described in Section 3.2.1 on page 35 and Section 3.2.2 on page 38 respectively.

If desired, the external $\overline{\text{GENLOCK}}$ pin may be ignored by setting bit 5 of the Genlock_Control register (address 16h) so that genlock can instead be controlled via the host interface (see Section 3.10.3 on page 66). Although the external $\overline{\text{GENLOCK}}$ pin will be ignored in this case, it should not be left floating.

### 3.2.1 Genlock Mode

When the application layer sets the $\overline{\text{GENLOCK}}$ pin LOW and the device has successfully genlocked the outputs to the input reference, the GS4901B/GS4900B will enter Genlock mode. In this mode, all clock and timing generator outputs will be frequency and phase locked to the detected input reference signal. The PCLK outputs will be locked to the H reference.

When in Genlock mode, the output clock and timing signals are generated using the applied reference signal. The 27MHz crystal reference is necessary for operation; however, neither crystal accuracy nor changes in crystal frequency (due to a shift in operating temperature) will affect the output signals. For example, the output signals will be generated with the same accuracy whether the 27MHz reference crystal has an accuracy of 10ppm or 100ppm.

The GS4901B/GS4900B supports cross-locking, allowing the outputs to be genlocked to an incoming reference that is different from the output video standard selected (see Section 3.6 on page 46).

NOTE: The user must apply a reference to the input of the device prior to setting $\overline{\text{GENLOCK}}$ = LOW. If the $\overline{\text{GENLOCK}}$ pin is set LOW and no reference signal is present, the generated clock and timing outputs of the device may correspond to the internal default settings of the chip until a reference is applied.

#### 3.2.1.1 Genlock Timing Offset

By default, the phase of the clock and timing out signals is genlocked to the input reference signal. These output signals may be phase adjusted with respect to the input reference by programming the host interface (see Section 3.10.3 on page 66). Offsets are separately programmable in terms of clock phase, horizontal phase, and vertical phase (i.e. fractions of a pixel, pixels, and lines).

Genlock timing offsets can be used to co-time the output of a piece of equipment containing the GS4901B/GS4900B with the outputs of other equipment at different locations. The signal leaving the piece of equipment containing the GS4901B/GS4900B may pass through processing equipment with significant fixed delays before arriving at the switcher. These delays may include video line delays or even field delays. To compensate for these delays, genlock timing offsets allow the user to back-time the output of the equipment relative to the input reference.

Using the host interface, the following registers may be programmed once the device is stably locked:

- Clock_Phase_Offset (1Dh) - with a range of zero to one clock pulse in increments of between 1/128 and 1/512 of a clock period (depending on the PCLK frequency). The increments will be between 100ps and 150ps. All clock and timing output signals will be delayed by the clock phase offset programmed in this register.
- H_Offset (1Bh) - the difference between the reference HSYNC signal and the output H Sync and/or H Blanking signal in clock pulses, with a control range of zero to +1 line. All timing output signals will be delayed by the horizontal offset programmed in this register.

- V_Offset (1Ch) - the difference between the reference VSYNC signal and the output V Sync and/or V Blanking in lines, with a control range of zero to +1 frame. All line-based timing output signals will be delayed by the vertical offset programmed in this register.

The encoding scheme for the Clock_Phase_Offset register (1Dh) is shown in Table 3-1. The offset programmed will be in the positive direction. Note that the step size will depend on the frequency of the output video clock.

**Table 3-1: Clock_Phase_Offset[15:0] Encoding Scheme**

| VID_STD[5:0] Setting | Output Video Clock Frequency | Step Size (Fraction of a PCLK) | Maximum Number of Steps | Bits Required to Set the Number of Steps | Clock_Phase_Offset [15:0] Settings |
|---|---|---|---|---|---|
| 1 | $f_{PCLK} \leq 20MHz$ | $\frac{1}{512}$ | 511 | $b_8b_7b_6b_5b_4b_3b_2b_1b_0$ | $\overline{b}_8000001b_8b_7b_6b_5b_4b_3b_2b_1b_0$ |
| 3-6 | $20MHz < f_{PCLK} \leq 40MHz$ | $\frac{1}{256}$ | 255 | $b_7b_6b_5b_4b_3b_2b_1b_0$ | $\overline{b}_7000010b_7b_6b_5b_40b_3b_2b_1b_0$ |
| 7-10 | $40MHz < f_{PCLK} \leq 54MHz$ | $\frac{1}{128}$ | 127 | $b_6b_5b_4b_3b_2b_1b_0$ | $\overline{b}_6000100b_6b_5b_400b_3b_2b_1b_0$ |

Note: Program Clock_Phase_Offset = 0000 0000 0000 0000b to achieve a zero clock phase offset.

The value programmed in the H_Offset register (1Bh) must not exceed the maximum number of clock periods per line of the outgoing video standard. Similarly, the value programmed in the V_Offset register (1Ch) must not exceed the maximum number of lines per frame of the outgoing standard. Both horizontal and vertical offsets will be in the positive direction. Negative offsets (advances) are achieved by programming a value in the appropriate register equal to the maximum allowable offset minus the desired advance.

NOTES:

1. The device will delay all output timing signals by 2 PCLKs relative to the input HSYNC reference. This will occur even when the H_Offset register is not programmed. The user may compensate for this delay by subtracting 2 PCLK cycles from the desired horizontal offset before loading the value into the host interface.
2. For both sync and blanking-based input references, the device will advance all line-based output timing signals by 1 line relative to the input VSYNC reference for all output standards except VID_STD[5:0] = 4, 6, and 8. This will occur even when the V_Offset register is not programmed. The user may compensate for this advance by adding 1 line to the desired vertical offset before loading this value into the register.

3. When locking the 525-line SD output standards to the *"f/1.001"* HD input reference standards, the device will delay all line-based output timing signals by ΔVSync lines relative to the input VSYNC reference. This will occur even when the V_Offset register is not programmed. The user may compensate for this delay by subtracting ΔVSync lines from the desired vertical offset before loading this value into the register.

   The value ΔVSync is given by the equation:

$$\Delta VSync = HSYNC\_IN\_Period + \Delta VSYNC\_HSYNC - (2 \times HSYNC\_OUT\_Period)$$

   where:

   HSYNC_IN_Period = the period of the H reference pulse
   ΔVSYNC_HSYNC = the time difference between the leading edges of the applied V and H reference pulses
   Hsync_OUT_Period = the period of the generated H Sync output

   See Figure 3-1. H_Feedback_Divide represents the numerator of the ratio of the output clock frequency to the frequency of the H reference pulse.

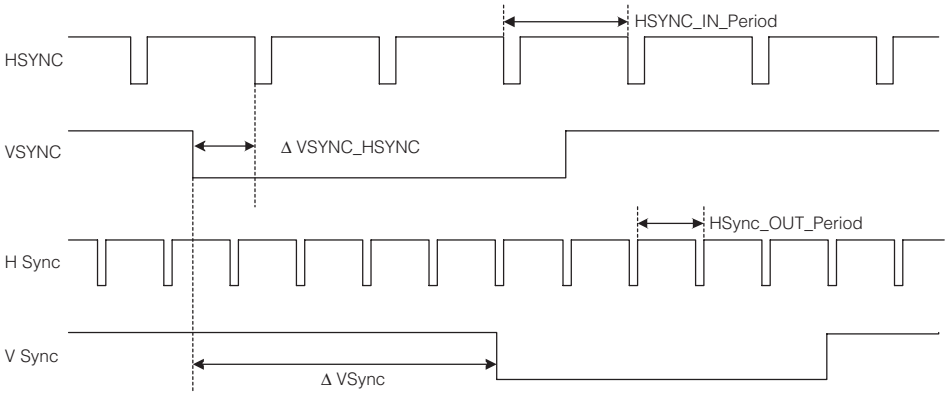



**Figure 3-1: SD-HD Calculation**

4. For sync-based input references, the device will advance all line-based output timing signals by 1 line if the value programmed in the H_Offset register is greater than 20. The user may compensate for this advance by adding 1 line to the desired vertical offset before loading this value into the register. In addition, the internal V_lock and F_lock signals reported in bits 3 and 4 of register 16h will be LOW when H_Offset = 21 only, although the device will remained genlocked. The user may choose to mask these lock signals such that the device will continue to report genlock under this condition.

5. For blanking-based input references, the device will advance all line-based output timing signals by 1 line if the value programmed in the H_Offset register is greater than the number of output video clock cycles from the start of H Sync to the end of active video (Hsync_to_EAV) + 20. The value of Hsync_to_EAV is reported in register 51h and changes according to the output VID_STD selected. The user may compensate for this advance by adding 1 line to the desired vertical offset before loading this value into the register. In addition, the internal V_lock and F_lock signals reported in bits 3 and 4 of register 16h will be LOW when H_Offset = Hsync_to_EAV + 21 only, although the device will remained genlocked. The user may choose to mask these lock signals such that the device will continue to report genlock under this condition.
6. The offsets that occur as described in notes 1-5 are independent of one another and must be accounted for as such.

#### 3.2.1.2 Freeze Mode

When the device is in Genlock mode and the input reference is removed, the GS4901B/GS4900B will enter Freeze mode. The behaviour of the device during loss and re-acquisition of an input reference signal is described in Section 3.5.3 on page 44.

In Freeze mode, the frequency of the output clock and timing signals will be maintained to within +/- 2ppm. This assumes a loop bandwidth of 10Hz. Also, if the frequency of the 27MHz reference crystal shifts while in Freeze mode, the frequency of the output clock and timing signals will shift as well.

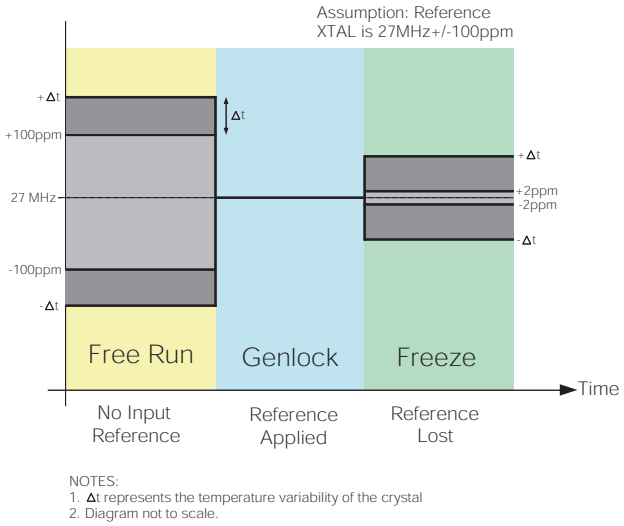
### 3.2.2 Free Run Mode

The GS4901B/GS4900B will enter Free Run mode when the $\overline{\text{GENLOCK}}$ pin is set HIGH by the application layer. In this mode, the occurrence of all frequencies is based on the external 27MHz reference input. Therefore, the frequency of the output clock and timing signals will have the same accuracy as the crystal reference.

If operating in Free Run mode, using a more accurate crystal (e.g. 10ppm) ensures more accurate clock and timing signals are generated.

NOTE: In Free Run mode, the audio clocks of the GS4901B will remain genlocked to the video clock.

Figure 3-2 summarizes the differences in output accuracy in each mode of operation. Assuming a crystal reference of +/-100ppm, in Free Run mode the frequency of the output clock and timing signals will be as accurate as the crystal. In Genlock mode the frequency will be as accurate as the input reference regardless of the crystal accuracy. In Freeze mode, the frequency of the output clock and timing signals will be maintained to within +/- 2ppm.




NOTES:
1. Δt represents the temperature variability of the crystal
2. Diagram not to scale.

**Figure 3-2: Output Accuracy and Modes of Operation**

## 3.3 Output Timing Format Selection

At device power-up (described in Section 3.12 on page 88), the application layer should immediately set the external VID_STD[5:0] and ASR_SEL[2:0] pins. The VID_STD[5:0] pins are used to select a pre-programmed output video format. The ASR_SEL[2:0] pins are only available on the GS4901B, and are used to select the fundamental audio frequency or to turn off audio clock generation.

The output timing formats selectable by the user via the VID_STD[5:0] pins are listed in Section 1.4 on page 20. Table 3-7 in Section 3.7.2 on page 53 lists the audio sample rates available via the ASR_SEL[2:0] pins.

NOTE: The VID_STD[5:4] pins should be grounded by the application layer since these pins are not required to select output video standards 1 to 10.

On power-up, the device will first check the status of the $\overline{\text{GENLOCK}}$ pin. If $\overline{\text{GENLOCK}}$ is set LOW and a valid reference has been applied to the inputs, the device will output the selected video standard while attempting to genlock. However, if a reference signal has not been applied and $\overline{\text{GENLOCK}}$=LOW, the initial clock and timing outputs may be determined by the internal default settings of the chip. If $\overline{\text{GENLOCK}}$ is set HIGH, the device will immediately enter Free Run mode and will correctly output the selected video standard.

When operating in Free Run or Genlock mode, the GS4901B/GS4900B will continuously monitor the settings of the VID_STD[5:0] and ASR_SEL[2:0] pins. If the user wishes to change the format of the output clocks and timing signals, these pins may be reconfigured at any time, although it is recommended that the device be reset when changing output video standards.

## 3.4 Input Reference Signals

The HSYNC, VSYNC, FSYNC, and 10FID reference signals are applied to the GS4901B/GS4900B via the designated input pins.

To operate in Genlock mode, the input reference signals must be valid and must conform to a recognized video standard (see Section 3.5 on page 42).

In Free Run mode, no input reference is required.

Section 3.4.1 on page 40 describes the HSYNC, VSYNC and FSYNC input timing. The 10FID input signal is discussed in Section 3.4.2 on page 41.

### 3.4.1 HSYNC, VSYNC, and FSYNC

The HSYNC, VSYNC, and FSYNC input reference signals may have analog timing, such as from Gennum's GS4981/82 sync separators (Figure 3-3), or may have digital timing, such as from Gennum's GS1559/60A/61 deserializers (Figure 3-4). Section 1.4 on page 20 lists the 36 pre-programmed video timing formats recognized by the GS4901B/GS4900B.

If the input reference format does not include an F sync signal, the FSYNC pin should be held LOW.

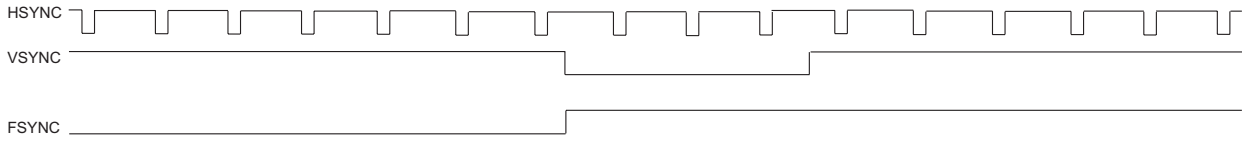



**Figure 3-3: Example HSYNC, VSYNC, and FSYNC Analog Input Timing from a Sync Separator**

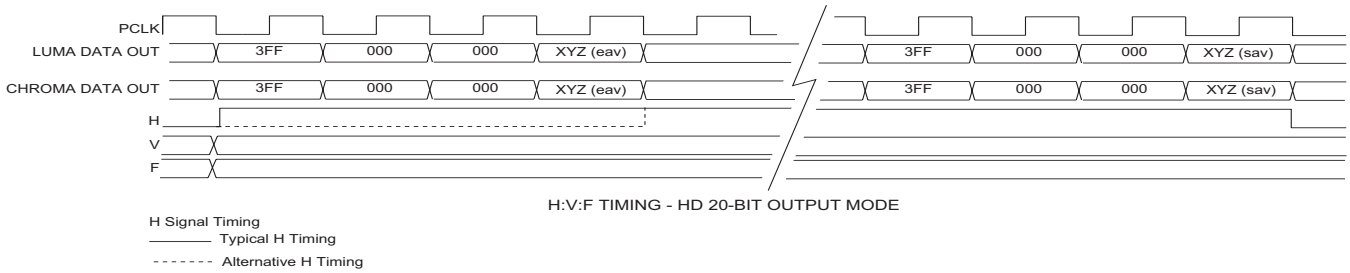



**Figure 3-4: Example H Blanking, V Blanking, and F Digital Input Timing from an SDI Deserializer**

### 3.4.2 10FID

The 10FID input is a reset pin, which can be used to reset the divider for the 10FID output signal. In the GS4901B, the 10FID input pin will also reset the divider for the AFS output signal. This default setting may be modified using the Audio_Control register of the host interface (see Section 3.10.3 on page 66).

The GS4901B will reset the phase of the audio clocks to the leading edge of the H Sync output on line 1 of every output frame in which the 10FID input is HIGH.

If the input reference format does not include a 10 Field ID signal, the external 10FID input pin should be held LOW.

The timing of the 10FID input signal is shown in Figure 3-5.

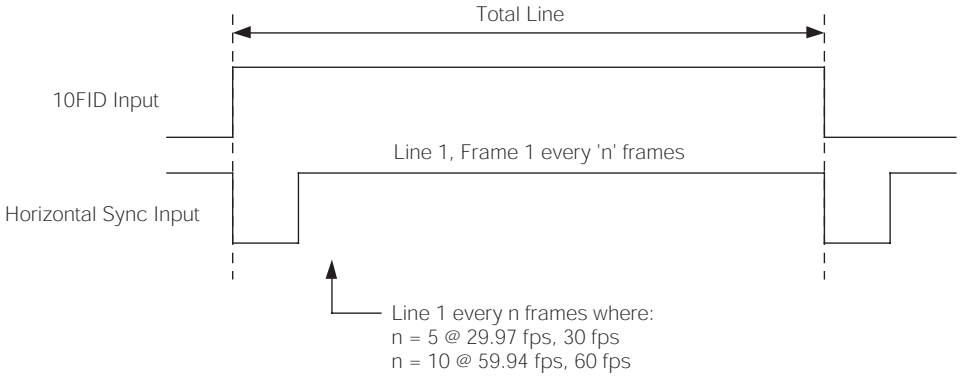



**Figure 3-5: 10FID Input Timing**

### 3.4.3 Automatic Polarity Recognition

To accommodate any standards that employ the polarity of the H and V sync signals to indicate the format of the display, the GS4901B/GS4900B will recognize H and V sync polarity and automatically synchronize to the leading edge.

The polarities of the HSYNC and VSYNC signals are reported in bits 3 and 4 of the Video_Status register. Additionally, bit 2 of this register reports the detection of either analog or digital input timing. See Section 3.10.3 on page 66 for detailed register descriptions.

## 3.5 Reference Format Detector

The reference format detector checks the validity and analyzes the format of the input reference signal. It is designed to accurately differentiate between 59.94 and 60Hz frame rates.

As described in Section 1.4 on page 20, the GS4901B / GS4900B will automatically recognize the SD video standards defined by VID_STD[5:0] = 1 to 10. However, in order to enable the device to recognize and lock to any of the HD reference formats defined by VID_STD[5:0] = 11 to 38, the user must set the corresponding bit LOW in the Reference_Standard_Disable register, located at address 11h-13h of the host interface. The user must also set the HD_Reference_Enable bit of register 82h[7] HIGH. See the description of the Reference_Standard_Disable and HD_Reference_Enable registers in Section 3.10.3 on page 66.

### 3.5.1 Horizontal and Vertical Timing Characteristic Measurements

When a reference signal is applied to the designated input pins, the GS4901B/GS4900B will analyse the signal and report the following in registers 0Ah to 0Eh of the host interface:

- the number of 27MHz clock pulses between leading edges of the H input reference signal (H_Period register)
- the number of 27MHz clock pulses in 16 horizontal periods (H_16_Period register)
- the number of H reference pulses between leading edges of the V input reference signal (V_Lines register)
- the number of H reference pulses in two vertical periods (V_2_Lines register)
- the number of H reference pulses in one F period (F_Lines register)

These parameters may be read via the host interface and are used by the device to determine reference signal validity.

### 3.5.2 Input Reference Validity

Before the device attempts to operate in Genlock mode, the input signals applied to HSYNC and VSYNC must be valid (SD references only) and must conform to one of the recognized and enabled video standards, as described in Section 1.4 on page 20.

For an SD input reference signal to be considered valid, the periodicity of HSYNC must be between 29.66us and 70us, and the periodicity of VSYNC must be between 16ms and 25ms. The FSYNC signal is not essential for validity. The REF_LOST pin will be set LOW once the SD input reference signal is determined to be valid.

For HD input reference signals where the user has set the HD_Reference_Enable bit of register 82h[7] HIGH, the device will not measure signal validity. In this case, the REF_LOST pin will be LOW whenever any reference signal is present on the input.

The device then compares the timing parameters of the input reference signal to each of the video standards that has been enabled in the the Reference_Standard_Disable register (there may be up to 36 video standards if all HD standards are enabled). The device will then determine if the input reference is one of the enabled and recognized standards. If it is, the VID_STD[5:0] value for the format is written to the Input_Standard register at address 0Fh of the host interface. If the reference format is unrecognized or disabled, 00h is programmed in this register.

Once a reference signal is recognized by the device, VSYNC and FSYNC will no longer be monitored. Loss of signal on these pins will not affect the operation of the device.

If the REF_LOST pin is HIGH, or if the input signal is unrecognized as one of the enable video formats, the GENLOCK pin should not be set LOW.

The REF_LOST output pin may also be read via bit 0 of the Genlock_Status register (see Section 3.10.3 on page 66).

#### 3.5.2.1 Ambiguous Standard Selection

There are some standards with identical H, V, and F timing parameters, such that the GS4901B/GS4900B's reference format detector cannot distinguish between them. Table 3-2 groups standards with shared H, V, and F periods. Using the Amb_Std_Sel register at address 10h of the host interface, the user may select their choice of standard to be identified with a particular set of measurements. For example, to have 1716 clocks of 27MHz per line with 525 lines per frame identified as 4fsc 525, program Amb_Std_Sel[10:0] = XXX10XXXXXX, where 'X' signifies 'don't care'.

**Table 3-2: Ambiguous Standard Identification**

| Number | Standard | H (27MHz Clocks) | 16_H (27MHz Clocks) | V (lines) | F (lines) | Amb_Std_Sel[10:0] |
|---|---|---|---|---|---|---|
| 1 | 1920x1080/60/2:1 interlace (25) | 800 | 12800 | 562.5 | 1125 | X X X X X X X X X 0 0 |
| | 1920x1080/30/PsF (30) | 800 | 12800 | 562.5 | 1125 | X X X X X X X X X 0 1 |
| | 1920x1035/60/2:1 interlace (19) | 800 | 12800 | 562.5 | 1125 | X X X X X X X X X 1 0 |
| 2 | 1920x1080/59.94/2:1 interlace (26) | 800.8 | 12813 | 562.5 | 1125 | X X X X X X X 0 0 X X |
| | 1920x1080/29.97/PsF (32) | 800.8 | 12813 | 562.5 | 1125 | X X X X X X X 0 1 X X |
| | 1920x1035/59.94/2:1 interlace (20) | 800.8 | 12813 | 562.5 | 1125 | X X X X X X X 1 0 X X |
| 3 | 1920x1080/50/2:1 interlace (27) | 960 | 15360 | 562.4 | 1125 | X X X X X 0 0 X X X X |
| | 1920x1080/25/PsF (34) | 960 | 15360 | 562.4 | 1125 | X X X X X 0 1 X X X X |
| 4 | 601 525 / 2:1 interlace (3) | 1716 | 27456 | 262.5 | 525 | X X X 0 0 X X X X X X |
| | 720x486/59.94/2:1 interlace (7) | 1716 | 27456 | 262.5 | 525 | X X X 0 1 X X X X X X |
| | 4fsc 525 / 2:1 interlace (1) | 1716 | 27456 | 262.5 | 525 | X X X 1 0 X X X X X X |
| | 601 - 18MHz 525/2:1 interlace (5) | 1716 | 27456 | 262.5 | 525 | X X X 1 1 X X X X X X |
| 5 | 601 625 / 2:1 interlace (4) | 1728 | 27648 | 312.5 | 625 | X 0 0 X X X X X X X X |
| | 720x576/50/2:1 interlace (8) | 1728 | 27648 | 312.5 | 625 | X 0 1 X X X X X X X X |
| | Composite PAL 625/2:1/25 (2) | 1728 | 27648 | 312.5 | 625 | X 1 0 X X X X X X X X |
| | 601 - 18MHz 625/2:1 interlace (6) | 1728 | 27648 | 312.5 | 625 | X 1 1 X X X X X X X X |
| 6 | RSVD | RSVD | RSVD | RSVD | RSVD | 0 X X X X X X X X X X |
| | 720x483/59.94/1:1 progressive (9) | 858 | 13728 | 525 | 525 | 1 X X X X X X X X X X |

'X' signifies 'don't care.' The X bit will be ignored when determining which standard to select in each of the 6 groups above.

NOTE: When the SD input reference format of 720x483/59.94/1:1 (VID_STD = 9) is applied to the input, the user must set bit [15] of the of the Amb_Std_Sel register address to '1' before the device will recognize this reference.

## 3.5.3 Behaviour on Loss and Re-acquisition of the Reference Signal

By default, the GS4901B/GS4900B will ignore one missing H pulse on the HSYNC pin and will continue to operate in Genlock mode (although the LOCK_LOST pin will temporarily be set HIGH). This behaviour is controlled by the Run_Window bits of register address 24h.

If there are two consecutive missing H pulses on the HSYNC input pin, the REF_LOST and LOCK_LOST pins will both go HIGH and the device will enter Freeze mode. An internal flywheel ensures the selected output clock and timing signals maintain their previous phase and frequency and continue to operate without glitches.

The VSYNC and FSYNC signals are not monitored in Genlock mode; loss of signal on these pins will not affect the operation of the device.

NOTE 1: If the input reference is removed and re-applied, all line-based timing outputs will be inaccurate for up to one frame for all output standards.

NOTE 2: When locking the SD input reference standards 3, 5, 7, or 9 to the *"f/1.001"* HD input reference standards, there may be a random phase difference between the input VSYNC and output V Sync signals occuring each time the input reference is removed and re-applied. This will affect all line-based timing outputs. The user may reset the line-based counters after the reference is re-applied without disrupting the pixel or audio clocks by toggling bit 15 of register address 83h in the host interface. This will cause the input VSYNC and line-based timing output signals to take on their default timing relationship, as described in Note 3 of Section 3.2.1.1 on page 35.

### Re-acquisition of the Same Reference

Upon re-application of the reference signal, the device checks whether the reference has drifted more than +/- 2us from its expected location by comparing the current relative position of the H pulses with the previous position, over a 16-line interval. If the reference returns with the H pulses in the expected location +/- 2us, the PLL will drift lock and the clock generator will continue to operate without a glitch. The REF_LOST and LOCK_LOST pins will be set back LOW.

If the reference returns with the H pulses outside the +/- 2us window, the device will crash lock the output timing to the new input phase. The principles of crash lock and drift lock are described in Section 3.6.1 on page 47.

NOTE: To resume proper genlock operation upon re-application of the reference signal, the user must implement the following register manipulation every time the reference is removed and re-applied:

1. Read the value contained in register address 24h
2. Clear the Run_Window bits [2:0] of register 24h
3. Re-write the value read in step 1 to register address 24h.

This procedure will force the device to lock to the reference as described above, but will maintain the flywheeling capability of the GS4901B/GS4900B should a single missing H pulse occur in the genlocked state.

To avoid the above procedure, the user may choose to clear the Run_Window bits [2:0] of register address 24h upon power-up or reset. However, this will disable the flywheeling feature of the device that allows it to maintain genlock through one missing input H pulse.

### Acquisition of a New Reference

When a new reference is applied, the device continues to operate in Freeze mode while the reference format detector checks for validity as described in Section 3.5.2 on page 43. Once validity is detected, the REF_LOST pin is set LOW.

Assuming $\overline{\text{GENLOCK}}$ is LOW, the device will then attempt to genlock the selected output clock and timing signals to the new input reference. If the output can be automatically genlocked to the new input reference, LOCK_LOST will go LOW and the device will re-enter Genlock mode. Otherwise, the LOCK_LOST pin will remain HIGH and the device will enter Free Run mode.

### 3.5.4 Allowable Frequency Drift on the Reference

By default, the frequency of the reference H pulse on HSYNC may drift from its expected value by approximately +/- 0.2% before the internal video PLL loses lock. This tolerance may be adjusted using the Max_Ref_Delta register at address 1Eh of the host interface.

The encoding scheme is shown in Table 3-3. The default value of the register is Bh.

NOTE: Regardless of the setting of this register, the device will always differentiate between 59.94Hz and 60Hz reference standards.

**Table 3-3: Max_Ref_Delta Encoding Scheme**

| Register Setting | Maximum Allowable Frequency Drift | Register Setting | Maximum Allowable Frequency Drift |
|---|---|---|---|
| 0h | $+/- 2^{-20}$ | 8h | $+/- 2^{-12}$ |
| 1h | $+/- 2^{-19}$ | 9h | $+/- 2^{-11}$ |
| 2h | $+/- 2^{-18}$ | Ah | $+/- 2^{-10}$ |
| 3h | $+/- 2^{-17}$ | Bh | $+/- 2^{-9}$ |
| 4h | $+/- 2^{-16}$ | Ch | $+/- 2^{-8}$ |
| 5h | $+/- 2^{-15}$ | Dh | $+/- 2^{-7}$ |
| 6h | $+/- 2^{-14}$ | Eh | $+/- 2^{-6}$ |
| 7h | $+/- 2^{-13}$ | Fh | $+/- 2^{-5}$ |

The maximum allowable frequency drift is measured as a fraction of the frequency of the reference H pulse.

## 3.6 Genlock

When both the REF_LOST output and the $\overline{\text{GENLOCK}}$ input are LOW, the device will attempt to genlock the output clock and timing signals to the input reference.

NOTE: The user must apply a reference to the input of the device prior to setting $\overline{\text{GENLOCK}}$ = LOW. If the $\overline{\text{GENLOCK}}$ pin is set LOW and no reference signal is present, the generated clock and timing outputs of the device may correspond to the internal default settings of the chip until a reference is applied.

Once reference validity is established and the reference format is recognized, the device uses an internal cross-reference genlock look-up table to determine whether the  input can be used to genlock the output. A simplified version of this look-up table is shown in Table 3-4. The table represents a matrix with the VID_STD[5:0] number representation of each possible reference format along the top axis, and the VID_STD[5:0] representation of each possible output timing format along the vertical axis. A shaded box indicates that the output format can be automatically genlocked to the input reference.

If the device determines that the output can be automatically genlocked to the input reference, it will lock the output format to the reference, adjust the output timing signals based on the genlock timing offset registers (Section 3.2.1.1 on page 37), and then set the LOCK_LOST pin LOW.

If the device cannot automatically genlock the output to the applied reference, the LOCK_LOST pin will be set HIGH and the device will operate in Free Run mode.

Individual H, V, and F-locked signals can be read from the Genlock_Status register of the host interface. Additionally, designated bits in the Genlock_Control register may be configured to permit the genlock block to ignore invalid timing on the HSYNC, VSYNC, or FSYNC pin when determining the locked status of the device. These registers are described in Section 3.9.3 on page 66.

The user may disable one or more of the 36 video standards listed in Table 1-2 from being used to genlock the output by setting the Reference_Standard_Disable register located at address 11h-13h of the host interface. If a reference is applied that is disabled in the Reference_Standard_Disable register, the lock process will fail when the application layer sets GENLOCKb = LOW.

NOTE: If the device is already genlocked to an input reference and the applied standard is subsequently disabled in the Reference_Standard_Disable register, the device will remain locked.

By default, the HD video reference formats are disabled in the Reference_Standard_Disable register and so must be enabled by the user before attempting to lock to an HD reference. See Section 1.4 on page 20.

**Table 3-4: Cross-reference Genlock Table**

| Input Reference Format | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 25 | 26 | 27 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ■ | | ■ | | ■ | | ■ | | ■ | | | ■ | | | ■ | | | ■ | | ■ | | ■ | | | ■ | | | | ■ | ■ | | | | | | ■ | ■ |
| 3 | ■ | | ■ | | ■ | | ■ | | ■ | | | ■ | | | ■ | | | ■ | | ■ | | ■ | | | ■ | | | | ■ | ■ | | | | | | ■ | ■ |
| 4 | | ■ | | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | | ■ | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | ■ | | | ■ | ■ | ■ | ■ | | |
| 5 | ■ | | ■ | | ■ | | ■ | | ■ | | | ■ | | | ■ | | | ■ | ■ | | | ■ | | ■ | | | | ■ | ■ | | | | | | ■ | ■ |
| 6 | | ■ | | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | | ■ | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | ■ | | | | | ■ | ■ | | |
| 7 | ■ | | ■ | | ■ | | ■ | | ■ | | | ■ | | | ■ | | | ■ | | ■ | | ■ | | | ■ | | | | ■ | ■ | | | | | | ■ | ■ |
| 8 | | ■ | | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | | ■ | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | ■ | | | ■ | ■ | ■ | ■ | | |
| 9 | ■ | | ■ | | ■ | | ■ | | ■ | | | ■ | | | ■ | | | ■ | | ■ | | ■ | | | ■ | | | | ■ | ■ | | | | | | ■ | ■ |
| 10 | | ■ | | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | | ■ | ■ | | ■ | | ■ | | ■ | ■ | | ■ | ■ | ■ | | | ■ | ■ | ■ | ■ | | |

## 3.6.1 Adjustable Locking Time

The GS4901B/GS4900B offers two different locking mechanisms to allow the user to control the PLL lock time and the integrity of the output signal during the locking process. The locking process is said to take place after the application of the input reference and before the LOCK_LOST signal is set LOW.

By default, the internal PLL will crash lock. This locking process will ensure a minimum PLL locking time; however, crash lock will cause the phase of the output clock and timing signals to jump during the locking process. The crash behaviour of the video PLL is controlled by the Crash_Time bits of register address 24h.

Alternatively, the user may set bit 1 of register 16h HIGH to force the PLL to drift lock. Drift lock will increase the locking time of the PLL, but will maintain the signal integrity of the output clock and timing pulses during the locking process.

As discussed in Section 3.5.3 on page 44, the device will normally drift lock when the reference is removed and subsequently re-applied during Genlock mode.

## 3.6.2 Adjustable Loop Bandwidth

The default loop bandwidth of the GS4901B/GS4900B's internal video PLL is 10Hz when the output video standard is the same as the input reference format. For other cross-locking combinations, the default loop bandwidth may be smaller than 1Hz or as large as 30Hz.

The user may adjust the loop bandwidth of both the video and audio PLLs depending on the input, output, and audio standards selected. Increasing the loop bandwidth will result in a shorter PLL lock time, but will allow more frequency components of jitter to be passed to the outputs. Decreasing the loop bandwidth will decrease the output jitter, but will result in a longer PLL lock time.

### 3.6.2.1 Loop Bandwidth of the Video PLL

The capacitive component of the filter controlling the video loop bandwidth is determined by the Video_Cap_Genlock register and the resistive component is determined by the Video_Res_Genlock register. These two registers are located at addresses 26h and 27h, respectively, of the host interface.

To determine the setting of Video_Res_Genlock and Video_Cap_Genlock, the following equations must be solved:

$$Video\_Res\_Genlock = \lceil 47 + \log_2(6 \times BW \times JITTERIN \times H\_Feedback\_Divide) \rceil$$

$$Video\_Cap\_Genlock \leq Video\_Res\_Genlock - 21$$

where:
BW = the desired video PLL loop bandwidth
JITTERIN = Jitter present on applied HSYNC reference signal, in seconds
H_Feedback_Divide = the numerator of the video PLL divide ratio

H_Feedback_Divide represents the numerator of the ratio of the output clock frequency to the frequency of the H reference signal.

For example, to program a loop bandwidth of 25Hz given a 54MHz video clock and a reference with a 27MHz video clock and 1716 clocks per line, the following steps are necessary:

1. Calculate H_Feedback_Divide:

$$\frac{H\_Feedback\_Divide}{H\_Reference\_Divide} \times \frac{f_{pclkout}}{f_{Hrefin}}$$

$$f_{pclkout} = 27MHz$$

$$f_{Hrefin} = \frac{27}{1716}MHz$$

$$\therefore \frac{H\_Feedback\_Divide}{H\_Reference\_Divide} = 27 \times \frac{1716}{27} = \frac{1716}{1}$$

Therefore, H_Feedback_Divide = 1716.

2. Calculate the value for Video_Res_Genlock:

$$Video\_Res\_Genlock = \left\lceil 47 + \log_2(6 \times 25 \times (3 \times 10^{-9}) \times 1716) \right\rceil = 37$$

3. Calculate the value for Video_Cap_Genlock:

$$Video\_Cap\_Genlock = 37 - 21 = 16$$

Therefore, program Video_Res_Genlock = 37 and Video_Cap_Genlock = 16.

NOTE: The value programmed in the Video_Res_Genlock register must be between 32 and 42. The value programmed in the Video_Cap_Genlock register must be greater than 10. These limits define the exact range of loop bandwidth adjustment available.

#### 3.6.2.2 Loop Bandwidth of the Audio PLL (GS4901B only)

The capacitive component of the filter controlling the audio loop bandwidth is determined by the Audio_Cap_Genlock register and the resistive component is determined by the Audio_Res_Genlock register. These two registers are located at addresses 39h and 3Ah, respectively, of the host interface.

To determine the setting of Audio_Res_Genlock and Audio_Cap_Genlock, the following equations must be solved:

$$Audio\_Res\_Genlock = \lceil 47 + \log_2(6 \times BW \times JITTERIN \times \text{A\_Feedback\_Divide}) \rceil$$

$$Audio\_Cap\_Genlock \leq Audio\_Res\_Genlock - 21$$

where:

BW = the desired audio PLL loop bandwidth
JITTERIN = Jitter present on output PCLK, in seconds.
A_Feedback_Divide = the numerator of the audio PLL divide ratio

A_Feedback_Divide is defined by the following equation:

$$\frac{A\_Feedback\_Divide}{A\_Reference\_Divide} = n \times \frac{f_s}{f_{out}}$$

Where $f_s$ is the fundamental audio sampling frequency and $f_{out}$ is the output video clock frequency. The integer constant, n, will depend on the fundamental audio sampling frequency as shown in Table 3-5.

**Table 3-5: Integer Constant Value**

| ASR_SEL[2:0]=100b | Enable_384fs = 0 | Value of constant (n) |
|---|---|---|
| NO | X | 3072 |
| YES | YES | 1024 |
| YES | NO | 1536 |

NOTES:
1. Enable_384fs corresponds to bit 5 of address 31h of the host interface. It is LOW by default.
2. 'X' signifies 'don't care.' This bit will be ignored when determining n.

NOTE: The value programmed in the Audio_Res_Genlock register must be between 32 and 42. The value programmed in the Audio_Cap_Genlock register must be greater than 10. These limits define the exact range of loop bandwidth adjustment available.

### 3.6.3 Locking to Digital Timing from a Deserializer

As described in Section 3.4.1 on page 40, the GS4901B/GS4900B may be genlocked to either an analog reference, such as a Black & Burst signal, or to an SDI input via the digital H, V, and F blanking signals normally produced by a deserializer. When locking to an SDI input, the user should consider the possibility of a switch of the SDI signal upstream from the system.

If the GS4901B/GS4900B is locked to the digital H, V, and F blanking signals produced by a deserializer, and the SDI input to the deserializer is switched such that the phase of the H input changes abruptly, the REF_LOST output will remain LOW and the GS4901B/GS4900B will not crash lock to the new H phase. Instead, the clock and timing outputs will very slowly drift towards the new phase. During this period of drift, the LOCK_LOST output will be LOW, even though the device is not genlocked.

The user should clear the Run_Window bits [2:0] of register adress 24h to force the device to crash lock should such a switch occur. This will cause the GS4901B/GS4900B to crash lock whenever it sees a disturbance of the input H signal.

NOTE: Any action that causes an abrupt phase change of the H input to the GS4901B/GS4900B such that REF_LOST is not triggered will cause the device to respond in the manner described above.

In addition to the slow drifting behaviour outlined above, there may also be a random phase difference between the input VSYNC and output V Sync signals occurring each time a switch in the SDI stream causes an abrupt phase change of the H input to the GS4901B/GS4900B. This will only occur when attempting to lock the 525-line SD output standards to the "*f/1.001*" HD input reference standards. All line-based timing outputs are affected.

The only way to ensure a constant phase difference between the input VSYNC signal and the line-based timing outputs is to reset the line-based counters after such a switch occurs. This is acheived by toggling bit 15 of register address 83h in the host interface. The device will then delay all line-based output timing signals by ∆Vsync lines relative to the input VSYNC reference, as described in NOTE 3 of Section 3.2.1.1 on page 35.

## 3.7 Clock Synthesis

The clock synthesis circuit generates the video clocks based on the VID_STD[5:0] pins and host register settings. In the GS4901B, the clock synthesis circuit also generates the audio clock signals based on the ASR_SEL[2:0] pins and host register settings.

The generated video and audio clocks may be further divided and are presented to the application layer via pins PCLK1-PCLK3 and ACLK1-ACLK3 respectively.

### 3.7.1 Video Clock Synthesis

The video clock generator is referenced to an internal crystal oscillator and is responsible for generating the PCLK output signals.

The crystal oscillator requires an external 27MHz crystal connected to pins X1 and X2, or can be driven at LVTTL levels from an external 27MHz source connected to X1. These two configurations are shown in Figure 1-1.

Four different video sample clock rates may be selected using the VID_STD[5:0] pins of the device. Section 1.4 on page 20 lists the video formats available using the VID_STD[5:0] pins.

If desired, the external VID_STD[5:0] pins may be ignored by setting bit 1 of the Video_Control register, and the video standard may instead be selected via the VID_STD[5:0] register of the host interface (see Section 3.10.3 on page 66). Although the external VID_STD[5:0] pins will be ignored, they should not be left floating.

Once the video clock has been generated, it will be presented to the application layer via the PCLK1 to PCLK3 pins. By default, each of the 3 video clock outputs will produce the generated fundamental clock frequency. However, it is possible to select other rates for each PCLK output by programming the PCLK_Phase/Divide registers beginning at address 2Ch of the host interface (see Section 3.10.3 on page 66).

Each PCLK output may be individually programmed to provide one of the following:

- PCLK fundamental frequency
- Fundamental frequency /2
- Fundamental frequency /4

When all six VID_STD[5:0] pins are set LOW, the video clocks will be disabled. PCLK1 and PCLK2 will go LOW and PCLK3/$\overline{\text{PCLK3}}$ will be high impedance.

NOTE: If the PCLK divider bits of registers 2Ch - 2Eh are set to enable a divide by 2 or divide by 4, the resultant divided clock will align with the falling edge of the output H Sync timing signal either on its rising or falling edge.

The PCLK1 to PCLK3 outputs may also be individually delayed with respect to the eight TIMING_OUT signals to allow for skew control downstream from the GS4901B/GS4900B. Using the PCLK_Phase/Divide registers, the phase of each clock may be delayed up to a nominal 10.3ns in 16 steps of approximately 700ps each (Table 3-6). This delay is available in addition to the genlock timing offset phase adjustment described in Section 3.2.1 on page 35.

**Table 3-6: Video Clock Phase Adjustment Host Settings**

| PCLKn_Phase[3:0] Setting | 0h | 1h | 2h | 3h | 4h | 5h | 6h | 7h | 8h | 9h | Ah | Bh | Ch | Dh | Eh | Fh |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Phase Increment (ns) | 0 | 0.7 | 1.4 | 2.1 | 2.8 | 3.5 | 4.2 | 4.9 | 5.6 | 6.3 | 7.0 | 7.7 | 8.4 | 9.1 | 9.8 | 10.3 |

NOTES:

1. The phase increments listed above are nominal values.
2. The phase of PCLK is delayed relative to the TIMING_OUT pins.

Additionally, the current drive capability of PCLK1 and PCLK2 may be set high or low using the PCLK_Phase/Divide registers. By default the current drive will be low.

## 3.7.2 Audio Clock Synthesis (GS4901B only)

The audio clock generator is referenced to the internal PCLK signal and is responsible for generating the ACLK output signals. Three audio clock output pins, ACLK1 to ACLK3, are available to the application layer.

The fundamental sampling frequency, fs, is selected using the ASR_SEL[2:0] pins as shown in Table 3-7.

If desired, the external ASR_SEL[2:0] pins may be ignored by setting bit 2 of the Audio_Control register and the sampling frequency may instead be programmed in the ASR_SEL[2:0] register of the host interface (see Section 3.10.3 on page 66). Although the external ASR_SEL[2:0] pins will be ignored, they should not be left floating.

**Table 3-7: Audio Sample Rate Select**

| ASR_SEL[2:0] | Sampling Frequency (kHz) |
|---|---|
| 000 | Audio Clock Generation Disabled |
| 001 | 32 |
| 010 | 44.1 |
| 011 | 48 |
| 100 | 96 |
| 101 | Slow 32* |
| 110 | Slow 44.1* |
| 111 | Slow 48* |

*Slow 32, 44.1, and 48 are available only when the video standard selected is 23.98, 29.97, or 59.94 frame rate based. They refer to 32kHz, 44.1kHz, or 48kHz multiplied by 1000/1001 to maintain the 1, 2, or 3 frame sequence normally associated with 24, 30, and 60 fps video.

When all three ASR_SEL[2:0] pins are set LOW, the audio clock outputs will be high impedance. In this case, the application layer may continue to power the AUD_PLL_VDD pin; however, to minimize noise and power consumption, AUD_PLL_VDD may be grounded.

By default, after system reset, ACLK1 to ACLK3 will output clock signals at 256fs, 64fs, and fs respectively. Different division ratios for each output pin may be selected by programming the ACLK_fs_Multiple registers beginning at address 3Fh of the host interface (see Section 3.10.3 on page 66). The encoding of this register is shown in Table 3-8. Clock outputs of 512fs, 348fs, 256fs, 192fs, 128fs, 64fs, fs, and z bit are selectable on a pin by pin basis. The z bit will go HIGH for one fs period every 192 fs periods. Its phase is not defined by any timing event in the GS4901B, and so is arbitrary.

**Table 3-8: Audio Clock Divider**

| ACLKn_fs_Multiple[3:0] | Audio Clock Frequency |
|---|---|
| 000 | fs |
| 001 | 64fs |
| 010 | 128fs |
| 011 | 192fs* |
| 100 | 256fs |
| 101 | 384fs* |
| 110 | 512fs** |
| 111 | z-bit |

*This setting is only available when the enable_384fs bit of the Audio_Control register is HIGH.
**512fs clock will have a 33% duty cycle when the enable_384fs bit is HIGH and fs = 96kHz.

The fs signal on ACLK1-3 has an accurate 50% duty cycle, and can be used for left/right definition, with the following exception: if fs = 96kHz and the user configures the host interface such that one of the three ACLK pins is set to output a clock signal at 192fs or 384fs, the 512fs clock will have a 33% duty cycle.

All audio clocks are initially reset on the rising edge of the AFS pulse, ensuring that video to audio clock synchronization is correct. During normal operation, the audio clock edge is allowed to drift slightly with respect to the AFS pulse. By default, the audio clock will be reset directly by the AFS pulse if it drifts more than approximately +/-0.1us from the rising edge of the AFS pulse. However, after device reset, or after the application of a new input reference, the ACLK outputs may sometimes be offset from the AFS pulse by up to several microseconds. The offset will remain until the device is reset or the reference removed and re-applied. The user may avoid this offset by minimizing the width of the AFS_Reset_Window using bits 9-7 of register 31h for the duration of the audio PLL locking process. Once the audio PLL is locked, bit 1 of register 1Fh will be set HIGH, and the AFS_Reset_Window may be set as desired. See Table 3-9.

**Table 3-9: Encoding Scheme for AFS_Reset_Window**

| AFS_Reset_Window (address 31h) | Window Tolerance (us) | | | | |
|---|---|---|---|---|---|
| | fs = 32kHz | fs = 44.1kHz | fs = 48 kHz | fs = 96 kHz (enable_384fs = 1) | fs = 96 kHz (enable_384fs = 0) |
| 000 | 0.044 | 0.033 | 0.030 | 0.030 | 0.044 |
| 001 | 0.084 | 0.062 | 0.057 | 0.057 | 0.084 |
| 010 (default) | 0.166 | 0.121 | 0.112 | 0.112 | 0.166 |
| 011 | 0.329 | 0.239 | 0.220 | 0.220 | 0.329 |
| 1XX | 0.654 | 0.475 | 0.437 | 0.437 | 0.654 |

NOTE: ‘X’ signifies ‘don’t care.’ The bit setting will be ignored.

### 3.7.2.1 Audio to Video Clock Phasing

The important aspect of the audio to video phase relates to the way in which the AFS pulse is used to reset the audio clock dividers so as to line up the leading edge of the audio clocks with the leading edge of the H Sync pulse on line 1 of the first field in the audio frame sequence. The AFS pulse is further discussed in Section 3.8.2 on page 58.

#### 625i 50 Format

For the 48kHz sampling rate, the audio to video phase relationship for 625/50i reference signals is provided by the device in accordance with the EBU recommended practice R83-1996. The start of an audio frame (fs clock) will align with the 50% point of the H sync input of line 1 of each video frame (+/- the allowable drift specified in Table 3-9).

### 525i 59.94 Format

For 525/59.94 NTSC reference signals, the device will observe the 5-frame phase-relationship inherent with this video standard, aligning the audio clocks with the 50% point of the H sync input of line 1 on every fifth frame (+/- the allowable drift specified in Table 3-9).

The number of audio sample clocks during a video frame is shown in Table 3-10 for 32, 44.1, and 48kHz audio sampling frequencies.

**Table 3-10: Audio Sampling Frequency to Video Frame Rate Synchronization**

| | Audio Samples per Video Frame | | | | | | |
|---|---|---|---|---|---|---|---|
| Audio Sample Rate (kHz) | 24fps | 25fps | 29.97fps | 30fps | 50fps | 59.94fps | 60fps |
| 32 | 4000/3 | 1280 | 16016/15 | 3200/3 | 640 | 8008/15 | 1600/3 |
| 44.1 | 3675/2 | 1764 | 147147/100 | 1470 | 882 | 147147/200 | 735 |
| 48 | 2000 | 1920 | 8008/5 | 1600 | 960 | 4004/5 | 800 |

* fps = frames per second.

The external 10FID input pin may be used to resynchronize other audio clock frequencies, according to Table 3-10, by applying an active signal during the reference HSYNC of line 1 of the appropriate video frame. Please see Section 3.4.2 on page 41 for more details on the 10FID input pin.

In the case where 10FID is not present as a reference signal, the GS4901B will automatically generate an AFS pulse appropriate to the format selected, and use it to create an audio frame sequence.

### Host Interface Control of AFS and 10FID

Alternatively, the user may program the device via the host interface to re-time the audio frame sequence and 10 field-ID. Using register 1Ah, a pulse may be generated to reset the AFS and/or 10FID dividers at the start of an output video frame (see Section 3.10.3 on page 66).

If using the host interface to reset the AFS pulse, the device may be configured to ignore the input 10FID reference pin. To disable the signal on the external 10FID pin from resetting the AFS output pulse, set bit 0 of the Audio_Control register HIGH.

If using the host interface to reset the 10FID pulse, the external 10FID pin must be grounded.

## 3.8 Video Timing Generator

The internal PCLK signal generated by the clock synthesis circuit is used to produce horizontal, vertical, and frame based timing output signals.

The signals generated and available to the application layer via the TIMING_OUT pins are: H Sync, H Blanking, V Sync, V Blanking, F Sync, F Digital, DE, 10FID, AFS (GS4901B only), and USER_1~4. These signals are defined in Section 1.5 on page 24. Additional information pertaining to the 10FID, AFS, and USER_1~4 signals can be found in the sub-sections below.

When the GS4901B/GS4900B is operating in Genlock mode, the H, V, and F based output timing signals are synchronized to the H, V, and F reference signals applied to the inputs by the application layer. The video timing outputs may be offset from the input reference by programming the Genlock Offset registers beginning at address 1Bh of the host interface (see Section 3.2.1.1 on page 35).

All TIMING_OUT signals have selectable polarity. The default polarities for each signal are given in the descriptions in Section 1.5 on page 24.

### 3.8.1 10 Field ID Pulse

As described in Table 1-3, the 10 field ID (10FID) output signal is used in the identification of film to video cadence. It is only generated for 29.97, 30, 59.94, and 60fps formats.

The 10FID pulse is generated on every 5$^{th}$ frame for 29.97 and 30fps formats, and every 10$^{th}$ frame on 59.94 and 60fps formats.

By default, the 10FID signal is set HIGH on the leading edge of the H Sync output for the duration of line 1 of field 1 at the start of the 10 field sequence. This is shown in Figure 3-6.

Alternatively, by setting bit 4 of the Video_Control register at address 4Ch of the host interface, the 10FID output signal may be configured to go HIGH (default polarity) on the leading edge of the H Sync pulse of line 1 of the first field in the 10 field sequence, and be reset LOW on the leading edge of the H Sync pulse of line 1 of the second field in the 10 field sequence. This is shown in Figure 3-7.

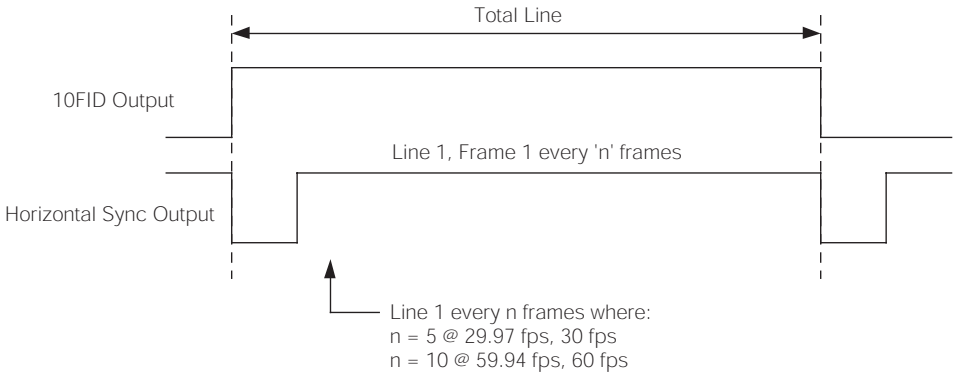



**Figure 3-6: Default 10FID Output Timing**

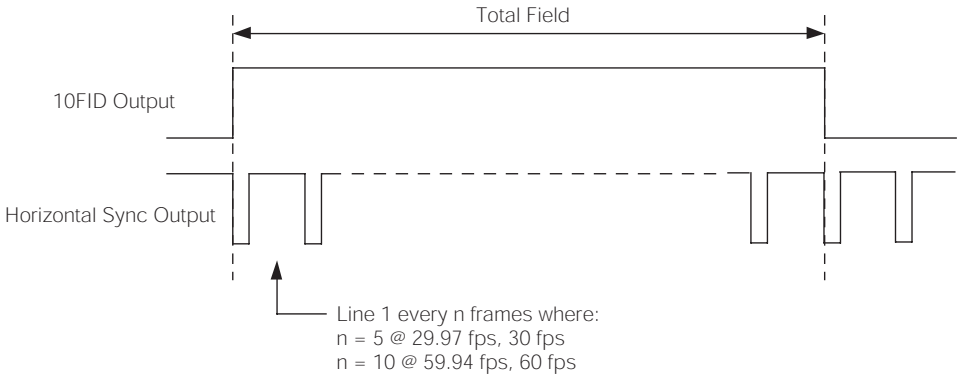



**Figure 3-7: Optional 10FID Output Timing**

The phasing of the divide by n frame counter may be reset by an external pulse on the 10FID input pin, or via register 1Ah of the host interface (see Section 3.10.3 on page 66).

NOTE: If a 10FID input signal is not provided to the device, the 10FID output signal will be invalid until the user initiates a reset via the host interface. The user should also reset the 10FID signal via the host if at any time the H input reference signal is removed and then re-applied.

## 3.8.2 Audio Frame Synchronizing Pulse (GS4901B only)

As described in Table 1-3, the audio frame synchronizing (AFS) pulse identifies the frame, within an n frame sequence, in which the audio sample rate clock is aligned with the H Sync of line 1. It is generated for all video formats.

The leading edge of the AFS output pulse is co-timed with the H Sync corresponding to line 1 of every $n^{th}$ frame in the sequence, and therefore identifies the exact time at which the audio sample rate clock and video PCLK have synchronous leading edges.

The number of frames in the sequence, n, is determined by the video frame rate and the audio clock frequency. These are selected using the VID_STD[5:0] and ASR_SEL[2:0] pins or via the host interface.

By default, the AFS pulse is 1 line long, as shown in Figure 3-8. Alternatively, by setting bit 1 of the Audio_Control register, the AFS output signal may be configured to go HIGH on the leading edge of the H Sync pulse of line 1 of the first field in the ‘n’ frame sequence, and be reset LOW on the leading edge of the H Sync pulse of line 1 of the second field in the sequence. The AFS timing in this configuration is similar to the 10FID optional timing shown in Figure 3-7.

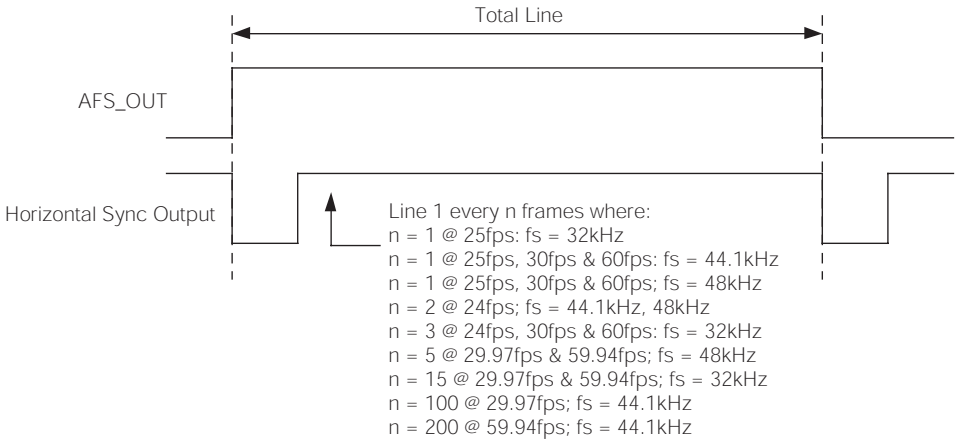



**Figure 3-8: AFS Output Timing**

The phasing of the divide by n counter can be controlled by the 10FID input or via designated registers in the host interface.

By default, the 10FID input pin controls the AFS phase (in addition to controlling the 10FID phase); however, this feature may be disabled by setting bit 0 of the Audio_Control register (see Section 3.10.3 on page 66). In addition, the AFS signal may be reset via register 1Ah.

### 3.8.3 USER_1~4

As described in Table 1-3, the GS4901B/GS4900B offers 4 user programmable output signals which are available independent of the selected output video format.

Each user signal is individually programmable and the polarity, position, and width of each output may be defined with respect to the digital output timing of the device. Each output signal may be programmed in both the horizontal and vertical dimensions relative to the leading edges of H Blanking and V Blanking. If desired, the pulses produced may then be combined with a logical AND, OR, or XOR function to produce a composite signal (for example, a horizontal back porch pulse during active lines only, or the active part of lines 15 through 20 for vertical information retrieval).

By default, the AND, OR, and XOR functions are disabled. Therefore, when a USER signal is selected using the Output_Select registers of the host interface, the signal will go LOW (default polarity) at the H_Start pixel and return HIGH after the H_Stop pixel. Setting the AND bit HIGH, for example, will cause the USER signal to be active only when USER_H is active and USER_V is active (i.e. the pixel is between both H_Start and H_Stop and V_Start and V_Stop). See Figure 3-9.

NOTE: The effective horizontal range of the four user-defined timing signals is [H_Start + 1, H_Stop], except when H_Start = 1, in which case the range is [H_Start, H_Stop]. This prevents the user from specifying an output USER signal that begins on pixel 2 of a line.

In the case of interlaced output formats, the programmed vertical start and stop lines refer to the start and stop lines of the generated USER signal on the odd fields. The start and stop lines of the USER signal on the even fields will be V_Start - 1 and V_Stop - 1, respectively.

For example, if VID_STD[5:0] = 3, the odd fields will have 263 lines and the even fields will have 262 lines. A user-defined vertical pulse programmed to start on line 12 and stop on line 17 will start on frame lines 12 and 274, and stop on frame lines 17 and 279.

The designated registers for programming each user signal are located in the host interface beginning at address 57h. See Section 3.10.3 on page 66.

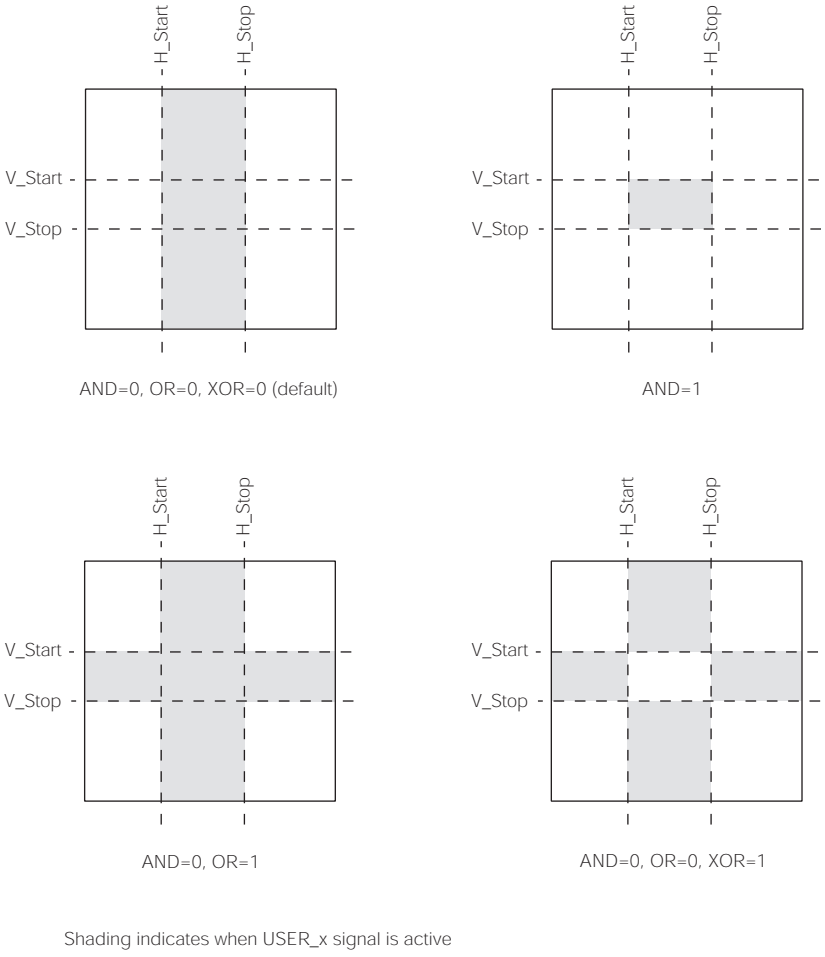



**Figure 3-9: USER Programmable Output Signal**

## 3.8.4 TIMING_OUT Pins

The horizontal, vertical, and frame based timing output signals for the selected video format are available to the application layer via the TIMING_OUT_1 to TIMING_OUT_8 pins.

### Programmable Crosspoint Switch

Each TIMING_OUT pin outputs a default signal as shown in Table 1-3. Alternatively, a crosspoint switch may be programmed via the eight Output_Select registers of the host interface, allowing the user to select which output signal is directed to each TIMING_OUT pin (see Section 3.10.3 on page 66). Any signal may be sent to more than one pin if desired.

Table 3-11 outlines the encoding scheme of the eight Output_Select registers, which begin at address 43h of the host interface.

**Table 3-11: Crosspoint Select**

| Output_Select_n Bit Settings | Output Signal |
|---|---|
| 0000 | High Impedance |
| 0001 | H Sync |
| 0010 | H Blanking |
| 0011 | V Sync |
| 0100 | V Blanking |
| 0101 | F Sync |
| 0110 | F Digital |
| 0111 | 10FID |
| 1000 | DE |
| 1001 | Reserved |
| 1010 | AFS* |
| 1011 | USER_1 |
| 1100 | USER_2 |
| 1101 | USER_3 |
| 1110 | USER_4 |
| 1111 | Reserved |

*AFS is only available on the GS4901B. The bit setting 1010b will be ignored by the GS4900B.

### 3.8.4.1 Selectable Current Drive and Polarity

The current-drive of each timing output pin is also selectable via the Output_Select registers. The current drive of each TIMING_OUT pin is low by default. However, it may be set high to accommodate certain applications.

Additionally, the Polarity register of the host interface may be programmed to select the polarity of each timing output signal.

## 3.9 Extended Audio Mode for HD Demux using the Gennum Audio Core

The GS4901B/GS4900B has been designed to interface with Gennum's FPGA Audio Core in order to provide a 24.576MHz clock (512 * 48kHz) locked to the audio clock contained in the embedded audio data packets of an HD-SDI stream. It is the responsibility of the user to divide this clock by 4 to obtain the 6.144MHz required by the core.

In HD Demux mode, the FPGA Audio Core will extract an audio clock from the embedded audio data packets and present a 24kHz clock to the GS4901B/GS4900B via the aclkdiv2a (for Group A) and aclkdiv2b (for Group B) outputs. The embedded clock must be 48kHz.

The 24kHz reference signals for each audio group must be applied to the HSYNC input pin of a GS4901B/GS4900B, while a divided version of this signal must be applied to the VSYNC input pin. The divided signal must meet the requirements for VSYNC validity given in Section 3.5.2 on page 43. It is recommended that the VSYNC signal be generated by dividing the 24kHz reference applied to HSYNC by 512 to give 46.875Hz.

To enable the extended audio mode, the user must do the following:

1. Set VID_STD[5:0] = 4d.
2. Set the F_Lock_Mask and V_Lock_Mask bits [4:3] of register address 16h to 1.
3. Set the Ext_Audio_Mode register address 81h to 20C1h.
4. Toggle bit [6] of register address 16h.

In this mode, the GS4901B/GS4900B will produce a 24.576MHz clock on its PCLK output pins that is locked to the 24kHz extracted audio clock reference applied to HSYNC. It will not lock to any other reference frequency. The user may then divide this frequency by 4 using the programmable dividers in the GS4901B/GS4900B.

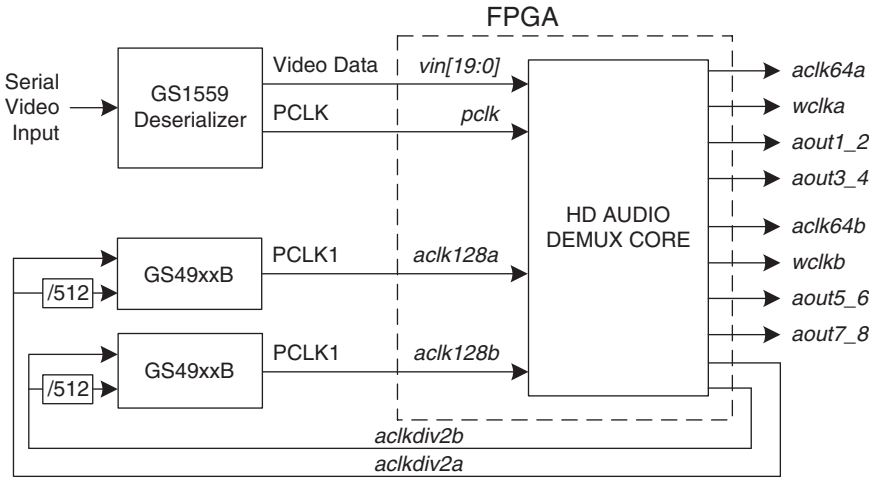



**Figure 3-10: Audio Clock Block Diagram for HD Demux Operation**

## 3.10 GSPI Host Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the host to enable additional features of the GS4901B/GS4900B and/or to provide additional status information through configuration registers in the device.

The GSPI comprises a serial data input signal, SDIN, a serial data output signal, SDOUT, an active low chip select, $\overline{CS}$, and a burst clock, SCLK. The burst clock must have a duty cycle between 40% and 60%.

Because these pins are shared with the JTAG interface port, an additional control signal pin, JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin is a non-clocked loop-through of SDIN and may be connected to the SDIN pin of another device, allowing multiple devices to be connected to the GSPI chain. The interface is illustrated in Figure 3-11.

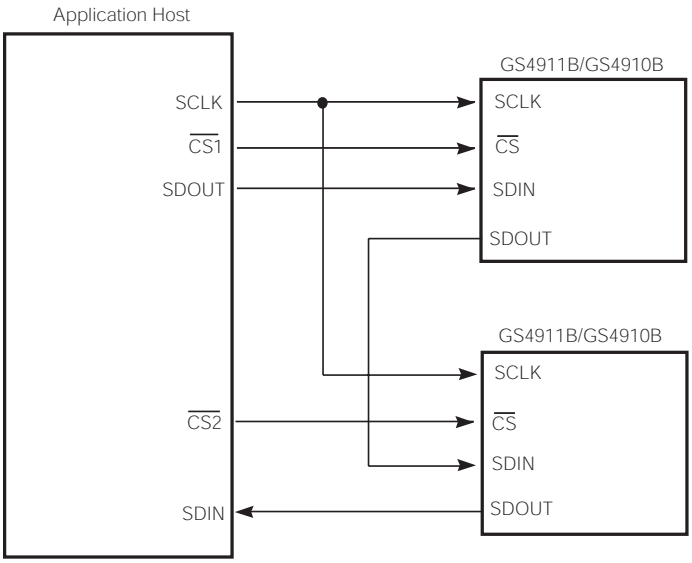



**Figure 3-11: GSPI Application Interface Connection**

All read or write access to the GS4901B/GS4900B is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

### 3.10.1 Command Word Description

The command word consists of 16 bits transmitted MSB first and includes a read/write bit, an Auto-Increment bit and a 12-bit address. Figure 3-12 shows the command word format and bit configurations.

Command words are clocked into the GS4901B/GS4900B on the rising edge of the serial clock, SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each command word must be followed by only one data word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following data word will be written into the address specified in the command word, and subsequent data words will be written into incremental addresses. This facilitates multiple address writes without sending a command word for each data word.

Auto-Increment may be used for both read and write access.

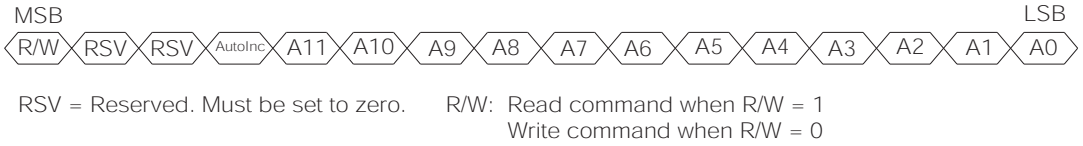



**Figure 3-12: Command Word Format**

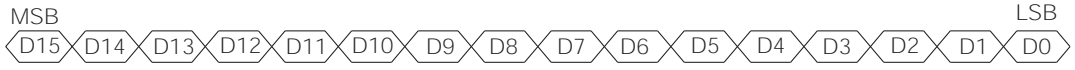



**Figure 3-13: Data Word Format**

### 3.10.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 3-14 and Figure 3-15 respectively. The timing parameters are defined in Table 3-12.

When several devices are connected to the GSPI chain, only one $\overline{CS}$ should be asserted during a read sequence.

During the write sequence, all command and following data words input at the SDIN pin are output at the SDOUT pin as is. Where several devices are connected to the GSPI chain, data can be written simultaneously to all the devices that have $\overline{CS}$ set LOW.

**Table 3-12: GSPI Timing Parameters**

| Parameter | Definition | Specification |
|---|---|---|
| $t_0$ | The minimum duration of time chip select, $\overline{CS}$, must be LOW before the first SCLK rising edge. | 1.5 ns |
| $t_1$ | The minimum SCLK period. | 100 ns |
| $t_2$ | Duty cycle tolerated by SCLK. | 40% to 60% |
| $t_3$ | Minimum input setup time. | 1.5 ns |
| $t_4$ | The minimum duration of time between the last SCLK command word (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word (write cycle). | 37.1 ns |
| $t_5$ | The minimum duration of time between the last SCLK command word (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word (read cycle). | 148.4 ns |
| $t_6$ | Minimum output hold time (15pF load). | 1.5 ns |
| $t_7$ | The minimum duration of time between the last SCLK of the GSPI transaction and when $\overline{CS}$ can be set HIGH. | 37.1 ns |
| $t_8$ | Minimum input hold time. | 1.5 ns |

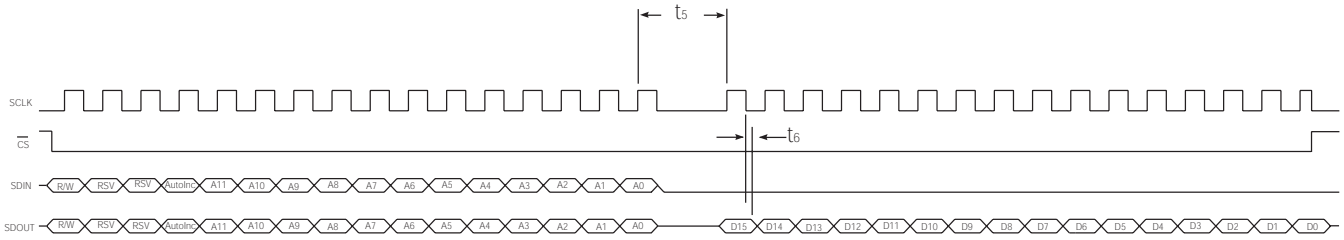



**Figure 3-14: GSPI Read Mode Timing**

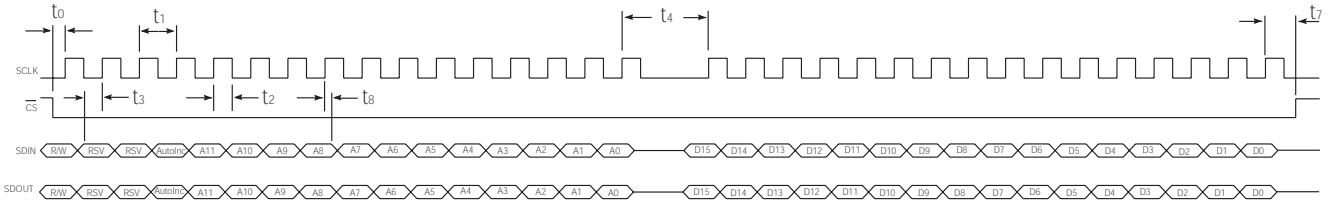



**Figure 3-15: GSPI Write Mode Timing**

### 3.10.3 Configuration and Status Registers

Table 3-13 summarizes the GS4901B/GS4900B's internal status and configuration registers.

All registers are available to the host via the GSPI and are all individually addressable.

**Table 3-13: Configuration and Status Registers**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| RSVD | 00h - 09h | – | Reserved. | – | – |
| H_Period | 0Ah | 15-0 | Contains the number of 27MHz pulses in the input H Sync period. This register is set by the Reference Format Detector block using the H Sync signal present on the external HSYNC input pin.<br>NOTE: If the reference is removed this register will remain unchanged until a new reference with a different HSYNC period is applied.<br>Reference: Section 3.5.1 on page 42 | R | N/A |
| H_16_Period | 0Bh | 15-0 | Contains the number of 27MHz pulses in 16 H Sync periods. This register is set by the Reference Format Detector block using the H Sync signal present on the external HSYNC input pin. It is useful for 1/1.001 data detection.<br>NOTE: If the reference is removed this register will remain unchanged until a new reference with a different HSYNC period is applied.<br>Reference: Section 3.5.1 on page 42 | R | N/A |
| V_Lines | 0Ch | 15-0 | Contains the number of H Sync periods in the input V Sync interval. This register is set by the Reference Format Detector block using the signals present on the external HSYNC and VSYNC input pins.<br>NOTE: If the reference is removed this register will remain unchanged until a new reference with a different VSYNC period is applied.<br>Reference: Section 3.5.1 on page 42 | R | N/A |
| V_2_Lines | 0Dh | 15-0 | Contains the number of H Sync periods in 2 V Sync intervals. This register is set by the Reference Format Detector block using the signals present on the external HSYNC and VSYNC input pins.<br>NOTE: If the reference is removed this register will remain unchanged until a new reference with a different VSYNC period is applied.<br>Reference: Section 3.5.1 on page 42 | R | N/A |
| F_Lines | 0Eh | 15-0 | Contains the number of H Sync periods in the input F Sync interval. This register is set by the Reference Format Detector block using the signals present on the external HSYNC and FSYNC input pins.<br>NOTE: If the reference is removed this register will remain unchanged until a new reference is applied. If the new reference does not include an FSYNC pulse, this register will be set to zero.<br>Reference: Section 3.5.1 on page 42 | R | N/A |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Input_Standard | 0Fh | 15-13 | Reserved. Set these bits to zero when writing to 0Fh. | – | – |
| | 0Fh | 12 | Force_Input - Set this bit HIGH to force the GS4901B/GS4900B to recognize the applied input reference format as the standard programmed in bits 11-6 of this register. | R/W | 0 |
| | 0Fh | 11-6 | Forced_Standard - When bit 12 is set HIGH, the GS4901B/GS4900B will use the value programmed in these bits, rather than the value in bits 5-0, to determine the input reference format. The 6-bit value programmed here should always correspond to the VID_STD[5:0] value of the applied reference.<br>These bits should not be programmed for normal operation. | R/W | 0 |
| | 0Fh | 5-0 | Detected_Standard - Contains the video standard applied to the input reference pins once it has been detected. These bits are set by the Reference Format Detector block and correspond to the VID_STD[5:0] value of the standard as listed in Table 1-2.<br>The Detected_Standard bits will be set to zero if no input reference signal is applied or if the input reference signal is not an automatically recognized video format. Otherwise the value will be between 1 and 54.<br>Reference: Section 3.5.2 on page 43 | R/W | N/A |
| Amb_Std_Sel | 10h | 15-11 | Reserved. Set these bits to zero when writing to 10h. | – | – |
| | 10h | 10-0 | The user may set this register to distinguish between different formats that look identical to the internal Reference Format Detector block. See Table 3-2.<br>Reference: Section 3.5.2.1 on page 43 | R/W | 0 |
| Reference_Standard_Disable | 13h-11h | 38-0 | The Reference_Standard_Disable register may be used to disable/enable one or more of the input standards given in Table 1-2 from being recognized by the device and used to genlock the output. This is done by setting the bit HIGH that corresponds to the VID_STD[5:0] value of the video format.<br>For example, if bit 5 is set HIGH, then the output clock and timing signals will not genlock to an input reference with timing corresponding to VID_STD[5:0] = 5 in Table 1-2.<br>Likewise, to enable recognition of VID_STD[5:0] = 26 (1080i/59.94) as an input reference format, the user must set bit 26 LOW.<br>Address 13h = bits 38-32*<br>Address 12h = bits 31-16<br>Address 11h = bits 15-0<br>*Bits 47-39 of address 13h should always be written HIGH.<br>Reference: Section 3.5 on page 42 | R/W | FFFFh<br>FFFFh<br>F800h |
| RSVD | 14h | – | Reserved | – | – |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Genlock_Status | 15h | 15-6 | Reserved. | – | – |
| | 15h | 5 | Reference_Lock - this bit will be HIGH when the output is successfully genlocked to the input (i.e. when bits 4-1 of this register are HIGH and are not masked by bits 4-2 of register 16h).<br>The LOCK_LOST output pin is an inverted copy of this bit.<br>Reference: Section 3.6.1 on page 47 | R | N/A |
| | 15h | 4 | F_Lock - this bit will be HIGH when the output F is successfully genlocked to the FSYNC input.<br>NOTE: If the input reference does not include an FSYNC input, this bit will have the same setting as V_Lock (bit 3).<br>Reference: Section 3.6.1 on page 47 | R | N/A |
| | 15h | 3 | V_Lock - this bit will be HIGH when the output V is successfully genlocked to the VSYNC input.<br>Reference: Section 3.6.1 on page 47 | R | N/A |
| | 15h | 2 | H_Lock - this bit will be HIGH when the output H is successfully genlocked to the HSYNC input.<br>Reference: Section 3.6.1 on page 47 | R | N/A |
| | 15h | 1 | Clock_Lock - this bit will be HIGH when the video clock is locked to the internal V_pll AND the audio clock is locked to the internal A_pll (i.e. bits 0 and 1 of register 1Fh are HIGH).<br>Reference: Section 3.6.1 on page 47 | R | N/A |
| | 15h | 0 | Reference_Present - this bit will be HIGH when a valid input reference signal has been applied to the device. The REF_LOST output pin is an inverted copy of this bit.<br>Reference: Section 3.5.2 on page 43 | R | N/A |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Genlock_Control | 16h | 15-7 | Reserved. Set these bits to zero when writing to 16h. | – | – |
| | 16h | 6 | This bit is used to enable the Extended Audio Mode of the device. | R/W | 0 |
| | 16h | 5 | Genlock_From_Host - set this bit HIGH to enable video genlock control via the Host Interface instead of the external $\overline{\text{GENLOCK}}$ pin (see bit 0 of this register).<br>Reference: Section 3.2 on page 34 | R/W | 0 |
| | 16h | 4 | F_Lock_Mask - if this bit is set HIGH, the GS4901B/GS4900B will ignore the status of F_Lock (bit 4 of register 15h) when determining the status of Reference_Lock (bit 5 of register 15h).<br>Reference: Section 3.6.1 on page 47 | R/W | 0 |
| | 16h | 3 | V_Lock_Mask - if this bit is set HIGH, the GS4901B/GS4900B will ignore the status of V_Lock (bit 3 of register 15h) when determining the status of Reference_Lock (bit 5 of register 15h).<br>Reference: Section 3.6.1 on page 47 | R/W | 0 |
| | 16h | 2 | H_Lock_Mask - if this bit is set HIGH, the GS4901B/GS4900B will ignore the status of H_Lock (bit 2 of register 15h) when determining the status of Reference_Lock (bit 5 of register 15h).<br>Reference: Section 3.6.1 on page 47 | R/W | 0 |
| | 16h | 1 | Drift_$\overline{\text{Crash}}$ - when this bit is set HIGH, the generated video clock will drift lock to a new input reference rather than crash lock.<br>Reference: Section 3.6.1 on page 47 | R/W | 0 |
| | 16h | 0 | $\overline{\text{GENLOCK}}$ - this bit may be used instead of the external pin to Genlock the output video format to the input reference. This bit will be ignored if bit 5 of this register is LOW.<br>Reference: Section 3.2 on page 34 | R/W | 0 |
| RSVD | 17h-19h | – | Reserved | – | – |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| 10FID_AFS_Reset | 1Ah | 15-4 | Reserved. Set these bits to zero when writing to 1Ah. | – | – |
| | 1Ah | 3 | AFS_Reset (GS4901B only) - set this bit HIGH to use Reset_Sync (bit 0 of register 1Ah) to reset the output AFS pulse.<br>NOTE: This bit will remain LOW in the GS4900B. Set this bit LOW when writing to address 1Ah of the GS4900B.<br>Reference: Section 3.7.2.1 on page 55 | R/W | 0 |
| | 1Ah | 2 | 10FID_Reset - set this bit HIGH to use Reset_Sync (bit 0 of register 1Ah) to reset the output 10FID pulse.<br>NOTE: If a 10FID input signal is not provided to the device, the user must generate a reset using this bit to initiate the 10FID timing output. In this case, the 10FID input pin must be grounded.<br>Reference: Section 3.7.2.1 on page 55 | R/W | 0 |
| | 1Ah | 1 | Reserved. Set this bit to zero when writing to 1Ah. | – | – |
| | 1Ah | 0 | Reset_Sync - resets the pulses described in bits 2, and 3 above.<br>The reset pulse is generated if this bit is pulsed (LOW to HIGH to LOW) during the output frame immediately prior to the frame the reset is to occur. This reset will operate independently of any other resets, for example from the reference input. | R/W | 0 |
| H_Offset | 1Bh | 15-0 | The output H signal may be delayed with respect to the input reference by the number of pixels programmed in this register. (See Section 3.2.1.1 on page 35).<br>The value programmed in this register should not exceed the maximum number of clock periods per line of the outgoing standard. Horizontal advances may be achieved by programming a value equal to the maximum allowable offset minus the desired advance.<br>NOTE: This register is internally read by the device once per field. At that time any new value programmed is sent to the internal offset circuitry.<br>Reference: Section 3.2.1.1 on page 35 | R/W | 0 |
| V_Offset | 1Ch | 15-0 | The output V signal may be delayed with respect to the input reference by the number of lines programmed in this register. (See Section 3.2.1.1 on page 35).<br>The value programmed in this register should not exceed the maximum number of lines per frame of the outgoing standard. Vertical advances may be achieved by programming a value equal to the maximum allowable offset minus the desired advance.<br>NOTE: This register is internally read by the device once per field. At that time any new value programmed is sent to the internal offset circuitry.<br>Reference: Section 3.2.1.1 on page 35 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Clock_Phase_Offset | 1Dh | 15-0 | Phase_Offset - The output clock and data phase may be offset with respect to the input reference by the number of increments programmed in this register. The increment step size depends on the video clock frequency.<br>The encoding scheme for this register is shown in Table 3-1.<br>NOTE: This register must be cleared to achieve a clock phase offset of zero.<br>Reference: Section 3.2.1.1 on page 35 | R/W | 0 |
| Max_Ref_Delta | 1Eh | 15-0 | The value programmed in this register controls the allowed deviance from the expected frequency on the reference HSYNC before the internal video PLL loses lock. The encoding scheme is shown in Table 3-3.<br>Reference: Section 3.5.4 on page 46 | R/W | 000Bh |
| Video_Status | 1Fh | 15-5 | Reserved. | – | – |
| | 1Fh | 4 | Ref_H_Polarity - status register to indicate the detected H Sync polarity ('1' for positive, '0' for negative).<br>This bit will be zero when no reference signal is present.<br>Reference: Section 3.4.3 on page 41 | R | N/A |
| | 1Fh | 3 | Ref_V_Polarity - status register to indicate the detected V Sync polarity ('1' for positive, '0' for negative).<br>This bit will be zero when no reference signal is present and for digital blanking input references.<br>Reference: Section 3.4.3 on page 41 | R | N/A |
| | 1Fh | 2 | Ref_Blank_Timing - status register to indicate the input detection of H blanking vs. H sync timing (‘1’ for blanking, '0' for sync timing).<br>This bit will be zero when no reference signal is present.<br>Reference: Section 3.4.3 on page 41 | R | N/A |
| | 1Fh | 1 | A_pll_Lock (GS4901B only)- this bit will be HIGH when the generated audio clock is locked to the video clock reference.<br>NOTE: This bit will remain high in the GS4900B.<br>Reference: bit 1 of register 15h. | R | N/A |
| | 1Fh | 0 | V_pll_Lock - this bit will be HIGH when the generated video clock is locked to the H Sync input reference.<br>Reference: bit 1 of register 15h. | R | N/A |
| RSVD | 20h-23h | – | Reserved | – | – |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Constcf_Genlock | 24h | 15-8 | Crash_Time - controls the crash lock period of video PLL locking process. This time contributes to the total PLL Lock Time given in the AC Characteristics Table.<br>The time of the crash process in H reference periods is determined by [Crash_Time x 4] + 1.<br>The default value of these bits will vary depending on the output video standard selected.<br>Reference: Section 3.6.1 on page 47 | R/W | – |
| | 24h | 7-3 | Lock_Lost_Threshold - controls the threshold of the lock indication circuit. A larger value programmed in this register can increase the stability of the LOCK_LOST output signal when the input H reference signal is subject to large amounts of low frequency jitter. A larger value in this register will also increase the lock indication time, although not the actual lock time of the device.<br>The default value of these bits will vary depending on the output video standard selected. | R/W | – |
| | 24h | 2-0 | Run_Window - controls the output frequency error in the case of a missing or mis-timed H reference transition. The default value of this register allows the device to maintain genlock through one missing input H pulse.<br>This feature can be disabled by programming Run_Window = 000b. In this case, the device will immediately react to any disturbance of the input H signal.<br>The default value of these bits will vary depending on the output video standard selected.<br>Reference: Section 3.5.3 on page 44 | R/W | – |
| RSVD | 25h | – | Reserved. | – | – |
| Video_Cap_Genlock | 26h | 15-6 | Reserved. Set these bits to zero when writing to 26h. | – | – |
| | 26h | 5-0 | Control signal to adjust loop bandwidth of video genlock block.<br>The value programmed in this register must be between 10 and Video_Res_Genlock - 21.<br>The default value of this register will vary depending on the output video standard selected.<br>Reference: Section 3.6.2 on page 48 | R/W | – |
| Video_Res_Genlock | 27h | 15-6 | Reserved. Set these bits to zero when writing to 27h. | – | – |
| | 27h | 5-0 | Control signal to adjust loop bandwidth of video genlock block.<br>The value programmed in this register must be between 32 and 42.<br>The default value of this register will vary depending on the output video standard selected.<br>Reference: Section 3.6.2 on page 48 | R/W | – |
| RSVD | 28h-2Bh | – | Reserved | – | – |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| PCLK1_Phase/Divide | 2Ch | 15-7 | Reserved. Set these bits to zero when writing to 2Ch. | – | – |
| | 2Ch | 6 | Current_P1 - selects the current drive capability of the PCLK1 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Ch | 5-2 | PCLK1_Phase - adjusts the output phase of the PCLK1 clock with respect to the timing output pins. Phase is delayed in 700ps (nominal) increments as shown in Table 3-6.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Ch | 1 | Divide_By_4 - set this bit HIGH to divide the output PCLK1 by four.<br>NOTE: Setting this bit and bit 0 simultaneously HIGH will hold the PCLK1 pin LOW.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Ch | 0 | Divide_By_2 - set this bit HIGH to divide the output PCLK1 by two.<br>NOTE: Setting this bit and bit 1 simultaneously HIGH will hold the PCLK1 pin LOW.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| PCLK2_Phase/Divide | 2Dh | 15-7 | Reserved. Set these bits to zero when writing to 2Dh. | – | – |
| | 2Dh | 6 | Current_P2 - selects the current drive capability of the PCLK2 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Dh | 5-2 | PCLK2_Phase - adjusts the output phase of the PCLK2 clock with respect to the timing output pins. Phase is delayed in 700ps (nominal) increments as shown in Table 3-6.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Dh | 1 | Divide_By_4 - set this bit HIGH to divide the output PCLK2 by four.<br>NOTE: Setting this bit and bit 0 simultaneously HIGH will hold the PCLK2 pin LOW.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Dh | 0 | Divide_By_2 - set this bit HIGH to divide the output PCLK2 by two.<br>NOTE: Setting this bit and bit 1 simultaneously HIGH will hold the PCLK2 pin LOW.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| PCLK3_Phase/Divide | 2Eh | 15-6 | Reserved. Set these bits to zero when writing to 2Eh. | – | – |
| | 2Eh | 5-2 | PCLK3_Phase - adjusts the output phase of the PCLK3/PCLK3 clock with respect to the timing output pins. Phase is delayed in 700ps (nominal) increments as shown in Table 3-6.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Eh | 1 | Divide_By_4 - set this bit HIGH to divide the output PCLK3/PCLK3 by four.<br>Setting this bit and bit 0 simultaneously HIGH will give the full rate video clock on the PCLK3 / PCLK3 pins.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| | 2Eh | 0 | Divide_By_2 - set this bit HIGH to divide the output PCLK3/PCLK3 by two.<br>Setting this bit and bit 1 simultaneously HIGH will give the full rate video clock on the PCLK3 / PCLK3 pins.<br>Reference: Section 3.7.1 on page 52 | R/W | 0 |
| PCLK3_Tristate | 2Fh | 15-2 | Reserved. Set these bits to zero when writing to 2Fh. | – | – |
| | 2Fh | 1-0 | Set these bits to 11b to tristate the PCLK3 / PCLK3 pins.<br>Reference: Section 3.7.1 on page 52 | R/W | 00b |
| RSVD | 2Fh - 30h | – | Reserved. | – | – |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Audio_Control (GS4901B only) | 31h | 15-10 | Reserved. Set these bits to zero when writing to 31h. | – | – |
| | 31h | 9-7 | AFS_Reset_Window - These bits may be used to adjust the value by which the audio clock counters are allowed to drift from the output AFS pulse.<br>The encoding scheme for this register is shown in Table 3-9.<br>NOTE: The default setting of this register will provide a reset window that is sufficient for most standards. To maintain correct audio clock frequencies for some VESA standards, the reset window may have to be increased from its default setting. In this case, set the value of this register to 1XX. See Table 3-9.<br>Reference: Section 3.7.2 on page 53 | R/W | 010b |
| | 31h | 6 | Reserved. Set this it to zero when writing to 31h. | R/W | 0 |
| | 31h | 5 | Enable_384fs - set this bit HIGH to enable the 384fs and 192fs audio clock outputs. This must be set in addition to registers 3Fh to 41h.<br>NOTE: If this bit is HIGH, then a 512fs audio clock will have a 33% duty cycle when fs = 96kHz.<br>Reference: Section 3.7.2 on page 53 | R/W | 0 |
| | 31h | 4-3 | Reserved. Set these bits to zero when writing to 31h. | – | – |
| | 31h | 2 | Host_ASR_SEL - set this bit HIGH to select the audio sample rate using register 32h instead of the external ASR_SEL[2:0] pins.<br>The external ASR_SEL[2:0] pins will be ignored, but should not be left floating.<br>Reference: Section 3.7.2 on page 53 | R/W | 0 |
| | 31h | 1 | AFS_F_Pulse - set this bit to 1 to stretch the AFS pulse duration from 1 line to 1 field.<br>Reference: Section 3.8.2 on page 58 | R/W | 0 |
| | 31h | 0 | AFS_Reset_Disable - set this bit HIGH to disable the 10FID input reference pin from resetting the output AFS pulse. If this bit is set HIGH, the output AFS pulse will free-run or may be reset using register 1Ah. The external 10FID pin should not be left floating.<br>Reference: Section 3.8.2 on page 58 | R/W | 0 |
| ASR_SEL[2:0] (GS4901B only) | 32h | 15-3 | Reserved. Set these bits to zero when writing to 32h. | – | – |
| | 32h | 2-0 | Replaces the external ASR_SEL[2:0] pins when Host_ASR_Select (bit 2 of address 31h) is HIGH.<br>The default setting of this register corresponds to an audio sample rate of 48kHz.<br>Reference: Section 3.7.2 on page 53 | R/W | 011b |
| RSVD | 33h - 38h | – | Reserved. | – | – |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Audio_Cap_Genlock (GS4901B only) | 39h | 15-6 | Reserved. Set these bits to zero when writing to 39h. | – | – |
| | 39h | 5-0 | Control signal to adjust loop bandwidth of audio genlock block.<br>The value programmed in this register must be between 10 and Audio_Res_Genlock - 21.<br>The default value of this register will depend on the fundamental sampling frequency selected.<br>Reference: Section 3.6.2 on page 48 | R/W | – |
| Audio_Res_Genlock (GS4901B only) | 3Ah | 15-6 | Reserved. Set these bits to zero when writing to 3Ah. | – | – |
| | 3Ah | 5-0 | Control signal to adjust loop bandwidth of audio genlock block.<br>The value programmed in this register must be between 32 and 42.<br>The default value of this register will depend on the fundamental sampling frequency selected.<br>Reference: Section 3.6.2 on page 48 | R/W | – |
| RSVD | 3Bh-3Eh | – | Reserved | – | – |
| ACLK1_fs_Multiple (GS4901B only) | 3Fh | 15-3 | Reserved. Set these bits to zero when writing to 3Fh. | – | – |
| | 3Fh | 2-0 | The user may set this register to select the desired frequency of the audio clock on ACLK1 (a multiple of the fundamental sampling rate, fs). The audio clock frequency may be set as: 512fs, 384fs, 256fs, 192fs, 128fs, 64fs, fs, or z-bit. See Table 3-8 for more details.<br>NOTE: To output a frequency of 348fs or 192fs, bit 5 of register 31h must also be set HIGH.<br>Reference: Section 3.7.2 on page 53 | R/W | 0 |
| ACLK2_fs_Multiple (GS4901B only) | 40h | 15-3 | Reserved. Set these bits to zero when writing to 40h. | – | – |
| | 40h | 2-0 | The user may set this register to select the desired frequency of the audio clock on ACLK2 (a multiple of the fundamental sampling rate, fs). The audio clock frequency may be set as: 512fs, 384fs, 256fs, 192fs, 128fs, 64fs, fs, or z-bit. See Table 3-8 for more details.<br>NOTE: To output a frequency of 348fs or 192fs, bit 5 of register 31h must also be set HIGH.<br>Reference: Section 3.7.2 on page 53 | R/W | 0 |
| ACLK3_fs_Multiple (GS4901B only) | 41h | 15-3 | Reserved. Set these bits to zero when writing to 41h. | – | – |
| | 41h | 2-0 | The user may set this register to select the desired frequency of the audio clock on ACLK3 (a multiple of the fundamental sampling rate, fs). The audio clock frequency may be set as: 512fs, 384fs, 256fs, 192fs, 128fs, 64fs, fs, or z-bit. See Table 3-8 for more details.<br>NOTE: To output a frequency of 348fs or 192fs, bit 5 of register 31h must also be set HIGH.<br>Reference: Section 3.7.2 on page 53 | R/W | 0 |
| RSVD | 42h | – | Reserved. | – | – |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Output_Select_1 | 43h | 15-5 | Reserved. Set these bits to zero when writing to 43h. | – | – |
| | 43h | 4 | Current_1 - selects the current drive capability of the TIMING_OUT_1 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 43h | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_1 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 0001b, which corresponds to H Sync.<br>Reference: Section 3.8.4 on page 61 | R/W | 0001b |
| Output_Select_2 | 44h | 15-5 | Reserved. Set these bits to zero when writing to 44h. | – | – |
| | 44h | 4 | Current_2 - selects the current drive capability of the TIMING_OUT_2 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 44h | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_2 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 0010b, which corresponds to H Blanking.<br>Reference: Section 3.8.4 on page 61 | R/W | 0010b |
| Output_Select_3 | 45h | 15-5 | Reserved. Set these bits to zero when writing to 45h. | – | – |
| | 45h | 4 | Current_3 - selects the current drive capability of the TIMING_OUT_3 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 45h | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_3 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 0011b, which corresponds to V Sync.<br>Reference: Section 3.8.4 on page 61 | R/W | 0011b |
| Output_Select_4 | 46h | 15-5 | Reserved. Set these bits to zero when writing to 46h. | – | – |
| | 46h | 4 | Current_4 - selects the current drive capability of the TIMING_OUT_4 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 46h | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_4 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 0100b, which corresponds to V Blanking.<br>Reference: Section 3.8.4 on page 61 | R/W | 0100b |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Output_Select_5 | 47h | 15-5 | Reserved. Set these bits to zero when writing to 47h. | – | – |
| | 47h | 4 | Current_5 - selects the current drive capability of the TIMING_OUT_5 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 47h | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_5 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 0101b, which corresponds to F Sync.<br>Reference: Section 3.8.4 on page 61 | R/W | 0101b |
| Output_Select_6 | 48h | 15-5 | Reserved. Set these bits to zero when writing to 48h. | – | – |
| | 48h | 4 | Current_6 - selects the current drive capability of the TIMING_OUT_6 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 48h | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_6 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 0110b, which corresponds to F Digital.<br>Reference: Section 3.8.4 on page 61 | R/W | 0110b |
| Output_Select_7 | 49h | 15-5 | Reserved. Set these bits to zero when writing to 49h. | – | – |
| | 49h | 4 | Current_7 - selects the current drive capability of the TIMING_OUT_7 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 49h | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_7 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 0111b, which corresponds to 10FID.<br>Reference: Section 3.8.4 on page 61 | R/W | 0111b |
| Output_Select_8 | 4Ah | 15-5 | Reserved. Set these bits to zero when writing to 4Ah. | – | – |
| | 4Ah | 4 | Current_8 - selects the current drive capability of the TIMING_OUT_8 pin. Set this bit HIGH for high current drive. Otherwise, the current drive will be low.<br>Reference: Section 3.8.4 on page 61 | R/W | 0 |
| | 4Ah | 3-0 | This register is used to select one of the 10 pre-programmed or 4 user programmed timing signals available for output on the TIMING_OUT_8 pin. See Table 3-11 for more details.<br>Note: The default setting of this register is 1000b, which corresponds to Display Enable (DE).<br>Reference: Section 3.8.4 on page 61 | R/W | 1000b |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| RSVD | 4Bh | – | Reserved. | – | – |
| Video_Control | 4Ch | 15-5 | Reserved. Set these bits to zero when writing to 4Ch. | – | – |
| | 4Ch | 4 | 10FID_F_pulse - set this bit HIGH to stretch the 10FID pulse duration from 1 line to 1 field.<br>Reference: Section 3.8.1 on page 57 | R/W | 0 |
| | 4Ch | 3-2 | Reserved. Set these bits to zero when writing to 4Ch. | – | – |
| | 4Ch | 1 | Host_VID_STD - set this bit HIGH to select the output video standard using register 4Dh instead of the external VID_STD[5:0] pins.<br>The external VID_STD[5:0] pins will be ignored, but should not be left floating.<br>Reference: Section 1.4 on page 20 | R/W | 0 |
| | 4Ch | 0 | Reserved. Set this bit to zero when writing to 4Ch. | – | – |
| VID_STD[5:0] | 4Dh | 15-6 | Reserved. Set these bits to zero when writing to 4Dh. | – | – |
| | 4Dh | 5-0 | Replaces the external VID_STD[5:0] pins when VID_From_Host (bit 1 of address 4Ch) is HIGH.<br>Reference: Section 1.4 on page 20 | R/W | 00h |
| RSVD | 4Eh-55h | – | Reserved | – | – |
| Polarity | 56h | 15-10 | Reserved. Set these bits to zero when writing to 56h. | – | – |
| | 56h | 9 | AFS (GS4901B only)- set this bit HIGH to invert the polarity of the AFS timing output signal.<br>By default, the AFS signal is HIGH for the duration of the first line of the n'th video frame to indicate that the ACLK dividers have been reset at the start of line 1 of that frame.<br>NOTE: The GS4900B does not generate an AFS pulse and will ignore the setting of this bit.<br>Reference: Table 1-3 | R/W | 0 |
| | 56h | 8 | 10FID - set this bit HIGH to invert the polarity of the 10FID timing output signal.<br>By default, the 10FID signal will go HIGH for one line at the start of the 10-field sequence.<br>Reference: Table 1-3 | R/W | 0 |
| | 56h | 7 | DE - set this bit HIGH to invert the polarity of the DE timing output signal.<br>By default, the DE signal will be HIGH whenever pixel information is to be displayed on the display device<br>Reference: Table 1-3 | R/W | 0 |
| | 56h | 6 | Reserved. Set this bit to zero when writing to 56h. | – | – |
| | 56h | 5 | F_Digital - set this bit HIGH to invert the polarity of the F Digital timing output signal.<br>By default, the F Digital signal will be HIGH for the entire period of field 1.<br>Reference: Table 1-3 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| | 56h | 4 | F_Sync - set this bit HIGH to invert the polarity of the F Sync timing output signal.<br>By default, the F Sync signal will be HIGH for the entire period of field 1.<br>Reference: Table 1-3 | R/W | 0 |
| | 56h | 3 | V_Blanking - set this bit HIGH to invert the polarity of the V Blanking timing output signal.<br>By default, the V Blanking signal will be LOW for the portion of the field/frame containing valid video data.<br>Reference: Table 1-3 | R/W | 0 |
| | 56h | 2 | V_Sync - set this bit HIGH to invert the polarity of the V Sync timing output signal.<br>By default, the V Sync signal is active LOW.<br>Reference: Table 1-3 | R/W | 0 |
| | 56h | 1 | H_Blanking - set this bit HIGH to invert the polarity of the H Blanking timing output signal.<br>By default, the H Blanking signal will be LOW for the portion of the video line containing valid video samples.<br>Reference: Table 1-3 | R/W | 0 |
| | 56h | 0 | H_Sync - set this bit HIGH to invert the polarity of the H Sync timing output signal.<br>By default, the H Sync signal is active LOW.<br>Reference: Table 1-3 | R/W | 0 |
| H_Start_1 | 57h | 15-0 | The value programmed in this register indicates the pixel start point for the leading edge of the user-programmed H Sync signal USER1_H.<br>NOTE: The value programmed in this register must be less than the value programmed in H_Stop_1.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| H_Stop_1 | 58h | 15-0 | The value programmed in this register indicates the pixel end point for the trailing edge of the user-programmed H Sync signal USER1_H.<br>NOTE: The value programmed in this register must not exceed the maximum number of clock periods per line of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| V_Start_1 | 59h | 15 | Reserved. Set this bit to zero when writing to 59h. | – | – |
| | 59h | 14-0 | The value programmed in this register indicates the start line number of the leading edge of the user-programmed V Sync signal USER1_V. For interlaced output standards, this value corresponds to the odd field number.<br>NOTE: The value programmed in this register must be less than the value programmed in V_Stop_1.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| V_Stop_1 | 5Ah | 15 | Reserved. Set this bit to zero when writing to 5Ah. | – | – |
| | 5Ah | 14-0 | The value programmed in this register indicates the end line number of the trailing edge of the user-programmed V Sync signal USER1_V. For interlaced output standards, this value corresponds to the odd field number.<br>NOTE: The value programmed in this register must not exceed the maximum number of lines per field of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| Operator_Polarity_1 | 5Bh | 15-4 | Reserved. Set these bits to zero when writing to 5Bh. | – | – |
| | 5Bh | 3 | Polarity_1 - Use this bit to invert the polarity of the final USER1 signal.<br>By default, the polarity of the user programmed signals is active LOW. The polarity may be switched to active HIGH by setting this bit LOW.<br>Reference: Section 3.8.3 on page 59 | R/W | 1 |
| | 5Bh | 2 | AND_1 - logical operator: USER1_H AND USER1_V<br>Set this bit HIGH to output a signal that is only active when both USER1_H and USER1_V are active.<br>When this bit is HIGH, bit 1 and bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 5Bh | 1 | OR_1 - logical operator: USER1_H OR USER1_V<br>Set this bit HIGH to output a signal that is active whenever USER1_H or USER1_V are active.<br>When this bit is HIGH bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 5Bh | 0 | XOR_1 - logical operator: USER1_H XOR USER1_V<br>Set this bit HIGH to output a signal with the following attributes: Signal becomes active when either USER1_H or USER1_V is active. Signal is inactive when USER1_H and USER1_V are both active or both inactive.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| H_Start_2 | 5Ch | 15-0 | The value programmed in this register indicates the pixel start point for the leading edge of the user-programmed H Sync signal USER2_H.<br>NOTE: The value programmed in this register must be less than the value programmed in H_Stop_2<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| H_Stop_2 | 5Dh | 15-0 | The value programmed in this register indicates the pixel end point for the trailing edge of the user-programmed H Sync signal USER2_H.<br>NOTE: The value programmed in this register must not exceed the maximum number of clock periods per line of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| V_Start_2 | 5Eh | 15 | Reserved. Set this bit to zero when writing to 5Eh. | – | – |
| | 5Eh | 14-0 | The value programmed in this register indicates the start line number of the leading edge of the user-programmed V Sync signal USER2_V. For interlaced output standards, this value corresponds to the odd field line number.<br>NOTE: The value programmed in this register must be less than the value programmed in V_Stop_2.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| V_Stop_2 | 5Fh | 15 | Reserved. Set this bit to zero when writing to 5Fh. | – | – |
| | 5Fh | 14-0 | The value programmed in this register indicates the end line number of the trailing edge of the user-programmed V Sync signal USER2_V. For interlaced output standards, this value corresponds to the odd field line number.<br>NOTE: The value programmed in this register must not exceed the maximum number of lines per field of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| Operator_Polarity_2 | 60h | 15-4 | Reserved. Set these bits to zero when writing to 60h. | – | – |
| | 60h | 3 | Polarity_2 - Use this bit to invert the polarity of the final USER2 signal.<br>By default, the polarity of the user programmed signals is active LOW. The polarity may be switched to active HIGH by setting this bit LOW.<br>Reference: Section 3.8.3 on page 59 | R/W | 1 |
| | 60h | 2 | AND_2 - logical operator: USER2_H AND USER2_V<br>Set this bit HIGH to output a signal that is only active when both USER2_H and USER2_V are active.<br>When this bit is HIGH, bit 1 and bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 60h | 1 | OR_2 - logical operator: USER2_H OR USER2_V<br>Set this bit HIGH to output a signal that is active whenever USER2_H or USER2_V are active.<br>When this bit is HIGH bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 60h | 0 | XOR_2 - logical operator: USER2_H XOR USER2_V<br>Set this bit HIGH to output a signal with the following attributes: Signal becomes active when either USER2_H or USER2_V is active. Signal is inactive when USER2_H and USER2_V are both active or both inactive.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| H_Start_3 | 61h | 15-0 | The value programmed in this register indicates the pixel start point for the leading edge of the user-programmed H Sync signal USER3_H.<br>NOTE: The value programmed in this register must be less than the value programmed in H_Stop_3.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| H_Stop_3 | 62h | 15-0 | The value programmed in this register indicates the pixel end point for the trailing edge of the user-programmed H Sync signal USER3_H.<br>NOTE: The value programmed in this register must not exceed the maximum number of clock periods per line of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| V_Start_3 | 63h | 15 | Reserved. Set this bit to zero when writing to 63h. | – | – |
| | 63h | 14-0 | The value programmed in this register indicates the start line number of the leading edge of the user-programmed V Sync signal USER3_V. For interlaced output standards, this value corresponds to the odd field line number.<br>NOTE: The value programmed in this register must be less than the value programmed in V_Stop_3.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| V_Stop_3 | 64h | 15 | Reserved. Set this bit to zero when writing to 64h. | – | – |
| | 64h | 14-0 | The value programmed in this register indicates the end line number of the trailing edge of the user-programmed V Sync signal USER3_V. For interlaced output standards, this value corresponds to the odd field line number.<br>NOTE: The value programmed in this register must not exceed the maximum number of lines per field of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| Operator_Polarity_3 | 65h | 15-4 | Reserved. Set these bits to zero when writing to 65h. | – | – |
| | 65h | 3 | Polarity_3 - Use this bit to invert the polarity of the final USER3 signal.<br>By default, the polarity of the user programmed signals is active LOW. The polarity may be switched to active HIGH by setting this bit LOW.<br>Reference: Section 3.8.3 on page 59 | R/W | 1 |
| | 65h | 2 | AND_3 - logical operator: USER3_H AND USER3_V<br>Set this bit HIGH to output a signal that is only active when both USER3_H and USER3_V are active.<br>When this bit is HIGH, bit 1 and bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 65h | 1 | OR_3 - logical operator: USER3_H OR USER3_V<br>Set this bit HIGH to output a signal that is active whenever USER3_H or USER3_V are active.<br>When this bit is HIGH bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 65h | 0 | XOR_3 - logical operator: USER3_H XOR USER3_V<br>Set this bit HIGH to output a signal with the following attributes: Signal becomes active when either USER3_H or USER3_V is active. Signal is inactive when USER3_H and USER3_V are both active or both inactive.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| H_Start_4 | 66h | 15-0 | The value programmed in this register indicates the pixel start point for the leading edge of the user-programmed H Sync signal USER4_H.<br>NOTE: The value programmed in this register must be less than the value programmed in H_Stop_4.<br>Reference: Section 3.8.3 | R/W | 0 |
| H_Stop_4 | 67h | 15-0 | The value programmed in this register indicates the pixel end point for the trailing edge of the user-programmed H Sync signal USER4_H.<br>NOTE: The value programmed in this register must not exceed the maximum number of clock periods per line of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| V_Start_4 | 68h | 15 | Reserved. Set this bit to zero when writing to 68h. | – | – |
| | 68h | 14-0 | The value programmed in this register indicates the start line number of the leading edge of the user-programmed V Sync signal USER4_V. For interlaced output standards, this value corresponds to the odd field line number.<br>NOTE: The value programmed in this register must be less than the value programmed in V_Stop_4.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| V_Stop_4 | 69h | 15 | Reserved. Set this bit to zero when writing to 69h. | – | – |
| | 69h | 14-0 | The value programmed in this register indicates the end line number of the trailing edge of the user-programmed V Sync signal USER4_V. For interlaced output standards, this value corresponds to the odd field line number.<br>NOTE: The value programmed in this register must not exceed the maximum number of lines per field of the outgoing standard.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| Operator_Polarity_4 | 6Ah | 15-4 | Reserved. Set these bits to zero when writing to 6Ah. | – | – |
| | 6Ah | 3 | Polarity_4 - Use this bit to invert the polarity of the final USER4 signal.<br>By default, the polarity of the user programmed signals is active LOW. The polarity may be switched to active HIGH by setting this bit LOW.<br>Reference: Section 3.8.3 on page 59 | R/W | 1 |
| | 6Ah | 2 | AND_4 - logical operator: USER4_H AND USER4_V<br>Set this bit HIGH to output a signal that is only active when both USER4_H and USER4_V are active.<br>When this bit is HIGH, bit 1 and bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 6Ah | 1 | OR_4 - logical operator: USER4_H OR USER4_V<br>Set this bit HIGH to output a signal that is active whenever USER4_H or USER4_V are active.<br>When this bit is HIGH bit 0 of this register will be ignored.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| | 6Ah | 0 | XOR_4 - logical operator: USER4_H XOR USER4_V<br>Set this bit HIGH to output a signal with the following attributes: Signal becomes active when either USER4_H or USER4_V is active. Signal is inactive when USER4_H and USER4_V are both active or both inactive.<br>Reference: Section 3.8.3 on page 59 | R/W | 0 |
| Ext_Audio_Mode | 81h | 15-0 | Set this register to 20C1h to enable the Extended Audio Mode of the device.<br>To fully enable this mode, VID_STD[5:0] must be set to 4d, and the F_Lock_Mask and V_Lock_Mask bits [4:3] of register address 16h must be set to 1.<br>NOTE: Once this register is programmed, it must be updated using bit 6 of register 16h.<br>Reference: Section 3.9 on page 62 | R/W | 0 |

**Table 3-13: Configuration and Status Registers (Continued)**

| Register Name | Address | Bit | Description | R/W | Default |
|---|---|---|---|---|---|
| HD_Reference_Enable | 82h | 15-8 | Reserved. Set these bits to zero when writing to 82h. | – | – |
| | 82h | 7 | HD_Ref_Enable - Set this bit HIGH to allow the device to recognize the HD input reference formats that have also been enabled in the Reference_Standard_Disable register (address 11h-13h).<br>When this bit is set HIGH, the GS4901B/GS4900B will only assert REF_LOST when the input signal is removed.<br>Reference: Section 3.5 on page 42. | R/W | 0 |
| | 82h | 6-0 | Reserved. Set these bits to zero when writing to 82h. | – | – |
| Ln_Count_Reset | 83h | 15 | Toggle this bit to reset the line-based counters in the device.<br>This is only required when locking the 525-line SD output standards to the *"f/1.001"* HD input reference standards, AND:<br>1. The reference has been removed and subsequently re-applied. In this case, the user should wait until the reference has been re-detected by the device, which may take up to 4 frames. See Section 3.5.3 on page 44.<br>OR<br>2. The device is locked to blanking signals from a deserializer, and the SDI input to the deserializer has been switched upstream from the system. See Section 3.6.3 on page 51. | R/W | 0 |
| | 83h | 14-0 | Reserved. Set these bits to zero when writing to 83h. | – | – |

## 3.11 JTAG

When the JTAG/$\overline{\text{HOST}}$ input pin of the GS4901B/GS4900B is set HIGH, the host interface port will be configured for JTAG test operation. In this mode, pins 57 through 60 become TCLK, TDI, TDO, and TMS. In addition, the $\overline{\text{RESET}}$ pin will operate as the test reset pin.

Boundary scan testing using the JTAG interface will be enabled in this mode.

There are two methods in which JTAG can be used on the GS4901B/GS4900B:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly; or
2. Under control of the host for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with high-impedance buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 3-16.

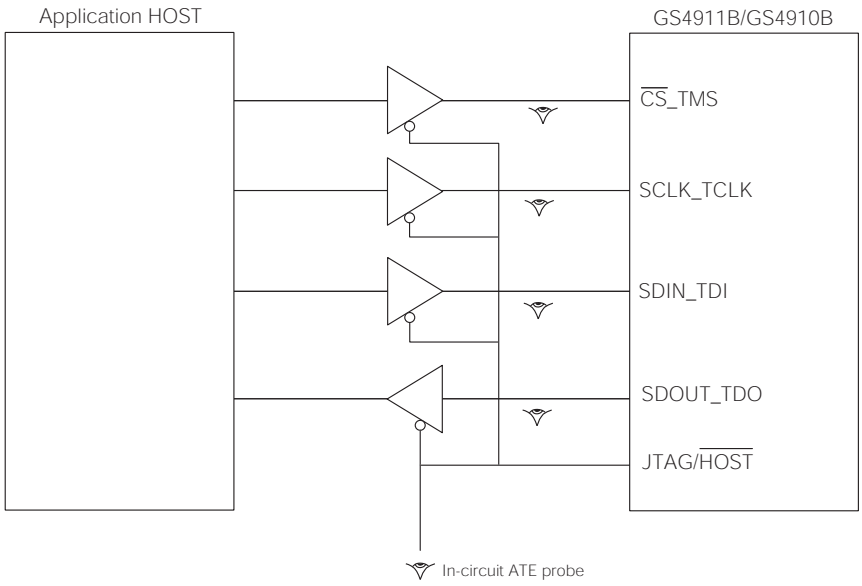



**Figure 3-16: In-Circuit JTAG**

Alternatively, if the test capabilities are to be used in the system, the host may still control the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 3-17.

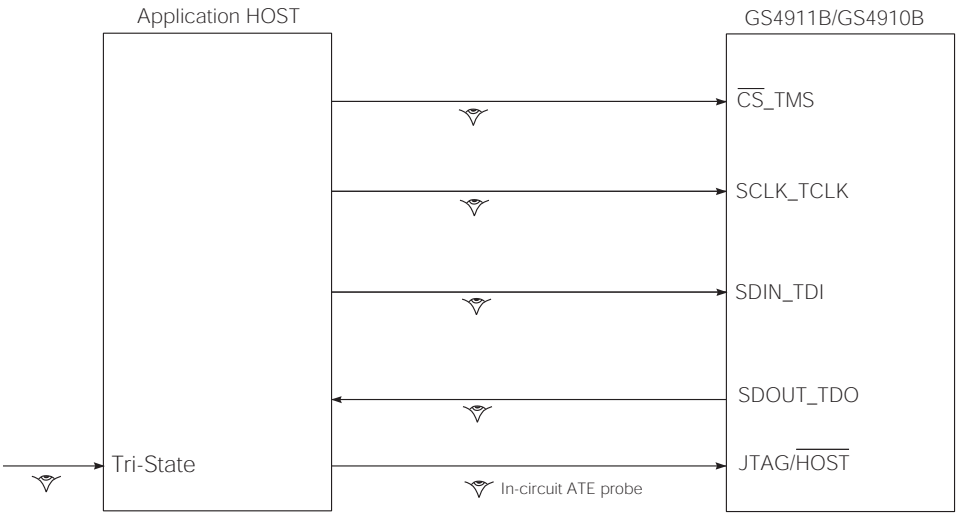



**Figure 3-17: System JTAG**

# 3.12 Device Power-Up

## 3.12.1 Power Supply Sequencing

The GS4901B/GS4900B has a recommended power supply sequence. To ensure correct power-up, the ANALOG_VDD and CORE_VDD power pins should be powered before IO_VDD.

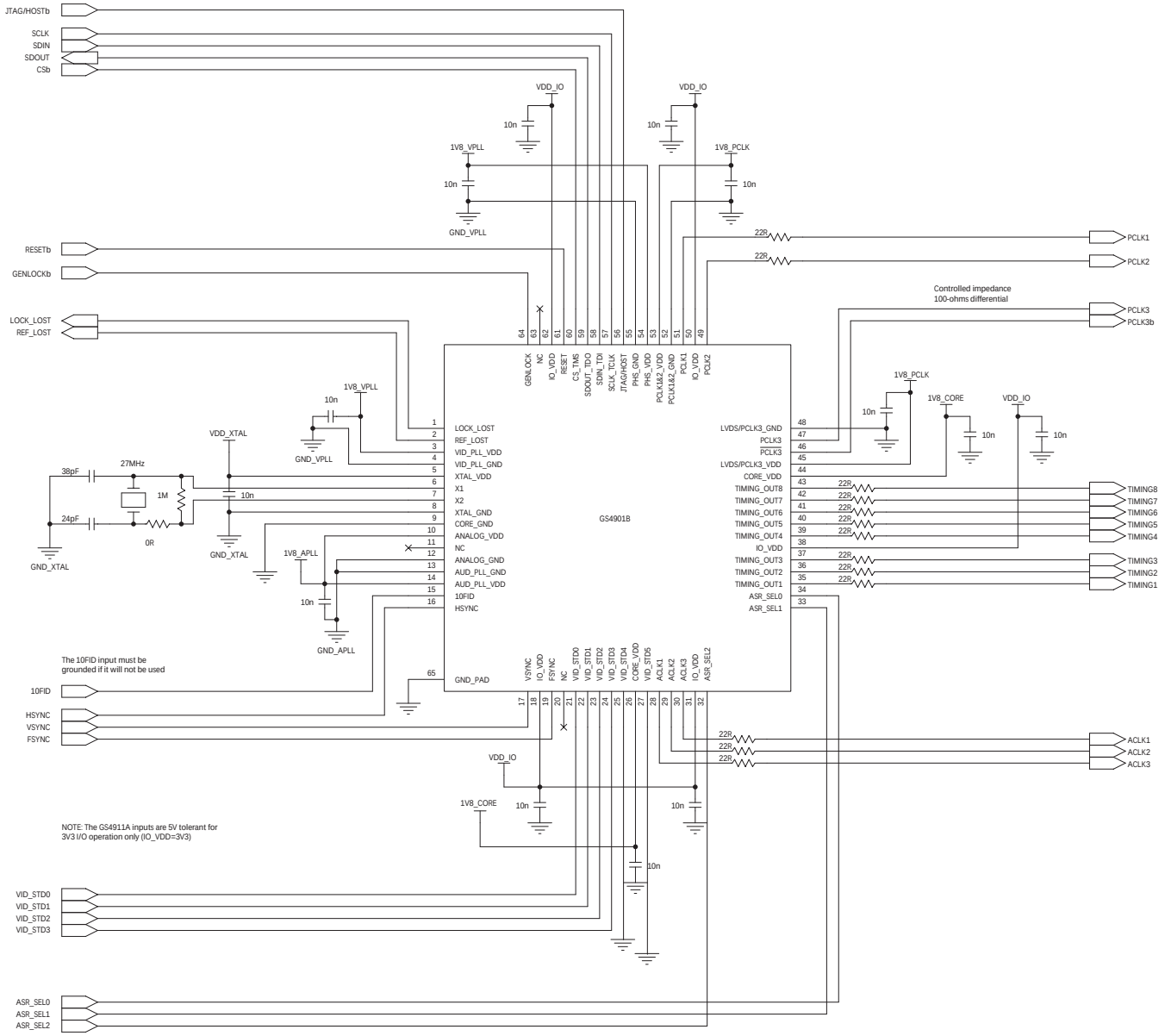
Device pins may be driven prior to power-up without causing damage.

# 3.13 Device Reset

In order to initialize operating conditions to their default states, the application layer must hold the RESET signal LOW during power up and for a minimum of 500us after the last supply has reached its operating voltage.

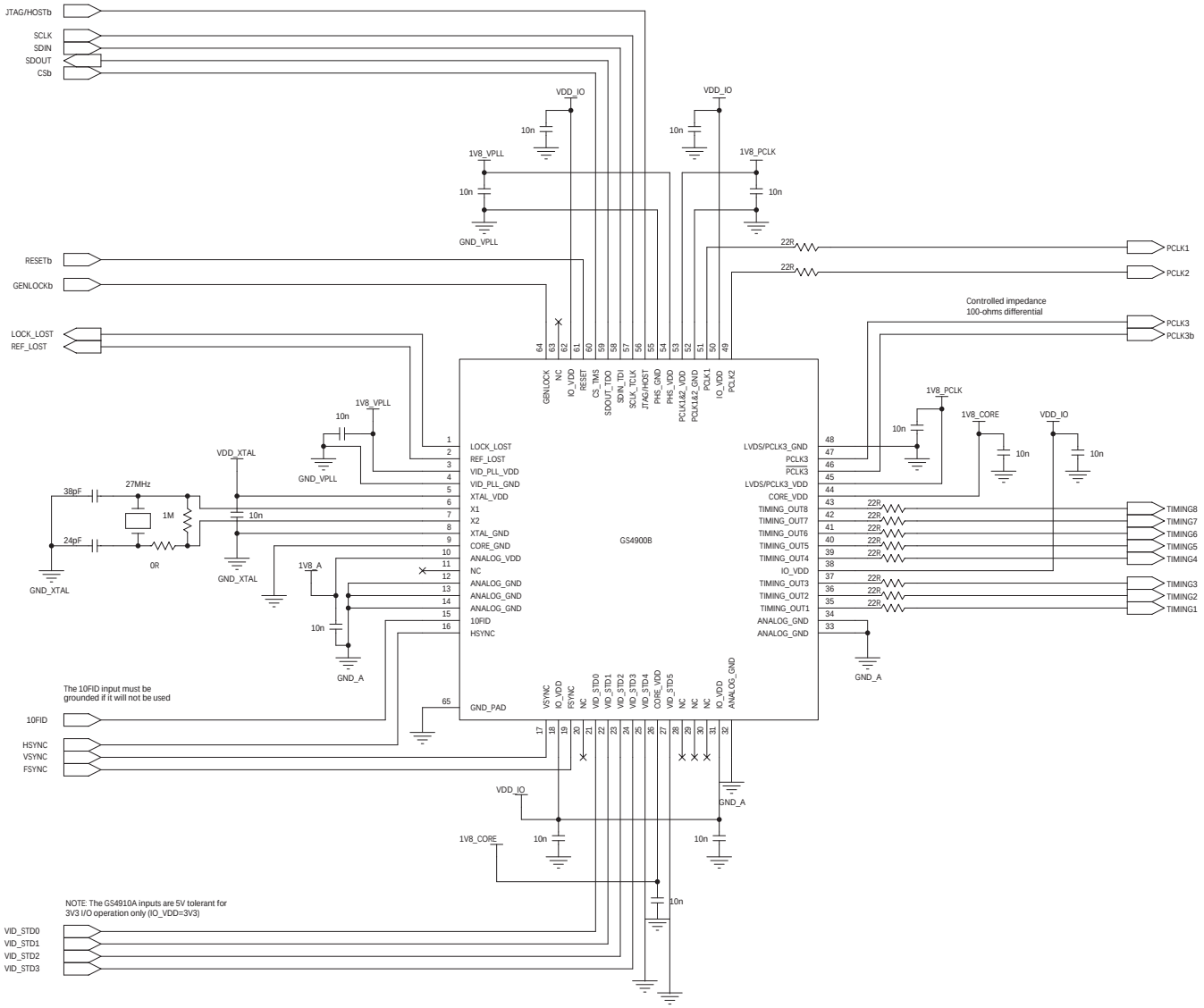
# 4. Application Reference Design

## 4.1 GS4901B Typical Application Circuit




NOTE: For a solution with the lowest output jitter, the GS9062 or GS9092A serializers are recommended for use with the GS4901B/GS4900B.

# 4.2 GS4900B Typical Application Circuit




NOTE: For a solution with the lowest output jitter, the GS9062 or GS9092A serializers are recommended for use with the GS4901B/GS4900B.

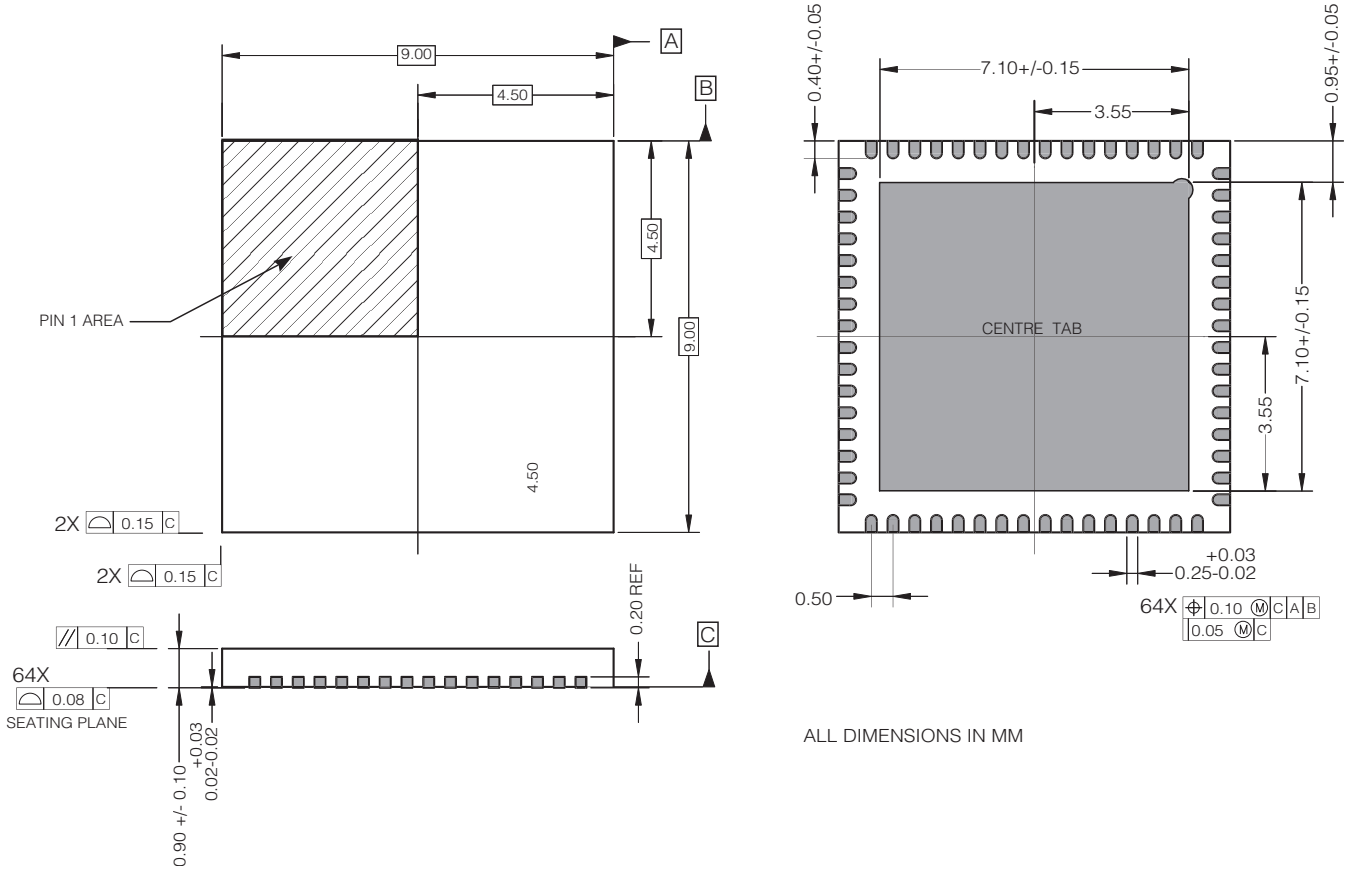
# 5. References & Relevant Standards

**Table 5-1: References & Relevant Standards**

| | |
|---|---|
| AES11-1997 | Synchronization of Digital Audio Equipment in Studio Operations |
| SMPTE 125M-1995 | Component Video Signal 4:2:2 – Bit-Parallel Digital Interface |
| SMPTE 170M-1999 | Composite Analog Video Signal – NTSC for Studio Applications |
| SMPTE 244M-1995 | System M/NTSC Composite Video Signals – Bit-Parallel Digital Interface |
| SMPTE 260M-1999 | 1125/60 High-Definition Production System – Digital Representation and Bit-Parallel Interface |
| SMPTE 267M-1995 | Bit-Parallel Digital Interface – Component Video Signal 4:2:2 16x9 Aspect Ratio |
| SMPTE 274M-1998 | 1920 x 1080 Scanning and Analog and Parallel Digital Interfaces for Multiple Picture Rates |
| SMPTE 293M-1996 | 720 x 483 Active Line at 59.94-Hz Progressive Scan Production – Digital Representation |
| SMPTE 296M-1997 | 1280 x 720 Scanning, Analog and Digital Representation an Analog Interface |
| SMPTE 318M-1999 | Synchronization of 59.94- or 50-Hz Related Video and Audio Systems in Analog and Digital Areas – Reference Signals |
| SMPTE 347M-2001 | 540 Mb/s Serial Digital Interface – Source Image Format Mapping |
| SMPTE RP 164-1996 | Location of Vertical Interval Time Code |
| SMPTE RP 168-1993 | Definition of Vertical Interval Switching Point for Synchronous Video Switching |
| SMPTE RP 211-2000 | Implementation of 24P, 25P and 30P Segmented Frames for 1920 x 1080 Production Format |
| ITU-R BT.601-5 | Studio Encoding Parameters of Digital Television for Standard 4:3 and Wide-screen 16:9 Aspect Ratios |
| ITU-R BT.709-4 | Parameter Values for the HDTV Standards for Production and International Program Exchange ITU-R BT.799.3 Interface for Digital Component Video Signals in 525-line and 625-line Television Systems Operating at the 4:4:4 Level of Recommendation ITU-R BT.601 (PART A) |
| ITU-R BT.1358 | Studio Parameters of 625 and 525 Line Progressive Scan Television Systems |
| VESA Monitor Timing Specifications | VESA and industry Standards and Guidelines for Computer Display Monitor Timing – Version 1.0, Revision 0.8 (Adoption Date: September 17, 1998) |

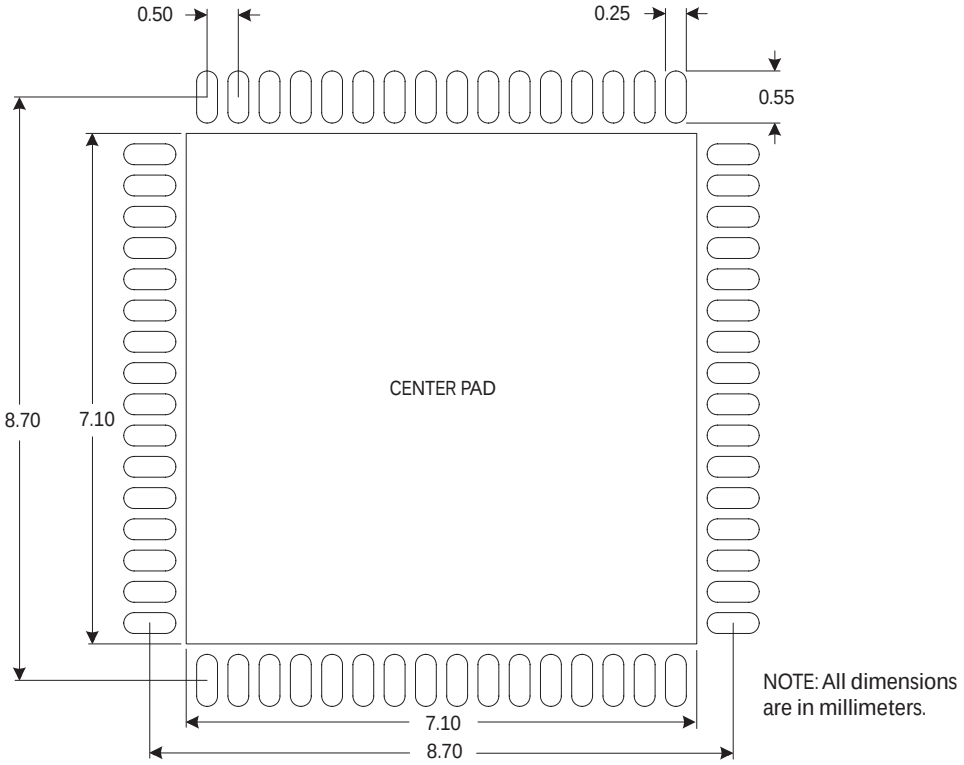
# 6. Package & Ordering Information

## 6.1 Package Dimensions




ALL DIMENSIONS IN MM

## 6.2 Recommended PCB Footprint




The center pad of the PCB footprint should be connected to the ground plane by a minimum of 36 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

## 6.3 Packaging Data

| Parameter | Value |
|---|---|
| Package Type | 9mm x 9mm 64-pin QFN |
| Moisture Sensitivity Level | 3 |
| Junction to Case Thermal Resistance, $\theta_{j-c}$ | 9.3°C/W |
| Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow) | 24.6°C/W |
| Psi, $\psi$ | 0.2°C/W |
| Pb-free and RoHS Compliant | Yes |

## 6.4 Ordering Information

| Part | Video Clocks | Audio Clocks | Max PCLK Rate |
|---|---|---|---|
| GS4901B | √ | √ | 54MHz |
| GS4900B | √ | – | 54MHz |

| Part Number | Package | Temperature Range |
|---|---|---|
| GS4901BCNE3 | Pb-free 64-pin QFN | 0°C to 70°C |
| GS4900BCNE3 | Pb-free 64-pin QFN | 0°C to 70°C |

# 7. Revision History

| Version | ECR | PCN | Date | Changes and/or Modifications |
|---|---|---|---|---|
| A | 138810 | – | January 2006 | New document. |
| 0 | 140153 | – | April 2006 | Converting to Preliminary Data Sheet. Corrected loop bandwidth calculations. Updated description of locking to HD formats. Updated power consumption. |

**CAUTION**
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
**PRELIMINARY DATA SHEET**
The product is in a preproduction phase and specifications are subject to change without notice.

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