FEATURES

- fully compatible with SMPTE 259M-ABC
- decodes 8 and 10 bit serial digital signals for data rates to 270Mb/s
- recommended alternative to GS9000C for use when interfacing directly to GS7025, GS9025A or GS9035A
- incorporates automatic standards selection
- 325mW power dissipation at 270MHz clock rate
- Pb-free and Green
- operates from single +5 or -5 volt supply
- 28 pin PLCC packaging

APPLICATIONS

- $4f_{SC}$ and 4:2:2 serial digital interfaces
- Automatic standards select controller for serial routing and distribution applications

DEVICE DESCRIPTION

The GS9000D is a CMOS integrated circuit specifically designed to deserialize SMPTE 259M serial digital signals at data rates up to 270Mb/s. The GS9000D is a pin and functional equivalent to the GS9000C, with the exception of SDI input levels which are compatible for direct interfacing to the GS7025, GS9025A and GS9035A.

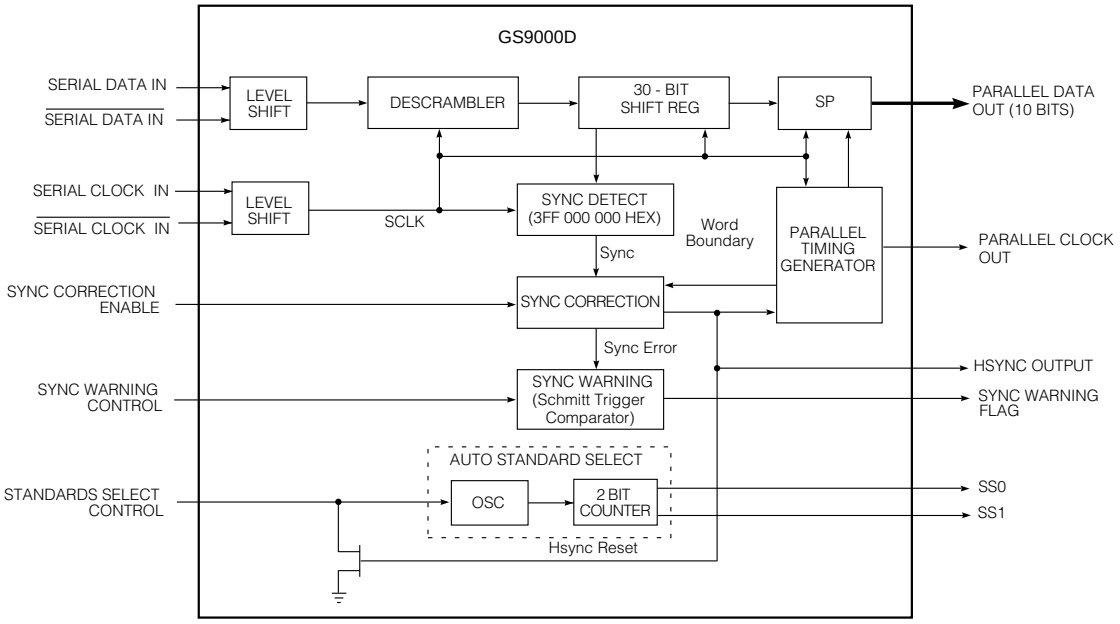
The device incorporates a descrambler, serial to parallel convertor, sync processing unit, sync warning unit and automatic standards select circuitry.

Differential pseudo-ECL inputs for both serial clock and data are internally level shifted to CMOS levels. Digital outputs such as parallel data, parallel clock, HSYNC, Sync Warning and Standard Select are all TTL compatible.

The GS9000D is packaged in a 28 pin PLCC and operates from a single 5 volt, ±5% power supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS9000DCPJ	28 Pin PLCC	0°C to 70°C	No
GS9000DCTJ	28 Pin PLCC Tape	0°C to 70°C	No
GS9000DCPJE3	28 Pin PLCC	0°C to 70°C	Yes
GS9000DCTJE3	28 Pin PLCC Tape	0°C to 70°C	Yes



FUNCTIONAL BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S = V_{DD} - V_{SS})	7V
Input Voltage Range (any input)	-0.3 to (V_{DD} + 0.3)
DC Input Current (any one input)	±10µA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to +150C
Lead Temperature (Soldering, 10 seconds)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, T_A = 0°C to 70°C unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Supply Voltage	V_S	Operating range	4.75	5.00	5.25	V		3
Power Consumption (outputs unloaded)	P_C	f = 143MHz	-	235	-	mW		7
		f = 270MHz	-	325	-	mW		7
CMOS Input Voltage	VIH_{MIN}	T_A = 25°C	3.4	-	-	V		1
	VIL_{MAX}		-	-	1.5	V		1
Output Voltage	VOH_{MIN}	I_{OH} = 4mA, 25°C	2.4	4.5	-	V		1
	VOL_{MAX}	I_{OL} = 4mA, 25°C	-	0.2	0.5	V		1
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} or V_{SS}	-	-	±10	µA		3
Serial Clock and Data Inputs Common Mode Voltage	V_{CM}	T_A = 25°C, V_{IN} = 700 to 1200mVpp	3.0	-	4.05	V	Centre of Swing	1

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, T_A = 0°C to 70°C unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Serial Input Clock Frequency	f_{SCI}		100	-	270	MHz		1
Serial Input Data Rate	DR_{SDI}		100	-	270	Mb/s		1
Serial Data and Clock Inputs:		T_A = 25°C						
Setup	t_{SU}		1.0	-	-	ns		7
Hold	t_{HOLD}		1.0	-	-	ns		7
Signal Swing	V_{IN}		700	800	1200	mVpp		1
Parallel Clock: Jitter	t_{JCLK}	T_A = 25°	-	1.0	-	ns p-p		7
Parallel Data: Risetime and Falltime	t_{R-PDn}	T_A = 25°C, C_L = 10pF	-	3	-	ns	20% to 80%	7
PDn to PCLK Delay Tolerance	t_D		-	-	±3	ns	Rising edge of PCLK to bit period centre	7

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
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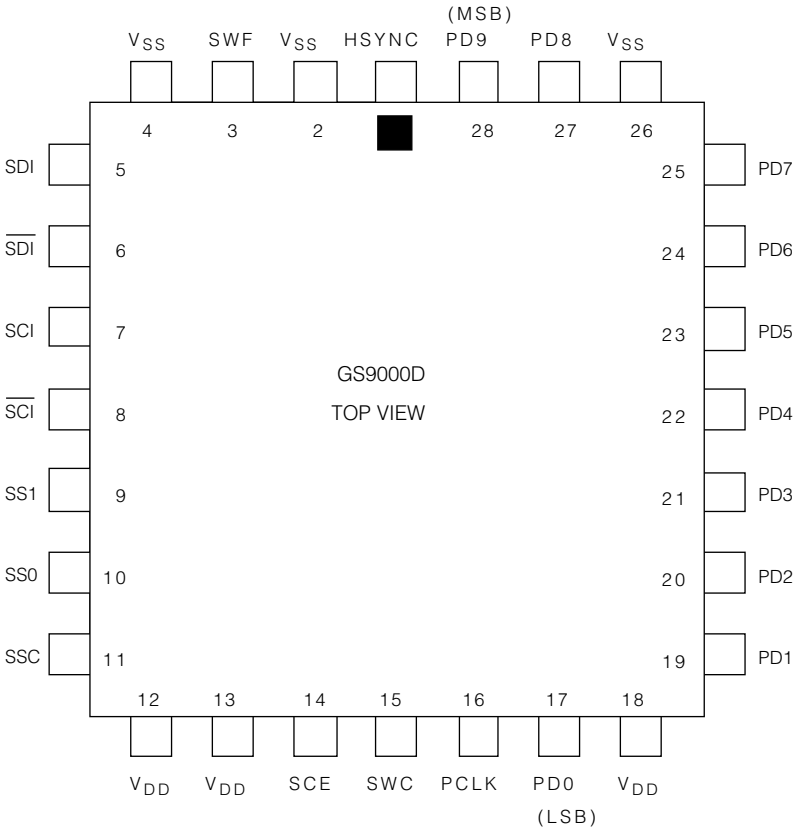


Fig. 1 GS9000D Pin Outs, 28 Pin PLCC Package

PIN DESCRIPTIONS

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1	HSYNC	Output	**Horizontal Sync Output.** CMOS (TTL compatible) output that toggles for each TRS detected.
2	V_{SS}		**Power Supply.** Most negative power supply connection.
3	SWF	Output	Sync Error Warning Flag. CMOS (TTL compatible) active high output that indicates the preselected HSYNC Error Rate (HER). The HER is set with an RC time constant on the SWC input.
4	V_{SS}		**Power Supply.** Most negative power supply connection.
5, 6	SDI/$\overline{SDI}$	Inputs	**Differential, pseudo-ECL serial data inputs.** ECL voltage levels with offset of 3.0V to 4.05V for operation up to 270MHz. See AC Electrical Characteristics Table for details.
7, 8	SCI/$\overline{SCI}$	Inputs	**Differential, pseudo-ECL serial clock inputs.** ECL voltage levels with offset of 3.0V to 4.05V for operation up to 270MHz. See AC Electrical Characteristics Table for details.
9,10	SS1/SS0	Output	**Standard Select Outputs.** CMOS (TTL compatible) outputs is generated by a 2-bit internal binary counter which stops cycling when a valid TRS is detected by the GS9000D.
11	SSC	Input	**Standards Select Control.** Analog input used to set a time constant for the standards select hunt period. An external RC sets the time constant.
12	V_{DD}		**Power Supply.** Most positive power supply connection.
13	V_{DD}		**Power Supply.** Most positive power supply connection.
14	SCE	Input	**Sync Correction Enable.** Active high CMOS input which enables sync correction by not resetting the GS9000D's internal parallel timing on the first sync error. If the next incoming sync is in error, internal parallel timing will be reset. This is to guard against spurious HSYNC errors. When SCE is low, a valid sync will always reset the GS9000D's parallel timing generator

PIN DESCRIPTIONS

PIN NO.	SYMBOL	TYPE	DESCRIPTION
15	SWC	Input	**Sync Warning Control**. Analog input used to set the HSYNC Error Rate (HER). This is accomplished by an external RC time constant connected to this pin.
16	PCLK	Output	**Parallel Clock Output.** CMOS (TTL compatible) clock output where the rising edge of the clock is located at the centre of the parallel data window within a given tolerance. See Fig. 7.
17	PD0	Output	**Parallel Data Output - Bit 0 (LSB)**. CMOS (TTL compatible) descrambled parallel data output from the serial to parallel convertor representing the least significant bit (LSB).
18	V_{DD}		**Power Supply.** Most positive power supply connection.
19-25	PD1 - PD7	Outputs	**Parallel Data Outputs - Bit 1 to Bit 7.** CMOS (TTL compatible) descrambled parallel data outputs from the serial to parallel convertor representing data bit 1 through data bit 7.
26	V_{SS}		**Power Supply**. Most negative power supply connection.
27	PD8	Output	**Parallel Data Output.** CMOS (TTL compatible) descrambled parallel data output from the serial to parallel convertor representing data bit 8.
28	PD9	Output	**Parallel Data Output - Bit 9 (MSB)**. CMOS (TTL compatible) descrambled data output from the serial to parallel convertor representing the most significant bit (MSB).

INPUT/OUTPUT CIRCUITS

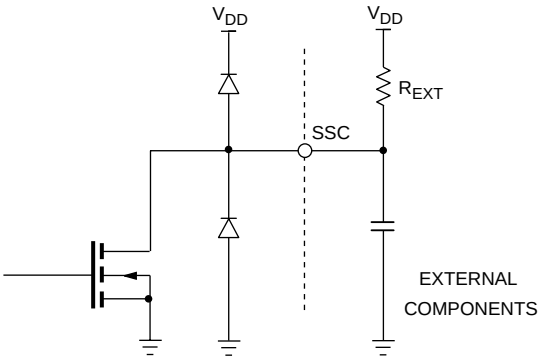


Fig. 2 Pin 11 SSC

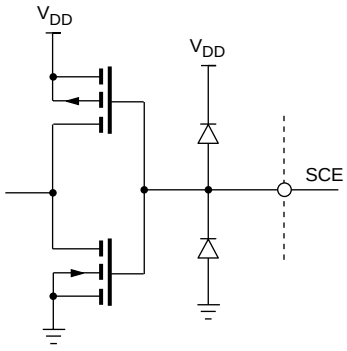


Fig. 3 Pin 14 SCE

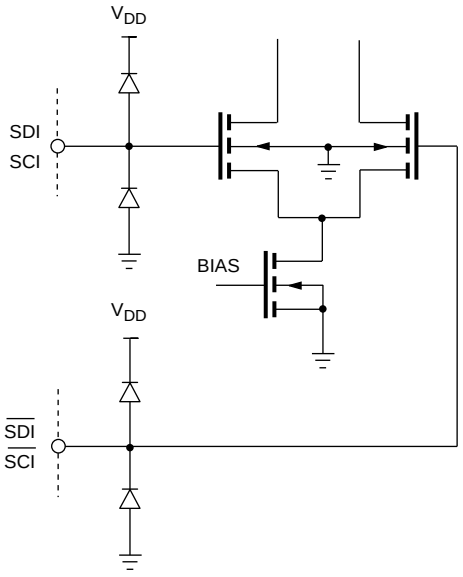


Fig. 4 Pins 5 - 8 SDI - SCI

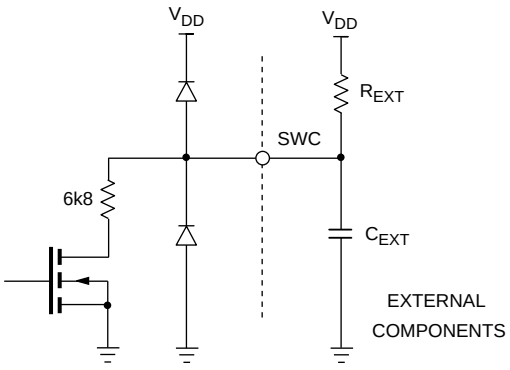


Fig. 5 Pin 15 SWC

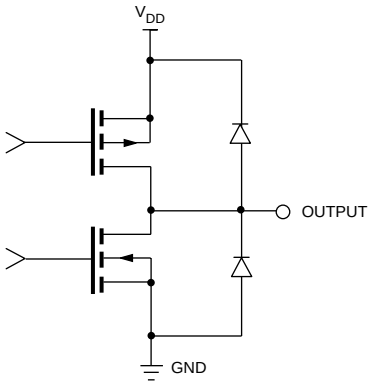


Fig. 6 Pins 3, 16, 17, 19 - 25, 27, 28
SWF, HSYNC, SSI, SSD, PCLK, PD0-9

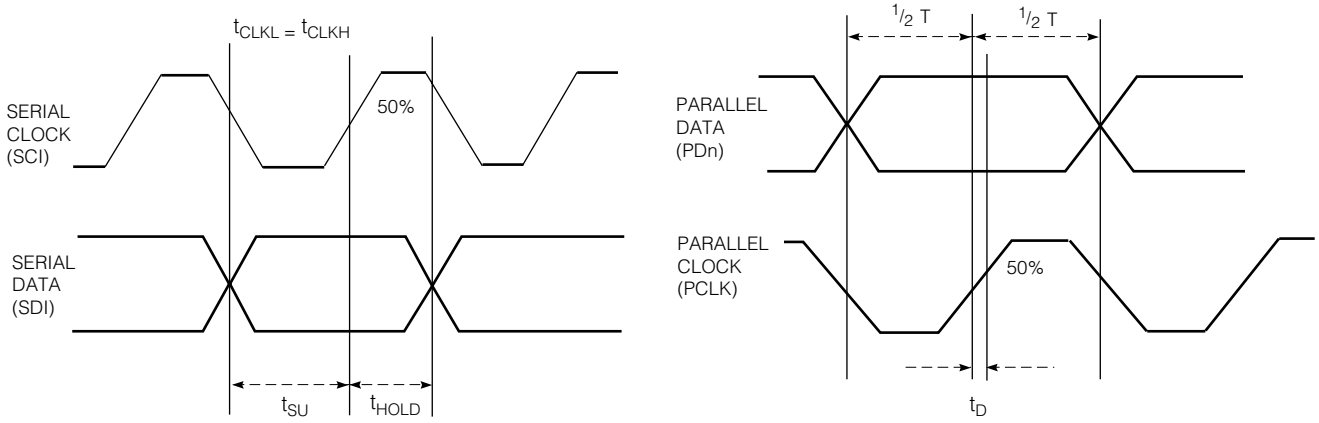


Fig. 7 Waveforms

TEST SET-UP & APPLICATION INFORMATION

Figure 8 shows the test set-up for the GS9000D operating from a V_{DD} supply of +5 volts. The differential pseudo ECL inputs for DATA and CLOCK (pins 5,6,7 and 8) must be biased between +3.0 and +4.05 volts. *In the application circuit shown in Figure 11, these inputs can be directly driven from the outputs of the GS7025 Reclocking Receiver with their resistor values set as shown.*

In other cases, such as true ECL level driver outputs, two biasing resistors are needed on the DATA and CLOCK inputs and the signals must be AC coupled.

It is critical that the decoupling capacitors connected to pins 12,13 and 18 are chip types and are located as close as possible to the device pins.

The critical high speed inputs, such as Serial Data (pins 5 and 6) and Serial Clock (pins 7 and 8), are located along one side of the device package to maintain very short interconnections when interfacing with the GS7025 Receiver.

If the automatic standard select function is not used, the Standard Select bits (pins 9 and 10) do not need to be connected, however the control input (pin 11) should be grounded.

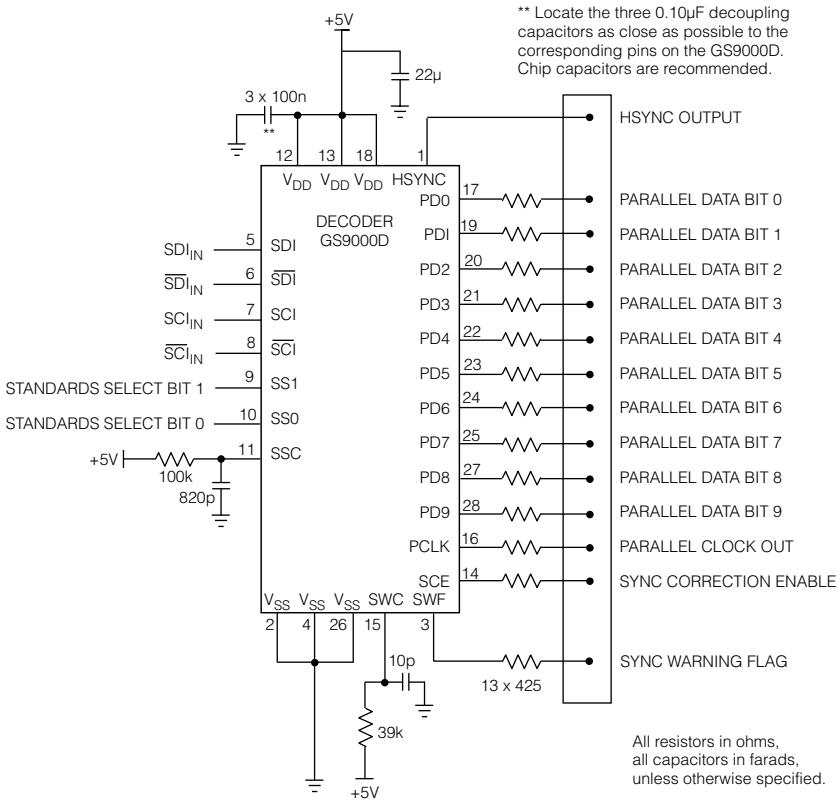


Fig. 8 GS9000D Test Set-Up

With synchronized serial data and clock connected to the GS9000D, the HSYNC output (pin 1) will toggle for each HSYNC detected. The Parallel Data bits PD0 through PD9 and the Parallel Clock can be observed on an oscilloscope or fed to a logic analyzer. To directly drive parallel inputs to receiving equipment, such as monitors or digital to analog converters, these outputs can be fed through a suitable TTL to ECL converter.

In operation, the HSYNC output from the GS9000D decoder toggles on each occurrence of the timing reference signal (TRS). The state of the HSYNC output is not significant, but the time at which it toggles is significant.

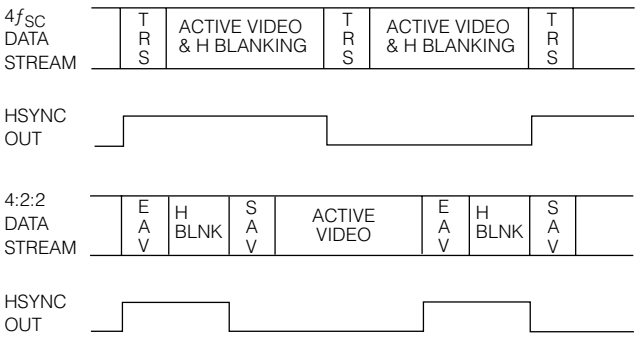


Fig. 9 Operation of HSYNC Output

The HSYNC output toggles to indicate the presence of the TRS on the falling edge of PCLK, one data symbol prior to the output of the first word in the TRS. In the following diagram, data is indicated in 10-bit Hex.

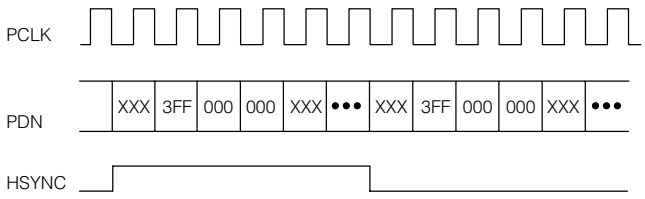
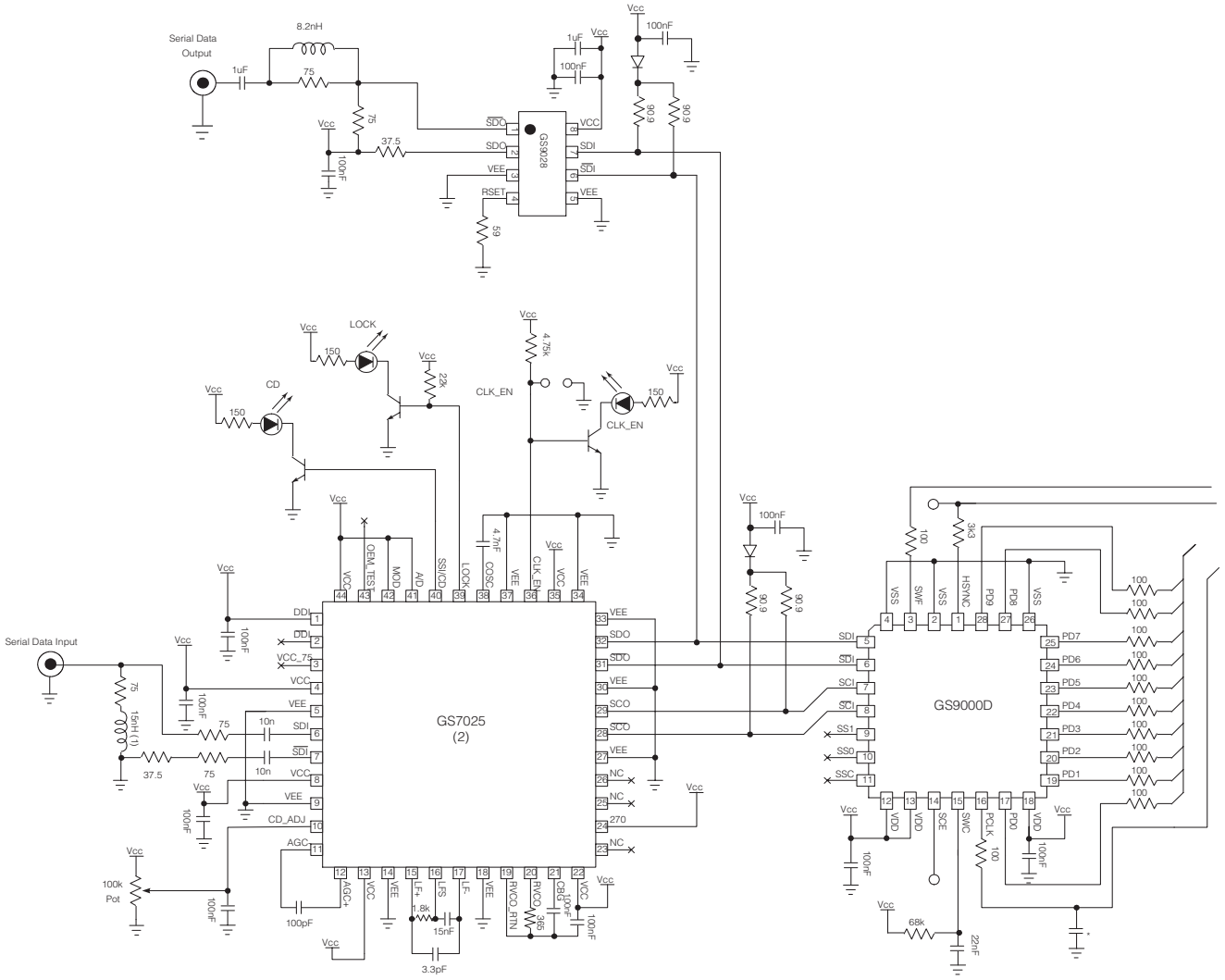


Fig. 10 Operation of HSYNC with Respect to PCLK

TYPICAL APPLICATION CIRCUIT - Adjustment Free Multi-standard Serial To Parallel Convertor



(1) Typical value for input return loss matching
(2) The GS7025 can be replaced by either the GS9025A or GS9035A for applications at data rates less then 270Mb/s or when equalization is not required

Fig. 11

GS9000D and GS7025 INTERCONNECTIONS

Figure 11 shows an application of the GS9000D in a 270Mb/s serial to parallel converter. This circuit uses the GS7025 Serial Digital Receiver. For datarates below 270Mb/s the GS9025A can be used. If cable equalization is not required the GS7025 or GS9025A may be replaced with a GS9035A Reclocker IC.

The GS9028 Cable Equalizer allows a serial loop through after the reclocker.

SYNC WARNING FLAG OPERATION

Each time HSYNC is not correctly detected, the Sync Warning Flag output (pin 3) will go HIGH. The RC network connected to the Sync Warning Control input (pin 15) sets the number of sync errors that will cause the SWF pin to go HIGH. The component values of the RC network shown in Figure 12 set the SWF error rate to approximately one HSYNC error in 10 lines. These component values are chosen for optimum performance of the SWF pin, and should not be adjusted.

Typically, HSYNC errors become visible on a monitor before the SWF provides an indication of HSYNC errors. As a result, the SWF function can be used in applications where the detection of significant signal degradation is desired.

A high SWF goes low when the input error rate decreases below the set rate. A small amount of hysteris in the comparator ensures noise immunity.

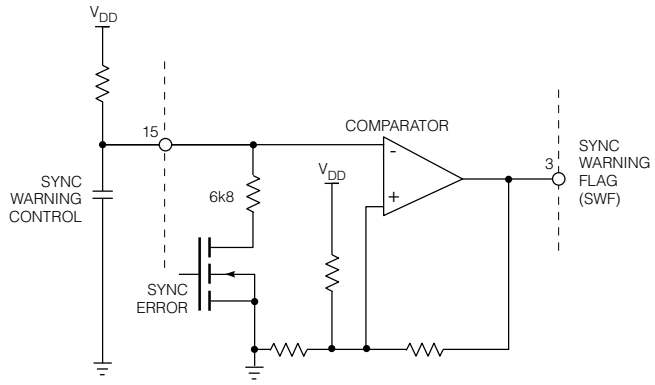


Fig. 12 Sync Warning Flag Circuit

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change without notice.

REVISION NOTES:
Added lead-free and green information.

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