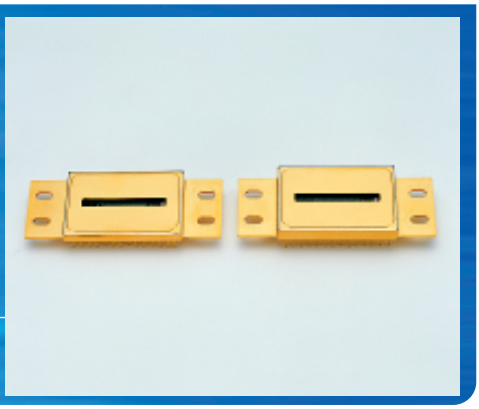
NEW

IMAGE SENSOR

InGaAs linear image sensor
G8160 to G8163/G8180 series

Near infrared image sensors (0.9 to 1.67 µm / 0.9 to 2.55 µm)



G8160 to G8163/G8180 series InGaAs linear image sensors are specifically designed for near infrared multichannel spectrophotometry. These linear image sensors consist of an InGaAs photodiode array, a charge amplifier array, an offset compensation circuit, a shift register and a timing generator formed on a CMOS chip. The charge amplifier array is made up of CMOS transistors connected to each pixel of the InGaAs photodiode array. Signals from each pixel are read out in charge integration mode to achieve high sensitivity and stable operation in the near infrared spectral range. The package is hermetically sealed for high reliability.
Signal processing circuits on the CMOS chip allow selecting a feedback capacitance (Cf) of 10 pF or 0.5 pF by using an external voltage input. The image sensor operates over a wide dynamic range when Cf=10 pF and delivers high gain when Cf=0.5 pF.

Features

- Wide dynamic range
- Low noise and low dark current
- Selectable gain
- Anti-saturation circuit
- CDS circuit *1
- Offset compensation circuit
- Simple operation (by built-in timing generator) *2
- High resolution: 25 µm pitch (512 ch)
- Low cross-talk
- 256 ch: 1 video line
  512 ch: 2 video lines

Applications

- Near infrared multichannel spectrophotometry
- Radiation thermometry
- Non-destructive inspection

Related products

- InGaAs multichannel detector head C8061/C8062
- Multichannel detector head controller C7557

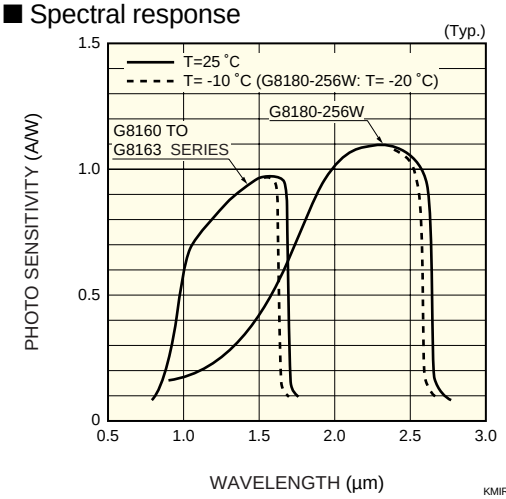
■ Selection guide

Type No.	Cooling	Number. of pixels	Pixel pitch (µm)	Pixel size [µm (H) × µm (V)]	Spectral response range (µm)	Defective pixel
G8160-256S	One-stage TE-cooled	256	50	50 × 250	0.9 to 1.67	2 % Max.
G8161-512S		512	25	25 × 250		
G8162-256S		256	50	50 × 500		
G8163-512S		512	25	25 × 500		
G8180-256W	Two-stage TE-cooled	256	50	50 × 250	0.9 to 2.55	5 % Max.

*1: CDS (Correlated Double Sampling) circuit
A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.

*2: Timing generator
Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (Programmable Logic Devices) are used to input the required timing signals. However, G8160 to G8163/G8180 series image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

■ Spectral response



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■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Clock pulse voltage	Vϕ	5.5	V
Operating temperature *1	Topr	0 to +70	°C
Storage temperature *1	Tstg	-40 to +70	°C

*1: Non condensation

■ Electrical characteristics (Ta=25 °C, Vϕ=5 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.5	5.0	5.5	V
		Vref	-	1.26	-	
Ground		Vss	-	0	-	V
Element bias		INP	3.5	4.5	4.6	V
Clock frequency		f	0.1	-	4	MHz
Clock pulse voltage	high	Vϕ	Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	low		0	0	0.4	V
Clock pulse rise/fall times		tr ϕ	0	20	100	ns
		tf ϕ				
Clock pulse width		tpw ϕ	200	-	-	ns
Reset pulse voltage	high	V (RES)	Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	low		0	0	0.4	V
Reset pulse rise/fall times		tr (RES)	0	20	100	ns
		tf (RES)				
Reset pulse width		tpw (RES)	6000	-	-	ns
Video output voltage	high	VH	-	4.4	-	V
	low	VL	0	1.26	-	
Data rate		fV	-	f/8	-	Hz

■ Electrical and optical characteristics
General ratings (T=25 °C)

Parameter	Symbol	G8160 to G8163 series			G8180-256W			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Peak sensitivity wavelength	λp	-	1.55	-	-	2.3	-	μm
Saturation charge *2	Qsat	-	30	-	-	30	-	pC
PRNU *3	PRNU	-	-	±5 *3	-	-	±10 *4	%

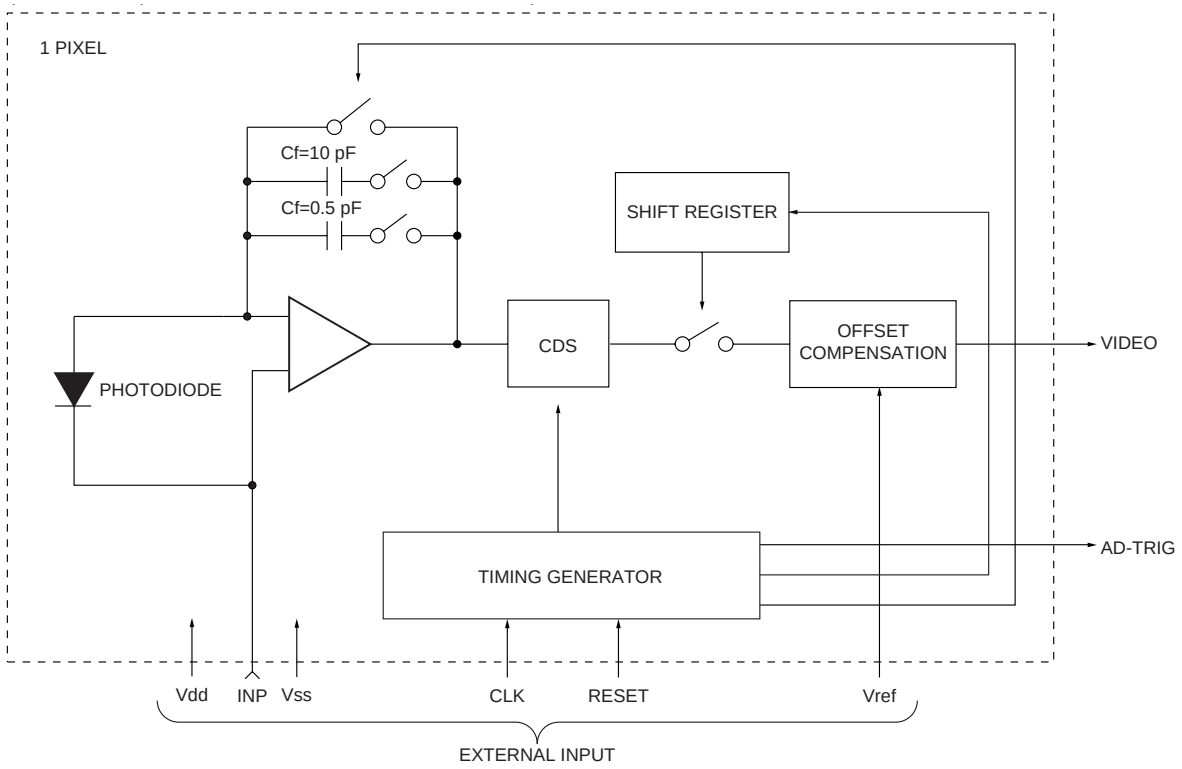
*2: Vϕ=5 V, Cf=10 pF
*3: 50 % of saturation, 10 ms integration time, after dark output subtraction, excluding first and last pixels.
*4: 50 % of saturation, 3 ms integration time, after dark output subtraction, excluding first and last pixels.

Dark current characteristics (T=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
G8160-256S	ID	-	2	8	pA
G8161-512S		-	1.5	6	
G8162-256S		-	4	16	
G8163-512S			4	16	
G8180-256W *5		-	1000	4000	

*5: TD= -25 °C

■ Equivalent circuit



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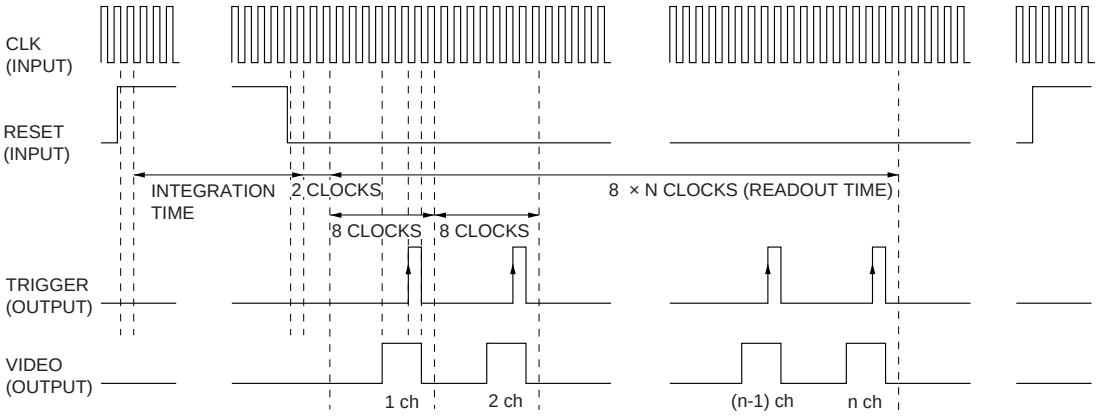
■ Timing chart



■ Basic circuit connection

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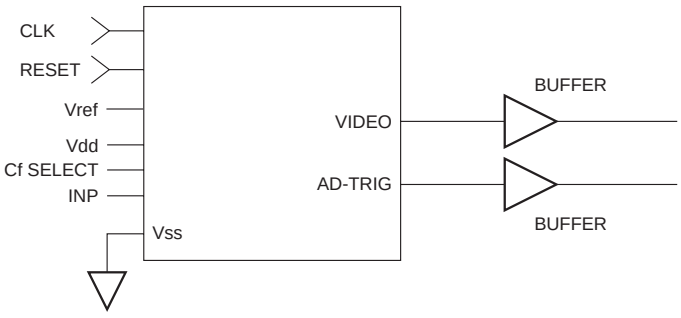

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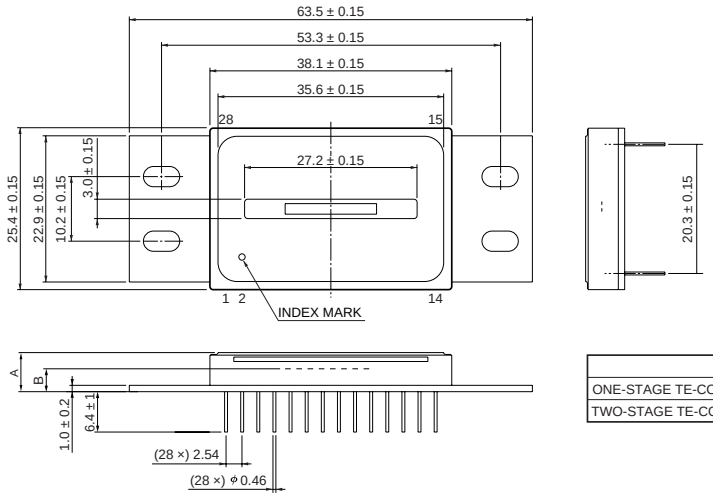
■ Dimensional outline (unit: mm)



	A	B
ONE-STAGE TE-COOLED	6.15	3.6
TWO-STAGE TE-COOLED	7.25	4.5

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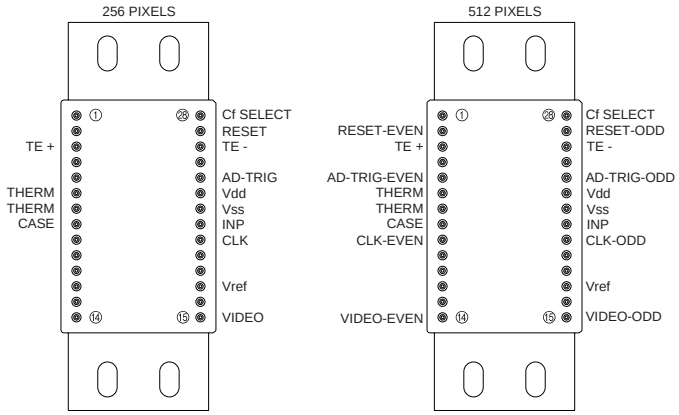
■ Pin connection (top view)



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Terminal name	Input/Output	Function and recommended connection
CLK	Input (CMOS logic compatible)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic compatible)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed on the CMOS chip. The width of the reset pulse is integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit on the CMOS chip.
Vss	-	Ground for the signal processing circuit on the CMOS chip.
INP	Input	Reset voltage for the charge amplifier array on the CMOS chip.
Cf SELECT	Input	Voltage that determines the feedback capacitance (Cf) on the CMOS chip. Cf=10 pF at 0 V, and Cf=0.5 pF at 5 V.
CASE	-	This terminal is electrically connected to the package.
THERM	-	Thermistor for monitoring temperature inside the package. No connection for room temperature operation type.
TE+, TE-	-	Power supply terminal for the thermoelectric cooler that cools the photodiode array. No connection for room temperature operation type.
AD-TRIG	Output	Digital signal for AD conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit at the CMOS chip

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