4AM15

Silicon N-Channel/P-Channel Power MOS FET Array

HITACHI

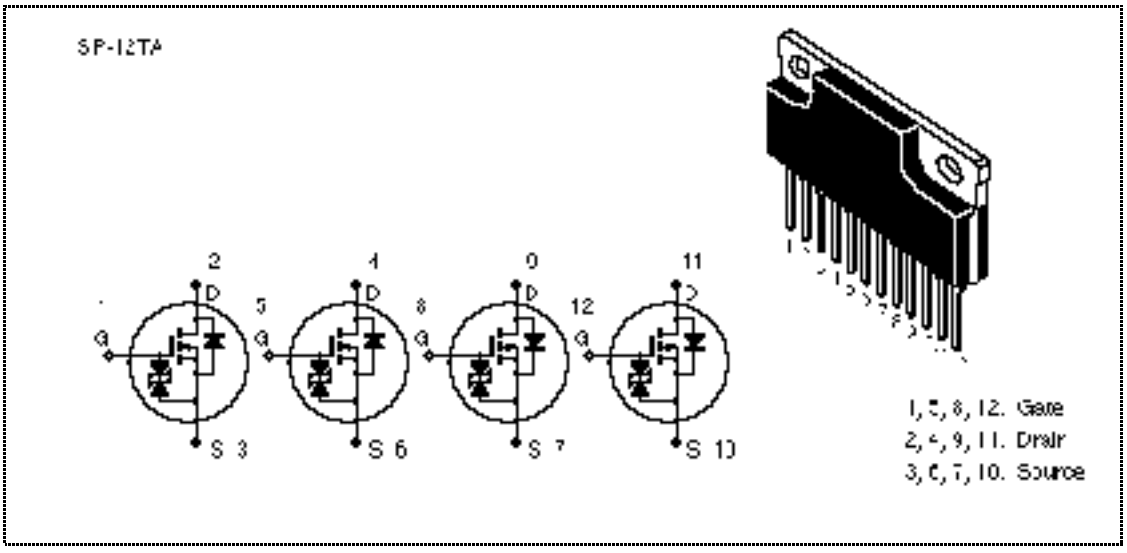
Application

High speed power switching

Features

- Low on-resistance
  N Channel: $R_{DS(on)} \leq 0.5\ \Omega$, $V_{GS} = 10$ V, $I_D = 2$ A
  P Channel: $R_{DS(on)} \leq 0.9\ \Omega$, $V_{GS} = -10$ V, $I_D = -2$ A
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	200	–200	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	4	–4	A
Drain peak current	$I_{D(pulse)}$*[1]	16	–16	A
Body to drain diode reverse drain current	I_{DR}	4	–4	A
Channel dissipation	Pch (Tc = 25°C)*[2]	32		W
	Pch*[2]	4.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. 4 Device Operation

Electrical Characteristics (Ta = 25°C)

		N Channel				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.33	0.5	Ω	I_D = 2 A, V_{GS} = 10 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	1.5	3.0	—	S	I_D = 2 A V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	750	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	260	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	40	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	19	—	ns	I_D = 2 A
Rise time	t_r	—	26	—	ns	V_{GS} = 10 V
Turn-off delay time	$t_{d(off)}$	—	45	—	ns	R_L = 15 Ω
Fall time	t_f	—	24	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.0	—	V	I_F = 4 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	125	—	ns	I_F = 4 A, V_{GS} = 0, diF/dt = 100 A/µs

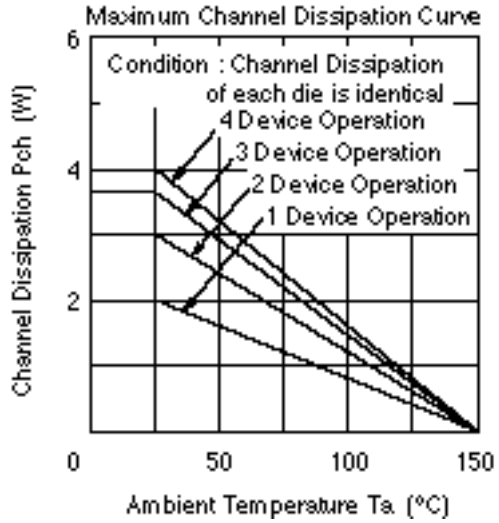
Note: 1. Pulse Test

See characteristic curves of 2SK1957

Electrical Characteristics (Ta = 25°C)

		P Channel				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test conditions**
Drain to source breakdown voltage	$V_{(BR)DSS}$	–200	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–250	µA	V_{DS} = –160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–2.0	—	–4.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.7	0.9	Ω	I_D = –2 A, V_{GS} = –10 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	1.5	3.0	—	S	I_D = –2 A V_{DS} = –10 V*[1]
Input capacitance	Ciss	—	920	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	23 0	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	70	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	I_D = –2 A
Rise time	t_r	—	40	—	ns	V_{GS} = –10 V
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	R_L = 15 Ω
Fall time	t_f	—	45	—	ns	
Body to drain diode forward voltage	V_{DF}	—	–1.0	—	V	I_F = –4 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	170	—	ns	I_F = –4 A, V_{GS} = 0, diF/dt = 100 A/µs

Note: 1. Pulse Test



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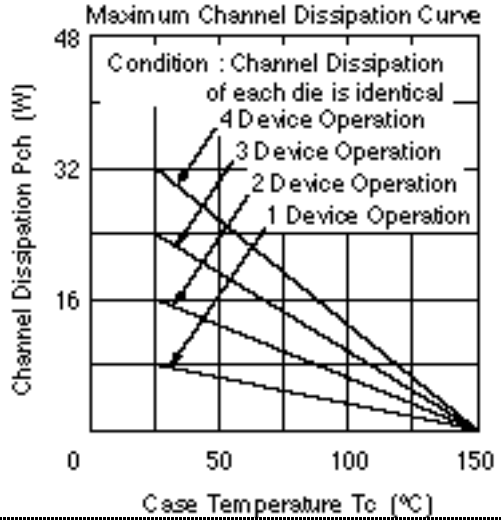
Maximum Channel Dissipation Curve
Condition : Channel Dissipation
of each die is identical
4 Device Operation
3 Device Operation
2 Device Operation
1 Device Operation
Channel Dissipation Pch (W)
48
32
16
0
50
100
150
Case Temperature Tc (°C)

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