
4AM16

Silicon N-Channel/P-Channel Power MOS FET Array

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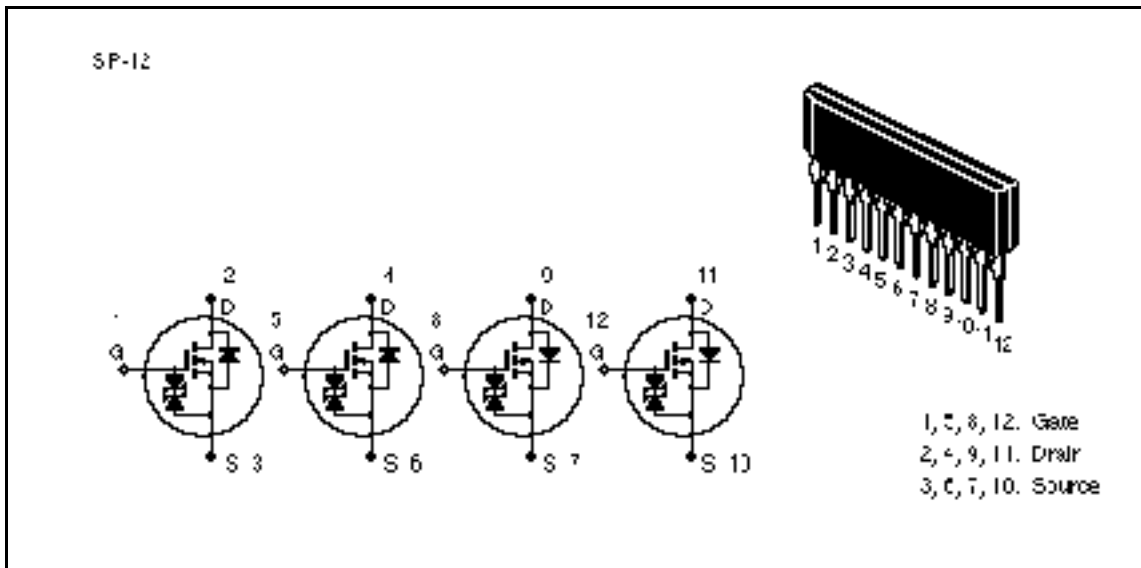
Application

High speed power switching

Features

- Low on-resistance
N Channel: $R_{DS(on)} = 0.17 \Omega$, $V_{GS} = 10 \text{ V}$, $I_D = 4 \text{ A}$
P Channel: $R_{DS(on)} = 0.2 \Omega$, $V_{GS} = -10 \text{ V}$, $I_D = -4 \text{ A}$
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline



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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	60	-60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	8	-8	A
Drain peak current	$I_{D(pulse)}^{*1}$	32	-32	A
Body to drain diode reverse drain current	I_{DR}	8	-8	A
Channel dissipation	$Pch (T_C = 25°C)^{*2}$	28		W
	Pch^{*2}	4.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	-55 to +150		°C

Notes: 1. PW 10 μs, duty cycle 1%

2. 4 Device Operation

Electrical Characteristics (Ta = 25°C)

Item	Symbol	N channel			Unit	Test conditions
		Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-250	μA	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.17		$I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}^{*1}$
		—	0.18	0.24		$I_D = 4 \text{ A}, V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	3.5	5.5	—	S	$I_D = 4 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	400	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	220	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	60	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	5	—	ns	$I_D = 4 \text{ A}$
Rise time	t_r	—	45	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	150	—	ns	$R_L = 7.5$
Fall time	t_f	—	85	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.2	—	V	$I_F = 8 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	120	—	ns	$I_F = 8 \text{ A}, V_{GS} = 0,$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 1. Pulse Test

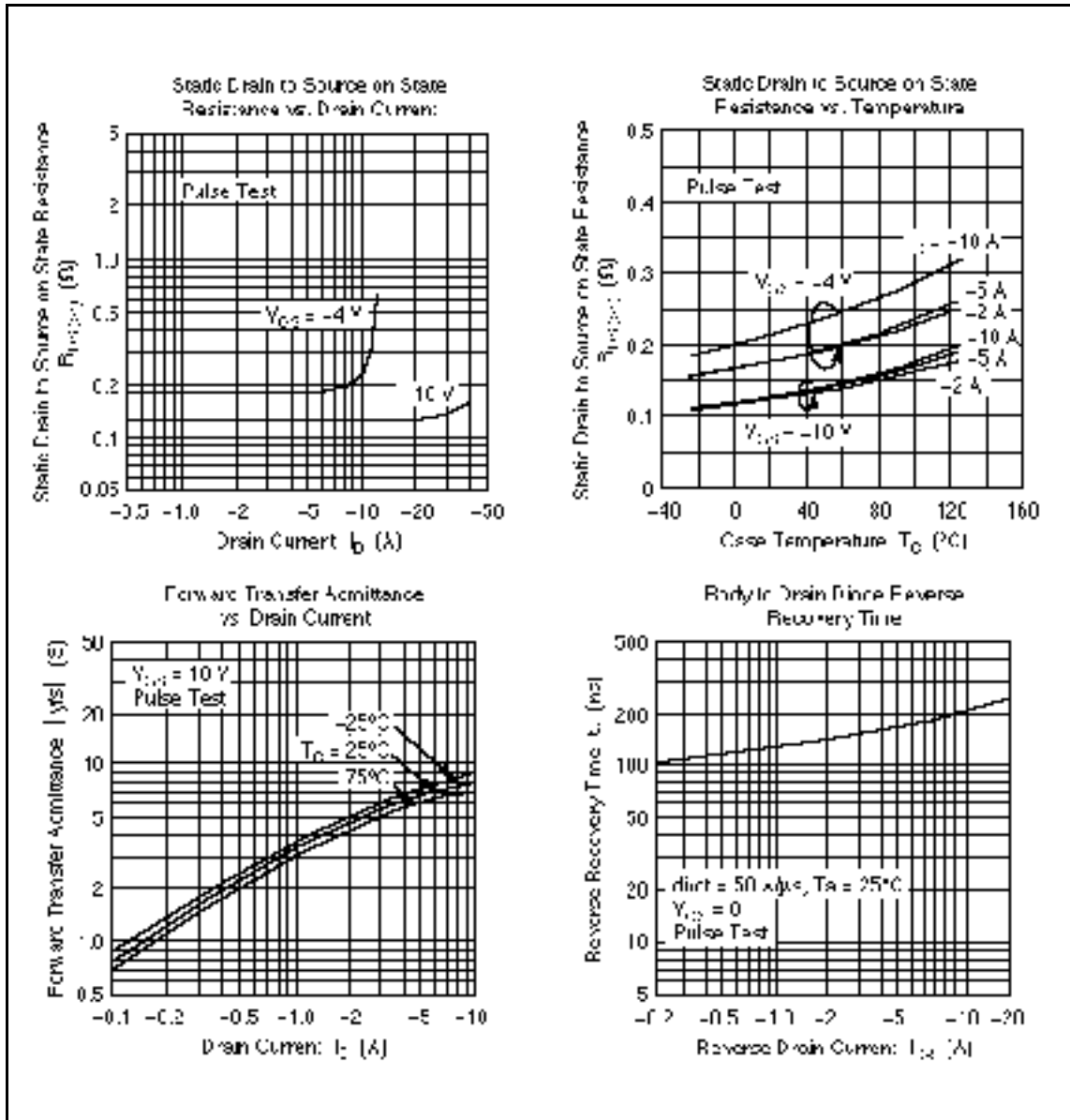
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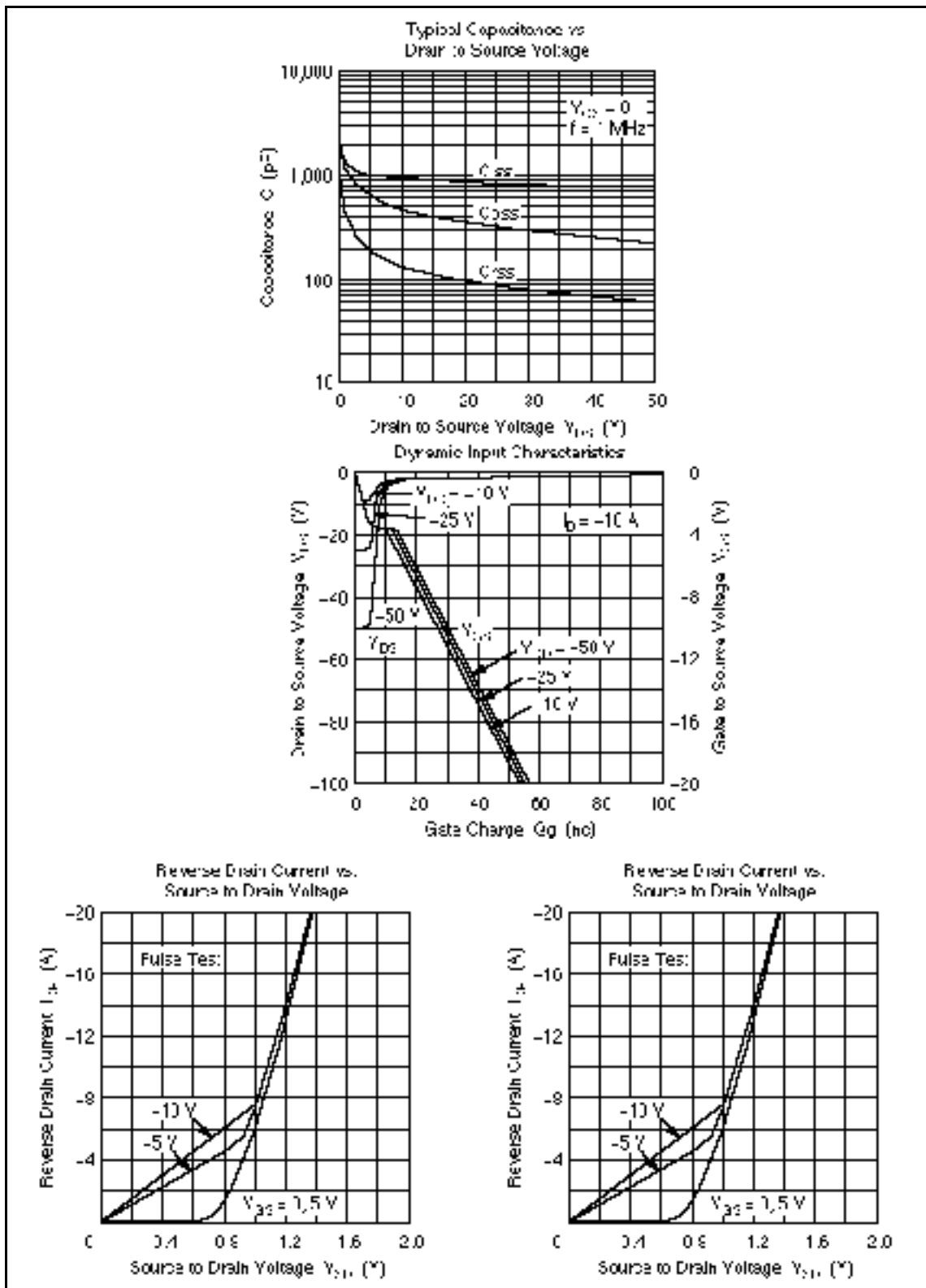
Electrical Characteristics (Ta = 25°C)

Item	Symbol	P channel			Unit	Test conditions
		Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-250	μA	$V_{DS} = -50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1 \text{ mA}, V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.15	0.20		$I_D = -4 \text{ A}, V_{GS} = -10 \text{ V}^{*1}$
		—	0.20	0.27		$I_D = -4 \text{ A}, V_{GS} = -4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	3.5	6.0	—	S	$I_D = -4 \text{ A}$ $V_{DS} = -10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	900	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	C_{oss}	—	460	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	130	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	8	—	ns	$I_D = -4 \text{ A}$
Rise time	t_r	—	50	—	ns	$V_{GS} = -10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	180	—	ns	$R_L = 7.5$
Fall time	t_f	—	95	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-1.2	—	V	$I_F = -8 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	185	—	ns	$I_F = -8 \text{ A}, V_{GS} = 0,$ $diF/dt = 50 \text{ A}/\mu\text{s}$

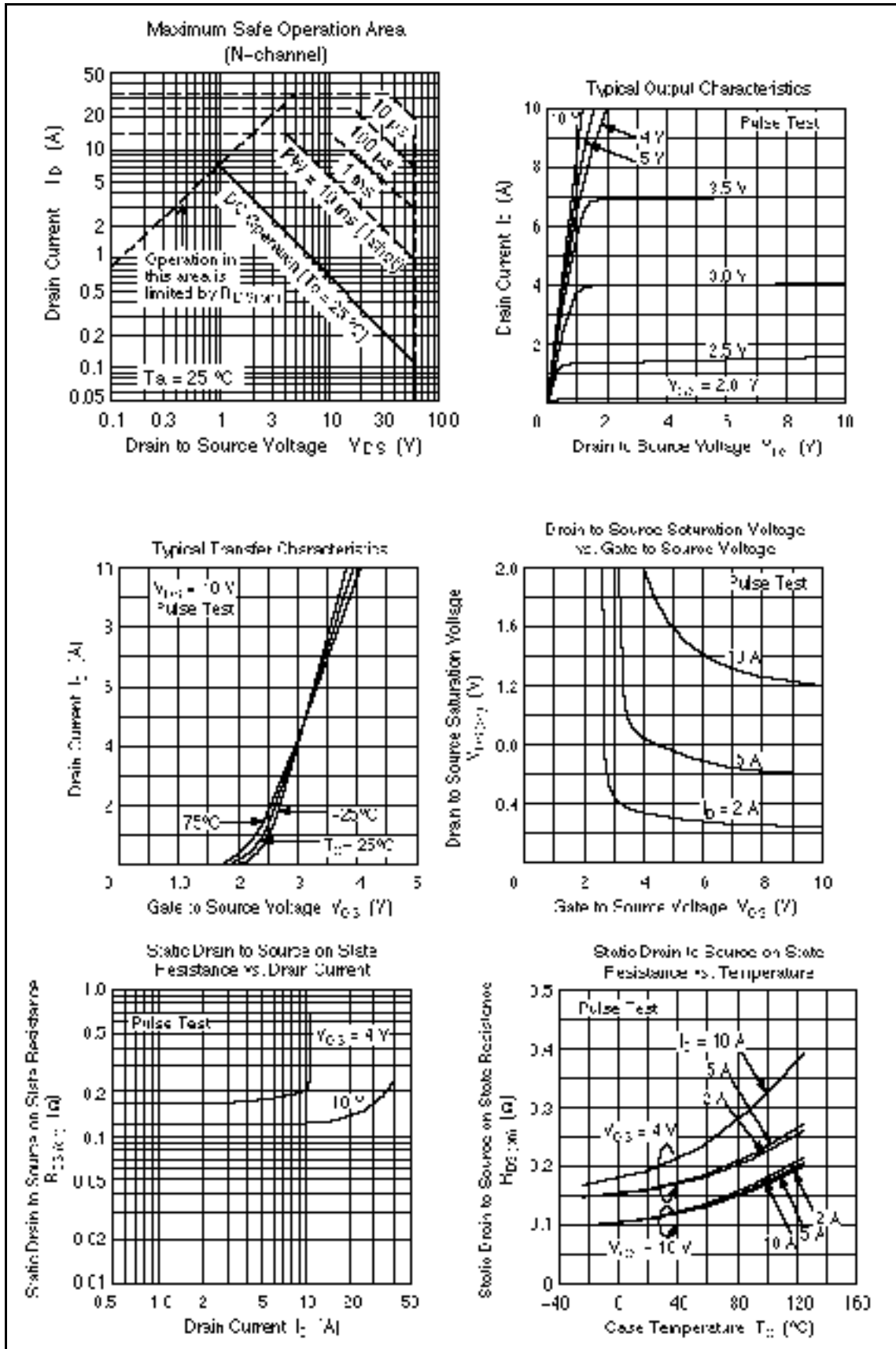
Note: 1. Pulse Test

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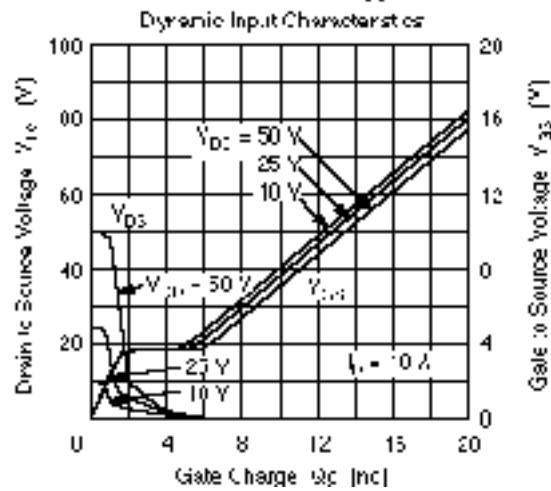
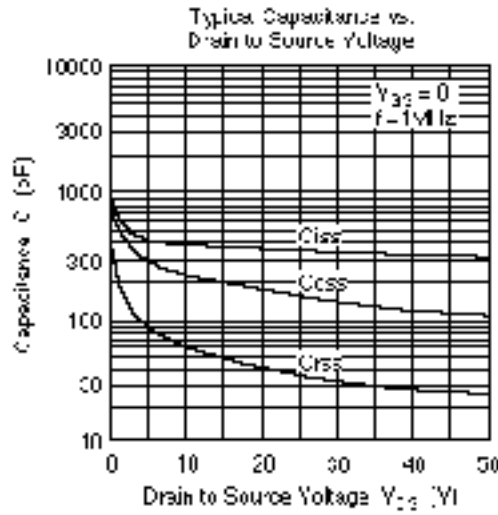
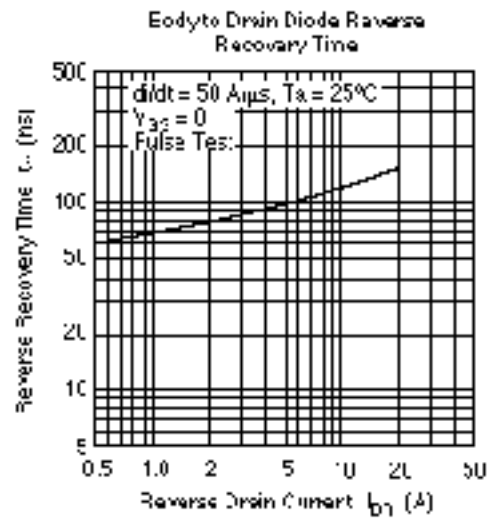
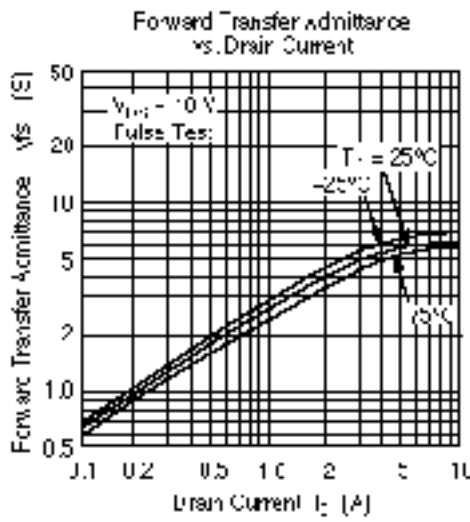




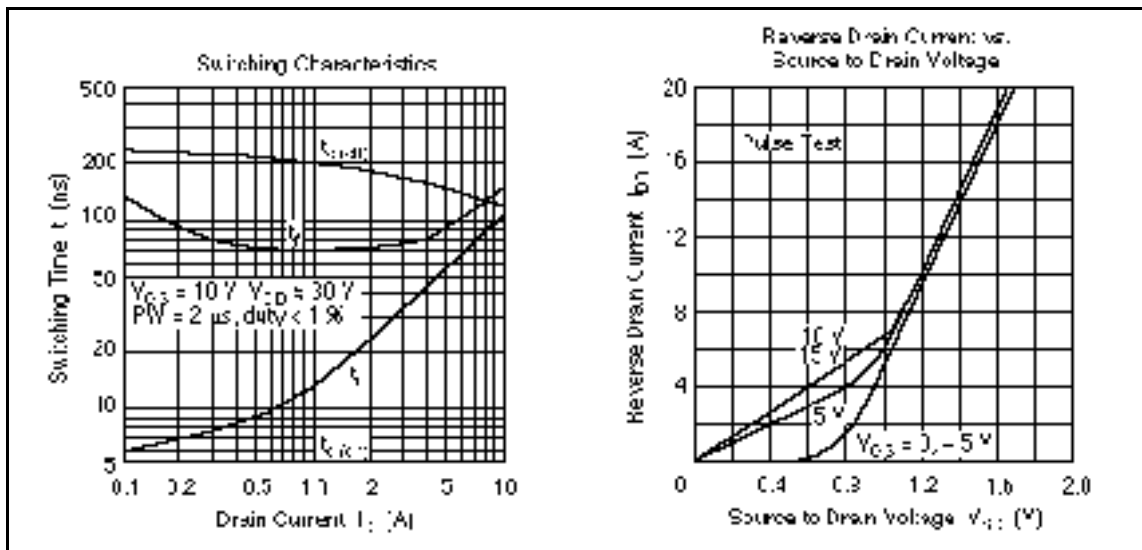
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