

# HD14017B

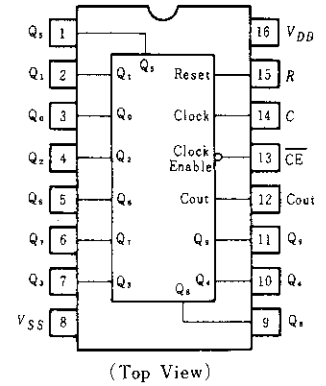
## Decade Counter/Divider

The HD14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

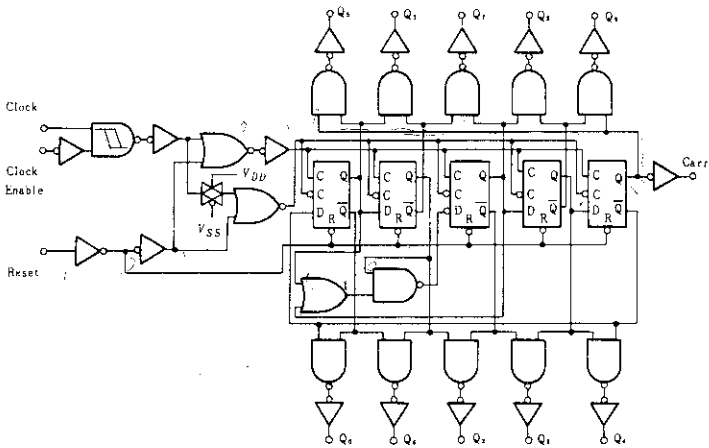
### FEATURES

- Carry Output for Cascading 12MHz (typ) Operation @10V
- Divide-by-N Counting
- Quiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B and MC14017B

### PIN ARRANGEMENT



### LOGIC DIAGRAM



### TRUTH TABLE

C	CE	R	Decode Output = n
0	x	0	n
x	1	0	n
x	x	1	Q <sub>0</sub>
	0	0	n + 1
	x	0	n
x		0	n
1		0	n + 1

Notes) 1. x : Don't Care.  
2. If n < 5 Carry = "1", Otherwise = "0"

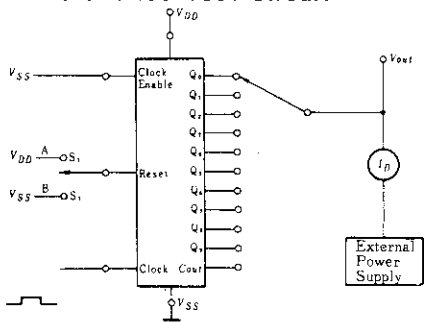
**ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	V <sub>DD</sub> (V)	Test Conditions	-40°C		25°C			85°C		Unit
				min	max	min	typ	max	min	max	
Output Voltage	V <sub>OL</sub>	5.0	V <sub>in</sub> = V <sub>DD</sub> or 0	-	0.05	-	0	0.05	-	0.05	V
		10		-	0.05	-	0	0.05	-	0.05	
		15		-	0.05	-	0	0.05	-	0.05	
	V <sub>OH</sub>	5.0	V <sub>in</sub> = 0 or V <sub>DD</sub>	4.95	-	4.95	5.0	-	4.95	-	V
		10		9.95	-	9.95	10	-	9.95	-	
		15		14.95	-	14.95	15	-	14.95	-	
Input Voltage	V <sub>IL</sub>	5.0	V <sub>out</sub> = 4.5 or 0.5V	-	1.5	-	2.25	1.5	-	1.5	V
		10	V <sub>out</sub> = 9.0 or 1.0V	-	3.0	-	4.50	3.0	-	3.0	
		15	V <sub>out</sub> = 13.5 or 1.5V	-	4.0	-	6.75	4.0	-	4.0	
	V <sub>IH</sub>	5.0	V <sub>out</sub> = 0.5 or 4.5V	3.5	-	3.5	2.75	-	3.5	-	V
		10	V <sub>out</sub> = 1.0 or 9.0V	7.0	-	7.0	5.50	-	7.0	-	
		15	V <sub>out</sub> = 1.5 or 13.5V	11.0	-	11.0	8.25	-	11.0	-	
Output Drive Current	I <sub>OH</sub>	5.0	V <sub>OH</sub> = 2.5V	-1.0	-	-0.8	-1.7	-	-0.6	-	mA
		5.0	V <sub>OH</sub> = 4.6V	-0.2	-	-0.16	-0.36	-	-0.12	-	
		10	V <sub>OH</sub> = 9.5V	-0.5	-	-0.4	-0.9	-	-0.3	-	
		15	V <sub>OH</sub> = 13.5V	-1.4	-	-1.2	-3.5	-	-1.0	-	
	I <sub>OL</sub>	5.0	V <sub>OL</sub> = 0.4V	0.52	-	0.44	0.88	-	0.36	-	mA
		10	V <sub>OL</sub> = 0.5V	1.3	-	1.1	2.25	-	0.9	-	
15		V <sub>OL</sub> = 1.5V	3.6	-	3.0	8.8	-	2.4	-		
Input Current	I <sub>in</sub>	15		-	±0.3	-	±0.0001	±0.3	-	±1.0	μA
Input Capacitance	C <sub>in</sub>	-	V <sub>in</sub> = 0	-	-	-	5.0	7.5	-	-	pF
Quiescent Current	I <sub>DD</sub>	5.0	Zero Signal, per Package	-	20	-	0.005	20	-	150	μA
		10		-	40	-	0.010	40	-	300	
		15		-	80	-	0.015	80	-	600	
Total Supply Current*	I <sub>T</sub>	5.0	Dynamic + I <sub>DD</sub> ,	-	-	-	0.27	-	-	-	μA
		10	C <sub>L</sub> = 50pF, f = 1 kHz,	-	-	-	0.55	-	-	-	
		15	per Gate	-	-	-	0.83	-	-	-	

\* To calculate total supply current at frequency other than 1kHz.  
 @ V<sub>DD</sub> = 5.0V I<sub>T</sub> = (0.27μA/kHz) f + I<sub>DD</sub>    @ V<sub>DD</sub> = 10V I<sub>T</sub> = (0.55μA/kHz) f + I<sub>DD</sub>    @ V<sub>DD</sub> = 15V I<sub>T</sub> = (0.83μA/kHz) f + I<sub>DD</sub>

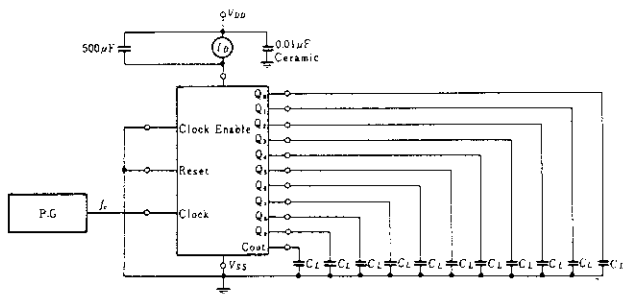
**DC CHARACTERISTIC TEST CIRCUIT**

● Typical Output Source and Output Sink Characteristics Test Circuit



	I <sub>OL</sub>	I <sub>OH</sub>
DECODE OUTPUTS	(S1 - A)	Clock to desired outputs (S1 to B)
Carry	Clock5-9(S1-B)	S1 - A
V <sub>CS</sub> =	V <sub>DD</sub>	- V <sub>DD</sub>
V <sub>OS</sub> =	V <sub>out</sub>	V <sub>out</sub> - V <sub>DD</sub>

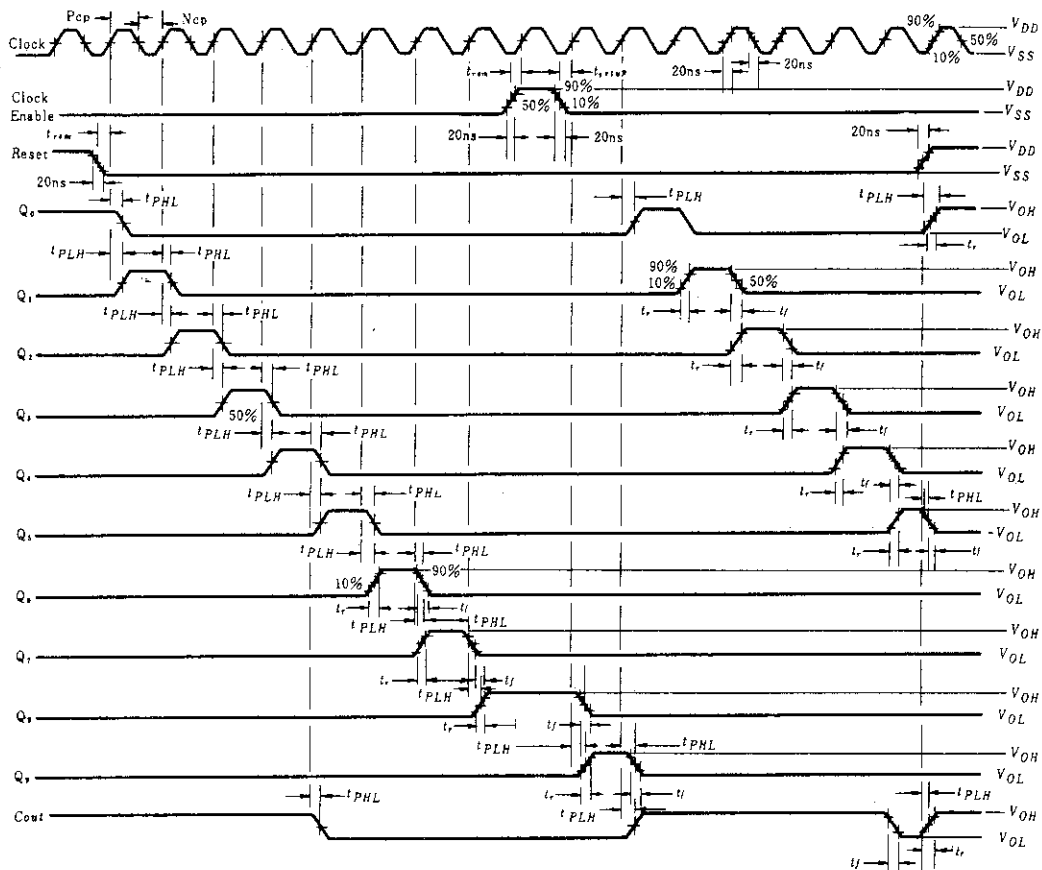
**POWER DISSIPATION TEST CIRCUIT**



**■ SWITCHING CHARACTERISTICS** ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic		Symbol	$V_{DD}(\text{V})$	min	typ	max	Unit			
Output Rise Time		$t_r$	5.0	—	180	400	ns			
			10	—	90	200				
			15	—	65	160				
Output Fall Time		$t_f$	5.0	—	100	200	ns			
			10	—	50	100				
			15	—	37	80				
Propagation Delay Time	Reset-to-Decode	$t_{PLH}, t_{PHL}$	5.0	—	500	1000	ns			
			10	—	230	460				
			15	—	140	350				
	Clock-to-Cout		5.0	—	400	800				
			10	—	150	350				
			15	—	100	250				
	Clock-to-Decode		5.0	—	500	1000				
			10	—	230	460				
			15	—	140	350				
	Reset-to-Cout			$t_{PLH}$	5.0	—		400	800	ns
					10	—		150	350	
					15	—		100	250	
Clock Pulse Width		$PWC$	5.0	250	100	—	ns			
			10	100	42	—				
			15	75	30	—				
Clock Pulse Frequency		$PRF$	5.0	—	5.0	2.0	MHz			
			10	—	12	5.0				
			15	—	16	6.7				
Reset Pulse Width		$PWR$	5.0	500	200	—	ns			
			10	250	100	—				
			15	190	75	—				
Reset Removal Time		$t_{rem}$	5.0	750	300	—	ns			
			10	275	100	—				
			15	210	80	—				
Clock Pulse Rise and Fall Time		$t_r, t_f$	5.0	No Limit						
			10							
			15							
Clock Enable Setup Time		$t_{setup}$	5.0	700	175	—	ns			
			10	300	75	—				
			15	225	52	—				
Clock Enable Removal Time		$t_{rem}$	5.0	700	260	—	ns			
			10	300	100	—				
			15	225	70	—				

■ DYNAMIC SIGNAL WAVEFORMS





Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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