

# CoolSET™-F2

**ICE2A0565/165/265/365**

**ICE2B0565/165/265/365**

**ICE2A180Z/280Z**

**ICE2A765P/2B765P**

Off-Line SMPS Current Mode  
Controller with integrated 650V/  
800V CoolMOS™

**Power Management & Supply**



Never stop thinking.

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**CoolSET™-F2****Revision History:****2002-08-08**

Datasheet

Previous Version:

First One

Page	Subjects (major changes since last revision)

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**Edition 2002-08-08**

**Published by Infineon Technologies AG,  
St.-Martin-Strasse 53,  
D-81541 München**

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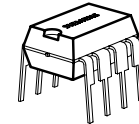
## Off-Line SMPS Current Mode Controller with integrated 650V/800V CoolMOS™

### Product Highlights

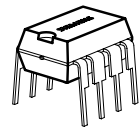
- Best in Class in DIP8, DIP7, TO220 Packages
- No Heatsink required for DIP8, DIP7
- Lowest Standby Power Dissipation
- Enhanced Protection Functions all with Auto Restart Mode
- Isolated Drain Package for TO220

### Features

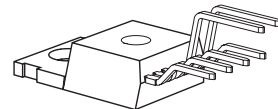
- 650V/800V Avalanche Rugged CoolMOS™
- Only few external Components required
- Input Undervoltage Lockout
- 67kHz/100kHz Switching Frequency
- Max Duty Cycle 72%
- Low Power Standby Mode to meet European Commission Requirements
- Thermal Shut Down with Auto Restart
- Overload and Open Loop Protection
- Overvoltage Protection during Auto Restart
- Adjustable Peak Current Limitation via External Resistor
- Overall Tolerance of Current Limiting <math>< \pm 5\%</math>
- Internal Leading Edge Blanking
- User defined Soft Start
- Soft Switching for Low EMI



P-DIP-8-6



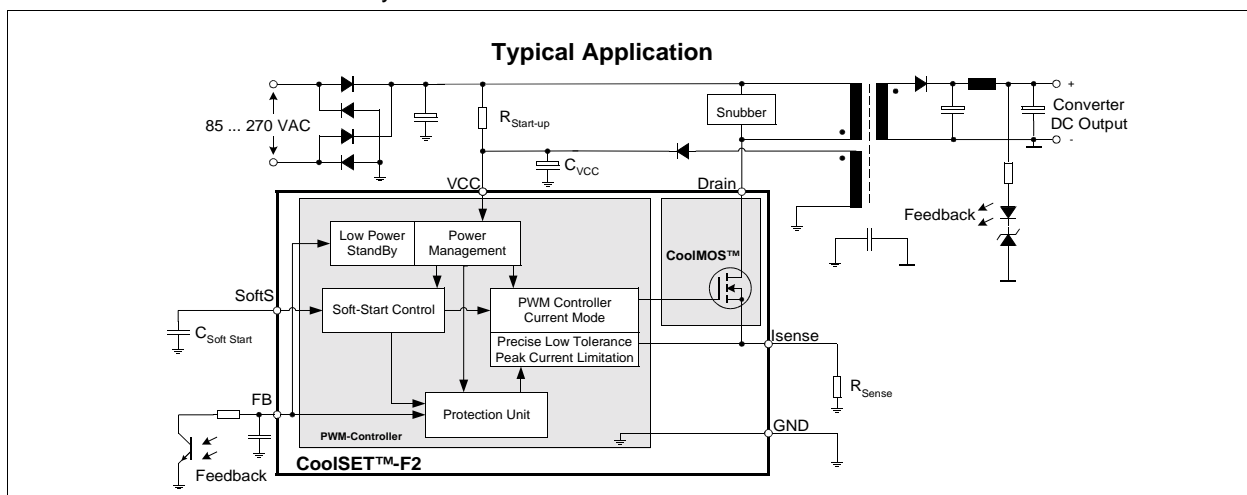
P-DIP-7-1



P-TO220-6-3

### Description

The second generation COOLSET™-F2 provides several special enhancements to satisfy the needs for low power standby and protection features. In standby mode frequency reduction is used to lower the power consumption and support a stable output voltage in this mode. The frequency reduction is limited to 20kHz/21.5 kHz to avoid audible noise. In case of failure modes like open loop, overvoltage or overload due to short circuit the device switches in Auto Restart Mode which is controlled by the internal protection unit. By means of the internal precise peak current limitation the dimension of the transformer and the secondary diode can be lower which leads to more cost efficiency.



## Ordering codes

Type	Ordering Code	Package	V <sub>DS</sub>	F <sub>OSC</sub>	R <sub>DSon</sub> <sup>1)</sup>	230VAC ±15% <sup>2)</sup>	85-265 VAC <sup>2)</sup>
ICE2A0565	Q67040-S4542-A101	P-DIP-8-6	650V	100kHz	4.7Ω	23W	13W
ICE2A165	Q67040-S4426	P-DIP-8-6	650V	100kHz	3.0Ω	31W	18W
ICE2A265	Q67040-S4414	P-DIP-8-6	650V	100kHz	0.9Ω	52W	32W
ICE2A365	Q67040-S4415	P-DIP-8-6	650V	100kHz	0.45Ω	67W	45W
ICE2B0565	Q67040-S4540-A101	P-DIP-8-6	650V	67kHz	4.7Ω	23W	13W
ICE2B165	Q67040-S4489-A001	P-DIP-8-6	650V	67kHz	3.0Ω	31W	18W
ICE2B265	Q67040-S4478-A001	P-DIP-8-6	650V	67kHz	0.9Ω	52W	32W
ICE2B365	Q67040-S4490-A001	P-DIP-8-6	650V	67kHz	0.45Ω	67W	45W
ICE2A180Z	Q67040-S4546-A101	P-DIP-7-1	800V	100kHz	3.0Ω	29W	17W
ICE2A280Z	Q67040-S4547-A101	P-DIP-7-1	800V	100kHz	0.8Ω	50W	31W

<sup>1)</sup> typ @ T=25°C

<sup>2)</sup> Maximum power rating at Ta=75°C, Tj=125°C and with copper area on PCB = 6cm<sup>2</sup>,

Type	Ordering Code	Package	V <sub>DS</sub>	F <sub>OSC</sub>	R <sub>DSon</sub> <sup>1)</sup>	230VAC ±15% <sup>2)</sup>	85-265 VAC <sup>2)</sup>
ICE2A765P	Q67040-S4533	P-TO-220-6-3	650V	100kHz	0.5Ω	240W	130W
ICE2B765P	Q67040-S4532	P-TO-220-6-3	650V	67kHz	0.5Ω	240W	130W

<sup>1)</sup> typ @ T=25°C

<sup>2)</sup> Maximum practical continuous power in an open frame design at Ta=75°C, Tj=125°C and Rth=2.7K/W.

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**Pin Configuration and Functionality**

# 1 Pin Configuration and Functionality

## 1.1 Pin Configuration with P-DIP-8-6

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	Isense	Controller Current Sense Input, CoolMOS™ Source Output
4	Drain	650V <sup>1)</sup> /800V CoolMOS™ Drain
5	Drain	650V <sup>1)</sup> /800V <sup>2)</sup> CoolMOS™ Drain
6	N.C	Not connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

1) at  $T_i = 110^\circ\text{C}$

2) at  $T_j = 25^\circ\text{C}$

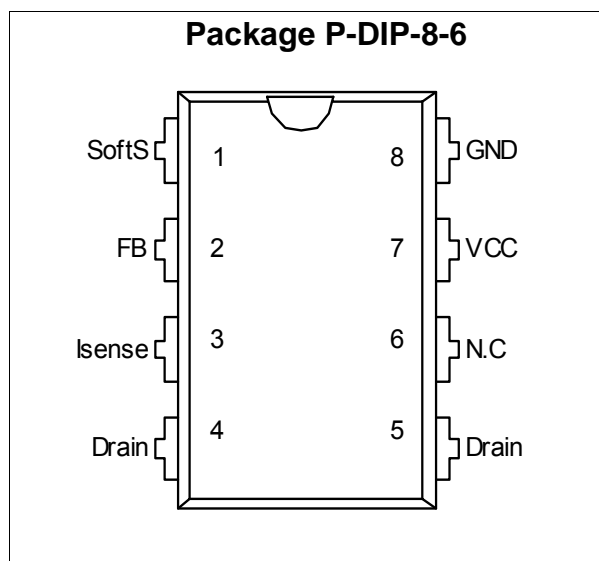


Figure 1 Pin Configuration (top view)

## 1.2 Pin Configuration with P-DIP-7-1

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	Isense	Controller Current Sense Input, CoolMOS™ Source Output
4	N.C.	Not connected
5	Drain	650V <sup>1)</sup> /800V <sup>2)</sup> CoolMOS™ Drain
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

1) at  $T_i = 110^\circ\text{C}$

2) at  $T_j = 25^\circ\text{C}$

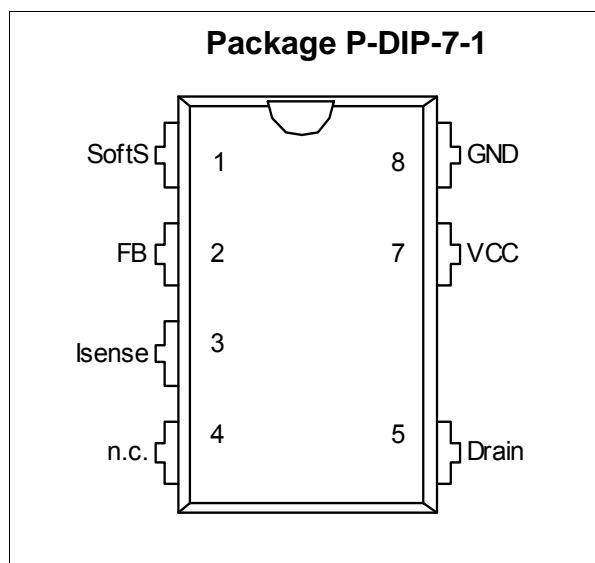


Figure 2 Pin Configuration (top view)

## Pin Configuration and Functionality

### 1.3 Pin Configuration with P-TO220-6-3

Pin	Symbol	Function
1	Drain	650V <sup>1)</sup> CoolMOS™ Drain
3	Isense	650V <sup>1)</sup> CoolMOS™ Source
4	GND	Controller Ground
5	VCC	Controller Supply Voltage
6	SoftS	Soft-Start
7	FB	Feedback

<sup>1)</sup> at  $T_j = 110^\circ\text{C}$

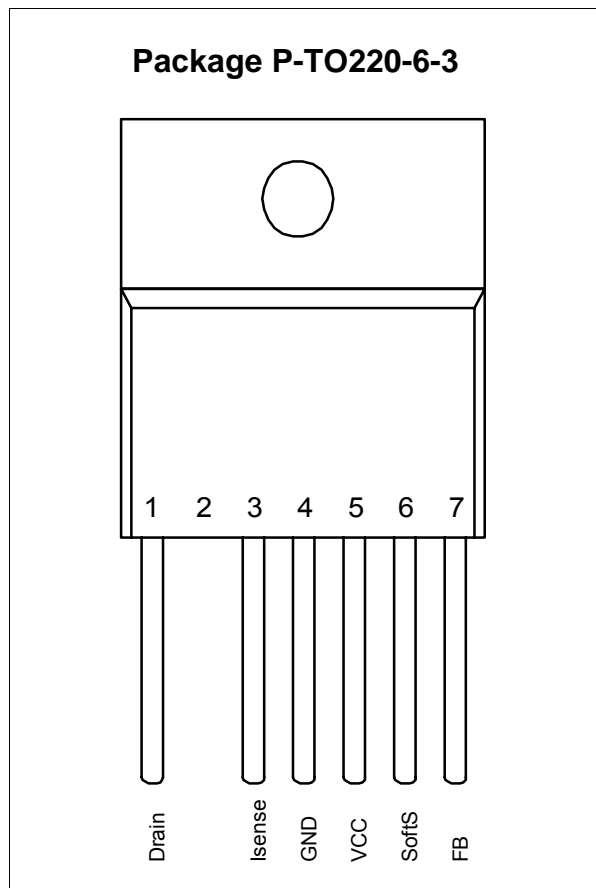


Figure 3 Pin Configuration (top view)

### 1.4 Pin Functionality

#### SoftS (Soft Start & Auto Restart Control)

This pin combines the function of Soft Start in case of Start Up and Auto Restart Mode and the controlling of the Auto Restart Mode in case of an error detection.

#### FB (Feedback)

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle.

#### Isense (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the integrated CoolMOS™. When Isense reaches the internal threshold of the Current Limit Comparator, the Driver output is disabled. By this means the Over Current Detection is realized.

Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.

#### Drain (Drain of integrated CoolMOS™)

Pin Drain is the connection to the Drain of the internal CoolMOS™.

#### VCC (Power supply)

This pin is the positive supply of the IC. The operating range is between 8.5V and 21V.

To provide overvoltage protection the driver gets disabled when the voltage becomes higher than 16.5V during Start Up Phase.

#### GND (Ground)

This pin is the ground of the primary side of the SMPS.

Representative Blockdiagram

## 2 Representative Blockdiagram

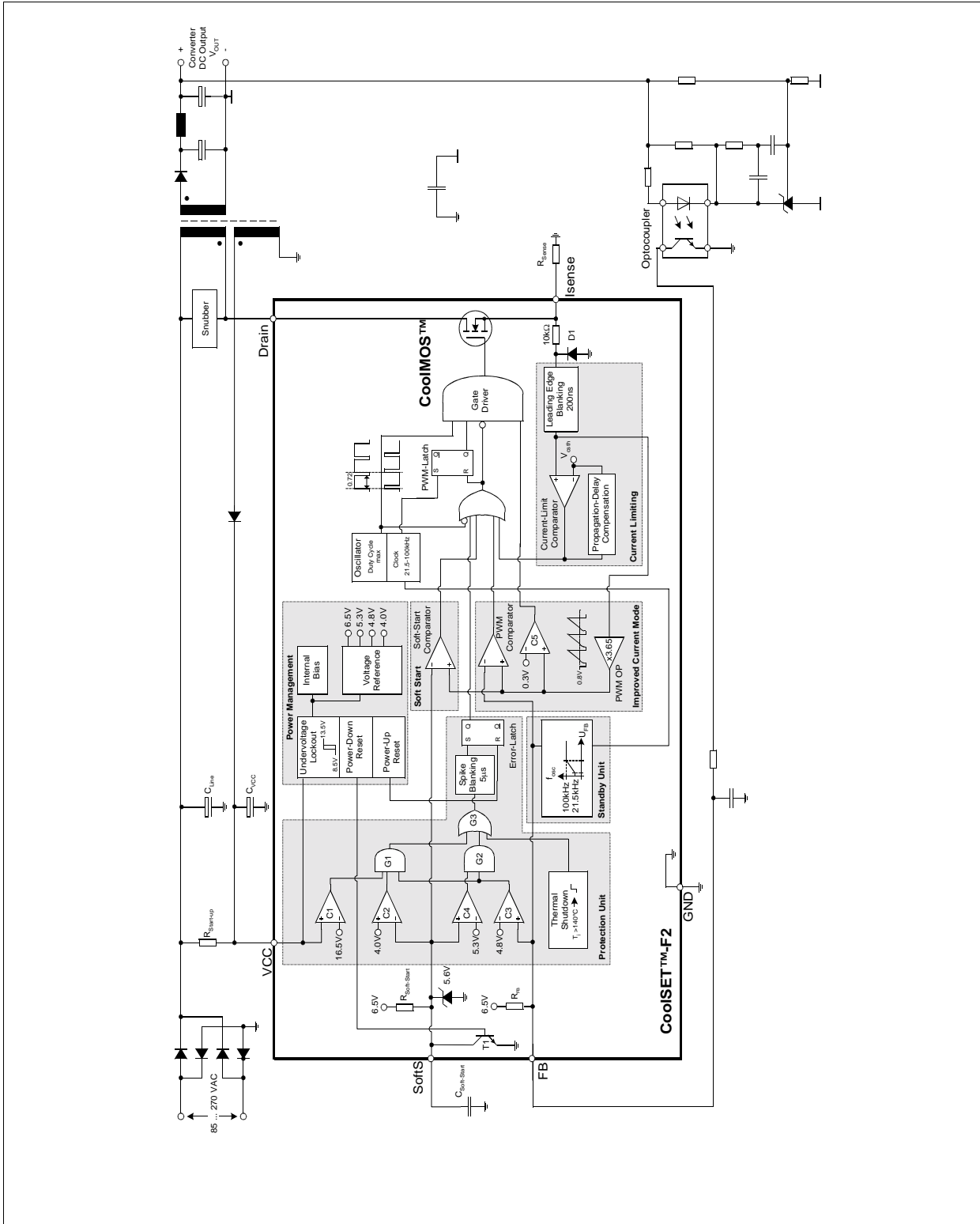


Figure 4 Representative Blockdiagram



Functional Description

### 3 Functional Description

#### 3.1 Power Management

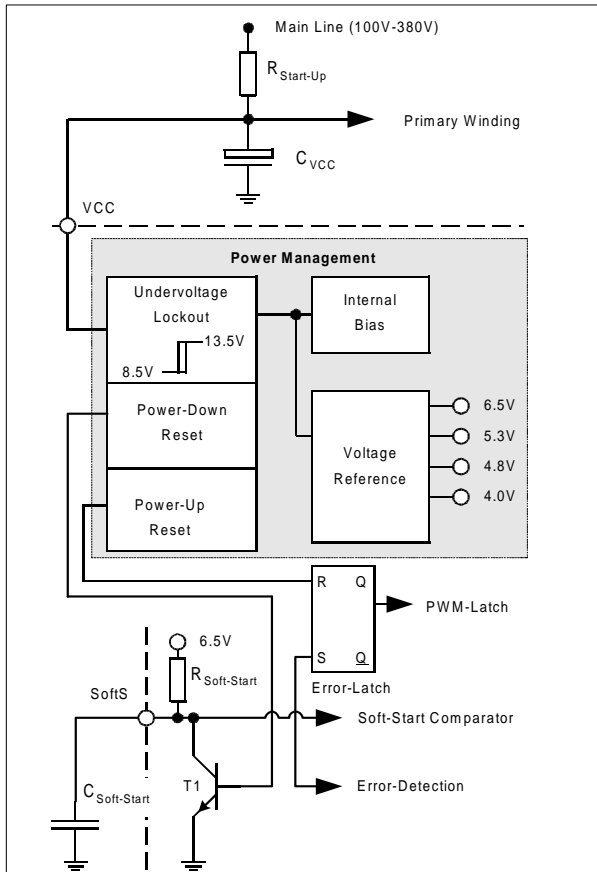


Figure 5 Power Management

The Undervoltage Lockout monitors the external supply voltage  $V_{VCC}$ . In case the IC is inactive the current consumption is max.  $55\mu A$ . When the SMPS is plugged to the main line the current through  $R_{Start-Up}$  charges the external Capacitor  $C_{VCC}$ . When  $V_{VCC}$  exceeds the on-threshold  $V_{CCon}=13.5V$  the internal bias circuit and the voltage reference are switched on. After it the internal bandgap generates a reference voltage  $V_{REF}=6.5V$  to supply the internal circuits. To avoid uncontrolled ringing at switch-on a hysteresis is implemented which means that switch-off is only after active mode when  $V_{CC}$  falls below  $8.5V$ .

In case of switch-on a Power Up Reset is done by resetting the internal error-latch in the protection unit.

When  $V_{VCC}$  falls below the off-threshold  $V_{CCoff}=8.5V$  the internal reference is switched off and the Power Down reset let T1 discharging the soft-start capacitor  $C_{Soft-Start}$  at pin SoftS. Thus it is ensured that at every switch-on the voltage ramp at pin SoftS starts at zero.

#### 3.2 Improved Current Mode

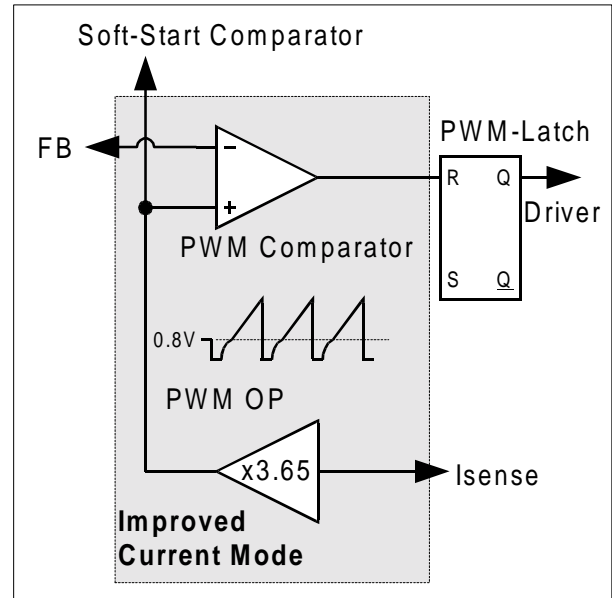


Figure 6 Current Mode

Current Mode means that the duty cycle is controlled by the slope of the primary current. This is done by comparison the FB signal with the amplified current sense signal.

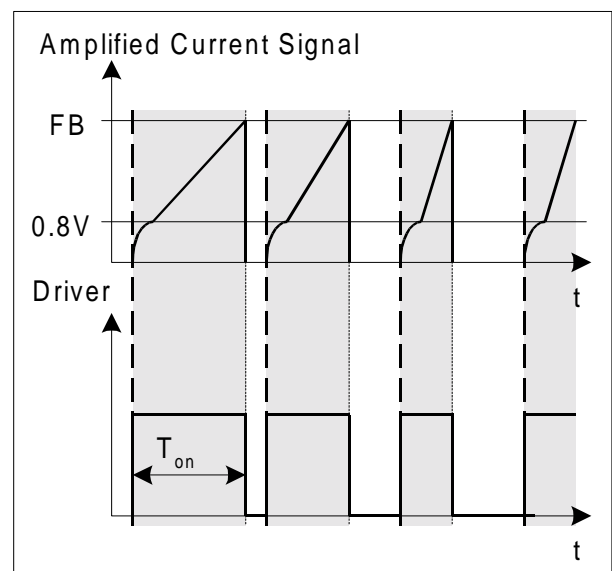


Figure 7 Pulse Width Modulation

In case the amplified current sense signal exceeds the FB signal the on-time  $T_{on}$  of the driver is finished by resetting the PWM-Latch (see Figure 5).

The primary current is sensed by the external series resistor  $R_{Sense}$  inserted in the source of the integrated CoolMOS™. By means of Current Mode the regulation of the secondary voltage is insensitive on line variations. Line variation causes variation of the increasing current slope which controls the duty cycle. The external  $R_{Sense}$  allows an individual adjustment of the maximum source current of the integrated CoolMOS™.

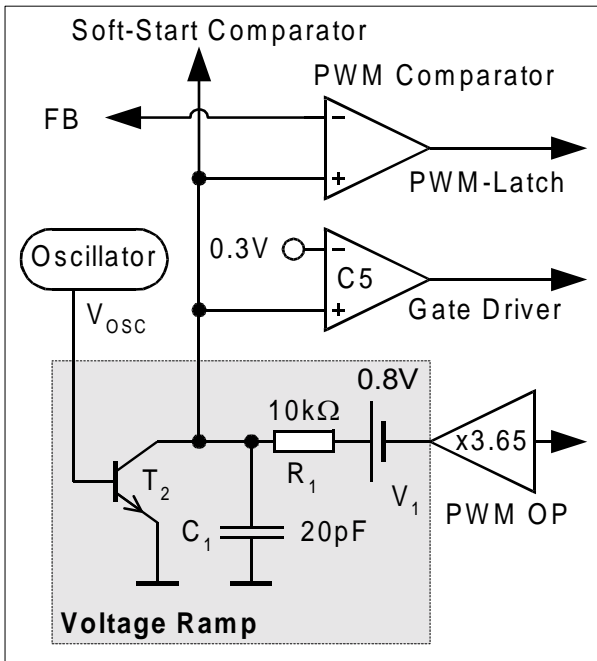


Figure 8 Improved Current Mode

To improve the Current Mode during light load conditions the amplified current ramp of the PWM-OP is superimposed on a voltage ramp, which is built by the switch  $T_2$ , the voltage source  $V_1$  and the 1st order low pass filter composed of  $R_1$  and  $C_1$  (see Figure 6, Figure 7). Every time the oscillator shuts down for max. duty cycle limitation the switch  $T_2$  is closed by  $V_{OSC}$ . When the oscillator triggers the Gate Driver  $T_2$  is opened so that the voltage ramp can start.

In case of light load the amplified current ramp is too small to ensure a stable regulation. In that case the Voltage Ramp is a well defined signal for the comparison with the FB-signal. The duty cycle is then controlled by the slope of the Voltage Ramp.

By means of the C5 Comparator the Gate Driver is switched-off until the voltage ramp exceeds 0.3V. It allows the duty cycle to be reduced continuously till 0% by decreasing  $V_{FB}$  below that threshold.

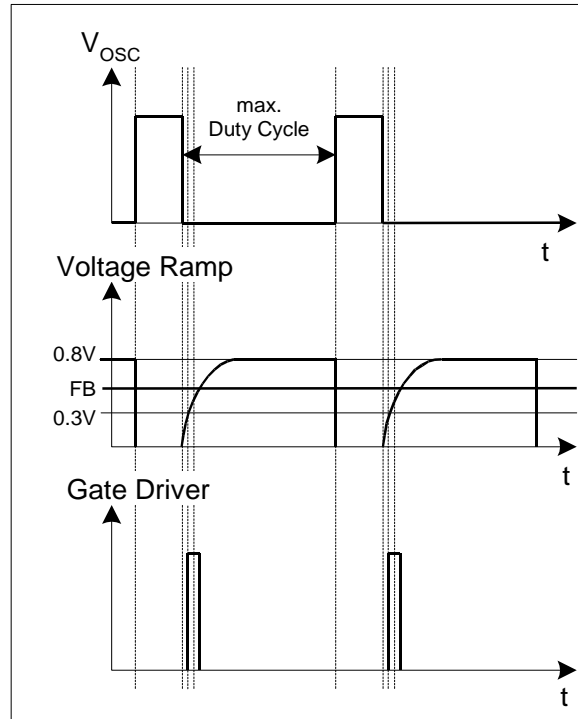


Figure 9 Light Load Conditions

### 3.2.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor  $R_{Sense}$  connected to pin ISense.  $R_{Sense}$  converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.65 by PWM OP. The output of the PWM-OP is connected to the voltage source  $V_1$ . The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM-Comparator, C5 and the Soft-Start-Comparator.

### 3.2.2 PWM-Comparator

The PWM-Comparator compares the sensed current signal of the integrated CoolMOS™ with the feedback signal  $V_{FB}$  (see Figure 8).  $V_{FB}$  is created by an external optocoupler or external transistor in combination with the internal pullup resistor  $R_{FB}$  and provides the load information of the feedback circuitry. When the amplified current signal of the integrated CoolMOS™ exceeds the signal  $V_{FB}$  the PWM-Comparator switches off the Gate Driver.

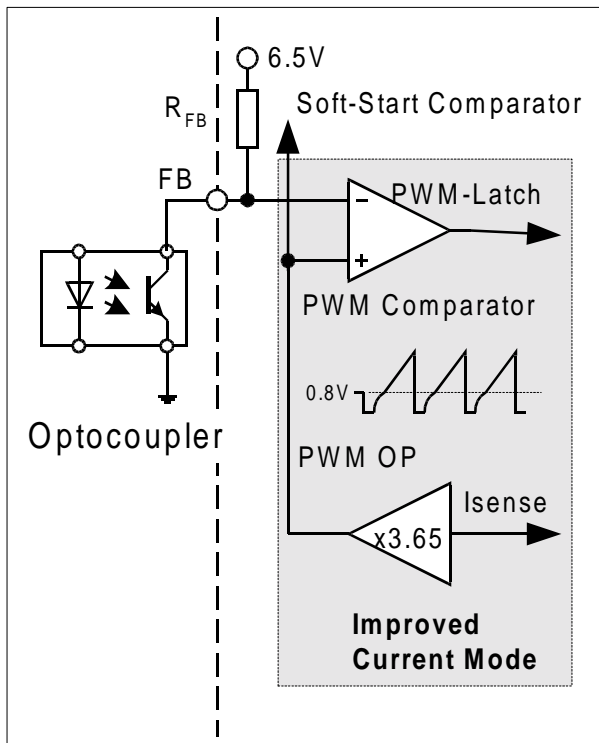


Figure 10 PWM Controlling

### 3.3 Soft-Start

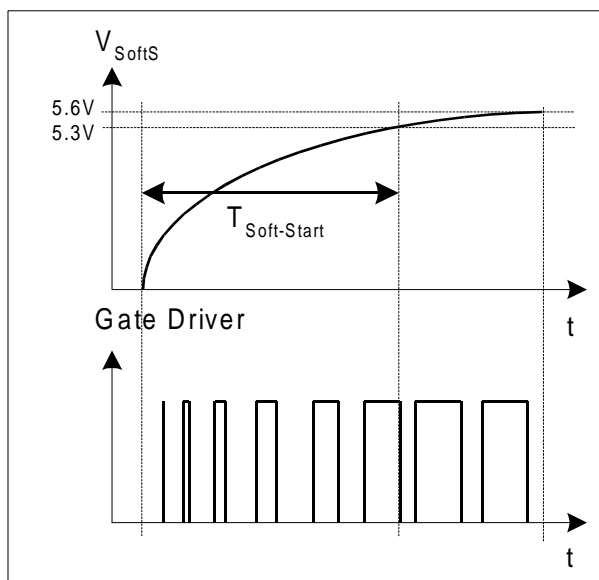


Figure 11 Soft-Start Phase

The Soft-Start is realized by the internal pullup resistor  $R_{Soft-Start}$  and the external Capacitor  $C_{Soft-Start}$  (see Figure 2). The Soft-Start voltage  $V_{SoftS}$  is generated by charging the external capacitor  $C_{Soft-Start}$  by the internal

pullup resistor  $R_{Soft-Start}$ . The Soft-Start-Comparator compares the voltage at pin SoftS at the negative input with the ramp signal of the PWM-OP at the positive input. When Soft-Start voltage  $V_{SoftS}$  is less than Feedback voltage  $V_{FB}$  the Soft-Start-Comparator limits the pulse width by resetting the PWM-Latch (see Figure 9). In addition to Start-Up, Soft-Start is also activated at each restart attempt during Auto Restart. By means of the above mentioned  $C_{Soft-Start}$  the Soft-Start can be defined by the user. The Soft-Start is finished when  $V_{SoftS}$  exceeds 5.3V. At that time the Protection Unit is activated by Comparator C4 and senses the FB by Comparator C3 whether the voltage is below 4.8V which means that the voltage on the secondary side of the SMPS is settled. The internal Zener Diode at SoftS with breakthrough voltage of 5.6V is to prevent the internal circuit from saturation (see Figure 10).

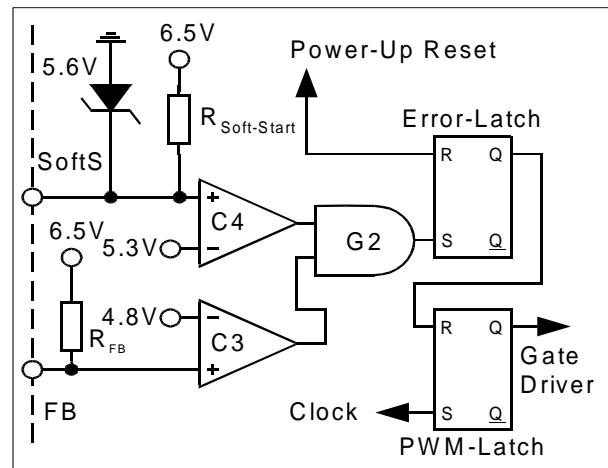


Figure 12 Activation of Protection Unit

The Start-Up time  $T_{Start-Up}$  within the converter output voltage  $V_{OUT}$  is settled must be shorter than the Soft-Start Phase  $T_{Soft-Start}$  (see Figure 11).

$$C_{Soft-Start} = \frac{T_{Soft-Start}}{R_{Soft-Start} \times 1,69}$$

By means of Soft-Start there is an effective minimization of current and voltage stresses on the integrated CoolMOS™, the clamp circuit and the output overshoot and prevents saturation of the transformer during Start-Up.

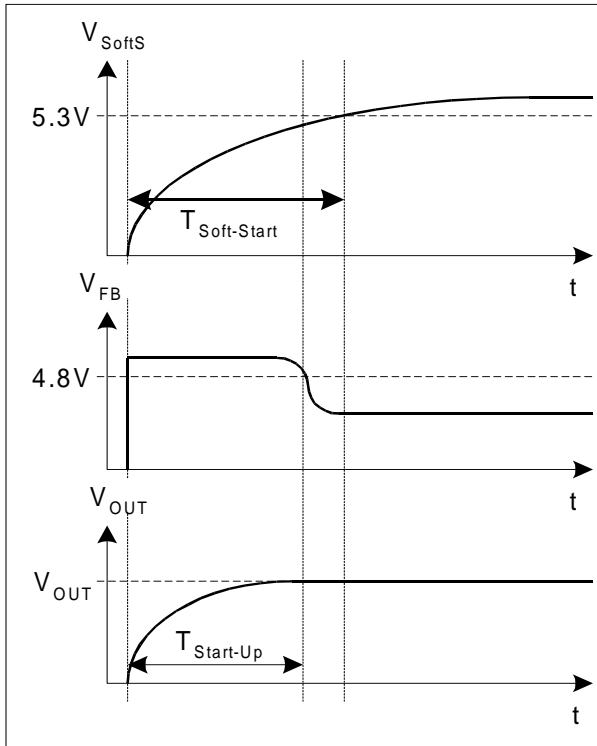


Figure 13 Start Up Phase

### 3.4 Oscillator and Frequency Reduction

#### 3.4.1 Oscillator

The oscillator generates a frequency  $f_{\text{switch}} = 67\text{kHz}/100\text{kHz}$ . A resistor, a capacitor and a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a max. duty cycle limitation of  $D_{\text{max}}=0.72$ .

#### 3.4.2 Frequency Reduction

The frequency of the oscillator is depending on the voltage at pin FB. The dependence is shown in Figure 12. This feature allows a power supply to operate at lower frequency at light loads thus lowering the switching losses while maintaining good cross regulation performance and low output ripple. In case of low power the power consumption of the whole SMPS can now be reduced very effectively. The minimal reachable frequency is limited to 20kHz/21.5 kHz to avoid audible noise in any case.

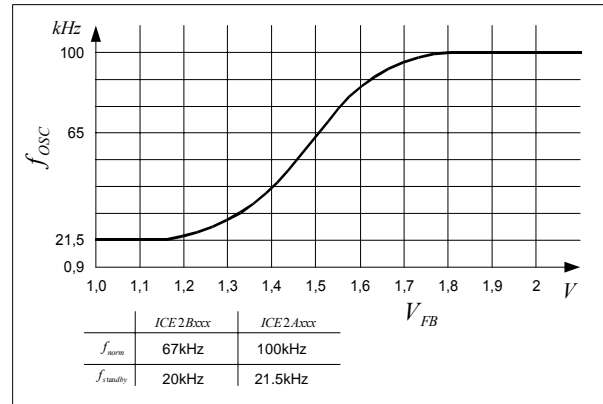


Figure 14 Frequency Dependence

### 3.5 Current Limiting

There is a cycle by cycle current limiting realised by the Current-Limit Comparator to provide an overcurrent detection. The source current of the integrated CoolMOS™ is sensed via an external sense resistor  $R_{\text{Sense}}$ . By means of  $R_{\text{Sense}}$  the source current is transformed to a sense voltage  $V_{\text{Sense}}$ . When the voltage  $V_{\text{Sense}}$  exceeds the internal threshold voltage  $V_{\text{csth}}$  the Current-Limit-Comparator immediately turns off the gate drive. To prevent the Current Limiting from distortions caused by leading edge spikes a Leading Edge Blanking is integrated at the Current Sense. Furthermore a Propagation Delay Compensation is added to support the immediate shut down of the CoolMOS™ in case of overcurrent.

#### 3.5.1 Leading Edge Blanking

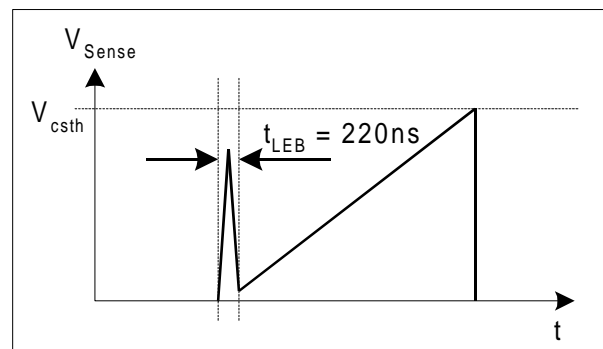


Figure 15 Leading Edge Blanking

Each time when CoolMOS™ is switched on a leading spike is generated due to the primary-side capacitances and secondary-side rectifier reverse recovery time. To avoid a premature termination of the switching pulse this spike is blanked out with a time constant of  $t_{\text{LEB}} = 220\text{ns}$ . During that time the output of

the Current-Limit Comparator cannot switch off the gate drive.

### 3.5.2 Propagation Delay Compensation

In case of overcurrent detection by  $I_{Limit}$  the shut down of CoolMOS™ is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current  $I_{peak}$  which depends on the ratio of  $dI/dt$  of the peak current (see Figure 14).

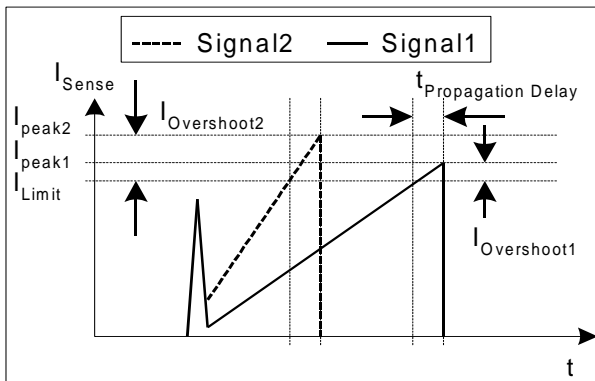


Figure 16 Current Limiting

The overshoot of Signal2 is bigger than of Signal1 due to the steeper rising waveform.

A propagation delay compensation is integrated to bound the overshoot dependent on  $dI/dt$  of the rising primary current. That means the propagation delay time between exceeding the current sense threshold  $V_{csth}$  and the switch off of CoolMOS™ is compensated over temperature within a range of at least.

$$0 \leq R_{Sense} \times \frac{dI_{peak}}{dt} \leq 1 \frac{dV_{Sense}}{dt}$$

So current limiting is now capable in a very accurate way (see Figure 16).

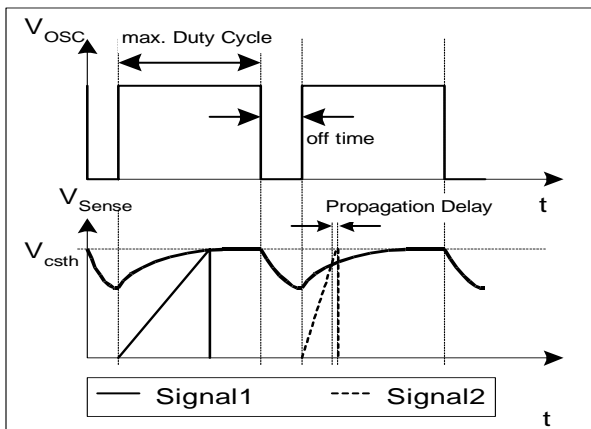


Figure 17 Dynamic Voltage Threshold  $V_{csth}$

The propagation delay compensation is done by means of a dynamic threshold voltage  $V_{csth}$  (see Figure 15). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

E.g.  $I_{peak} = 0.5A$  with  $R_{Sense} = 2$ . Without propagation delay compensation the current sense threshold is set to a static voltage level  $V_{csth} = 1V$ . A current ramp of  $dI/dt = 0.4A/\mu s$ , that means  $dV_{Sense}/dt = 0.8V/\mu s$ , and a propagation delay time of i.e.  $t_{Propagation Delay} = 180ns$  leads then to a  $I_{peak}$  overshoot of 12%. By means of propagation delay compensation the overshoot is only about 2% (see Figure 16).

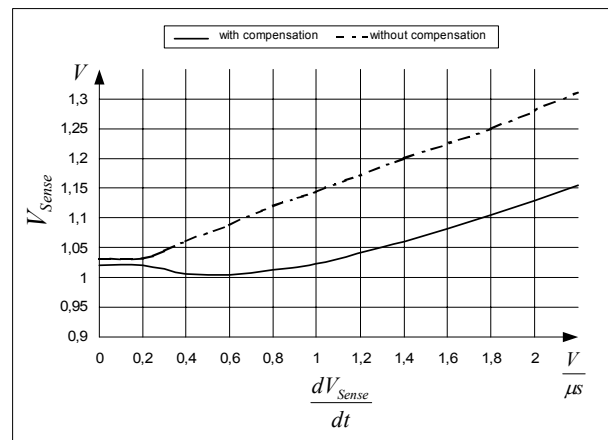


Figure 18 Overcurrent Shutdown

### 3.6 PWM-Latch

The oscillator clock output applies a set pulse to the PWM-Latch when initiating CoolMOS™ conduction. After setting the PWM-Latch can be reset by the PWM-OP, the Soft-Start-Comparator, the Current-Limit-Comparator, Comparator C3 or the Error-Latch of the Protection Unit. In case of resetting the driver is shut down immediately.

### 3.7 Driver

The driver-stage drives the gate of the CoolMOS™ and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the CoolMOS™ threshold. This is achieved by a slope control of the rising edge at the driver's output (see Figure 17).

Thus the leading switch on spike is minimized. When CoolMOS™ is switched off, the falling shape of the driver is slowed down when reaching 2V to prevent an overshoot below ground. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage. At voltages below the undervoltage lockout threshold  $V_{VCCoff}$  the gate drive is active low.

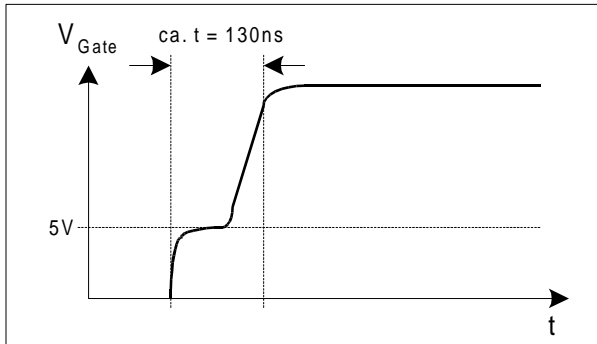


Figure 19 Gate Rising Slope

### 3.8 Protection Unit (Auto Restart Mode)

An overload, open loop and overvoltage detection is integrated within the Protection Unit. These three failure modes are latched by an Error-Latch. Additional thermal shutdown is latched by the Error-Latch. In case of those failure modes the Error-Latch is set after a blanking time of 5µs and the CoolMOS™ is shut down. That blanking prevents the Error-Latch from distortions caused by spikes during operation mode.

#### 3.8.1 Overload & Open loop with normal load

Figure 18 shows the Auto Restart Mode in case of overload or open loop with normal load. The detection of open loop or overload is provided by the Comparator C3, C4 and the AND-gate G2 (see Figure19). The detection is activated by C4 when the voltage at pin SoftS exceeds 5.3V. Till this time the IC operates in the Soft-Start Phase. After this phase the comparator C3 can set the Error-Latch in case of open loop or overload which leads the feedback voltage  $V_{FB}$  to exceed the threshold of 4.8V. After latching VCC decreases till 8.5V and inactivates the IC. At this time the external Soft-Start capacitor is discharged by the internal transistor T1 due to Power Down Reset. When the IC is inactive  $V_{VCC}$  increases till  $V_{CCon} = 13.5V$  by charging the Capacitor  $C_{VCC}$  by means of the Start-Up Resistor  $R_{Start-Up}$ . Then the Error-Latch is reset by Power Up Reset and the external Soft-Start capacitor  $C_{Soft-Start}$  is charged by the internal pullup resistor  $R_{Soft-Start}$ . During the Soft-Start Phase which ends when the voltage at pin SoftS exceeds 5.3V the detection of overload and open loop by C3 and G2 is inactive. In this way the Start Up Phase is not detected as an overload.

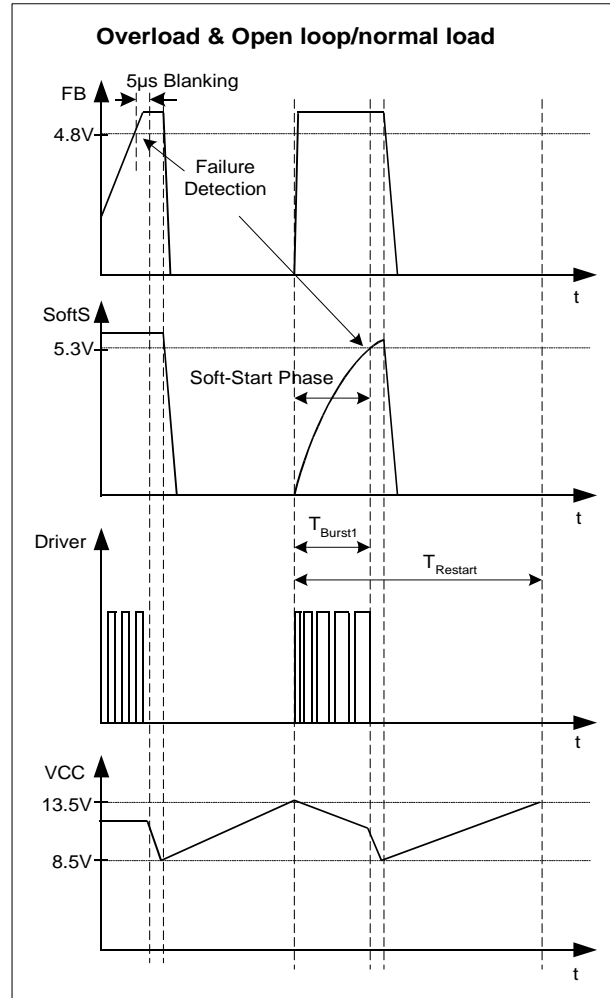


Figure 20 Auto Restart Mode

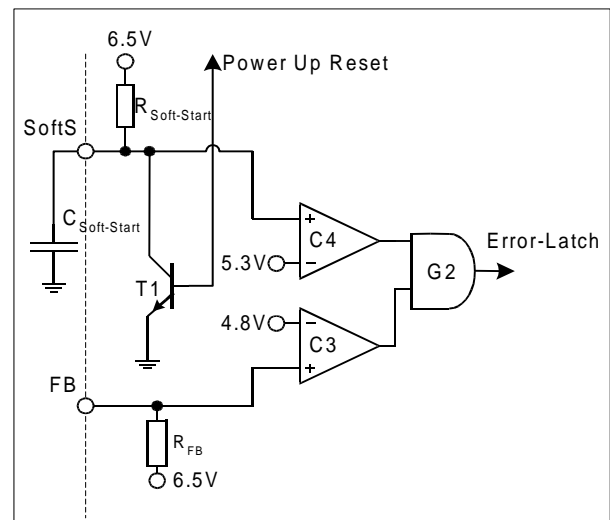


Figure 21 FB-Detection

But the Soft-Start Phase must be finished within the Start Up Phase to force the voltage at pin FB below the failure detection threshold of 4.8V.

### 3.8.2 Overvoltage due to open loop with no load

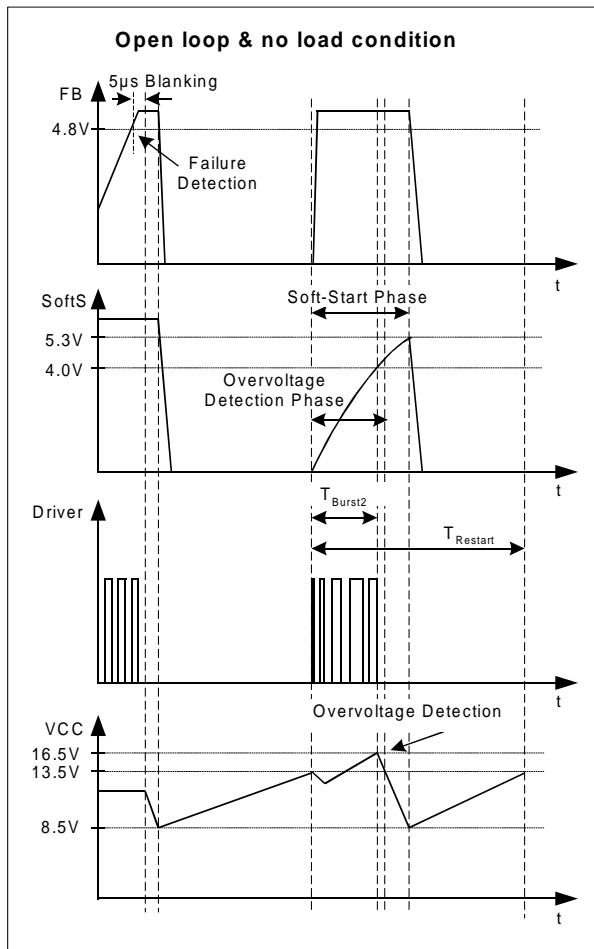


Figure 22 Auto Restart Mode

Figure 20 shows the Auto Restart Mode for open loop and no load condition. In case of this failure mode the converter output voltage increases and also VCC. An additional protection by the comparators C1, C2 and the AND-gate G1 is implemented to consider this failure mode (see Figure 21). The overvoltage detection is provided by Comparator C1 only in the first time during the Soft-Start Phase till the Soft-Start voltage exceeds the threshold of the Comparator C2 at 4.0V and the voltage at pin FB is above 4.8V. When VCC exceeds 16.5V during the overvoltage detection phase C1 can set the Error-Latch and the Burst Phase during Auto Restart Mode is finished earlier. In that case  $T_{Burst2}$  is shorter than  $T_{Soft-Start}$ . By means of C2 the

normal operation mode is prevented from overvoltage detection due to varying of VCC concerning the regulation of the converter output. When the voltage  $V_{SoftS}$  is above 4.0V the overvoltage detection by C1 is deactivated.

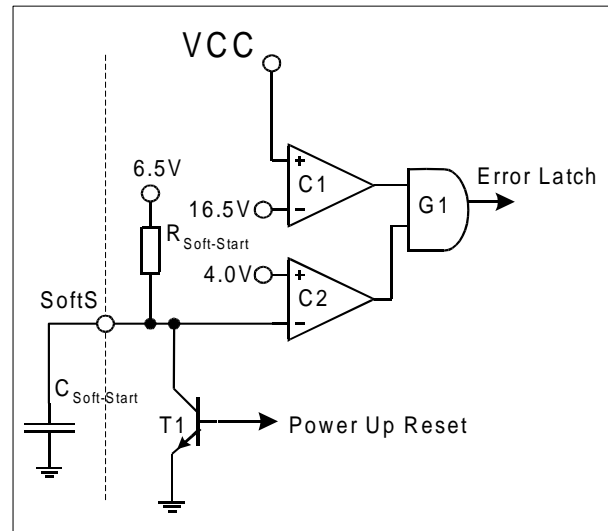


Figure 23 Overvoltage Detection

### 3.8.3 Thermal Shut Down

Thermal Shut Down is latched by the Error-Latch when junction temperature  $T_j$  of the pwm controller is exceeding an internal threshold of 140°C. In that case the IC switches in Auto Restart Mode.

*Note: All the values which are mentioned in the functional description are typical. Please refer to Electrical Characteristics for min/max limit values.*



**Electrical Characteristics**

## 4 Electrical Characteristics

### 4.1 Absolute Maximum Ratings

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 6 (VCC) is discharged before assembling the application circuit.*

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Drain Source Voltage ICE2A0565/165/265/365/765P ICE2B0565/165/265/365/765P	$V_{DS}$	-	650	V	$T_j=110^{\circ}\text{C}$
Drain Source Voltage ICE2A180Z/280Z	$V_{DS}$	-	800	V	$T_j=25^{\circ}\text{C}$
Avalanche energy, repetitive $t_{AR}$ limited by max. $T_j=150^{\circ}\text{C}$ <sup>1)</sup>	ICE2A0565	$E_{AR1}$	-	0.01	mJ
	ICE2A165	$E_{AR2}$	-	0.07	mJ
	ICE2A265	$E_{AR3}$	-	0.40	mJ
	ICE2A365	$E_{AR4}$	-	0.50	mJ
	ICE2B0565	$E_{AR5}$	-	0.01	mJ
	ICE2B165	$E_{AR6}$	-	0.07	mJ
	ICE2B265	$E_{AR7}$	-	0.40	mJ
	ICE2B365	$E_{AR8}$	-	0.50	mJ
	ICE2A180Z	$E_{AR9}$	-	0.07	mJ
	ICE2A280Z	$E_{AR10}$	-	0.40	mJ
	ICE2A765P	$E_{AR11}$	-	0.50	mJ
	ICE2B765P	$E_{AR12}$	-	0.50	mJ

<sup>1)</sup> Repetitive avalanche causes additional power losses that can be calculated as  $PAV=E_{AR} \cdot f$



**Electrical Characteristics**

Parameter	Symbol	Limit Values		Unit	Remarks	
		min.	max.			
Avalanche current, repetitive tAR limited by max. Tj=150°C1)	ICE2A0565	I <sub>AR1</sub>	-	0.5	A	
	ICE2A165	I <sub>AR2</sub>	-	1	A	
	ICE2A265	I <sub>AR3</sub>	-	2	A	
	ICE2A365	I <sub>AR4</sub>	-	3	A	
	ICE2B0565	I <sub>AR5</sub>	-	0.5	A	
	ICE2B165	I <sub>AR6</sub>	-	1	A	
	ICE2B265	I <sub>AR7</sub>	-	2	A	
	ICE2B365	I <sub>AR8</sub>	-	3	A	
	ICE2A180Z	I <sub>AR9</sub>	-	1	A	
	ICE2A280Z	I <sub>AR10</sub>	-	2	A	
	ICE2A765P	I <sub>AR11</sub>	-	7	A	
	ICE2B765P	I <sub>AR12</sub>	-	7	A	
V <sub>CC</sub> Supply Voltage	V <sub>CC</sub>	-0.3	22	V		
FB Voltage	V <sub>FB</sub>	-0.3	6.5	V		
SoftS Voltage	V <sub>SoftS</sub>	-0.3	6.5	V		
I <sub>Sense</sub>	I <sub>Sense</sub>	-0.3	3	V		
Junction Temperature	T <sub>j</sub>	-40	150	°C	Controller & CoolMOS™	
Storage Temperature	T <sub>s</sub>	-50	150	°C		
Thermal Resistance Junction-Ambient	R <sub>thJA1</sub>	-	90	K/W	P-DIP-8-6	
	R <sub>thJA2</sub>	-	96	K/W	P-DIP-7-1	
ESD Capability <sup>1)</sup>	V <sub>ESD</sub>	-	2 <sup>2)</sup>	kV	Human Body Model	

<sup>1)</sup> Equivalent to discharging a 100pF capacitor through a 1.5 kΩ series resistor

<sup>2)</sup> 1kV at pin drain of ICE2x0565

**4.2 Thermal Impedance (ICE2A765P and ICE2B765P)**

Parameter	Symbol	Limit Values		Unit	Remarks	
		min.	max.			
Thermal Resistance Junction-Ambient	ICE2A765P ICE2B765P	R <sub>thJA3</sub>	-	74	K/W	Free standing with no heat-sink
Junction-Case	ICE2A765P ICE2B765P	R <sub>thJC</sub>	-	2.5	k/W	

## Electrical Characteristics

### 4.3 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V <sub>CC</sub> Supply Voltage	V <sub>CC</sub>	V <sub>CCoff</sub>	21	V	
Junction Temperature of Controller	T <sub>JCon</sub>	-25	130	°C	Limited due to thermal shut down of controller
Junction Temperature of CoolMOS™	T <sub>JCoolMOS</sub>	-25	150	°C	

### 4.4 Characteristics

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T<sub>J</sub> from –25 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V<sub>CC</sub> = 15 V is assumed.

#### 4.4.1 Supply Section

Parameter	Symbol	Limit Values			Unit	Test Condition	
		min.	typ.	max.			
Start Up Current	I <sub>VCC1</sub>	-	27	55	µA	V <sub>CC</sub> =V <sub>CCon</sub> -0.1V	
Supply Current with Inactiv Gate	I <sub>VCC2</sub>	-	5.0	6.6	mA	V <sub>SoftS</sub> = 0 I <sub>FB</sub> = 0	
Supply Current with Activ Gate	ICE2A0565	I <sub>VCC3</sub>	-	5.3	6.7	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2A165	I <sub>VCC4</sub>	-	6.5	7.8	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2A265	I <sub>VCC5</sub>	-	6.7	8.0	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2A365	I <sub>VCC6</sub>	-	8.5	9.8	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2B0565	I <sub>VCC7</sub>	-	5.2	6.7	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2B165	I <sub>VCC8</sub>	-	5.5	7.0	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2B265	I <sub>VCC9</sub>	-	6.1	7.3	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2B365	I <sub>VCC10</sub>	-	7.1	8.3	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2A180Z	I <sub>VCC11</sub>	-	6.5	7.8	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0
	ICE2A280Z	I <sub>VCC12</sub>	-	7.7	9.0	mA	V <sub>SoftS</sub> = 5V I <sub>FB</sub> = 0

**Electrical Characteristics**

Parameter	Symbol	Limit Values			Unit	Test Condition	
		min.	typ.	max.			
Supply Current with Activ Gate	ICE2A765P	$I_{VCC13}$	-	8.5	9.8	mA	$V_{SoftS} = 5V$ $I_{FB} = 0$
	ICE2B765P	$I_{VCC14}$	-	7.1	8.3	mA	$V_{SoftS} = 5V$ $I_{FB} = 0$
VCC Turn-On Threshold	VCCOn	13	13.5	14	V		
VCC Turn-Off Threshold	VCCOff	-	8.5	-	V		
VCC Turn-On/Off Hysteresis	VCCHY	4.5	5	5.5	V		

**4.4.2 Internal Voltage Reference**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	$V_{REF}$	6.37	6.50	6.63	V	measured at pin FB

**4.4.3 Control Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Oscillator Frequency ICE2A0565/165/265/365/765P ICE2A180Z/280Z	$f_{OSC1}$	93	100	107	kHz	$V_{FB} = 4V$
Oscillator Frequency ICE2B0565/165/265/365/765P	$f_{OSC3}$	62	67	72	kHz	$V_{FB} = 4V$
Reduced Osc. Frequency ICE2A0565/165/265/365/765P ICE2A180Z/280Z	$f_{OSC2}$	-	21.5	-	kHz	$V_{FB} = 1V$
Reduced Osc. Frequency ICE2B0565/165/265/365/765P	$f_{OSC4}$	-	20	-	kHz	$V_{FB} = 1V$
Frequency Ratio $f_{osc1}/f_{osc2}$ ICE2A0565/165/265/365/765P ICE2A180Z/280Z		4.5	4.65	4.9		
Frequency Ratio $f_{osc3}/f_{osc4}$ ICE2B0565/165/265/365/765P		3.18	3.35	3.53		
Max Duty Cycle	$D_{max}$	0.67	0.72	0.77		
Min Duty Cycle	$D_{min}$	0	-	-		$V_{FB} < 0.3V$
PWM-OP Gain	$A_V$	3.45	3.65	3.85		
$V_{FB}$ Operating Range Min Level	$V_{FBmin}$	0.3	-	-	V	
$V_{FB}$ Operating Range Max level	$V_{FBmax}$	-	-	4.6	V	
Feedback Resistance	$R_{FB}$	3.0	3.7	4.9	k $\Omega$	
Soft-Start Resistance	$R_{Soft-Start}$	42	50	62	k $\Omega$	

**Electrical Characteristics**
**4.4.4 Protection Unit**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Over Load & Open Loop Detection Limit	$V_{FB2}$	4.65	4.8	4.95	V	$V_{SoftS} > 5.5V$
Activation Limit of Overload & Open Loop Detection	$V_{SoftS1}$	5.15	5.3	5.46	V	$V_{FB} > 5V$
Deactivation Limit of Overvoltage Detection	$V_{SoftS2}$	3.88	4.0	4.12	V	$V_{FB} > 5V$ $V_{CC} > 17.5V$
Overvoltage Detection Limit	$V_{VCC1}$	16	16.5	17.2	V	$V_{SoftS} < 3.8V$ $V_{FB} > 5V$
Latched Thermal Shutdown	$T_{jSD}$	130	140	150	°C	guaranteed by design
Spike Blanking	$t_{Spike}$	-	5	-	µs	

**4.4.5 Current Limiting**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay Time)	$V_{csth}$	0.95	1.0	1.05	V	$dV_{sense} / dt = 0.6V/\mu s$
Leading Edge Blanking	$t_{LEB}$	-	220	-	ns	

**Electrical Characteristics**
**4.4.6 CoolMOS™ Section**

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Drain Source Breakdown Voltage ICE2A0565/165/265/365/765P ICE2B0565/165/265/365/765P		$V_{(BR)DSS}$	600	-	-	V	$T_j=25^\circ\text{C}$
			650	-	-	V	$T_j=110^\circ\text{C}$
Drain Source Breakdown Voltage ICE2A180Z/280Z		$V_{(BR)DSS}$	800	-	-	V	$T_j=25^\circ\text{C}$
			870	-	-	V	$T_j=110^\circ\text{C}$
Drain Source On-Resistance	ICE2A0565	$R_{DSon1}$	-	4.7	5.5	$\Omega$	$T_j=25^\circ\text{C}$
			-	10.0	12.5	$\Omega$	$T_j=125^\circ\text{C}$
Drain Source On-Resistance	ICE2A165	$R_{DSon2}$	-	3	3.3	$\Omega$	$T_j=25^\circ\text{C}$
			-	6.6	7.3	$\Omega$	$T_j=125^\circ\text{C}$
	ICE2A265	$R_{DSon3}$	-	0.9	1.08	$\Omega$	$T_j=25^\circ\text{C}$
			-	1.9	2.28	$\Omega$	$T_j=125^\circ\text{C}$
	ICE2A365	$R_{DSon4}$	-	0.45	0.54	$\Omega$	$T_j=25^\circ\text{C}$
			-	0.95	1.14	$\Omega$	$T_j=125^\circ\text{C}$
	ICE2B0565	$R_{DSon5}$	-	4.7	5.5	$\Omega$	$T_j=25^\circ\text{C}$
			-	10.0	12.5	$\Omega$	$T_j=125^\circ\text{C}$
	ICE2B165	$R_{DSon6}$	-	3	3.3	$\Omega$	$T_j=25^\circ\text{C}$
			-	6.6	7.3	$\Omega$	$T_j=125^\circ\text{C}$
	ICE2B265	$R_{DSon7}$	-	0.9	1.08	$\Omega$	$T_j=25^\circ\text{C}$
			-	1.9	2.28	$\Omega$	$T_j=125^\circ\text{C}$
ICE2B365	$R_{DSon8}$	-	0.45	0.54	$\Omega$	$T_j=25^\circ\text{C}$	
		-	0.95	1.14	$\Omega$	$T_j=125^\circ\text{C}$	
ICE2A180Z	$R_{DSon9}$	-	3	3.3	$\Omega$	$T_j=25^\circ\text{C}$	
		-	6.6	7.3	$\Omega$	$T_j=125^\circ\text{C}$	
ICE2A280Z	$R_{DSon10}$	-	0.8	1.06	$\Omega$	$T_j=25^\circ\text{C}$	
		-	1.7	2.04	$\Omega$	$T_j=125^\circ\text{C}$	
ICE2A765P	$R_{DSon11}$	-	0.45	0.54	$\Omega$	$T_j=25^\circ\text{C}$	
		-	0.95	1.14	$\Omega$	$T_j=125^\circ\text{C}$	
ICE2B765P	$R_{DSon12}$	-	0.45	0.54	$\Omega$	$T_j=25^\circ\text{C}$	
		-	0.95	1.14	$\Omega$	$T_j=125^\circ\text{C}$	

**Electrical Characteristics**

Parameter		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Effective output capacitance, energy related	ICE2A0565	$C_{o(er)1}$	-	4.751	-	pF	$V_{DS} = 0V$ to 480V
	ICE2A165	$C_{o(er)2}$	-	7	-	pF	$V_{DS} = 0V$ to 480V
	ICE2A265	$C_{o(er)3}$	-	21	-	pF	$V_{DS} = 0V$ to 480V
	ICE2A365	$C_{o(er)4}$	-	30	-	pF	$V_{DS} = 0V$ to 480V
	ICE2B0565	$C_{o(er)5}$	-	4.751	-	pF	$V_{DS} = 0V$ to 480V
	ICE2B165	$C_{o(er)6}$	-	7	-	pF	$V_{DS} = 0V$ to 480V
	ICE2B265	$C_{o(er)7}$	-	21	-	pF	$V_{DS} = 0V$ to 480V
	ICE2B365	$C_{o(er)8}$	-	30	-	pF	$V_{DS} = 0V$ to 480V
	ICE2A180Z	$C_{o(er)9}$	-	7	-	pF	$V_{DS} = 0V$ to 480V
	ICE2A280Z	$C_{o(er)10}$	-	22	-	pF	$V_{DS} = 0V$ to 480V
	ICE2A765P	$C_{o(er)11}$	-	30	-	pF	$V_{DS} = 0V$ to 480V
	ICE2B765P	$C_{o(er)12}$	-	30	-	pF	$V_{DS} = 0V$ to 480V
Zero Gate Voltage Drain Current		$I_{DSS}$	-	0.5	-	$\mu A$	$V_{VCC} = 0V$
Rise Time		$t_{rise}$	-	30 <sup>1)</sup>	-	ns	
Fall Time		$t_{fall}$	-	30 <sup>1)</sup>	-	ns	

<sup>1)</sup> Measured in a Typical Flyback Converter Application

## 5 Typical Performance Characteristics

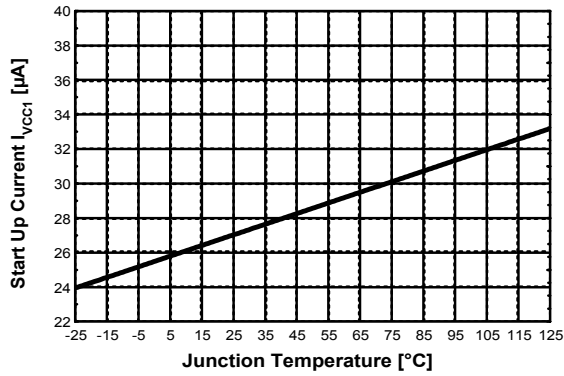


Figure 24 Start Up Current  $I_{VCC1}$  vs.  $T_j$

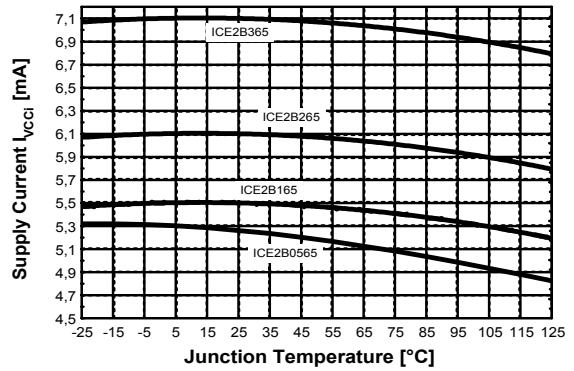


Figure 27 Supply Current  $I_{VCC1}$  vs.  $T_j$

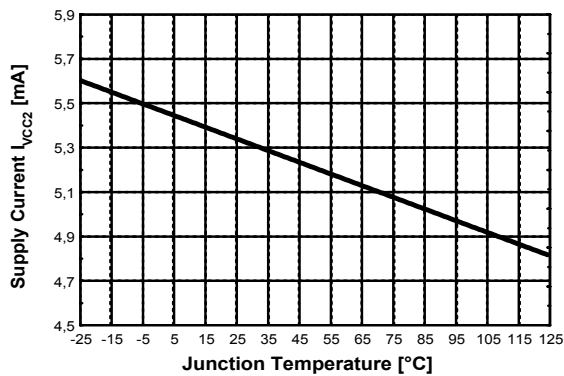


Figure 25 Static Supply Current  $I_{VCC2}$  vs.  $T_j$

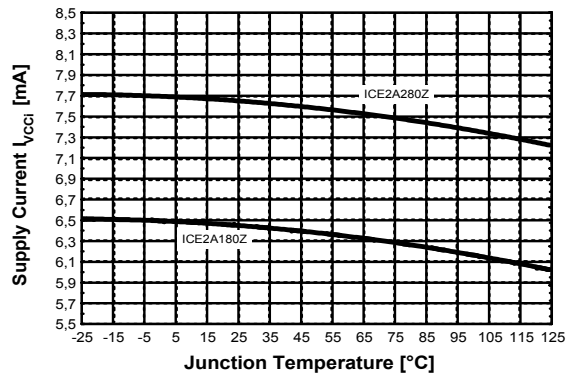


Figure 28 Supply Current  $I_{VCC1}$  vs.  $T_j$

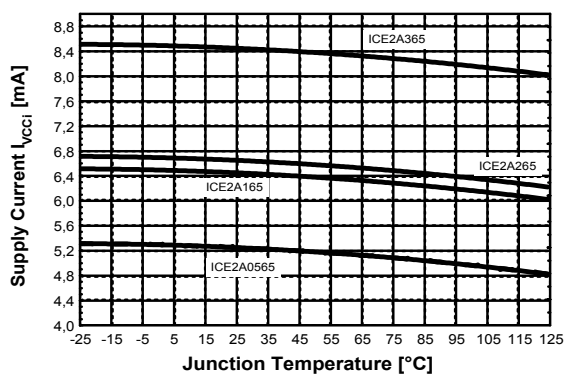


Figure 26 Supply Current  $I_{VCC1}$  vs.  $T_j$

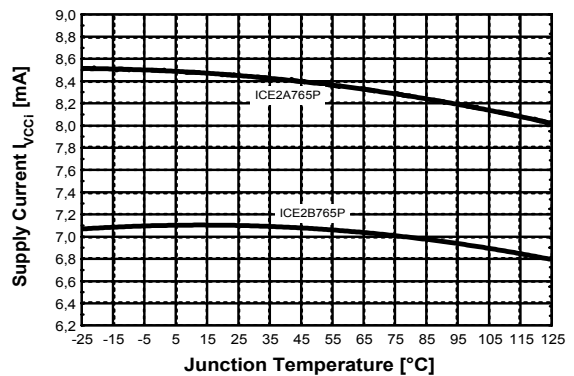


Figure 29 Supply Current  $I_{VCC1}$  vs.  $T_j$

Typical Performance Characteristics

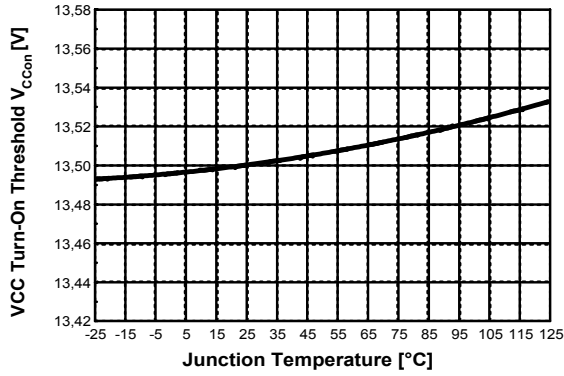


Figure 30 VCC Turn-On Threshold  $V_{VCCon}$  vs.  $T_j$

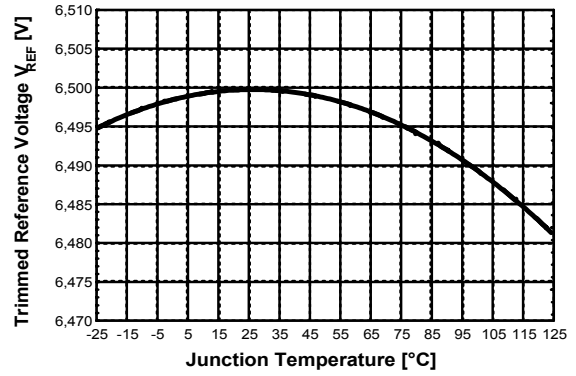


Figure 33 Trimmed Reference  $V_{REF}$  vs.  $T_j$

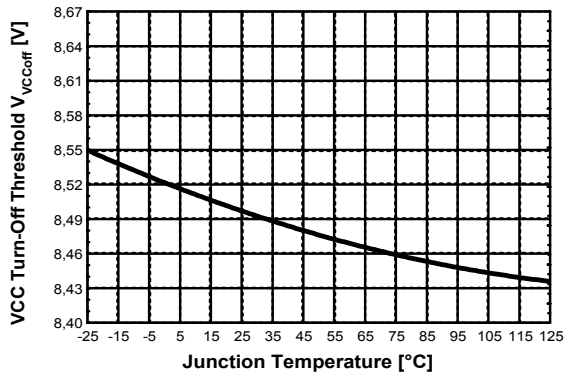


Figure 31 VCC Turn-Off Threshold  $V_{VCCoff}$  vs.  $T_j$

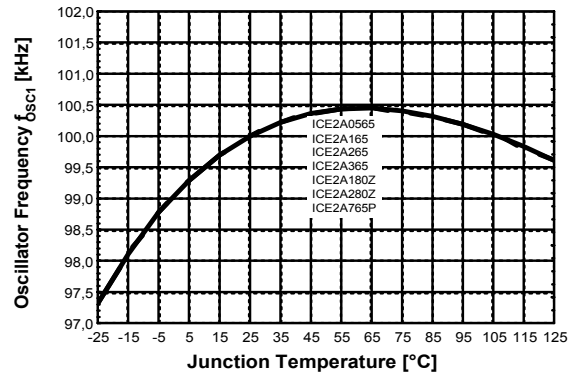


Figure 34 Oscillator Frequency  $f_{osc1}$  vs.  $T_j$

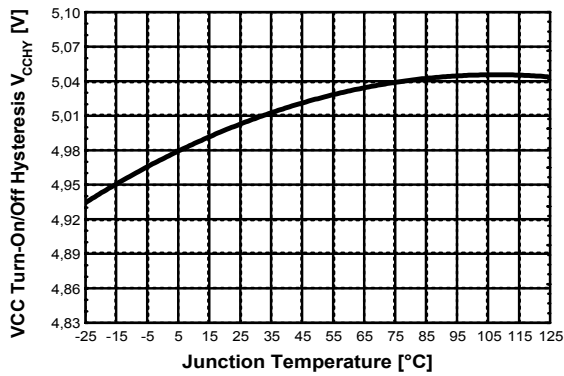


Figure 32 VCC Turn-On/Off Hysteresis  $V_{VCCHY}$  vs.  $T_j$

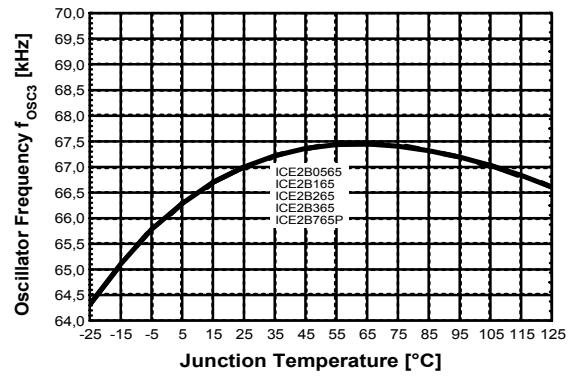


Figure 35 Oscillator Frequency  $f_{osc3}$  vs.  $T_j$



Typical Performance Characteristics

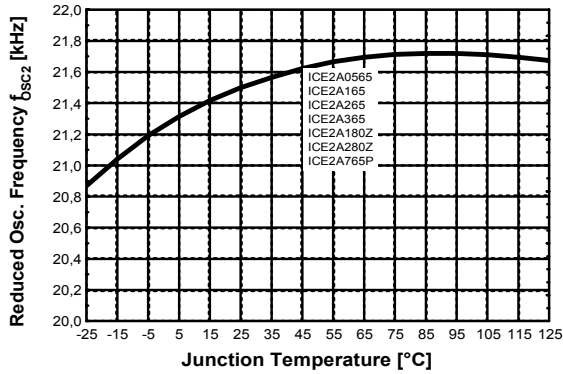


Figure 36 Reduced Osc. Frequency  $f_{OSC2}$  vs.  $T_j$

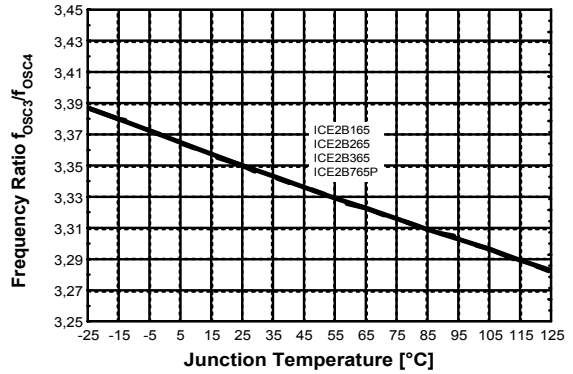


Figure 39 Frequency Ratio  $f_{OSC3}/f_{OSC4}$  vs.  $T_j$

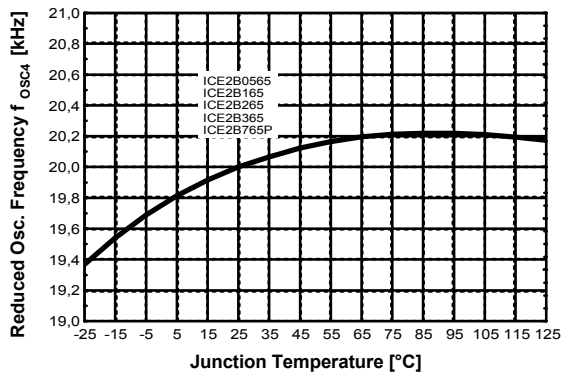


Figure 37 Reduced Osc. Frequency  $f_{OSC4}$  vs.  $T_j$

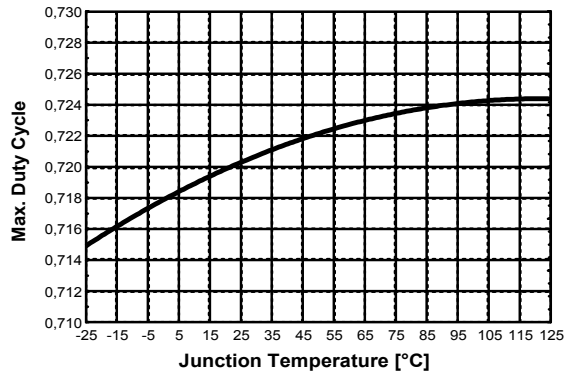


Figure 40 Max. Duty Cycle vs.  $T_j$

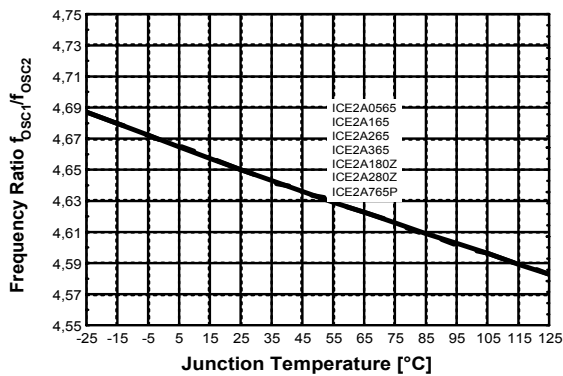


Figure 38 Frequency Ratio  $f_{OSC1}/f_{OSC2}$  vs.  $T_j$

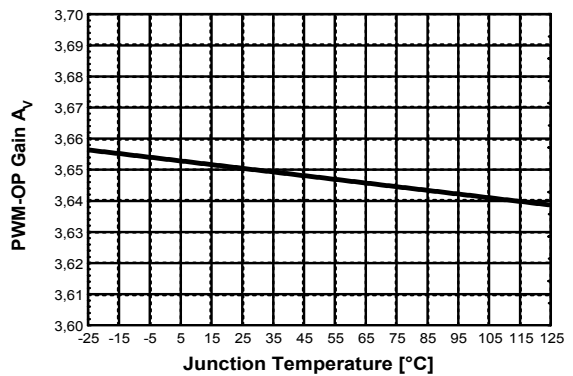


Figure 41 PWM-OP Gain  $A_V$  vs.  $T_j$

Typical Performance Characteristics

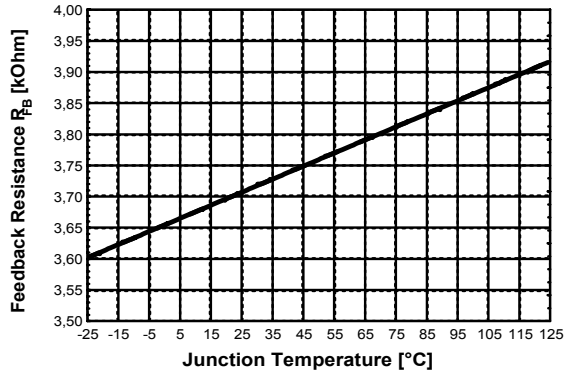


Figure 42 Feedback Resistance  $R_{FB}$  vs.  $T_j$

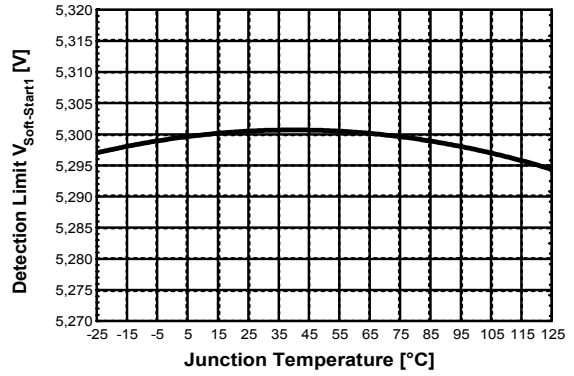


Figure 45 Detection Limit  $V_{Soft-Start1}$  vs.  $T_j$

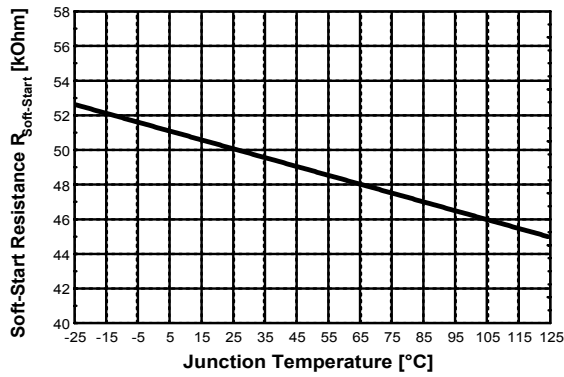


Figure 43 Soft-Start Resistance  $R_{Soft-Start}$  vs.  $T_j$

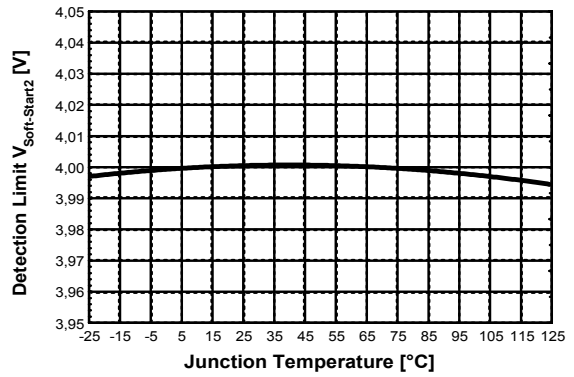


Figure 46 Detection Limit  $V_{Soft-Start2}$  vs.  $T_j$

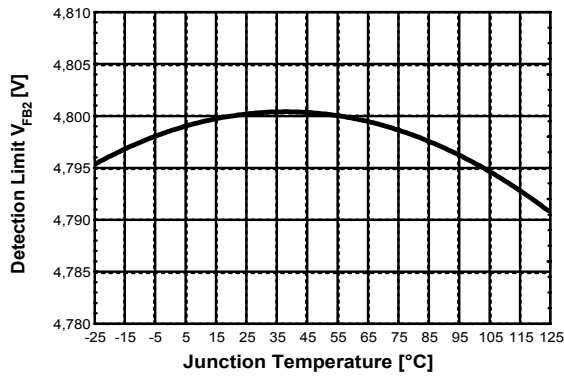


Figure 44 Detection Limit  $V_{FB2}$  vs.  $T_j$

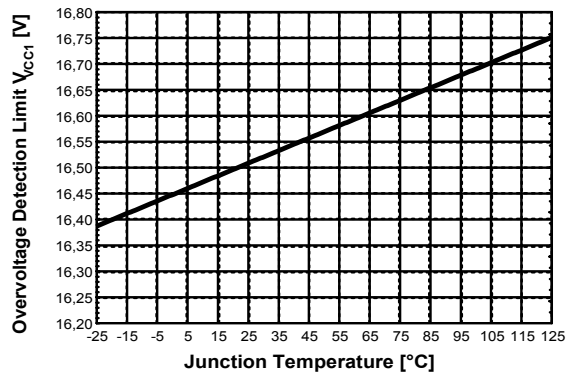


Figure 47 Overvoltage Detection Limit  $V_{VCC1}$  vs.  $T_j$

Typical Performance Characteristics

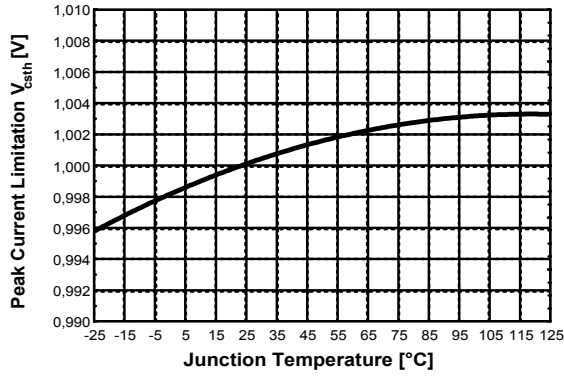


Figure 48 Peak Current Limitation  $V_{csth}$  vs.  $T_j$

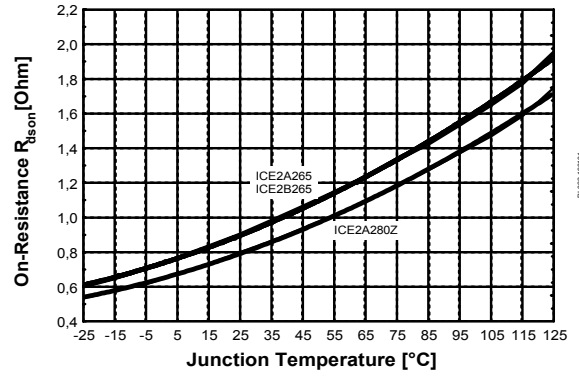


Figure 51 Drain Source On-Resistance  $R_{DS(on)}$  vs.  $T_j$

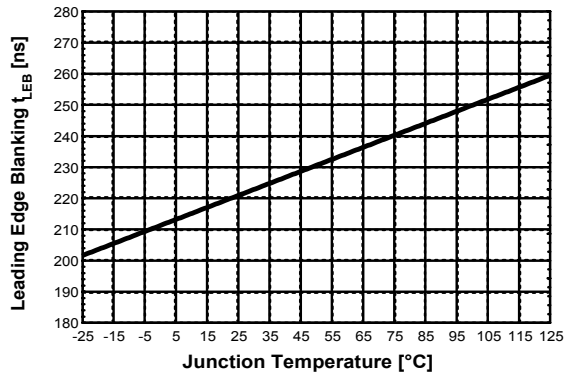


Figure 49 Leading Edge Blanking  $V_{VCC1}$  vs.  $T_j$

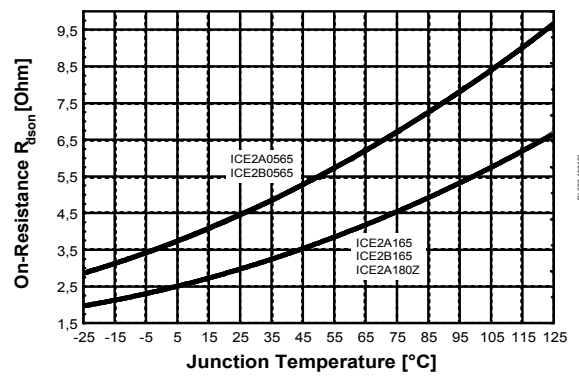


Figure 52 Drain Source On-Resistance  $R_{DS(on)}$  vs.  $T_j$

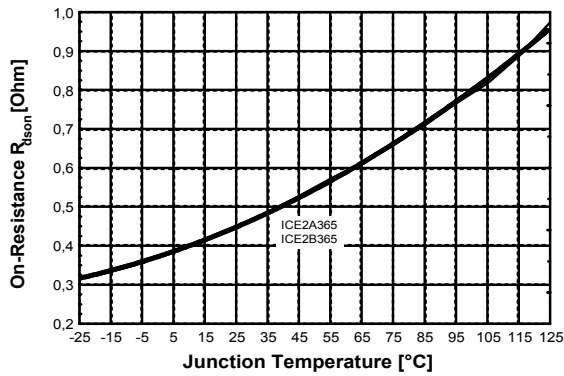


Figure 50 Drain Source On-Resistance  $R_{DS(on)}$  vs.  $T_j$

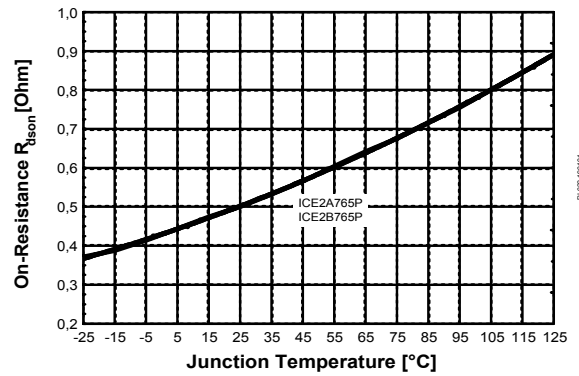


Figure 53 Drain Source On-Resistance  $R_{DS(on)}$  vs.  $T_j$

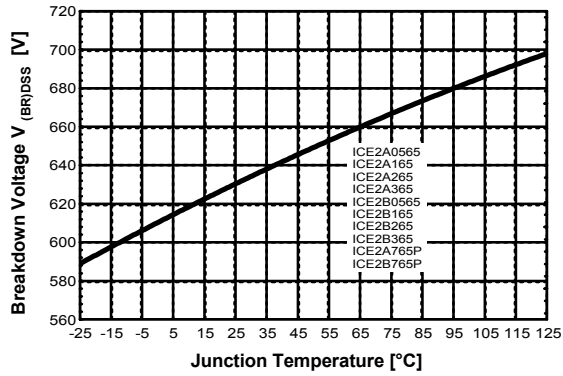


Figure 54 Breakdown Voltage  $V_{BR(DSS)}$  vs.  $T_j$

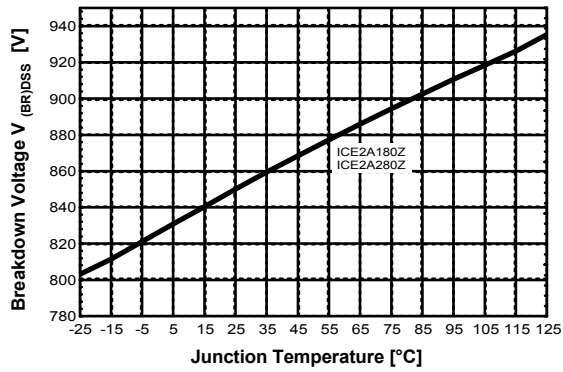


Figure 55 Breakdown Voltage  $V_{BR(DSS)}$  vs.  $T_j$

## 6 Layout recommendation for C<sub>18</sub>

### Only for ICE2A765P and ICE2B765P

#### Soft Start Capacitor Layout Recommendation in Detail

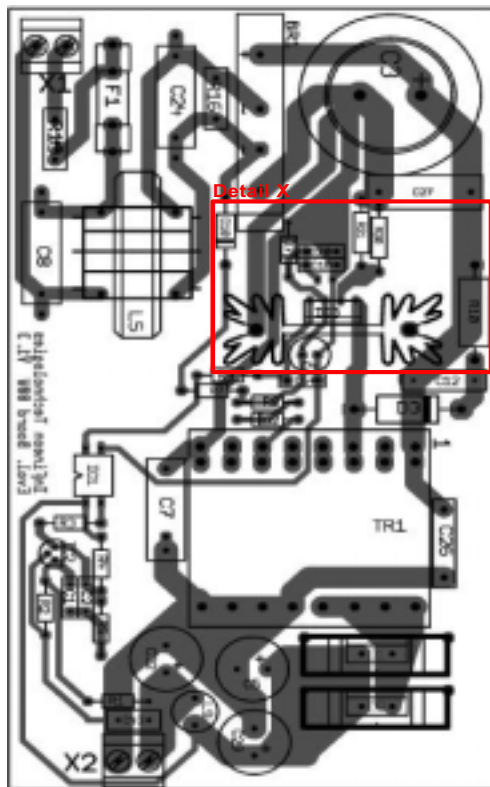


Figure 1 Layout of Board EVALSF2\_ICE2B765P

To improve the startup behavior of the IC during startup or auto restart mode, place the soft start capacitor C18 (red section Detail X in Figure 1) as close as possible to the soft start PIN 6 and GND PIN 4. More details see Detail X in Figure 2

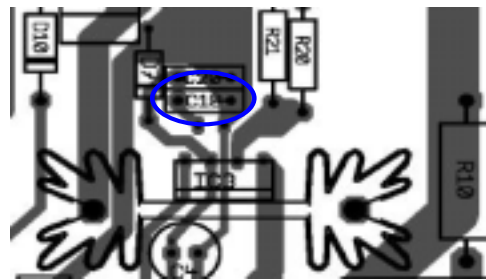


Figure 2 Detail X, Soft Start Capacitor C18 Layout Recommendation

Place soft start capacitor C18 in the same way as shown in Detail X (blue mark).

Outline Dimension

7 Outline Dimension

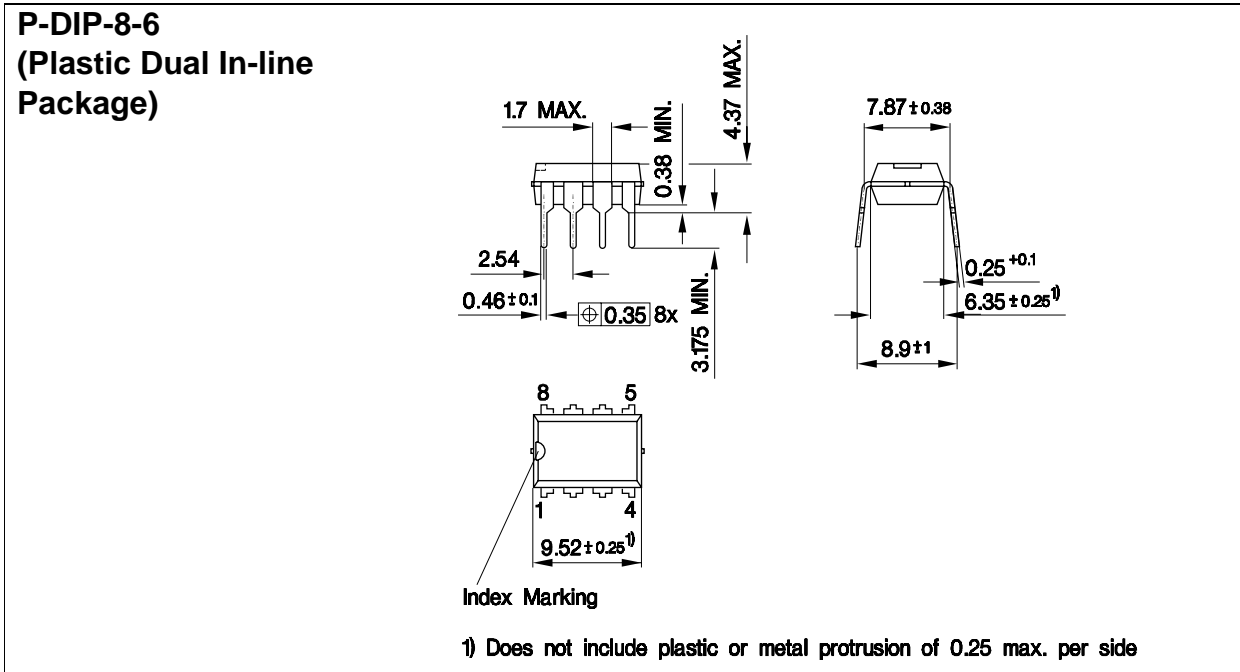


Figure 56

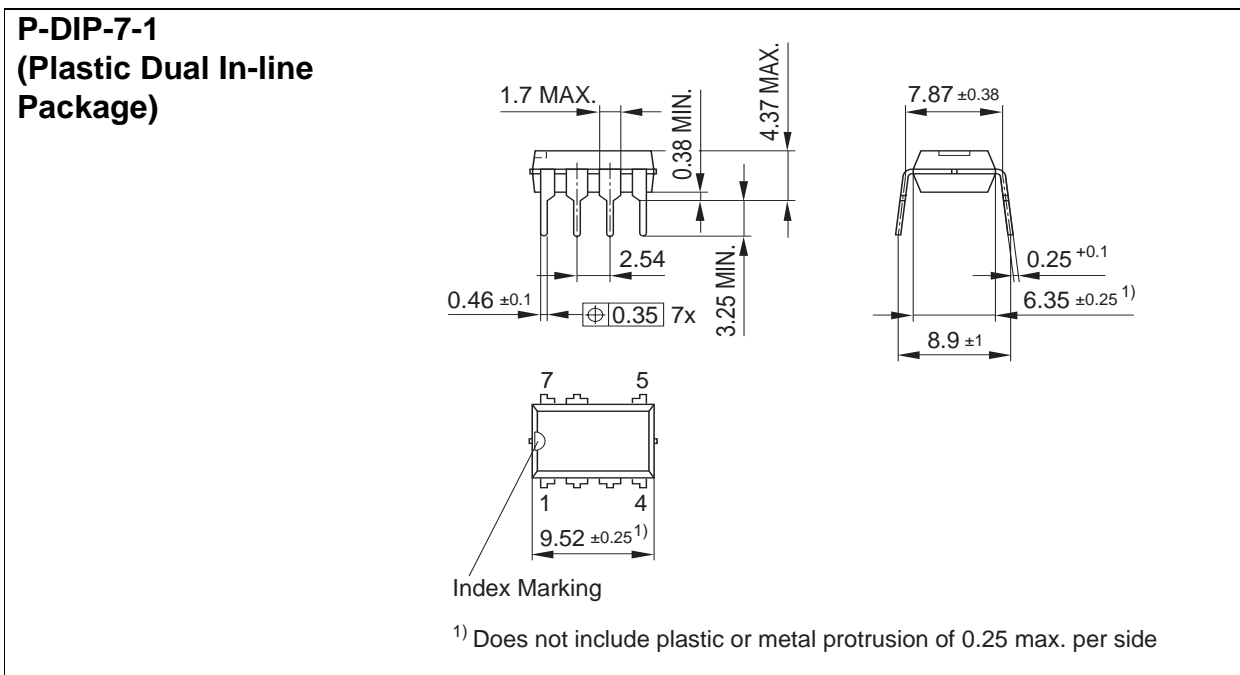


Figure 57

Dimensions in mm



# Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen. Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

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Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

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