µP Supervisor with Watchdog Timer, Power-Fail Comparator, Manual Reset and Adjustable Power-On Reset

Designed with high reset threshold accuracy and low power consumption, the ISL88705, ISL88706, ISL88707, ISL88708, ISL88716 and ISL88813 devices are microprocessor supervisors that are designed to monitor power-supply and battery functions in microprocessor systems. They can help to lower system cost, reduce board space requirements and increase the reliability of systems.

These devices provide essential functions such as supply voltage supervision by asserting a reset output during power-up and power-down as well as during brownout conditions. An auxiliary voltage monitor is provided for detecting power failures warning the system of low battery conditions or presence detection. In addition, an independent watchdog timer helps to monitor microprocessor activity every 1.6s (typical). An active-low manual reset is offered and reset signals remain asserted until V_{DD} returns to proper operating levels.

Users can increase the nominal 200ms power-on reset time-out delay by adding an external capacitor to the C_{POR} pin on the ISL88707 and ISL88708.

Features

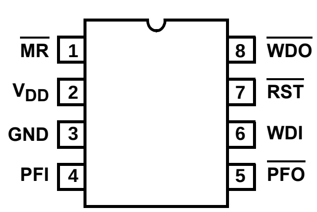
- Fixed-Voltage Options Allow Precise Monitoring of +3.0V, +3.3V, and +5.0V Power Supplies
- Additional Voltage Monitor for Power-Fail Detection or Low-Battery Warning
  - Monitors Voltages Down to 1.25V
  - Adjustable Power-Fail Input Threshold
- Watchdog Timer Capability With 1.6s Time-out
- Both RST and $\overline{RST}$ Outputs Available
- 140ms Minimum Reset Pulse Width with Option to Customize Using an External Capacitor
- Manual Reset Input On All Devices
- Reset Signal Valid Down to V_{DD} = 1V
- Accurate ±1.8% Voltage Threshold
- Immune to Power-Supply Transients
- Ultra Low 10µA Maximum Supply Current at 3V
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

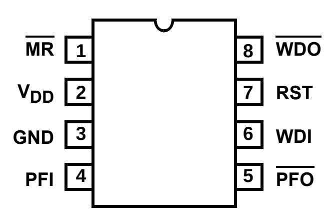
- Portable/Battery Powered Equipment
- Notebook/Desktop Computer Systems
- Designs Using DSPs, Microcontrollers or Microprocessors
- Controllers
- Intelligent Instruments
- Communications Systems
- Industrial Equipment

Pinouts

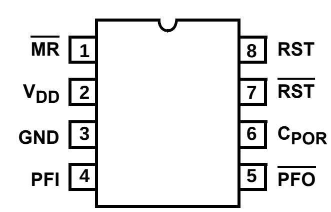
ISL88705, ISL88706
(8 LD PDIP/SOIC)
TOP VIEW



ISL88716, ISL88813
(8 LD PDIP/SOIC)
TOP VIEW



ISL88707, ISL88708
(8 LD PDIP/SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	V_{TH}	TEMP RANGE (°C)	PACKAGE (Pb-Free)
ISL88705IP846Z	ISL88705 Z I46	4.64V	-40 to 85	8 Ld PDIP*
ISL88706IP844Z	ISL88706 Z I44	4.38V	-40 to 85	8 Ld PDIP*
ISL88706IP831Z	ISL88706 Z I31	3.09V	-40 to 85	8 Ld PDIP*
ISL88706IP829Z	ISL88706 Z I29	2.92V	-40 to 85	8 Ld PDIP*
ISL88706IP826Z	ISL88706 Z I26	2.63V	-40 to 85	8 Ld PDIP*
ISL88813IP846Z	ISL88813 Z I46	4.64V	-40 to 85	8 Ld PDIP*
ISL88716IP826Z	ISL88716 Z I26	2.63V	-40 to 85	8 Ld PDIP*
ISL88707IP846Z	ISL88707 Z I46	4.64V	-40 to 85	8 Ld PDIP*
ISL88708IP844Z	ISL88708 Z I44	4.38V	-40 to 85	8 Ld PDIP*
ISL88708IP831Z	ISL88708 Z I31	3.09V	-40 to 85	8 Ld PDIP*
ISL88708IP829Z	ISL88708 Z I29	2.92V	-40 to 85	8 Ld PDIP*
ISL88708IP826Z	ISL88708 Z I26	2.63V	-40 to 85	8 Ld PDIP*
ISL88705IB846Z	88705 Z I46	4.64V	-40 to 85	8 Ld SOIC
ISL88706IB844Z	88706 Z I44	4.38V	-40 to 85	8 Ld SOIC
ISL88706IB831Z	88706 Z I31	3.09V	-40 to 85	8 Ld SOIC
ISL88706IB829Z	88706 Z I29	2.92V	-40 to 85	8 Ld SOIC

Ordering Information (Continued)

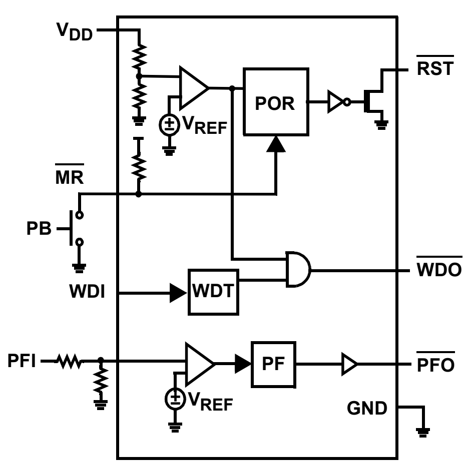
PART NUMBER (Notes 1, 2)	PART MARKING	V_{TH}	TEMP RANGE (°C)	PACKAGE (Pb-Free)
ISL88706IB826Z	88706 Z I26	2.63V	-40 to 85	8 Ld SOIC
ISL88813IB846Z	88813 Z I46	4.64V	-40 to 85	8 Ld SOIC
ISL88716IB826Z	88716 Z I26	2.63V	-40 to 85	8 Ld SOIC
ISL88707IB846Z	88707 ZI46	4.64V	-40 to 85	8 Ld SOIC
ISL88708IB844Z	88708 Z I44	4.38V	-40 to 85	8 Ld SOIC
ISL88708IB831Z	88708 Z I31	3.09V	-40 to 85	8 Ld SOIC
ISL88708IB829Z	88708 Z I29	2.92V	-40 to 85	8 Ld SOIC
ISL88708IB826Z	88708 Z I26	2.63V	-40 to 85	8 Ld SOIC

NOTES:

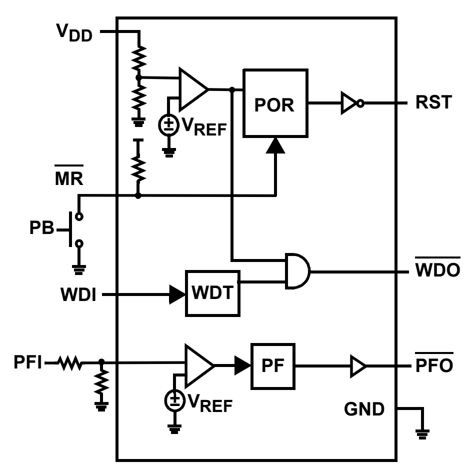
1. Add "-TK" suffix for SOIC Tape and Reel Packaging
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

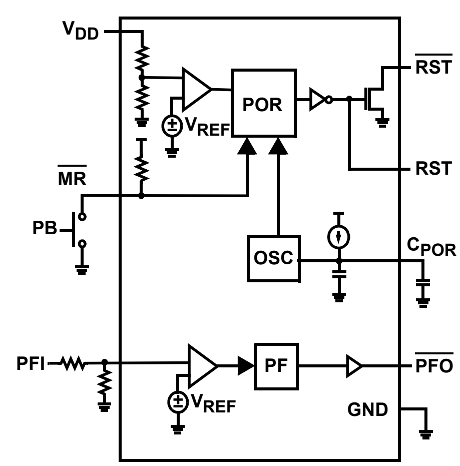
Functional Block Diagrams



ISL88705, ISL88706



ISL88716, ISL88813



ISL88707, ISL88708

Pin Descriptions

ISL88705, ISL88706	ISL88716, ISL88813	ISL88707, ISL88708	NAME	DESCRIPTION
1	1	1	$\overline{MR}$	**Manual Reset Input.** A reset signal is generated when this input is pulled low. The $\overline{MR}$ input is an active low debounced input to which a user can connect a push-button to add manual reset capability or drive with a signal. The $\overline{MR}$ pin has an internal 100kΩ pull-up.
2	2	2	V_{DD}	**Power Supply Terminal.** The voltage at this pin is compared against an internal factory-programmed voltage trip point, V_{TH1}. A reset is first asserted when the device is initially powered up to ensure that the power supply has stabilized. Thereafter, reset is again asserted whenever V_{DD} falls below V_{TH1}. The device is designed with hysteresis to help prevent chattering due to noise and is immune to brief power-supply transients. The voltage threshold V_{TH1} is specified in the part number suffix.
3	3	3	GND	**Ground Connection**
4	4	4	PFI	**Power-Fail Input** This is an auxiliary monitored voltage input with a 1.25V threshold that causes $\overline{PFO}$ state to follow the PFI input state.
5	5	5	$\overline{PFO}$	**Power-Fail Output.** This output goes high if the voltage on PFI is greater than 1.25V, otherwise $\overline{PFO}$ stays low.
		6	C_{POR}	**Adjustable POR Time-out Delay Input.** Connecting an external capacitor from C_{POR} to ground allows the user to increase the Power On Reset timeout (t_{POR}) from the nominal 200ms.
6	6		WDI	**Watchdog Input.** The Watchdog Input takes an input from a microprocessor and ensures that it periodically toggles the WDI pin, otherwise the internal nominal 1.6s watchdog timer runs out, then reset is asserted and WDO is pulled low. The internal Watchdog Timer is cleared whenever the WDI sees a rising or falling edge or the device is manually reset. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature.
7		7	$\overline{RST}$	**Active-Low Reset Output.** The $\overline{RST}$ output is an active low open drain output that is pulled low to GND when reset is asserted. Reset is asserted whenever; 1. The device is first powered up, 2. V_{DD} falls below its minimum voltage sense level or 3. $\overline{MR}$ is asserted. The reset output continues to be asserted for typically 200ms after V_{DD} rises above the reset threshold or $\overline{MR}$ input goes from low to high. A watchdog time-out will not trigger a reset unless WDO is connected to $\overline{MR}$.
	7	8	RST	**Active-High Reset Output.** The RST pin functions identically to its complementary $\overline{RST}$ output but is an active high push pull output. RST is set high to V_{DD} when reset is asserted. See the $\overline{RST}$ description for more details on conditions that cause a reset.
8	8		$\overline{WDO}$	**Watchdog Output**. This output is pulled low when the nominal 1.6s internal Watchdog Timer expires and does not go high again until the watchdog is cleared. WDO also goes low during low V_{DD} conditions. Whenever V_{DD} is below the reset threshold, WDO stays low. However, unlike RESET, WDO does not have a minimum pulse width. As soon as V_{DD} rises above the reset threshold, WDO goes high with no delay.

Absolute Maximum Ratings

Temperature Under Bias . . . . -40°C to +125°C
Storage Temperature . . . . -65°C to +150°C
Voltage on any Pin with Respect to GND . . . . -1.0V to +7V
DC Output Current 5mA
Lead Temperature (Soldering, 10s) . . . . 300°C
ESD Classification . . . . 2.0kV HBM
200V MM
1kV CDM

Recommended Operating Conditions

Temperature Range (Industrial) . . . . -40°C to 85°C

CAUTION: Absolute Maximum Ratings indicate limits beyond which permanent damage to the device and impaired reliability may occur. These are stress ratings provided for information only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied.

For guaranteed specifications and test conditions, see Electrical Specifications. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage Range		2.0		5.5	V
I_{DD}		V_{DD} = 5V, WDT Inactive		10	19	µA
		V_{DD} = 3V, WDT Inactive		8	10	µA
I_{LI}	Input Leakage Current (PFI)				100	nA
I_{LO}	Output Leakage Current				100	nA
VOLTAGE THRESHOLDS						
V_{TH1}	Fixed V_{DD} Voltage Trip Point		4.556	4.640	4.724	V
			4.301	4.380	4.459	V
			3.034	3.090	3.146	V
			2.867	2.920	2.973	V
			2.583	2.630	2.677	V
$V_{TH1HYST}$	Hysteresis at V_{TH1} Input Temperature = 25°C	V_{TH1} = 4.64V		46		mV
		V_{TH1} = 4.38V		44		mV
		V_{TH1} = 3.09V		37		mV
		V_{TH1} = 2.92V		29		mV
		V_{TH1} = 2.63V		31		mV
RST AND $\overline{\text{RST}}$						
V_{OL}	Reset Output Voltage Low	$V_{DD} \geq$ 3.3V, Sinking 2.5mA		0.05	0.40	V
		V_{DD} < 3.3V, Sinking 1.5mA		0.05	0.40	V
V_{OH}	Reset Output Voltage High	$V_{DD} \geq$ 3.3V, Sourcing 2.5mA	V_{DD}-0.6	V_{DD}-0.4		V
		V_{DD} < 3.3V, Sourcing 1.5mA	V_{DD}-0.6	V_{DD}-0.4		V
t_{RPD}	V_{TH} to Reset Asserted Delay			6		µs
t_{POR}	POR Time-Out Delay	C_{POR} is open	140	200	260	ms
C_{LOAD}	Load Capacitance on Reset Pins			5		pF
MANUAL RESET						
V_{MRL}	$\overline{\text{MR}}$ Input Voltage Low				0.8	V
V_{MRH}	$\overline{\text{MR}}$ Input Voltage High		V_{DD}-0.6			V
t_{MR}	$\overline{\text{MR}}$ Minimum Pulse Width		550			ns
R_{PU}	Internal $\overline{\text{MR}}$ Pull-Up Resistor			20		kΩ

Electrical Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG TIMER (Note 3)						
t_{WDT}	Watchdog Time-out Period		1.0	1.6	2.0	s
t_{WDPS}	WDI Minimum Pulse Width		100			ns
V_{IL}	Watchdog Input Voltage Low				0.3 x V_{DD}	V
V_{IH}	Watchdog Input Voltage High		0.7 x V_{DD}			V
V_{WDOL}	$\overline{WDO}$ Output Voltage Low	$V_{DD} \geq 3.3V$, Sinking 2.5mA		0.05	0.40	V
		$V_{DD} < 3.3V$, Sinking 1.5mA		0.05	0.40	V
V_{WDOH}	$\overline{WDO}$ Output Voltage High	$V_{DD} \geq 3.3V$, Sourcing 2.5mA	V_{DD}-0.6	V_{DD}-0.4		V
		$V_{DD} < 3.3V$, Sourcing 1.5mA	V_{DD}-0.6	V_{DD}-0.4		V
I_{WDT}	Watchdog Input Current				1	µA
POWER-FAIL DETECTION						
V_{THPFI}	PFI Input Threshold Voltage		1.20	1.25	1.30	V
$PFIV_{THHYST}$	Hysteresis Voltage			20		mV
V_{PFOL}	PFO Output Voltage Low	$V_{DD} \geq 3.3V$, Sinking 2.5mA		0.05	0.40	V
		$V_{DD} < 3.3V$, Sinking 1.5mA		0.05	0.40	V
V_{PFOH}	PFO Output Voltage High	$V_{DD} \geq 3.3V$, Sourcing 2.5mA	V_{DD}-0.6	V_{DD}-0.4		V
		$V_{DD} < 3.3V$, Sourcing 1.5mA	V_{DD}-0.6	V_{DD}-0.4		V

NOTES:

3. Applies to ISL88705, ISL88706, ISL88716, and ISL88813.

Typical Performance Curves

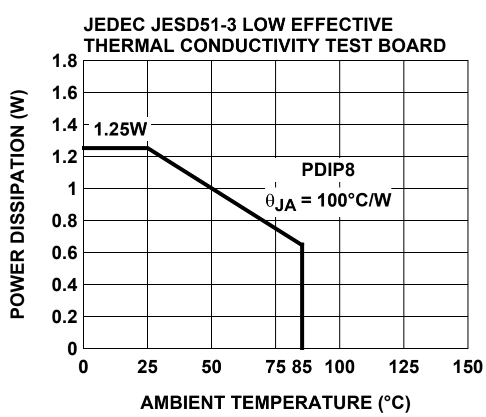


FIGURE 1. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

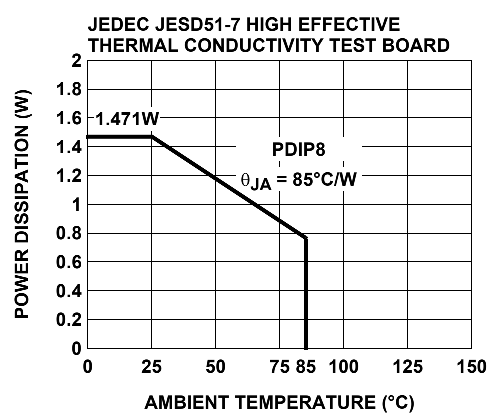


FIGURE 2. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

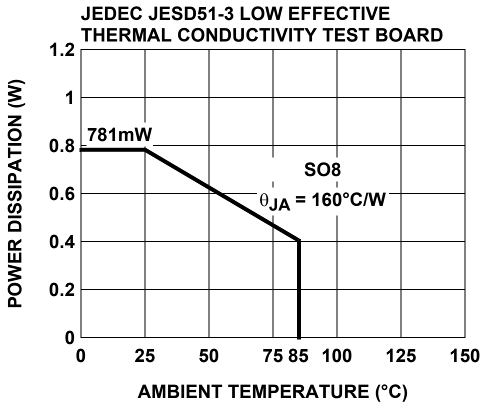


FIGURE 3. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

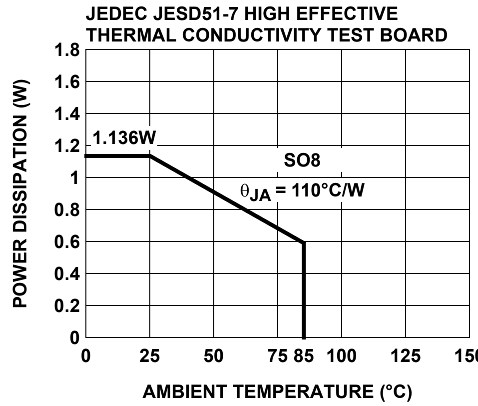


FIGURE 4. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Principles of Operation

The ISL88705 - ISL88813 devices provide those functions needed for monitoring critical voltages such as power-supply and battery functions in microprocessor systems. Features of these supervisors include Power On Reset control, Supply Voltage Supervision, Power-Fail Detection and Manual Reset Assertion. The integration of all these features along with high reset threshold accuracy and low power consumption make these devices ideal for portable or battery-powered equipment.

Power-On Reset (POR)

Applying power to the device activates a POR circuit which asserts reset (i.e. RST goes high while $\overline{RST}$ goes low). These signals provide several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

The reset signals remain active until V_{DD} rises above the minimum voltage sense level for time period t_{POR}. This ensures that the supply voltage has stabilized to sufficient operating levels.

Low Voltage Monitoring

These devices monitor both the voltage level of V_{DD} and an auxiliary voltage on PFI.

When IC is initially biased reset is asserted until the V_{DD} voltage is greater than the specific IC fixed-voltage trip point for the t_{POR} duration of 200ms. At any subsequent time that V_{DD} does not exceed its voltage threshold, reset is once again asserted, i.e. RST is high and $\overline{RST}$ is low.

Power Failure Monitor

These devices also have a Power-Failure Monitor that helps to monitor an additional critical voltage on the Power-Fail Input (PFI) pin. For example, the PFI pin could be used to provide an early power-fail warning, detect a low-battery condition, presence detection or simply monitor a power supply other than +5V. The 1.25V threshold detector can be adjusted using an external resistor divider network to provide custom voltage monitoring of voltages greater than 1.25V, according to the following formula (See Figure 1):

PFI V_{TH} = 1.25 (R1 + R2/R2)

$\overline{PFO}$ goes low whenever PFI is less than the 1.25V (or user-set) threshold voltage.

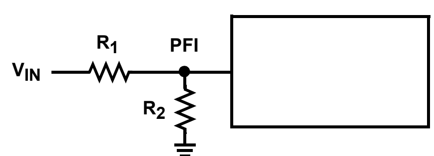


FIGURE 5. CUSTOM V_{TH} WITH RESISTOR DIVIDER ON PFI

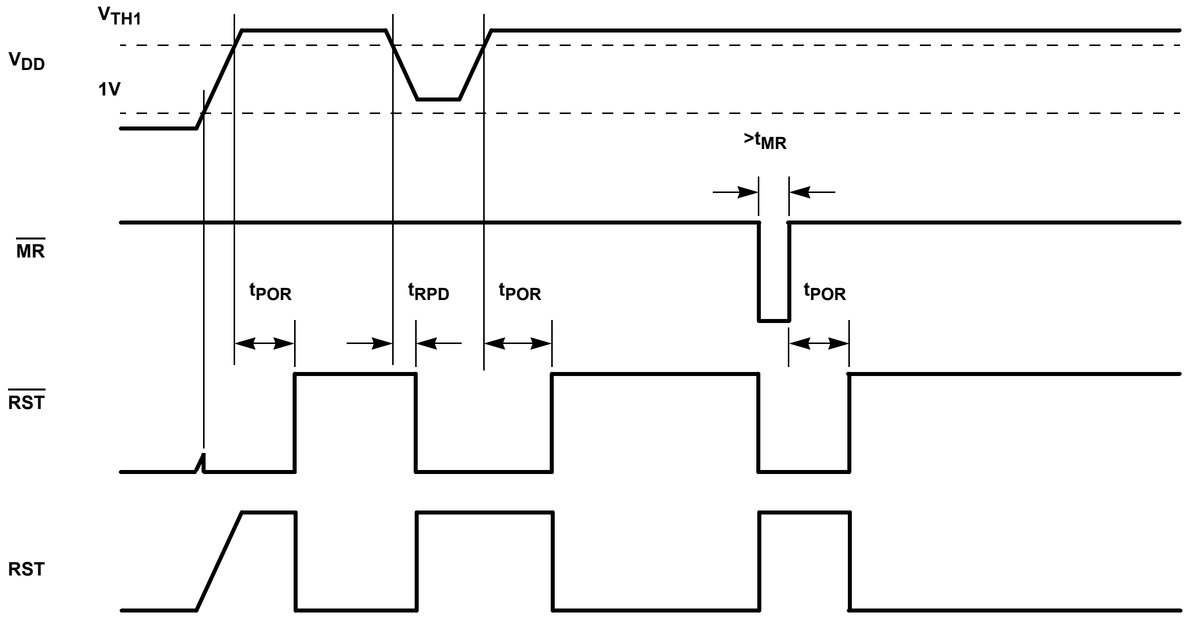


FIGURE 6. POWER-SUPPLY MONITORING TIMING DIAGRAM (WDI TRISTATED)

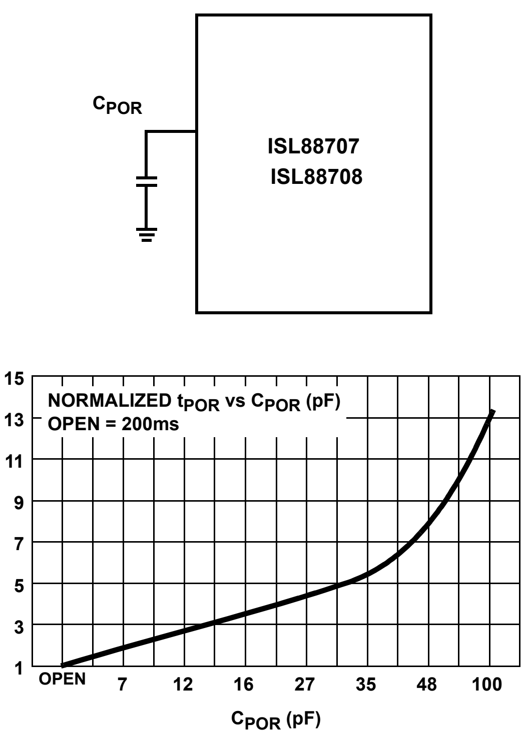


FIGURE 7. ADJUSTING t_{POR} WITH A CAPACITOR

Adjusting t_{POR}

On the ISL88707 and ISL88708, users can adjust the Power On Reset timeout delay (t_{POR}) to many times the nominal t_{POR} of 200ms. To do this, connect a capacitor between C_{POR} and ground (see Figure 3). For example, connecting a 50pF capacitor to CPOR will increase t_{POR} from 200ms to 10s. The maximum recommended capacitance that should be placed on the CPOR pin is 50pF. Care should be taken in PCB layout and capacitor placement in order to reduce stray capacitance as much as possible, which contributes to t_{POR} error.

Manual Reset

The manual-reset input ($\overline{MR}$) allows the user to trigger a reset by using a push-button switch. The $\overline{MR}$ input is an active low debounced input. By connecting a push-button directly from $\overline{MR}$ to ground, the designer adds manual system reset capability (see Figure 4). Reset is asserted if the $\overline{MR}$ pin is pulled low to less than 100mV for the minimum $\overline{MR}$ pulse width or longer while the push-button is closed. After $\overline{MR}$ is released, the reset outputs remain asserted for t_{POR} (200ms) and then released.

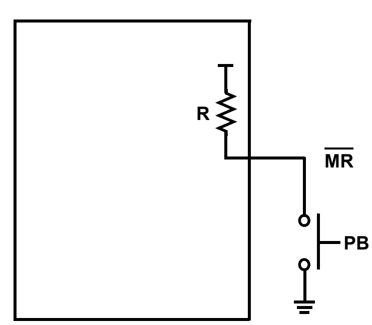


FIGURE 8. CONNECTING A MANUAL RESET PUSH-BUTTON

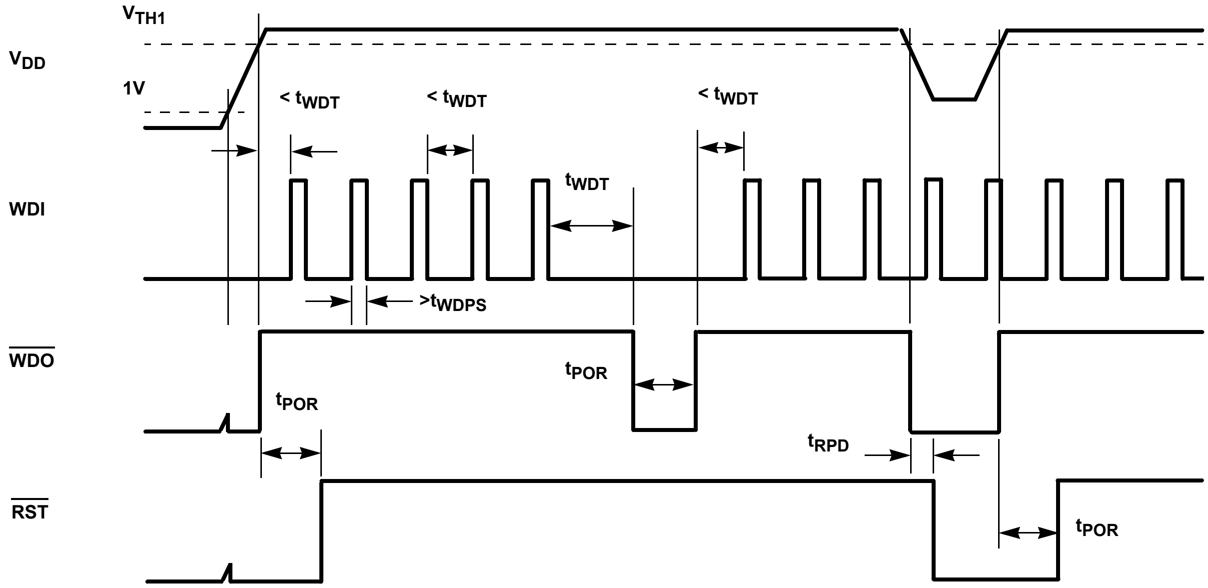


FIGURE 9. WATCHDOG TIMING DIAGRAM

Watchdog Timer

The Watchdog Timer circuit checks microprocessor activity by monitoring the WDI input pin. The microprocessor must periodically toggle the WDI pin within t_{WDT} (typically 1.6s), otherwise the $\overline{WDO}$ pin goes low (see Figure 9). Internally, the 1.6s timer is cleared by either a reset or by toggling the WDI input, which can detect pulses longer than 50ns.

Whenever there is a low-voltage V_{DD} condition, $\overline{WDO}$ goes low. Unlike the reset outputs, however, $\overline{WDO}$ does not have a minimum reset pulse width (t_{POR}). $\overline{WDO}$ goes high as soon as V_{DD} rises above its voltage trip point (see Figure 9). With WDI open or connected to a tristated high impedance input, the Watchdog Timer is disabled and only pulls low when $V_{DD} < V_{TH1}$.

ISL88705EVAL1 and Applications

The ISL88705EVAL1 supports all six of the ISL88705-ISL88813 devices, enabling evaluation of basic functional operation and common application implementations. Figures 11 and 17 illustrate the ISL88705EVAL1 in photographic and schematic forms respectively.

The ISL88705EVAL1 is divided into two banks; each bank having one each of the three available pinouts. The top bank is fully populated and immediately usable whereas the bottom bank is unpopulated. Samples of other sample variants can be evaluated singularly or in combination with any other variant to provide a specific voltage monitoring solution. The left position has a ISL88705IB846Z monitoring the V_{DD} rail voltage for a minimum of 4.64V with reset signaling. In addition, the power fail input (PFI) is being compared to the internal PFI voltage reference of 1.25V and the power fail output ($\overline{PFO}$) will report the PFI condition. This feature can be used for monitoring an auxiliary voltage, providing an early warning of a brownout or power failure or presence detection in a system.

The middle position has the ISL88813IB846Z installed and is set up as a 5V window detector with jumper J1 installed. The V_{DD} monitors for UV and the PFI for OV via the R3, R4 divider. The $\overline{PFO}$ output is inverted and connected to the manual reset input ($\overline{MR}$) via U4. Hence a reset signal is generated when $4.64V < V_{DD} > 5.38V$. With J1 removed the $\overline{PFO}$ will be an OV indicator but no reset signal will be generated. Both of these positions share a common Watchdog input (WDI) signal although each has its own Watchdog output ($\overline{WDO}$).

The right position has the ISL88707IB846Z and is set up as a +12V and +5V UV monitor with reset signal. The PFI allows monitoring of any voltage above the 1.25V PFI reference. The ISL88707 and ISL88708 have the unique feature of an adjustable time to reset (t_{POR})signal generation capability via the C_{POR} pin with an external capacitor to GND. This evaluation platform has an adjustable SMD capacitor, C4 (8pF to 45pF) that allows easy evaluation of this feature. Also unique to the ISL88707 and ISL88708 are both the RESET and $\overline{RESET}$ outputs, all other variants having only one or the other.

Figures 10 - 14, illustrate the basic IC functions and performance of the 3 implementations.

Special Application Considerations

Using good decoupling practices will prevent transients (i.e. due to switching noises and short duration droops in the supply voltage) from causing unwanted resets.

When using the C_{POR} pin, avoid stray capacitance during layout as much as possible in order to minimize its effect on the t_{POR} timing.

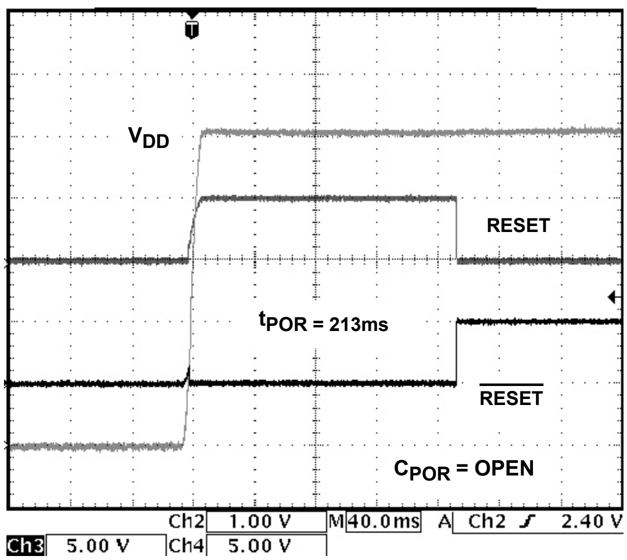


FIGURE 10. RESET & $\overline{\text{RESET}}$ ASSERTION

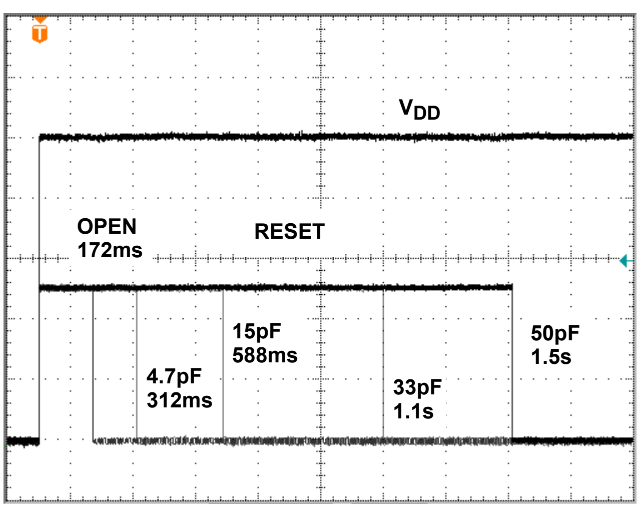


FIGURE 11. RESET ASSERTION vs CPOR

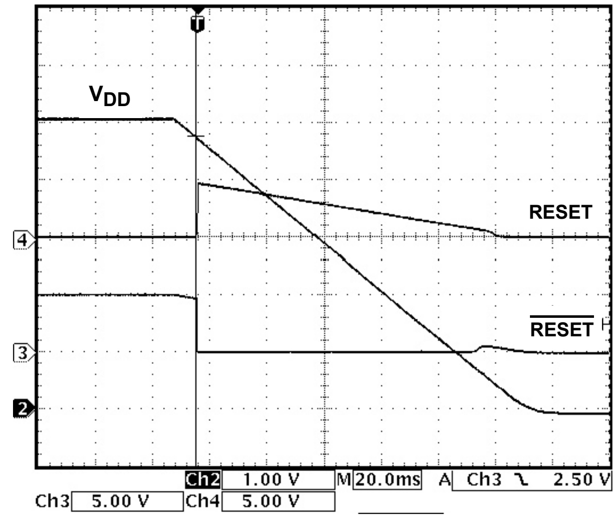


FIGURE 12. RESET & $\overline{\text{RESET}}$ DEASSERTION

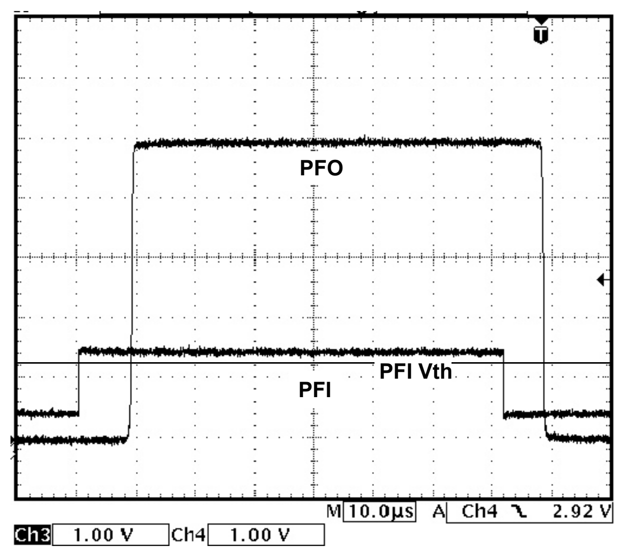


FIGURE 13. 5V PFI TO PFO RESPONSE

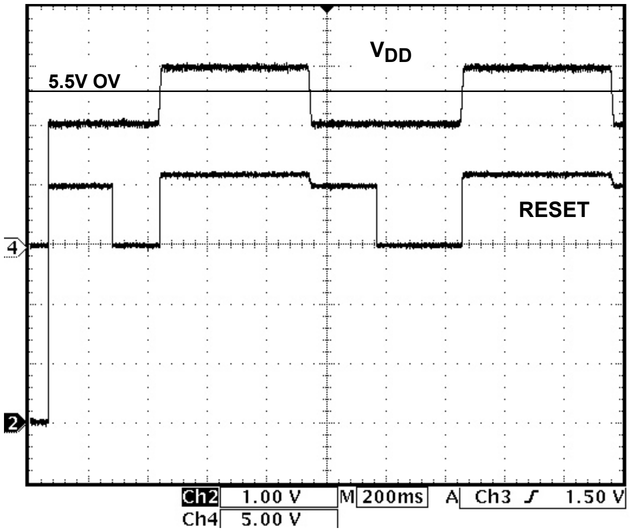


FIGURE 14. 5V OV/UV MONITORING

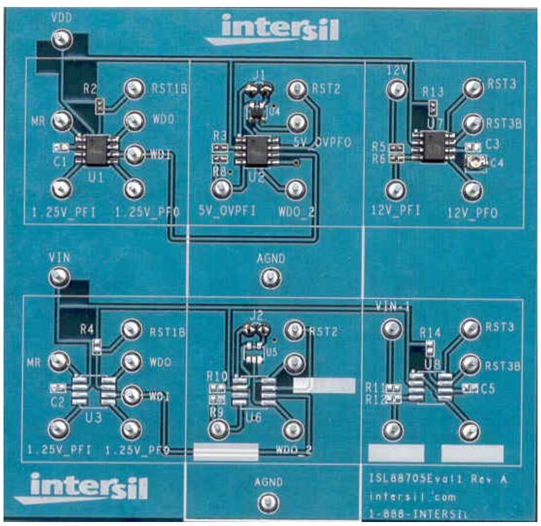
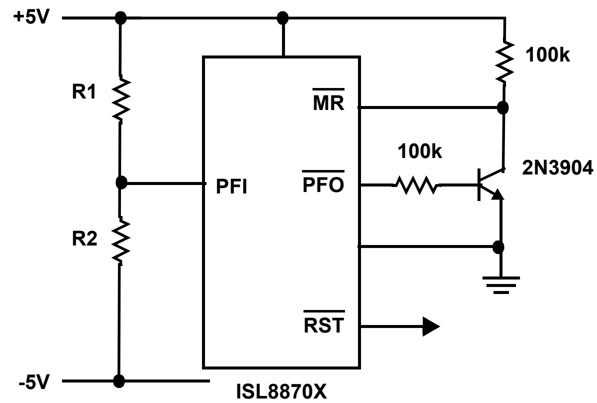


FIGURE 15. ISL88075EVAL1



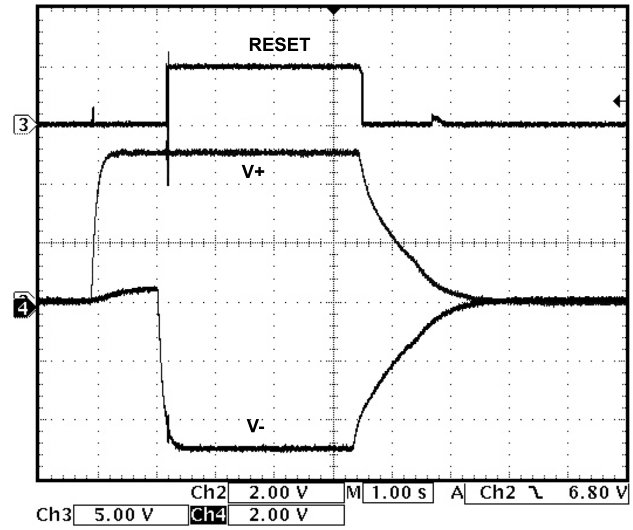


FIGURE 16. ±5V MONITORING

Bipolar Voltage Sensing

Any of the ISL88705 - ISL88813 devices can be used to sense and report the presence of both a positive and negative voltage via the PFI and $\overline{\text{PFO}}$ as shown in Figure 16. The V_{DD} monitors the positive voltage as normal and the PFI monitors the presence of the negative supply. As the differential voltage across the R1, R2 divider is increased the resistor values must be chosen such that the PFI node is <1.25V when the -V supply is satisfactory and the positive supply is at its maximum specified value. This allows the positive supply to fluctuate within its acceptable range without signaling a reset. Driving the $\overline{\text{MR}}$ with the inverted $\overline{\text{PFO}}$ signal as shown provides for reset generation when -V is not satisfactorily present. Reset will remain asserted as long as $\overline{\text{PFO}}$ is high.

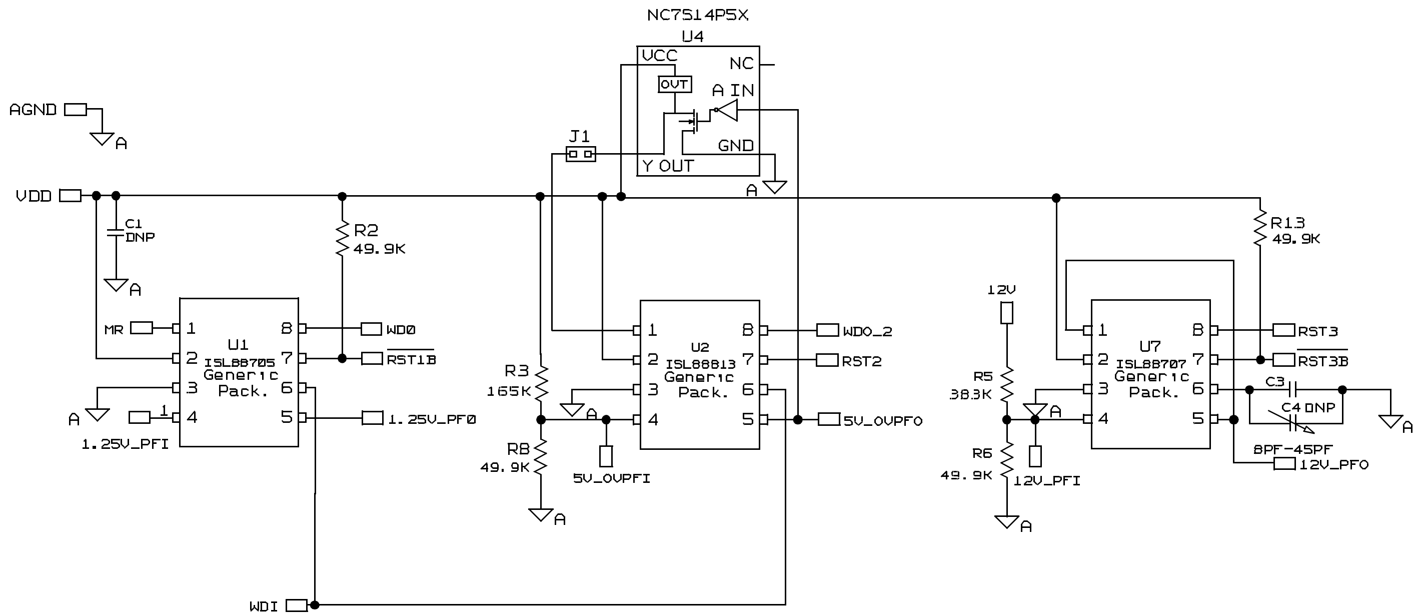
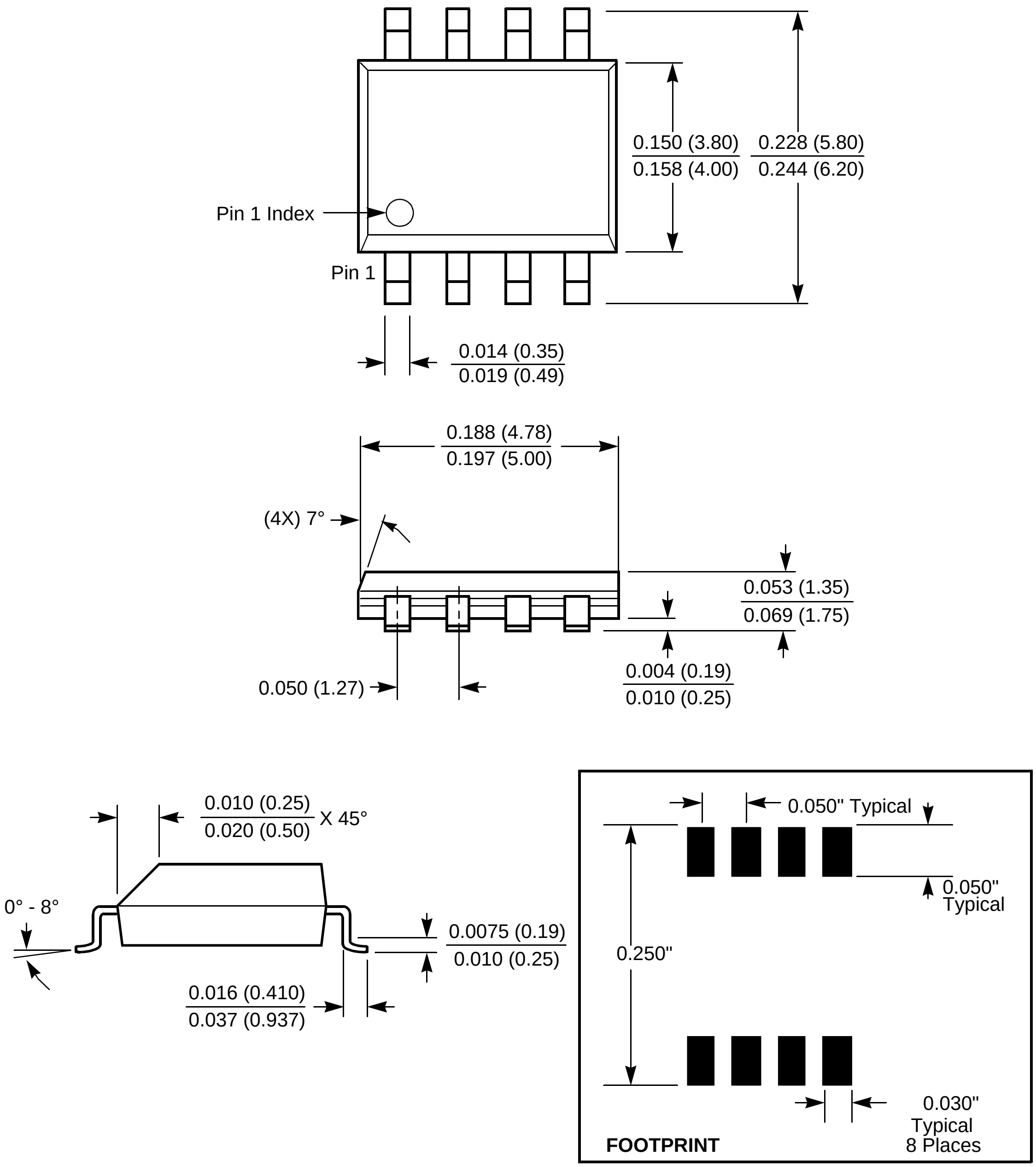


FIGURE 17. ISL88705EVAL1 SCHEMATIC (TOP BANK)

Packaging Information

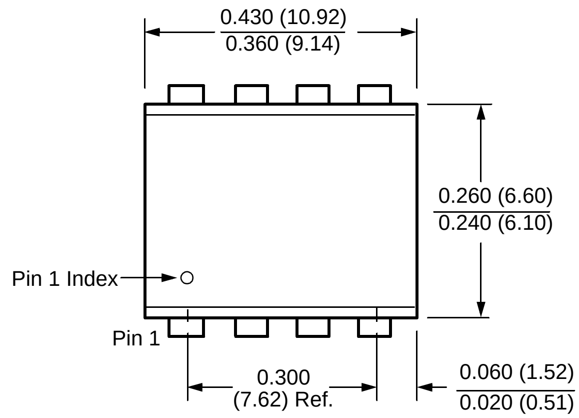
8-Lead Plastic, SOIC, Package Code B8

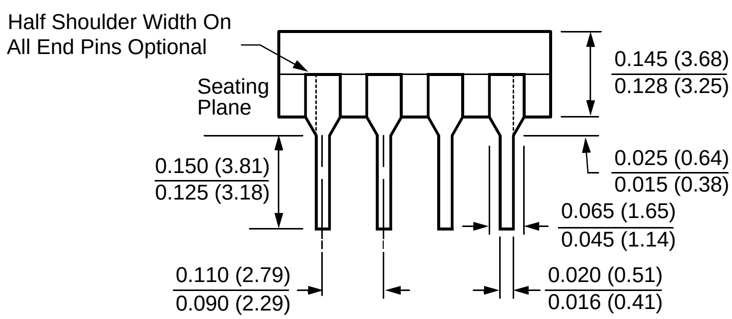


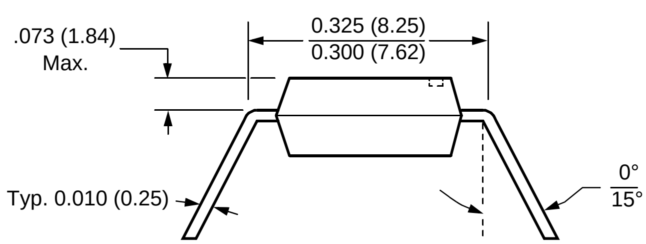
Note: All dimensions in inches (in parentheses in millimeters).

Packaging Information

8-Lead Plastic Dual In-Line Package Type P







NOTES:
1. All dimensions in inches (in parentheses in millimeters).
2. Package dimensions exclude molding flash.

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