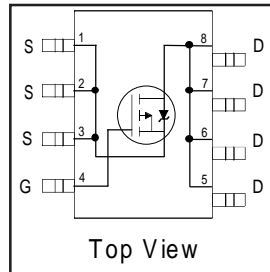


IRF7663

HEXFET® Power MOSFET

- Trench Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel

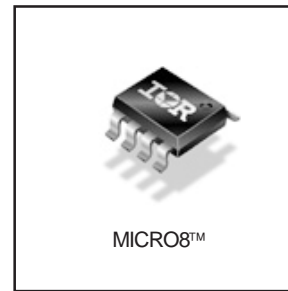


$V_{DSS} = -20V$
$R_{DS(on)} = 0.020\Omega$

Description

New trench HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8™ package has half the footprint area of the standard SO-8. This makes the Micro8 an ideal package for applications where printed circuit board space is at a premium. The low profile (<1.1 mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain- Source Voltage	-20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-8.2	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-6.6	
I_{DM}	Pulsed Drain Current ①	-66	
$P_D @ T_A = 25^\circ C$	Power Dissipation	1.8	W
$P_D @ T_A = 70^\circ C$	Power Dissipation	1.15	
	Linear Derating Factor	10	mW/°C
E_{AS}	Single Pulse Avalanche Energy ④	115	mJ
V_{GS}	Gate-to-Source Voltage	± 12	V
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

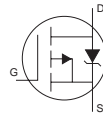
Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ③	70	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.01	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.020	Ω	$V_{GS} = -4.5V, I_D = -7.0A$ ②
		—	—	0.040		$V_{GS} = -2.5V, I_D = -5.1A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	-0.60	—	-1.2	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	14.5	—	—	S	$V_{DS} = -10V, I_D = -7.0A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	30	45	nC	$I_D = -6.0A$
Q_{gs}	Gate-to-Source Charge	—	5.0	7.5		$V_{DS} = -10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	7.0	10.5		$V_{GS} = -5.0V$ ②
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = -10V$
t_r	Rise Time	—	100	—		$I_D = -6.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	125	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	172	—		$R_D = 1.64\Omega$ ②
C_{iss}	Input Capacitance	—	2520	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	615	—		$V_{DS} = -10V$
C_{rss}	Reverse Transfer Capacitance	—	375	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-66		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -7.0A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	70	105	ns	$T_J = 25^\circ\text{C}, I_F = -2.5A$
Q_{rr}	Reverse Recovery Charge	—	50	75	nC	$di/dt = 100A/\mu s$ ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

③ When mounted on 1 inch square copper board, $t < 10$ sec

④ Starting $T_J = 25^\circ\text{C}$, $L = 17.8\text{mH}$
 $R_G = 25\Omega, I_{AS} = -3.6A$. (See Figure 10)

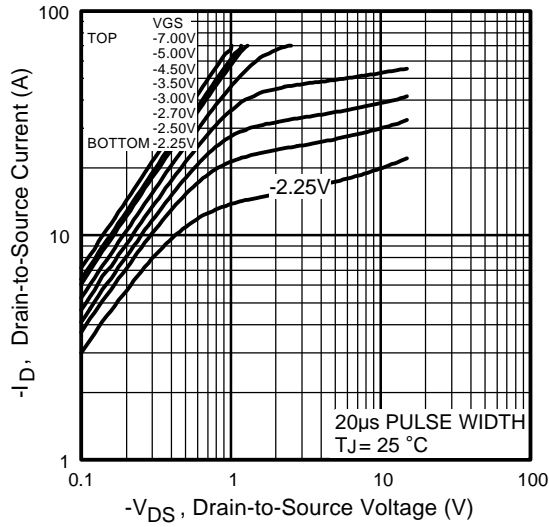


Fig 1. Typical Output Characteristics

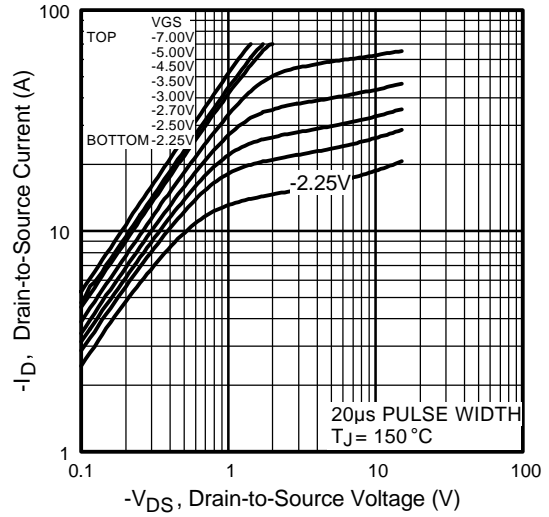


Fig 2. Typical Output Characteristics

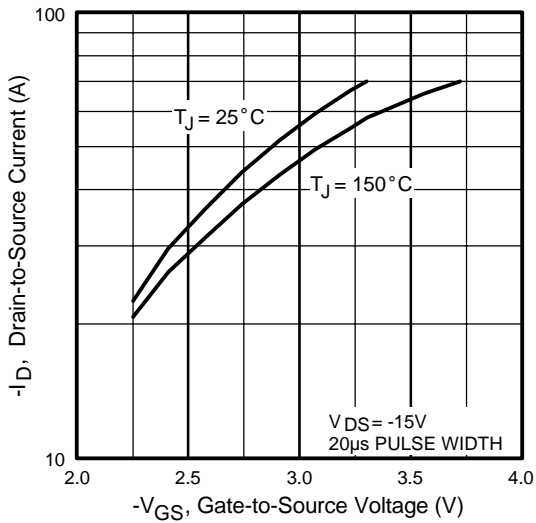


Fig 3. Typical Transfer Characteristics

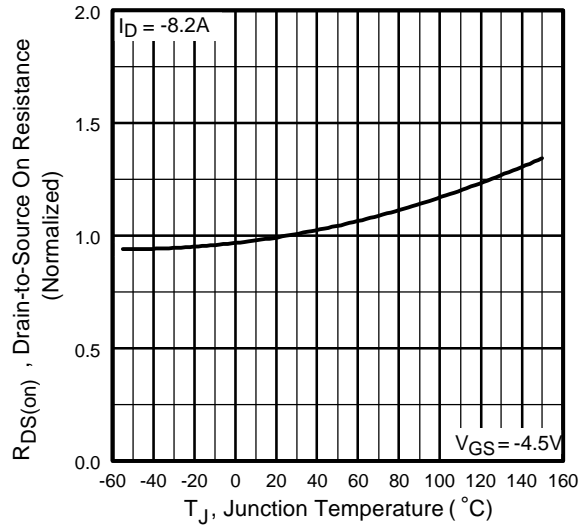


Fig 4. Normalized On-Resistance Vs. Temperature

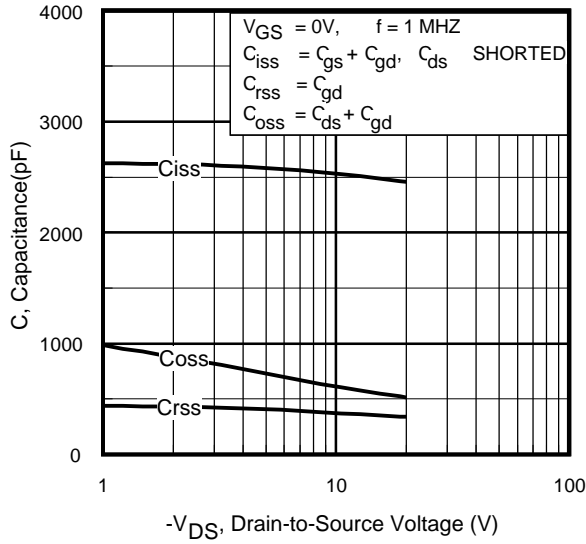


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

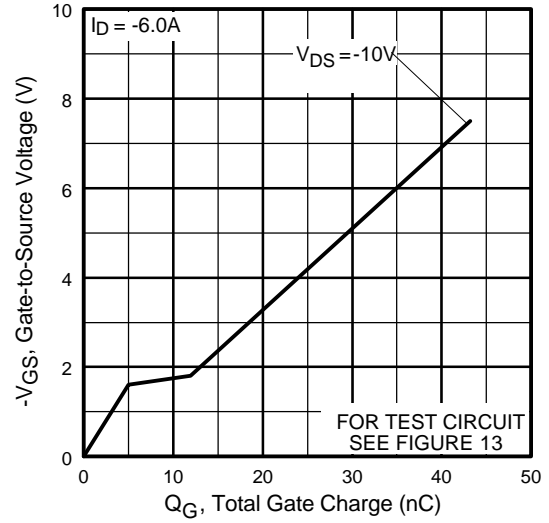


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

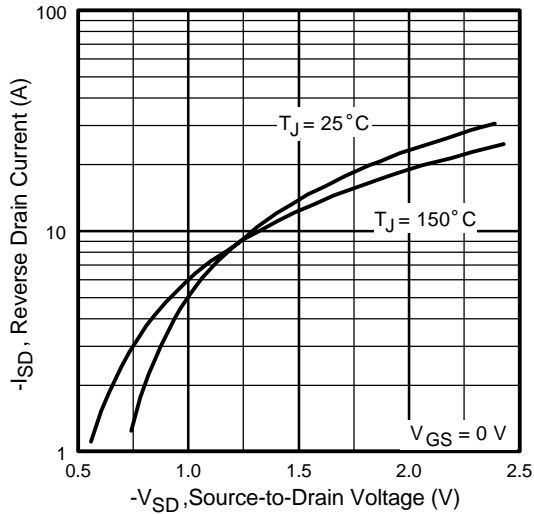


Fig 7. Typical Source-Drain Diode Forward Voltage

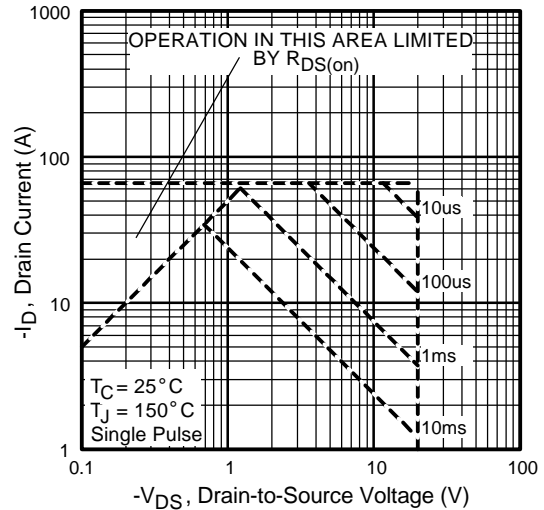


Fig 8. Maximum Safe Operating Area

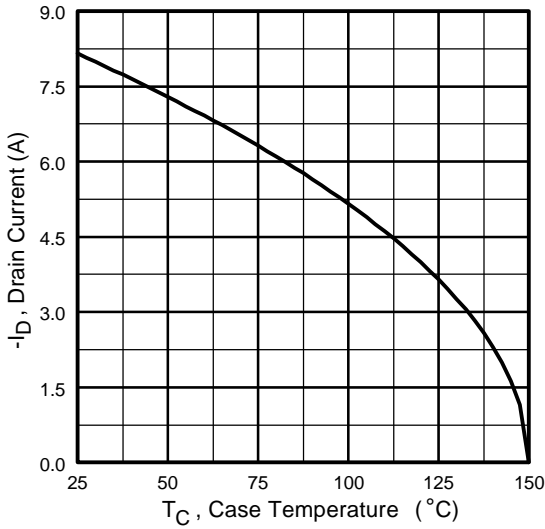


Fig 9. Maximum Drain Current Vs. Case Temperature

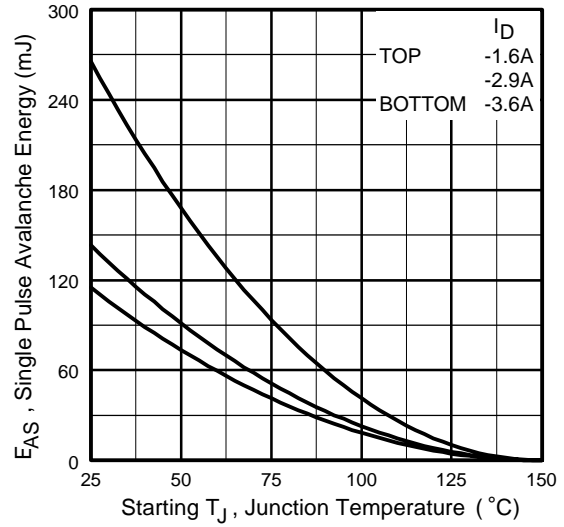


Fig 10. Maximum Avalanche Energy Vs. Drain Current

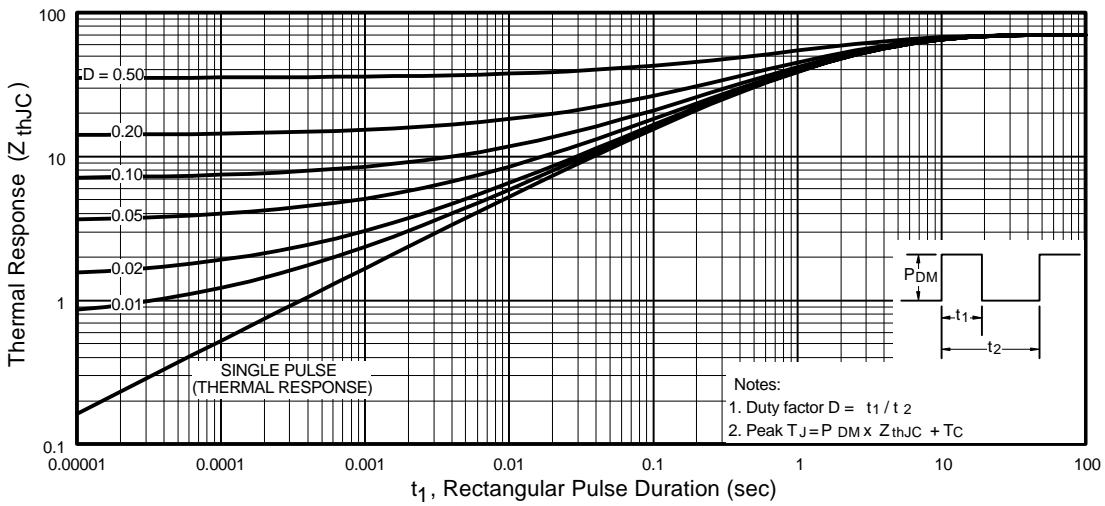


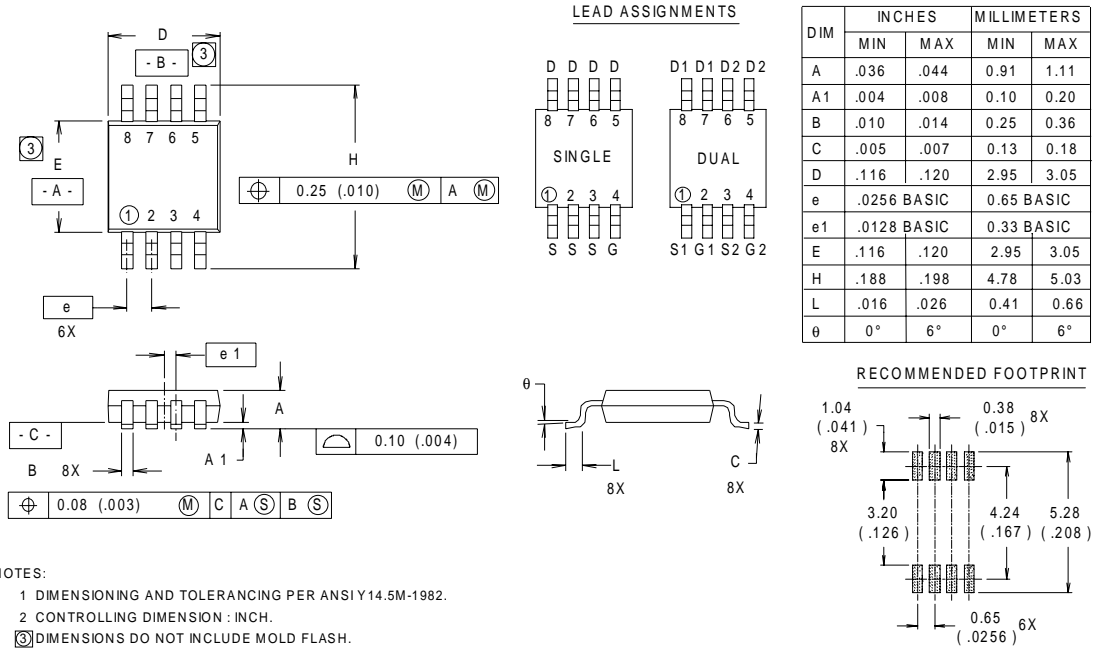
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

IRF7663

Package Outline

Micro8™

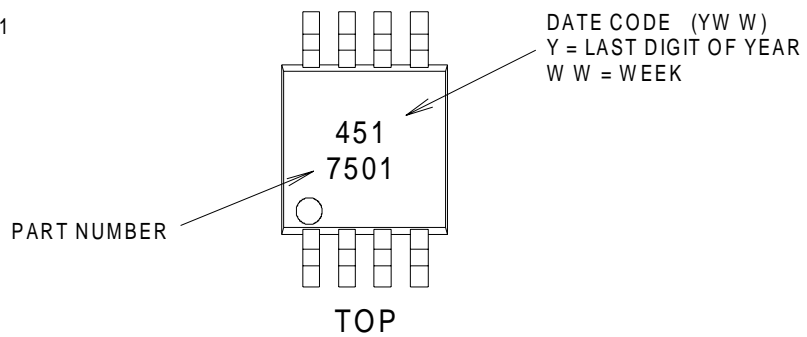
Dimensions are shown in millimeters (inches)



Part Marking Information

Micro8™

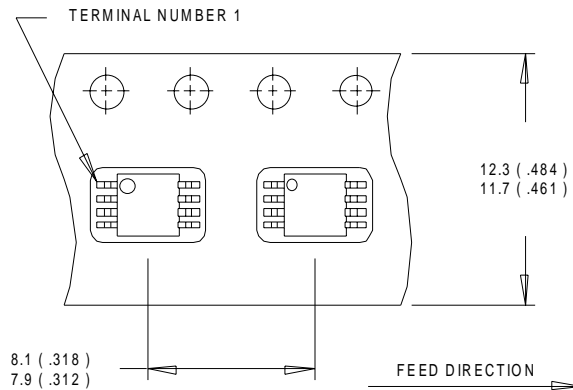
EXAMPLE : THIS IS AN IRF7501



Tape & Reel Information

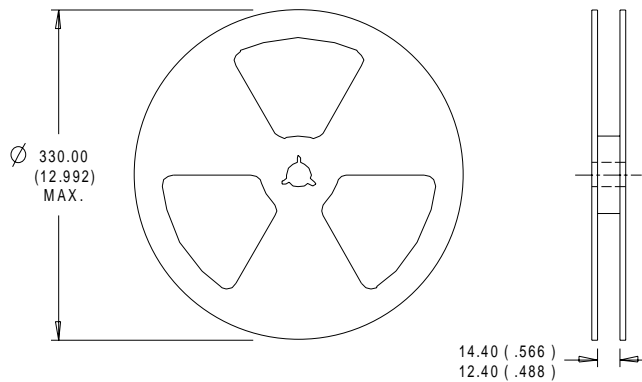
Micro8™

Dimensions are shown in millimeters (inches)



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630

IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

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