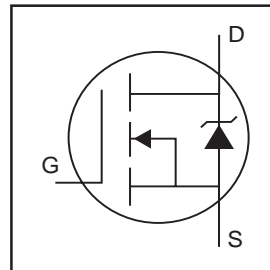


# IRL1404

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

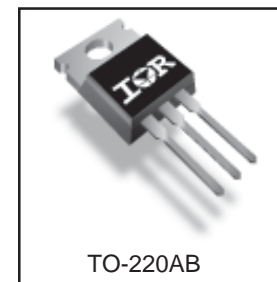


$V_{DSS} = 40V$
$R_{DS(on)} = 4.0m\Omega$
$I_D = 160A\text{Ⓞ}$

## Description

Seventh Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	160Ⓞ	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	110Ⓞ	
$I_{DM}$	Pulsed Drain Current ①	640	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②	620	mJ
$I_{AR}$	Avalanche Current①	95	A
$E_{AR}$	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

## Thermal Resistance

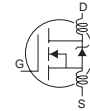
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted)④	—	62	

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## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.038	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	4.0 5.9	m $\Omega$	$V_{GS} = 10V, I_D = 95A$ ④ $V_{GS} = 4.3V, I_D = 40A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	93	—	—	S	$V_{DS} = 25V, I_D = 95A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20 250	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$ $V_{DS} = 32V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage Gate-to-Source Reverse Leakage	—	—	200 -200	nA	$V_{GS} = 20V$ $V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	—	140	nC	$I_D = 95A$ $V_{DS} = 32V$ $V_{GS} = 5.0V$ , See Fig. 6 ④
$Q_{gs}$	Gate-to-Source Charge	—	—	48		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	60		
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 20V$ $I_D = 95A$ $R_G = 2.5\Omega, V_{GS} = 4.5V$ $R_D = 0.25\Omega$ ④
$t_r$	Rise Time	—	270	—		
$t_{d(off)}$	Turn-Off Delay Time	—	38	—		
$t_f$	Fall Time	—	37	—		
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	6590	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$
$C_{oss}$	Output Capacitance	—	1710	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{rss}$	Reverse Transfer Capacitance	—	350	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	6650	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1510	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V$
$C_{oss \text{ eff.}}$	Effective Output Capacitance ⑤	—	1480	—		



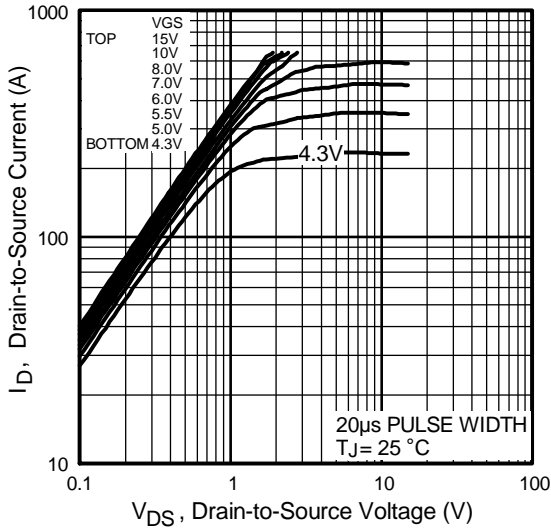
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	160	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	640		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 95A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	63	94	ns	$T_J = 25^\circ\text{C}, I_F = 95A$
$Q_{rr}$	Reverse Recovery Charge	—	170	250	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

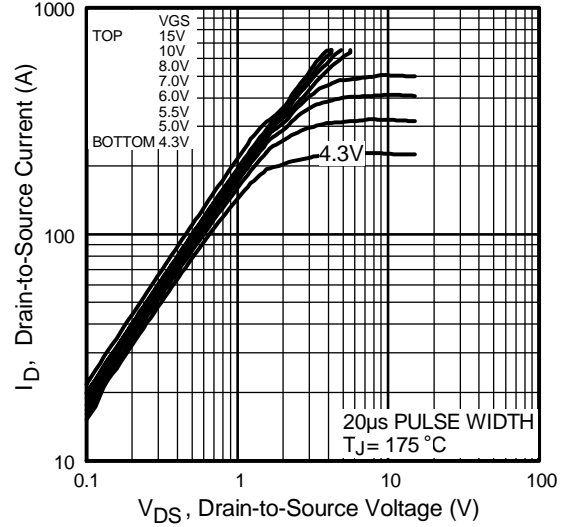
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.35\text{mH}$   
 $R_G = 25\Omega, I_{AS} = 95A$ . (See Figure 12).
- ③  $I_{SD} \leq 95A, di/dt \leq 160A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

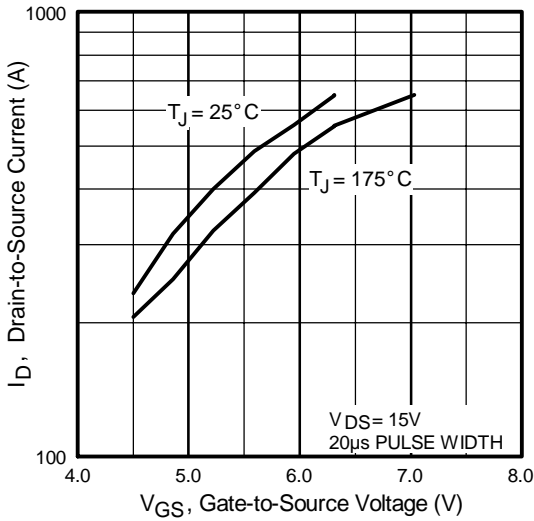
- ⑤  $C_{oss \text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handing of the package refer to Design Tip # 93-4.
- ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.



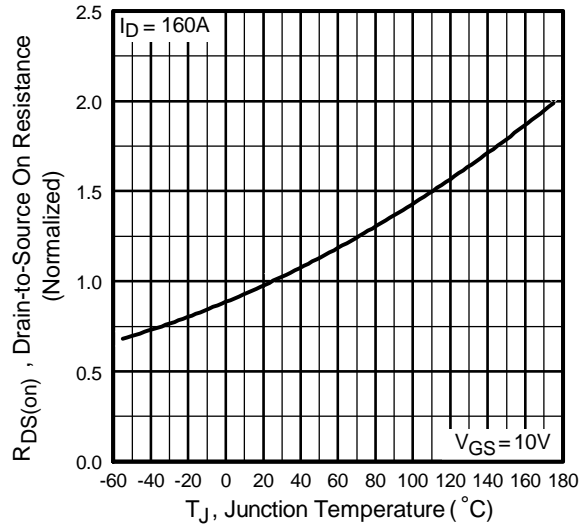
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

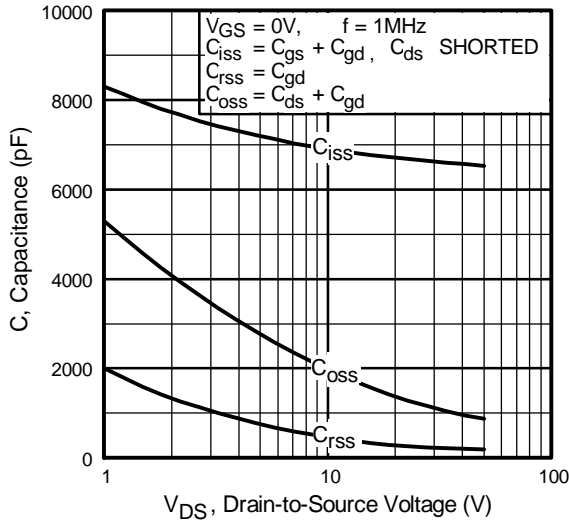


**Fig 3.** Typical Transfer Characteristics

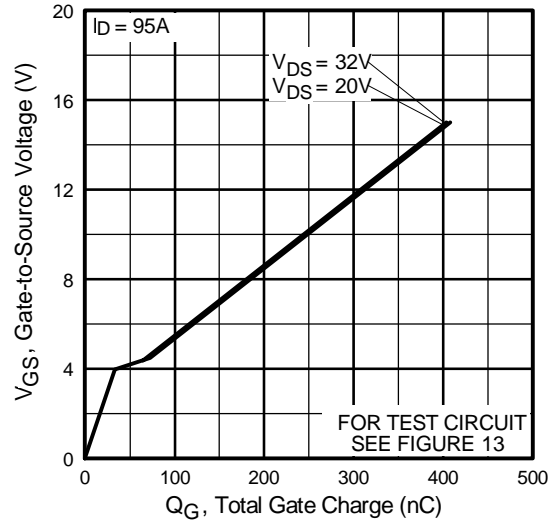


**Fig 4.** Normalized On-Resistance Vs. Temperature

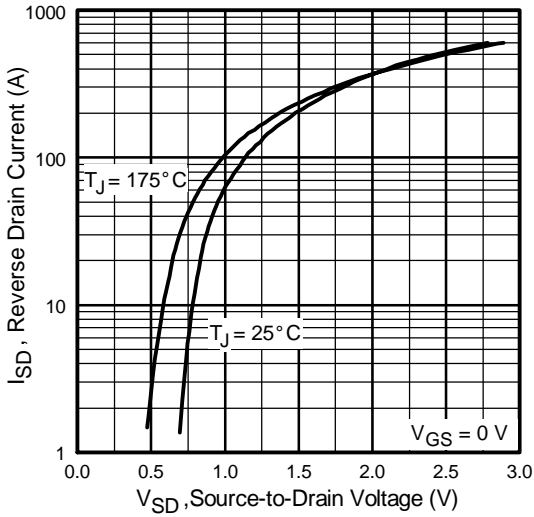
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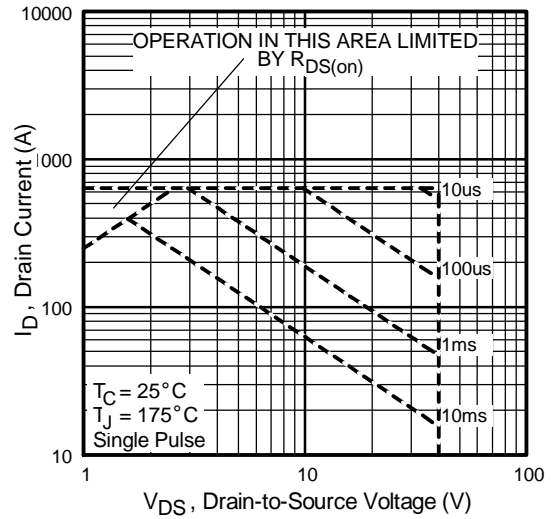
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



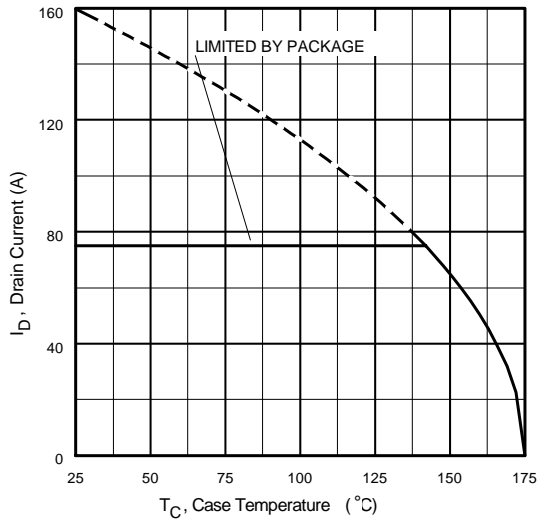
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



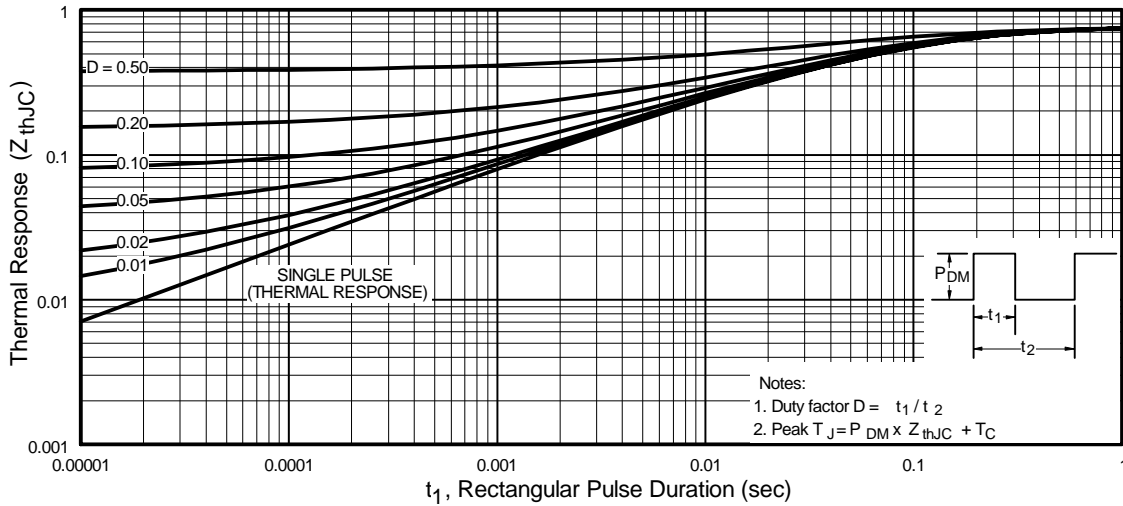
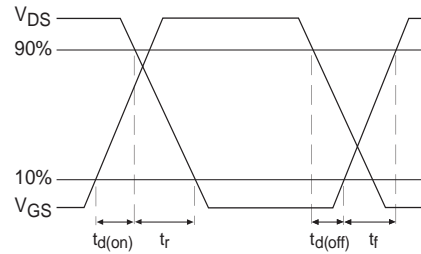
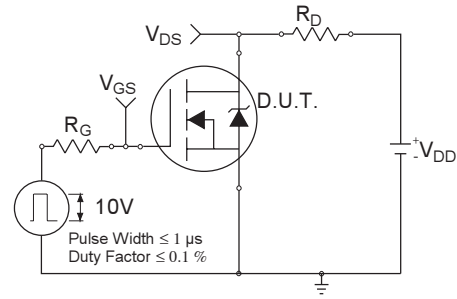
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



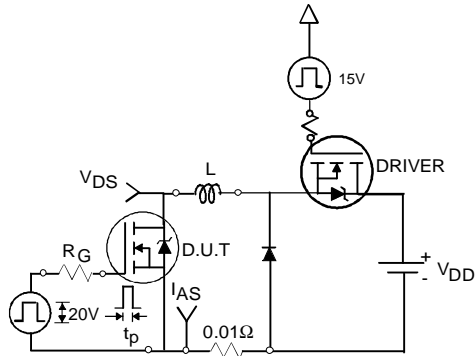
**Fig 9.** Maximum Drain Current Vs. Case Temperature



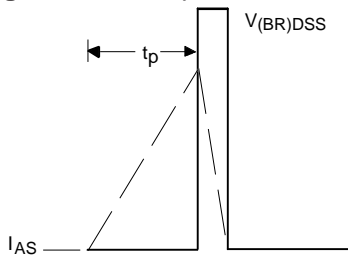
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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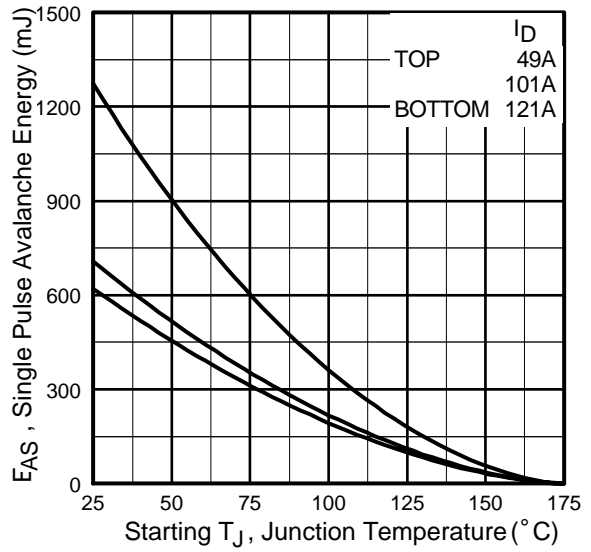
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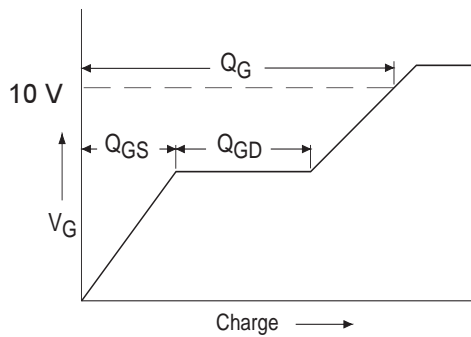
**Fig 12a.** Unclamped Inductive Test Circuit



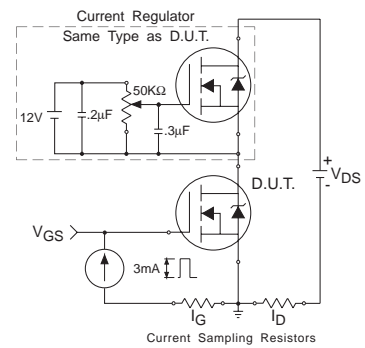
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

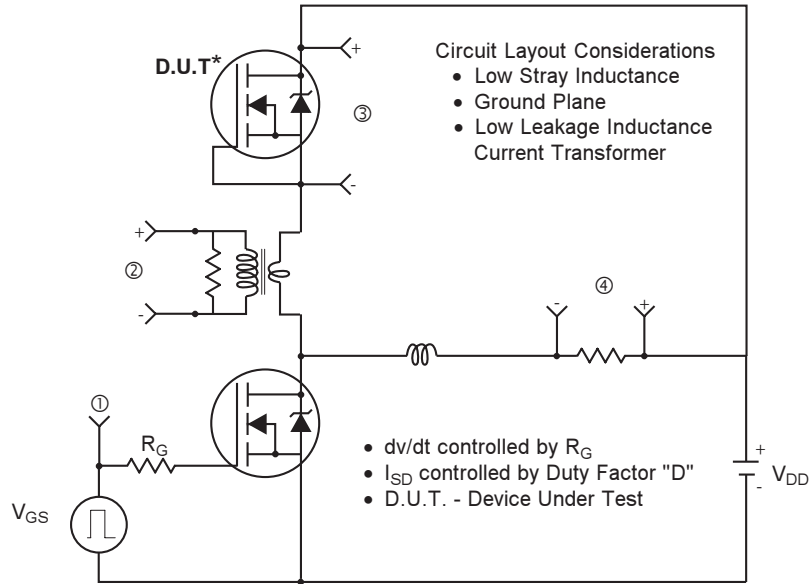


**Fig 13a.** Basic Gate Charge Waveform

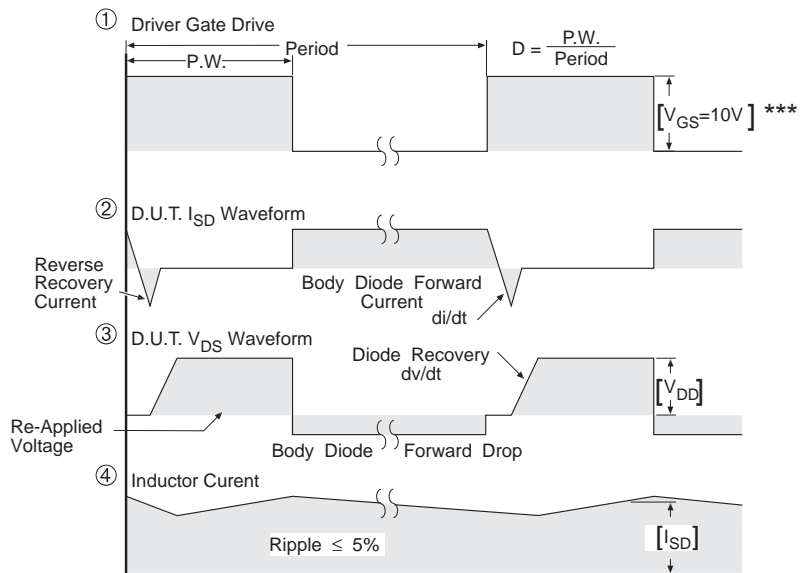


**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

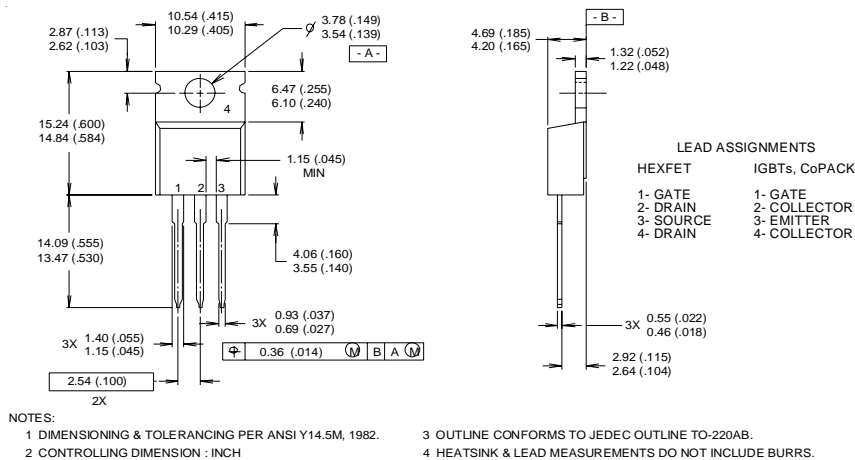
**Fig 14.** For N-channel HEXFET<sup>®</sup> power MOSFETs

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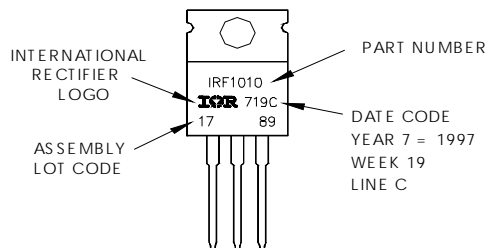
## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line  
 position indicates "Lead-Free"



Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Automotive [Q101] market.  
 Qualification Standards can be found on IR's Web site.

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