IS64LP12832
IS64LP12836, IS64LP25618

128K x 32, 128K x 36, 256K x 18 SYNCHRONOUS PIPELINED STATIC RAM

ADVANCED INFORMATION
JANUARY 2003

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP and 119-pin PBGA package
- Power-down snooze mode
- Power Supply
  + 3.3V V_{DD}
  + 3.3V OR 2.5V V_{DDQ} (I/O)
- Temperature offerings
  Option A1: -40° C to +85° C
  Option A2: -40° C to +105° C
  Option A3: -40° C to +125° C

DESCRIPTION

The *ISSI* IS64LP12832, IS64LP12836, and IS64LP25618 are high-speed synchronous static RAMs designed to provide high-performance memory with burst for high-speed networking and communication applications. IS64LP12832 is organized as 131,072 words by 32 bits. IS64LP12836 is organized as 131,072 words by 36 bits. IS64LP25618 is organized as 262,144 words by 18 bits. The IS64LP12832, IS64LP12836, and IS64LP25618 are fabricated with *ISSI*'s advanced CMOS technology. These devices integrate a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQa, $\overline{BW2}$ controls DQb, $\overline{BW3}$ controls DQc, $\overline{BW4}$ controls DQd, conditioned by $\overline{BWE}$ being LOW. A LOW on $\overline{GW}$ input would cause all bytes to be written.

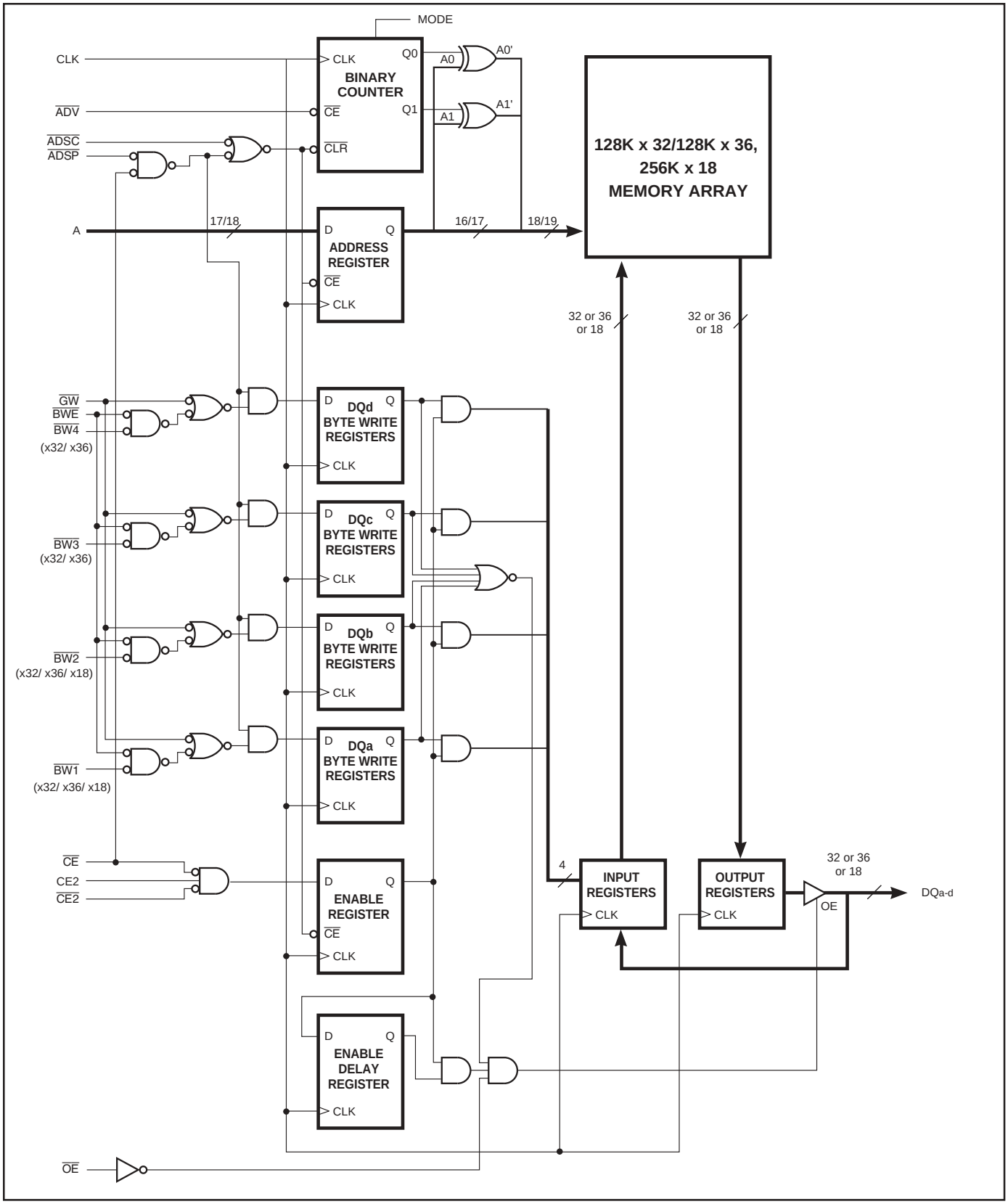
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

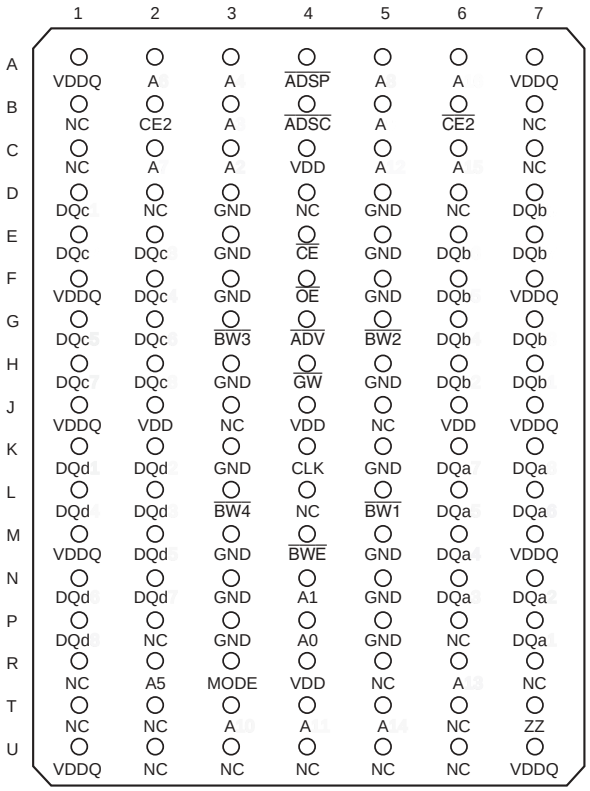
Symbol	Parameter	-166	-150	Units
t_{KQ}	Clock Access Time	3.5	3.8	ns
t_{KC}	Cycle Time	6	6.7	ns
	Frequency	166	150	MHz

BLOCK DIAGRAM

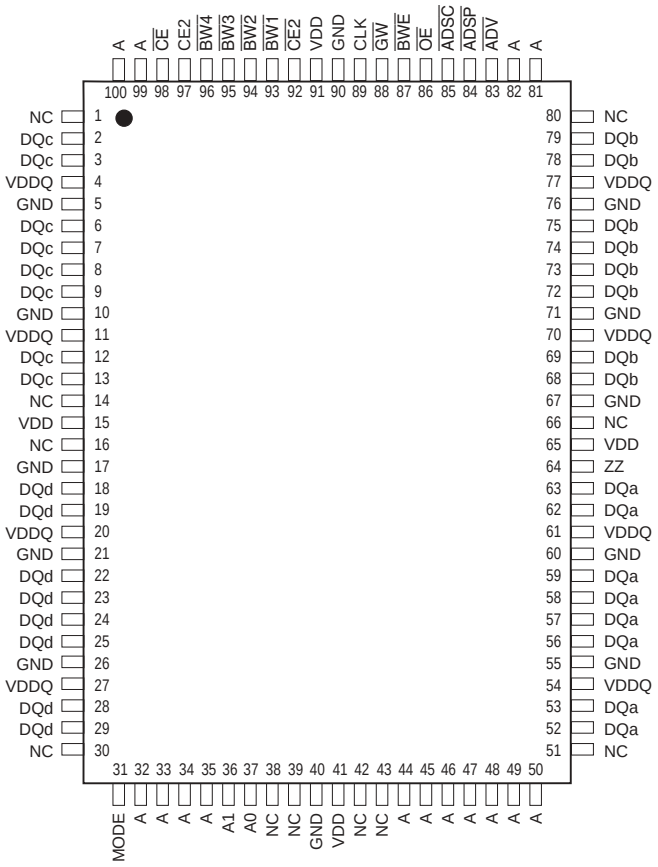


PIN CONFIGURATION

119-pin PBGA (Top View)



100-Pin TQFP



128K x 32

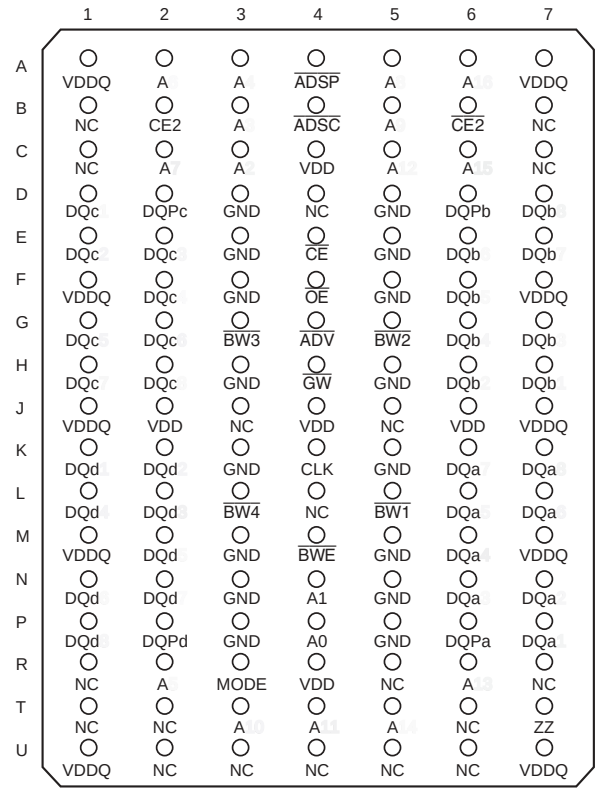
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BW1}$-$\overline{BW4}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

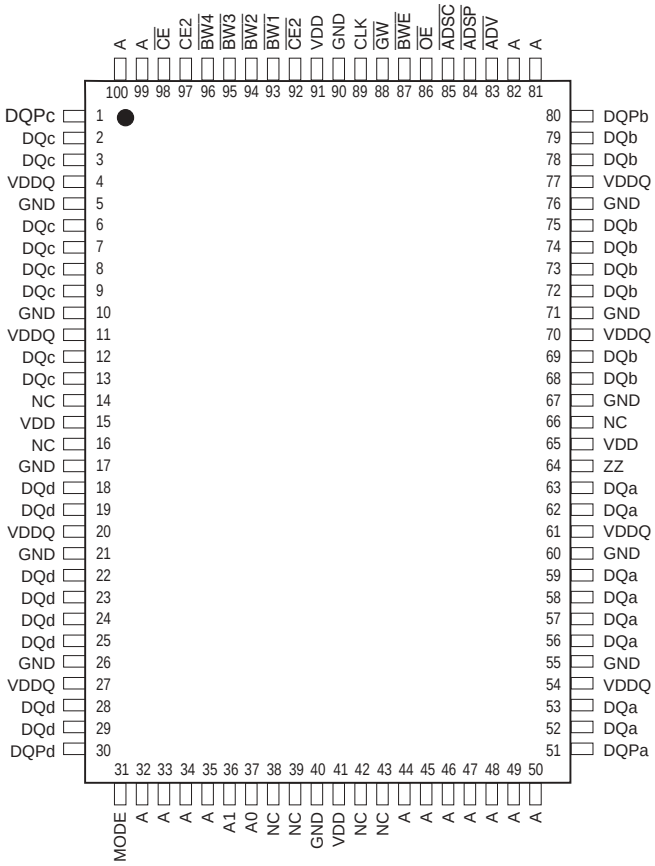
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable

PIN CONFIGURATION

119-pin PBGA (Top View)



100-Pin TQFP



128K x 36

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BW1}$-$\overline{BW4}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

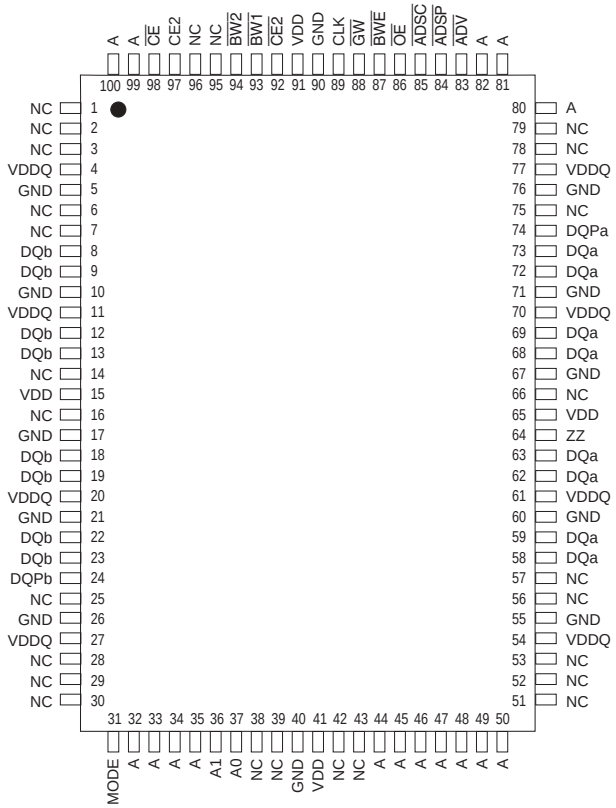
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

119-pin PBGA (Top View)

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{ADSP}$	A	A	VDDQ
B	NC	CE2	A	$\overline{ADSC}$	A	$\overline{CE2}$	NC
C	NC	A	A	VDD	A	A	NC
D	DQb	NC	GND	NC	GND	DQPa	NC
E	NC	DQb	GND	$\overline{CE}$	GND	NC	DQa
F	VDDQ	NC	GND	$\overline{OE}$	GND	DQa	VDDQ
G	NC	DQb	$\overline{BW2}$	$\overline{ADV}$	GND	NC	DQa
H	DQb	NC	GND	$\overline{GW}$	GND	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	GND	CLK	GND	NC	DQa
L	DQb	NC	GND	NC	$\overline{BW1}$	DQa	NC
M	VDDQ	DQb	GND	$\overline{BWE}$	GND	NC	VDDQ
N	DQb	NC	GND	A1	GND	DQa	NC
P	NC	DQPb	GND	A0	GND	NC	DQa
R	NC	A	MODE	VDD	GND	A	NC
T	NC	A	A	NC	A	A	ZZ
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

100-Pin TQFP



256K x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BW1}$-$\overline{BW2}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQb	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V
ZZ	Snooze Enable
DQPa-DQPb	Parity Data I/O

TRUTH TABLE

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	X	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	X	L	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	Q
Read Cycle, Begin Burst	External	L	H	L	H	L	X	Read	X	Q
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	D
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	D
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	D
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	D
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	D

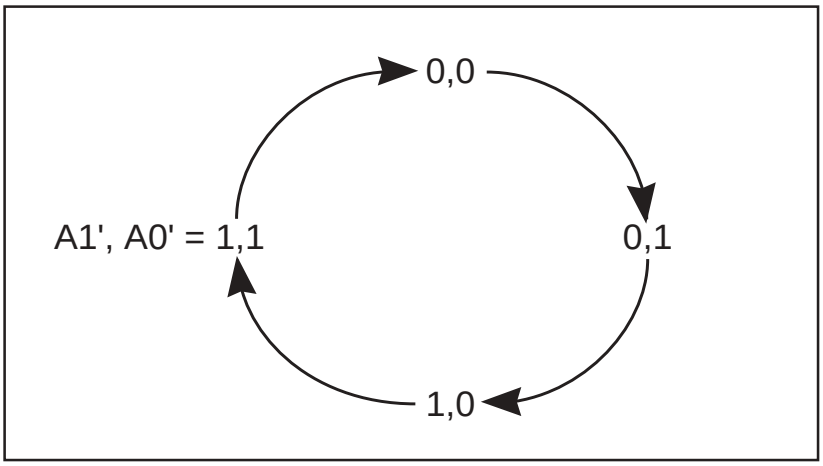
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{DDQ} + 0.3	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	V
V_{DD}	Voltage on V_{DD} Supply Relative to GND	–0.5 to 4.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V_{DD}	3.3V (I/O) V_{DDQ}	2.5V (I/O) V_{DDQ}
A1	–40°C to +85°C	3.3V, +10%, –5%	3.3V, +10%, –5%	2.5V ± 5%
A2	–40°C to +105°C	3.3V, +10%, –5%	3.3V, +10%, –5%	2.5V ± 5%
A3	–40°C to +125°C	3.3V, +10%, –5%	3.3V, +10%, –5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions	2.5V (I/O) Min.	2.5V (I/O) Max.	3.3V (I/O) Min.	3.3V (I/O) Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = 1.0 mA (2.5V)	2.0	—	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	–0.3	0.8	V
I_{LI}	Input Leakage Current	$GND \le V_{IN} \le V_{DD}$	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	$GND \le V_{OUT} \le V_{DDQ}$, $\overline{OE} = V_I$	–5	5	–5	5	µA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-166 Max.	-150 Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, V_{DD} = Max. Cycle Time ≥ t_{KC} min.	A1 A2 A3	290 - 	- 280 290	mA mA
I_{SB}	Standby Current	Device Deselected, V_{DD} = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time ≥ t_{KC} min.	A1 A2 A3	70 - 	- 80 90	mA mA
I_{ZZ}	Power-down Mode Current	ZZ = V_{DD} Clock Running All Inputs ≤ GND + 0.2V or ≥ V_{DD} – 0.2V	A1 A2 A3	15 - 	- 20 25	mA mA

Notes:
1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{DD}.
2. The MODE pin should be tied to V_{DD} or GND. It exhibits ±10 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{DD} – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

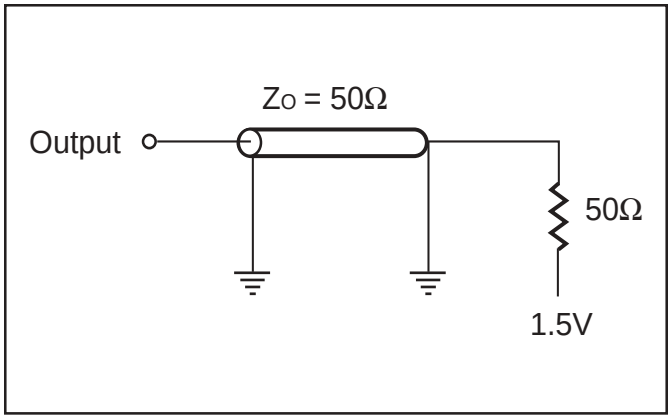


Figure 1

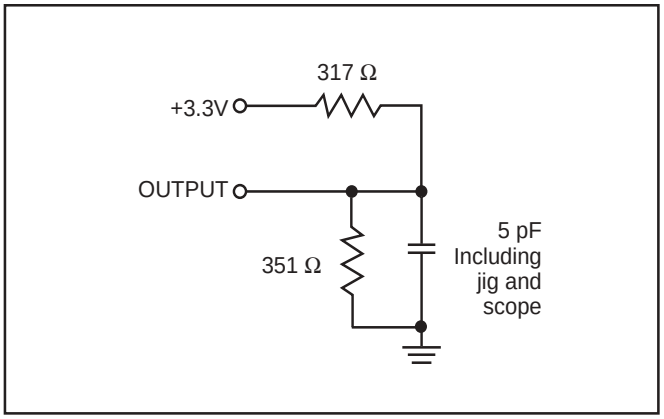


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

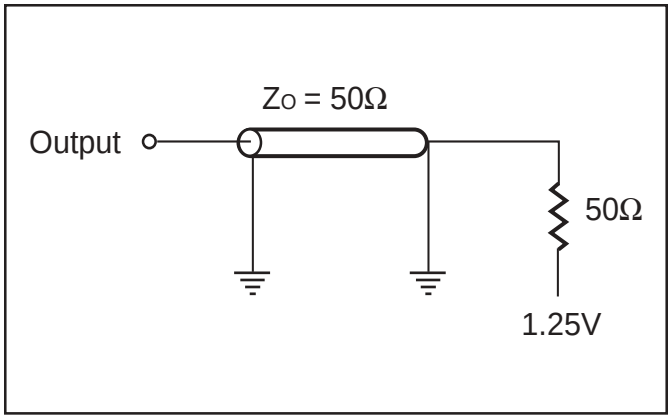


Figure 3

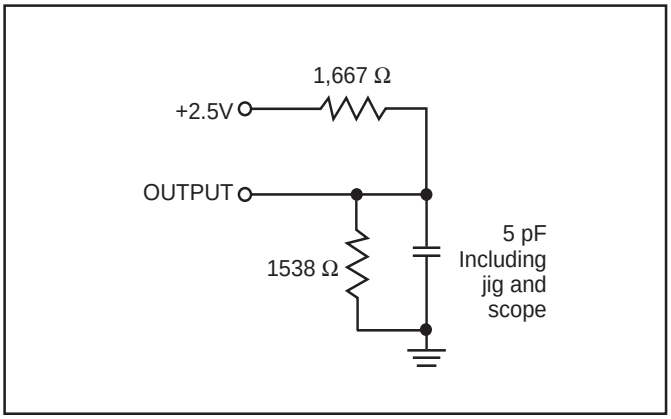


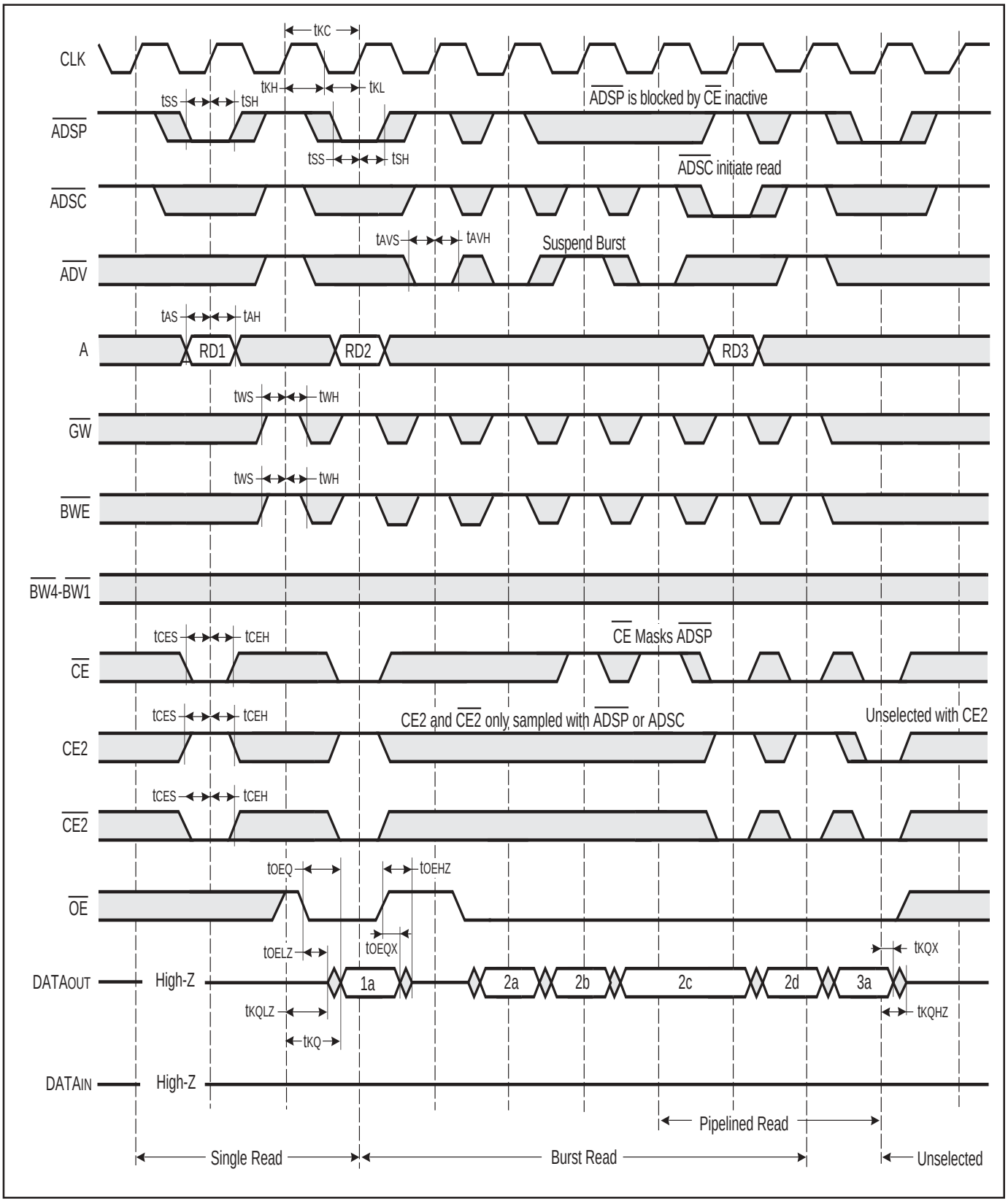
Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-150		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
f_{MAX}[3]	Clock Frequency	—	166	—	150	MHz
t_{KC}[3]	Cycle Time	6.0	—	6.7	—	ns
t_{KH}	Clock High Time	2.4	—	2.6	—	ns
t_{KL}[3]	Clock Low Time	2.4	—	2.6	—	ns
t_{KQ}[3]	Clock Access Time	—	3.5	—	3.8	ns
t_{KQX}[1]	Clock High to Output Invalid	3.0	—	3.0	—	ns
t_{KQLZ}[1,2]	Clock High to Output Low-Z	0	—	0	—	ns
t_{KQHZ}[1,2]	Clock High to Output High-Z	1.5	3.5	1.5	3.5	ns
t_{OEQ}[3]	Output Enable to Output Valid	—	3.8	—	3.8	ns
t_{OEQX}[1]	Output Disable to Output Invalid	0	—	0	—	ns
t_{OELZ}[1,2]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[1,2]	Output Disable to Output High-Z	2.0	3.5	2.0	3.5	ns
t_{AS}[3]	Address Setup Time	2.0	—	2.0	—	ns
t_{SS}[3]	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}[3]	Write Setup Time	1.5	—	1.5	—	ns
t_{CES}[3]	Chip Enable Setup Time	2.0	—	2.0	—	ns
t_{AVS}[3]	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{AH}[3]	Address Hold Time	1.0	—	1.0	—	ns
t_{SH}[3]	Address Status Hold Time	1.0	—	1.0	—	ns
t_{WH}[3]	Write Hold Time	1.0	—	1.0	—	ns
t_{CEH}[3]	Chip Enable Hold Time	1.0	—	1.0	—	ns
t_{AVH}[3]	Address Advance Hold Time	1.0	—	1.0	—	ns

Note:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.
3. Tested with load in Figure 1.

READ/WRITE CYCLE TIMING

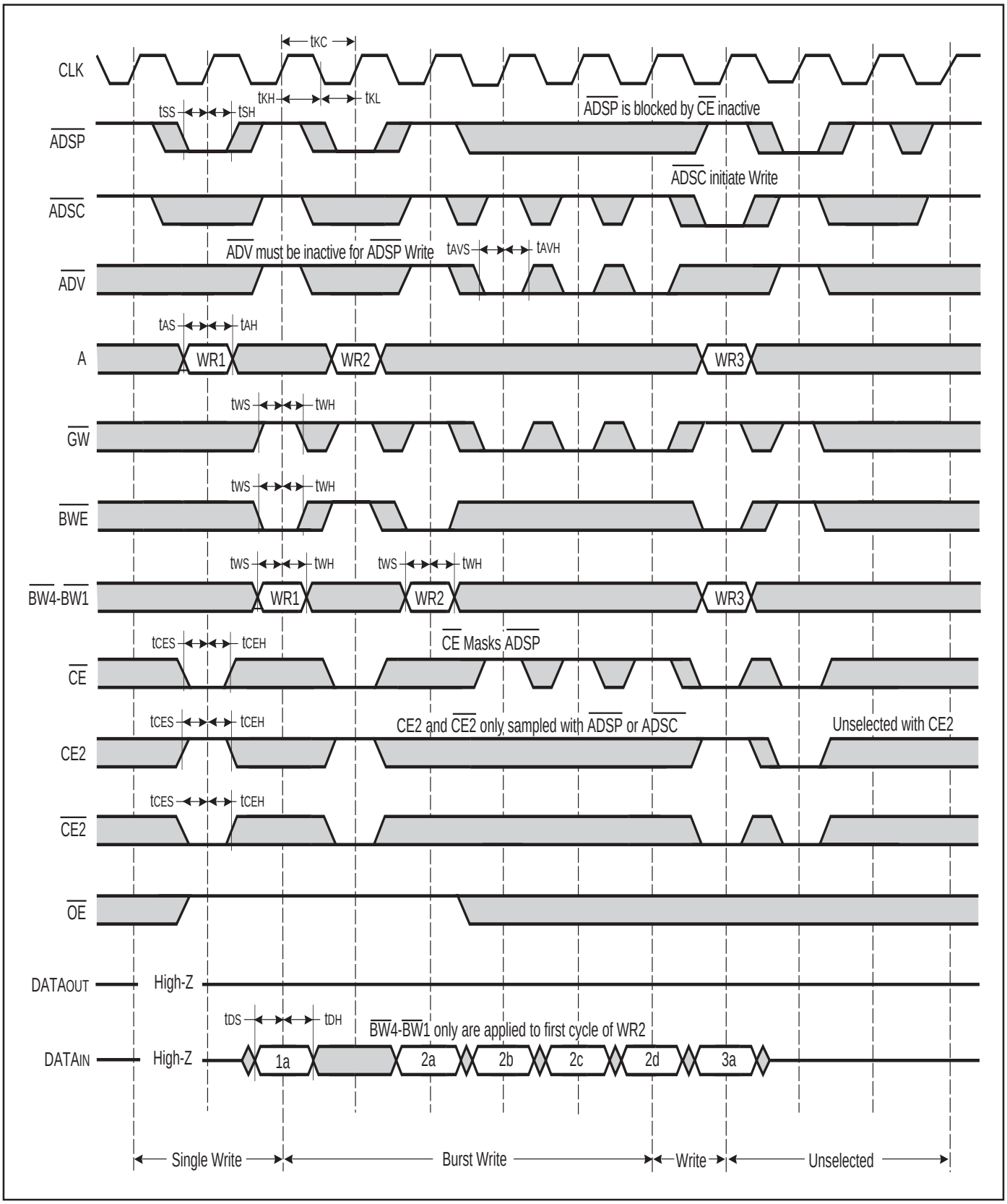


WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

		-166		-150		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{KC}[1]	Cycle Time	6	—	6.7	—	ns
t_{KH}[1]	Clock High Time	2.4	—	2.6	—	ns
t_{KL}[1]	Clock Low Time	2.4	—	2.6	—	ns
t_{AS}[1]	Address Setup Time	2.0	—	2.0	—	ns
t_{SS}[1]	Address Status Setup Time	1.5	—	1.5	—	ns
t_{WS}[1]	Write Setup Time	1.5	—	1.5	—	ns
t_{DS}[1]	Data In Setup Time	1.5	—	1.5	—	ns
t_{CES}[1]	Chip Enable Setup Time	2.0	—	2.0	—	ns
t_{AVS}[1]	Address Advance Setup Time	1.5	—	1.5	—	ns
t_{AH}[1]	Address Hold Time	1.0	—	1.0	—	ns
t_{SH}[1]	Address Status Hold Time	1.0	—	1.0	—	ns
t_{DH}[1]	Data In Hold Time	1.0	—	1.0	—	ns
t_{WH}[1]	Write Hold Time	1.0	—	1.0	—	ns
t_{CEH}[1]	Chip Enable Hold Time	1.0	—	1.0	—	ns
t_{AVH}[1]	Address Advance Hold Time	1.0	—	1.0	—	ns

Note:
1. Tested with load in Figure 1.

WRITE CYCLE TIMING



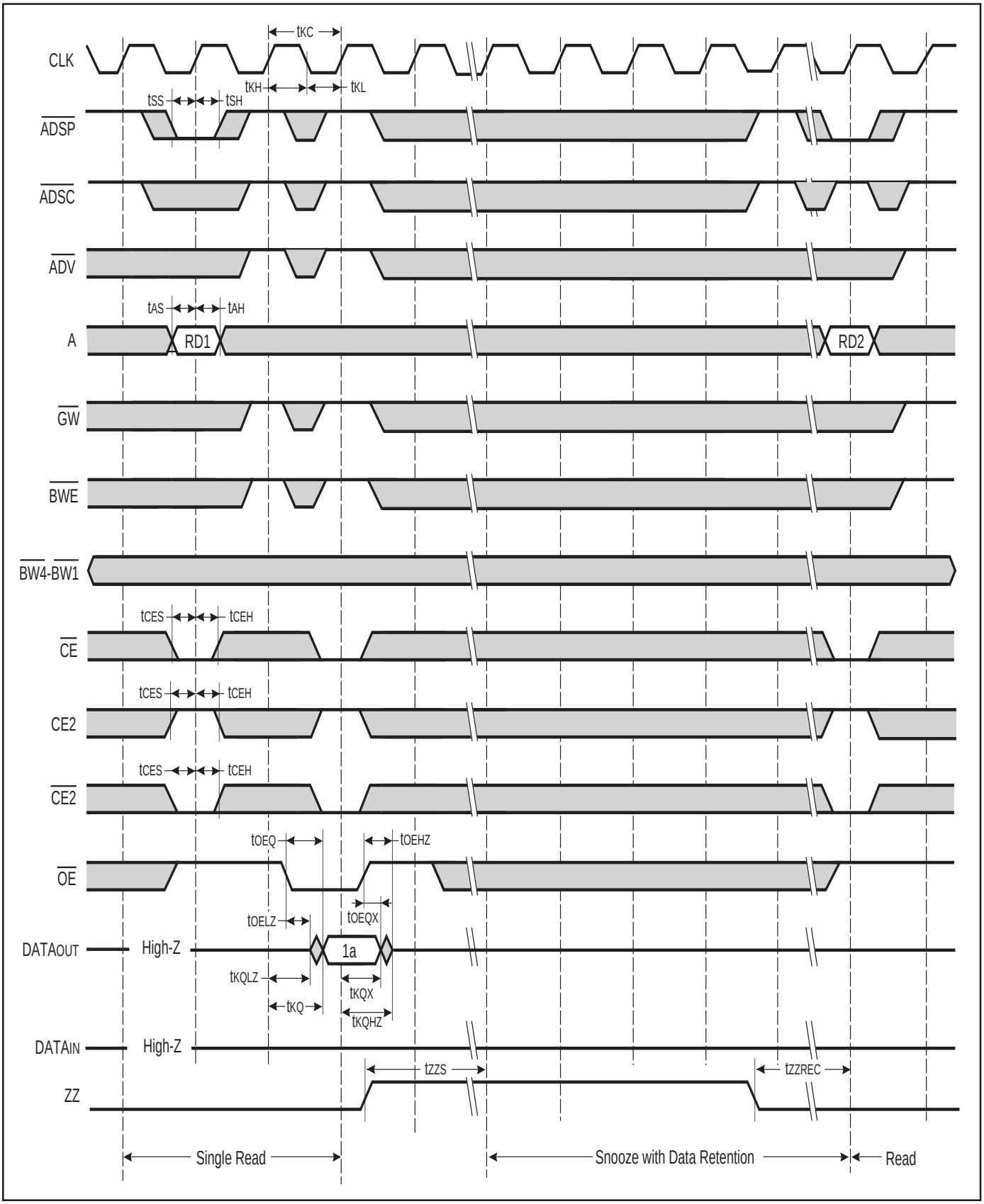
SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS

(Over Operating Range)

Symbol	Parameter	-166 Min.	-166 Max.	-150 Min.	-150 Max.	Unit
t_{KC}[3]	Cycle Time	6	—	6.7	—	ns
t_{KH}[3]	Clock High Time	2.4	—	2.6	—	ns
t_{KL}[3]	Clock Low Time	2.4	—	2.6	—	ns
t_{KQ}[3]	Clock Access Time	—	3.5	—	3.8	ns
t_{KQX}[1]	Clock High to Output Invalid	1.5	—	1.5	—	ns
t_{KQLZ}[1,2]	Clock High to Output Low-Z	0	—	0	—	ns
t_{KQHZ}[1,2]	Clock High to Output High-Z	1.5	3.5	1.5	3.5	ns
t_{OEQ}[3]	Output Enable to Output Valid	—	3.5	—	3.5	ns
t_{OEQX}[1]	Output Disable to Output Invalid	0	—	0	—	ns
t_{OELZ}[1,2]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[1,2]	Output Disable to Output High-Z	2	3.5	2	3.5	ns
t_{AS}[3]	Address Setup Time	2.0	—	2.0	—	ns
t_{SS}[3]	Address Status Setup Time	1.5	—	1.5	—	ns
t_{CES}[3]	Chip Enable Setup Time	2.0	—	2.0	—	ns
t_{AH}[3]	Address Hold Time	1.0	—	1.0	—	ns
t_{SH}[3]	Address Status Hold Time	1.0	—	1.0	—	ns
t_{CEH}[3]	Chip Enable Hold Time	1.0	—	1.0	—	ns
t_{ZZS}	ZZ Standby	2	—	2	—	cyc
t_{ZZREC}	ZZ Recovery	2	—	2	—	cyc

Notes:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION

Temperature Range (A1): –40°C to +85°C

Speed	Order Part No.	Organization	Package
166 MHz	IS64LP12832-166TQA1	128Kx32	TQFP
	IS64LP12832-166BA1	128Kx32	PBGA
	IS64LP12836-166TQA1	128Kx36	TQFP
	IS64LP12836-166BA1	128Kx36	PBGA
	IS64LP25618-166TQA1	256Kx18	TQFP
	IS64LP25618-166BA1	256Kx18	PBGA

Temperature Range (A2): –40°C to +105°C

Speed	Order Part No.	Organization	Package
150 MHz	IS64LP12832-150TQA2	128Kx32	TQFP
	IS64LP12832-150BA2	128Kx32	PBGA
	IS64LP12836-150TQA2	128Kx36	TQFP
	IS64LP12836-150BA2	128Kx36	PBGA
	IS64LP25618-150TQA2	256Kx18	TQFP
	IS64LP25618-150BA2	256Kx18	PBGA

Temperature Range (A3): –40°C to +125°C

Speed	Order Part No.	Organization	Package
150 MHz	IS64LP12832-150TQA3	128Kx32	TQFP
	IS64LP12832-150BA3	128Kx32	PBGA
	IS64LP12836-150TQA3	128Kx36	TQFP
	IS64LP12836-150BA3	128Kx36	PBGA
	IS64LP25618-150TQA3	256Kx18	TQFP
	IS64LP25618-150BA3	256Kx18	PBGA