IXYS

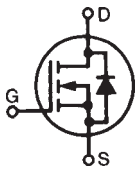
Advance Technical Information

PolarHT™ HiPerFET IXFR 140N20P
Power MOSFET
ISOPLUS247™

(Electrically Isolated Back Surface)

N-Channel Enhancement Mode
Avalanche Rated; Fast Intrinsic Diode

V_{DSS} = 200 V
I_{D25} = 75 A
$R_{DS(on)}$ = 22 mΩ
t_{rr} ≤ 150 ns



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 175°C	200	V
V_{DGR}	T_J = 25°C to 175°C; R_{GS} = 1 MΩ	200	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	T_C = 25°C	75	A
I_{DRMS}	External lead current limit	75	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	280	A
I_{AR}	T_C = 25°C	60	A
E_{AR}	T_C = 25°C	100	mJ
E_{AS}	T_C = 25°C	4	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/μs, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$, R_G = 4 Ω	10	V/ns
P_D	T_C = 25°C	300	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
F_C	Mounting force	20..120/4.5..20	N/lb.
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA	200			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	2.5		5.0	V
I_{GSS}	V_{GS} = ± 20 V_{DC}, V_{DS} = 0			± 200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			25	μA
	T_J = 150°C			250	μA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 70 A			22	mΩ
	V_{GS} = 15 V, I_D = 140A		17		mΩ
	Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %				

ISOPLUS247 (IXFR)
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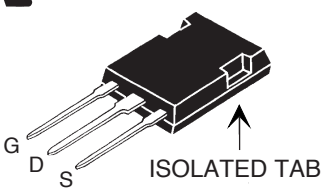


G = Gate D = Drain
S = Source

Features

- International standard isolated package
- UL recognized package
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic diode

Advantages

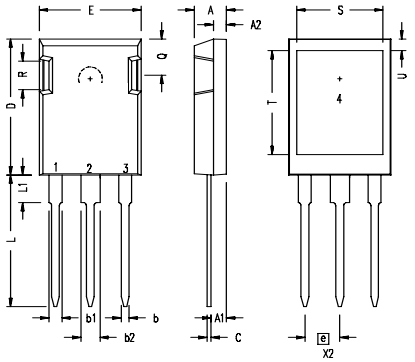
- Easy to mount
- Space savings
- High power density

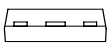
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10 V; I_D = 70 A, pulse test	50	84		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		7500		pF
C_{oss}			1800		pF
C_{rss}			280		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 70 A R_G = 3.3 Ω (External)		30		ns
t_r			35		ns
$t_{d(off)}$			150		ns
t_f			90		ns
$Q_{g(on)}$	V_{GS}= 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 70 A		240		nC
Q_{gs}			50		nC
Q_{gd}			100		nC
R_{thJC}				0.5	K/W
R_{thCK}			0.15		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			90	A
I_{SM}	Repetitive			280	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle d ≤ 2 %			1.5	V
t_{rr}	I_F = 25 A, -di/dt = 100 A/μs			150	ns
Q_{RM}	V_R = 100 V, V_{GS} = 0 V		0.6		μC

ISOPLUS 247 OUTLINE





1-Gate 2-Drain
3-Source 4-No connection

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	.244
R	4.32	4.83	.170	.190

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated objective result. Ixys reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ 25ºC

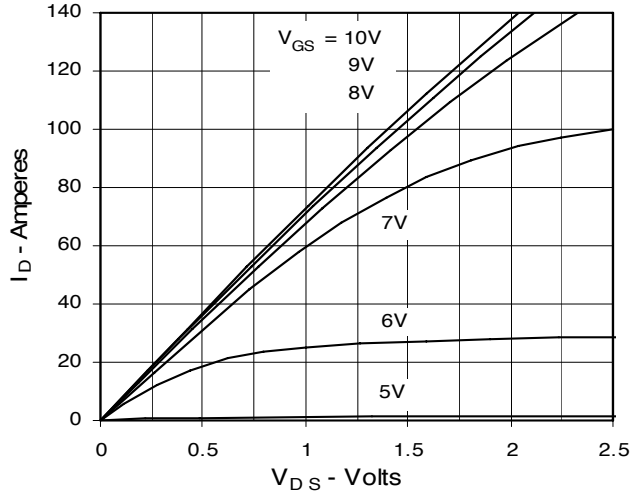


Fig. 2. Extended Output Characteristics @ 25ºC

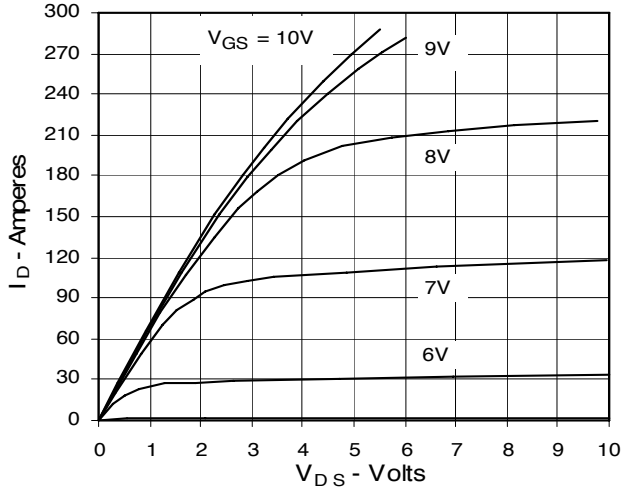


Fig. 3. Output Characteristics @ 150ºC

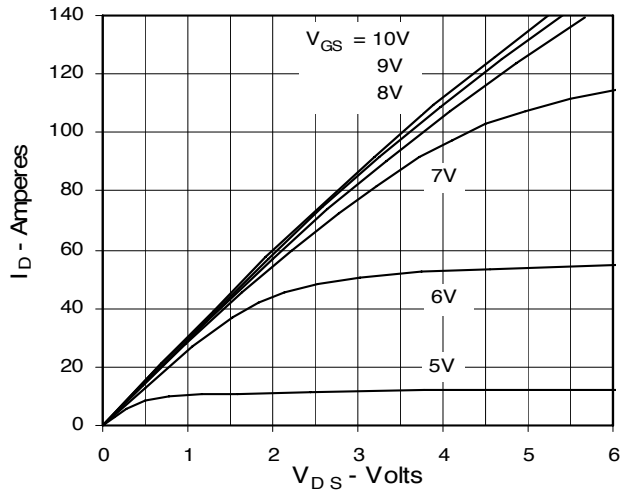


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 70A Value vs. Junction Temperature

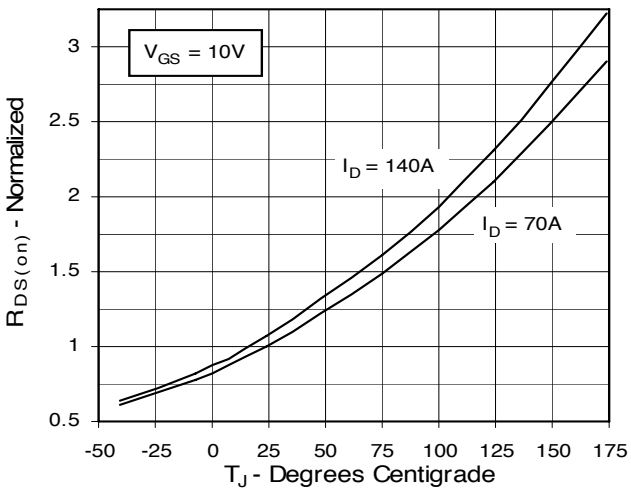


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 70A Value vs. Drain Current

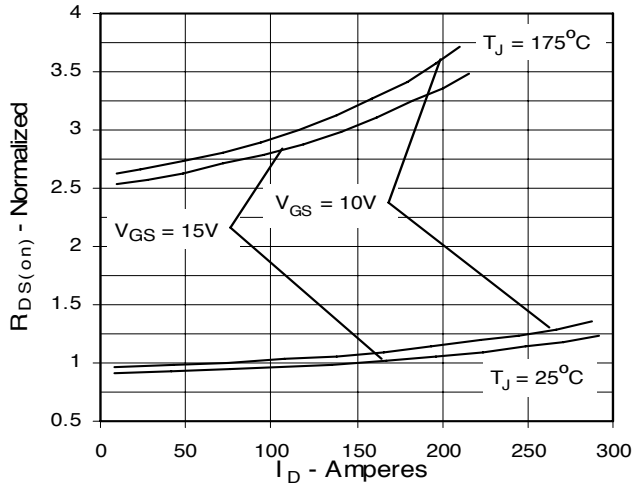


Fig. 6. Drain Current vs. Case Temperature

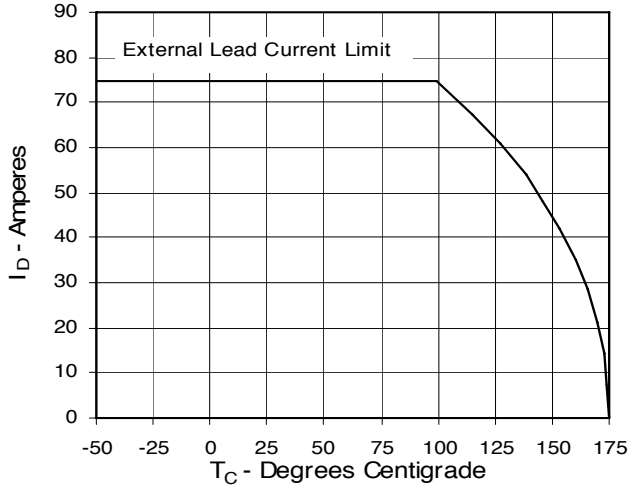


Fig. 7. Input Admittance

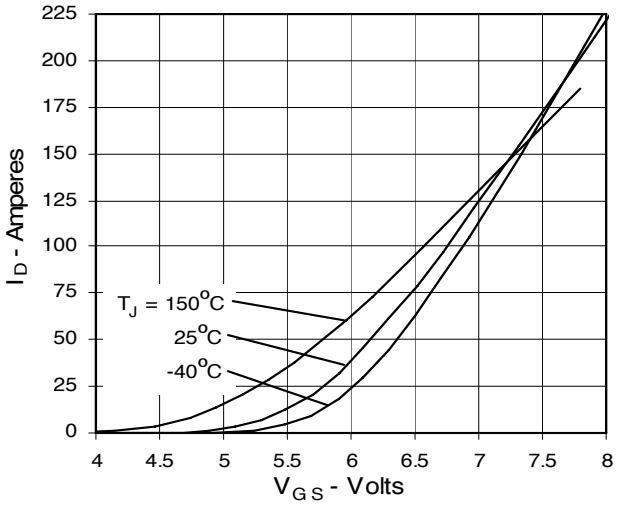


Fig. 8. Transconductance

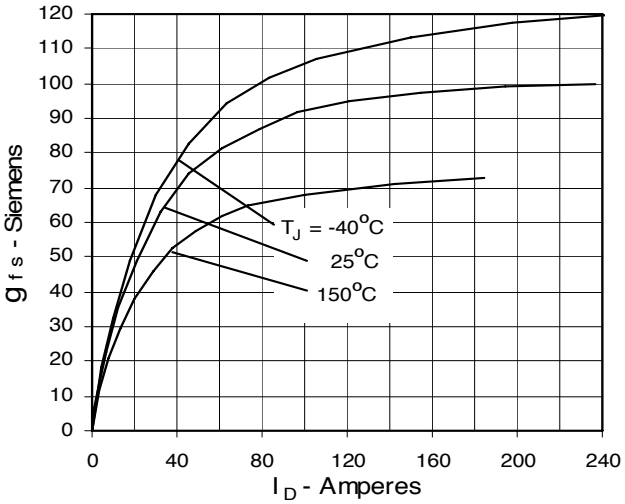


Fig. 9. Source Current vs. Source-To-Drain Voltage

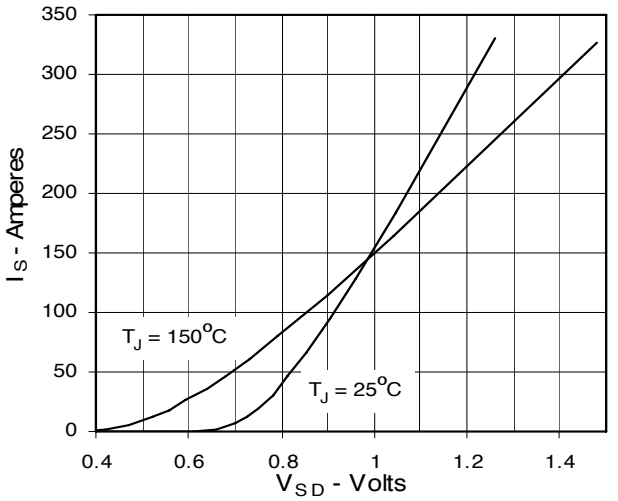


Fig. 10. Gate Charge

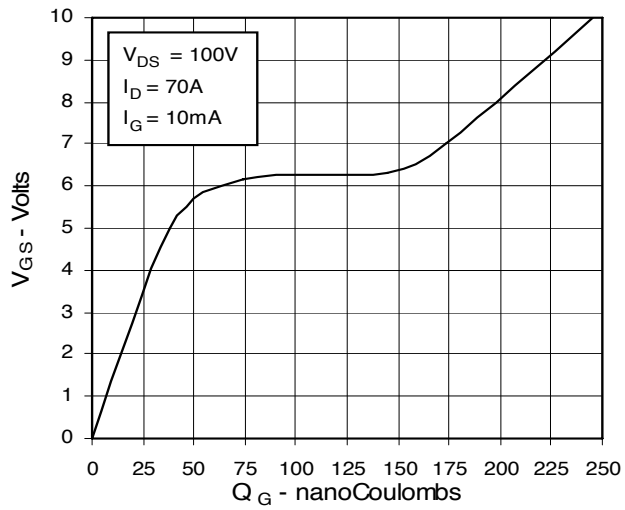


Fig. 11. Capacitance

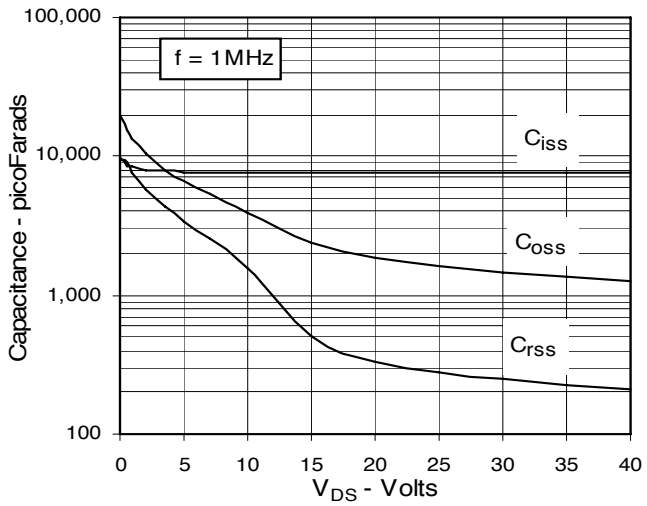


Fig. 12. Forward-Bias Safe Operating Area

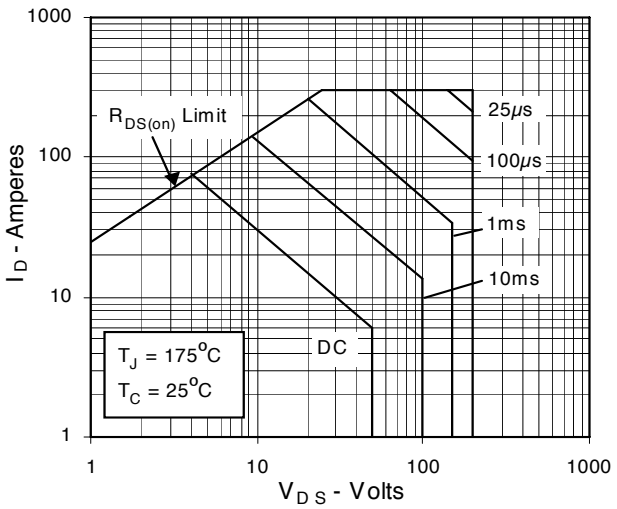


Fig. 13. Maximum Transient Thermal Resistance