Flip Chip Ball Grid Array (FPBGA) Package Family

Overview

LSI Logic's FPBGA packages offer flip chip die interconnect, and support leadcounts in excess of 1700 to target high performance, high pin count applications. LSI Logic is the first company to qualify a flip chip package using organic laminate substrates. Organic laminate substrates have better performance through copper interconnect and also have a lower dielectic constant. The FPBGA is lower in cost than conventional ceramic or the latest glass ceramic materials.

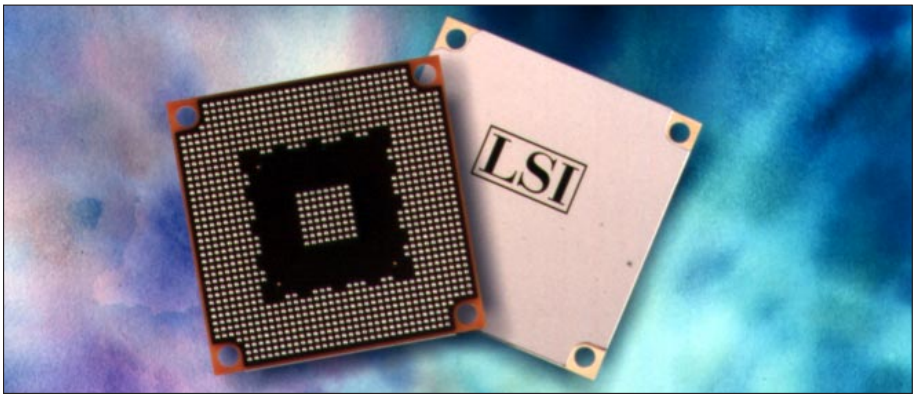
Description

Flip chip packages differ from the traditional wire bonded packages in that the silicon chip does not have a ring of wire bond pads around its perimeter. Instead, the chip is covered across its top surface by a matrix of solder bumps. The chip is then "flipped" over and attached to the package substrate using solder reflow techniques.

FPBGA provides the highest electrical performance available today through the elimination of the wire bond, separate core and I/O power and ground, reference planes, and the lowest available dielectric constant.

In addition, this innovative package family has excellent thermal performance. The backside of the flipped die is attached directly to a heatspreader which covers the entire package. If necessary, a heatsink can be added. The organic laminate substrate has a Thermal Coefficient of Expansion (TCE) which is a much closer match to PCB material than glass ceramic substrates. This enables package body sizes of up to 45mm per side to be available to the designer. Conventional ceramic BGA packages are limited to 35mm per side.

LSI Logic is offering a choice of two different organic substrate materials, namely BT laminate and Microlam™ buildup. The Microlam buildup offers the benefit of finer bump and interconnect feature sizes.



Designed for maximum electrical performance

Features

- Stripline I/O traces between power and ground planes
- Low inductance power and ground planes
- Core voltage and ground isolated and routed directly to solder balls under die
- Segmented power planes
- 100% differential or single-ended I/Os
- Ratio of signals:power:ground is 4:1:1
- Low dielectric constant in organic laminate materials

Benefits

- Controlled impedance I/O traces
- High integrity core power supplies with thermal path to PCB
- Multiple low inductance I/O voltages
- Suited for high-speed differential signals up to 2.4 Gbit/s
- Low power supply noise
- Reduced cross-talk
- Improved signal propagation delay

Designed for maximum thermal performance

Features

- Copper heatspreader covers entire package
- Direct thermal contact to flip chip die

Benefits

- Heatsink can be attached for increased performance
- Low thermal impedance path from chip to ambient surroundings

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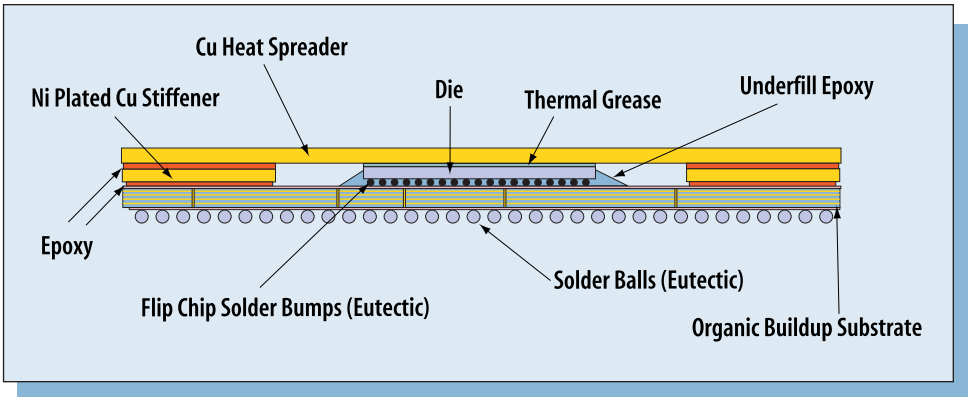
FPBGA Package Family

Ball Count	Body Size	#I/O	Array	Vss	Vdd	VssC	VddC
788	31	504	30 x 30	124	124	18	18
960	35	600	34 x 34	148	148	32	32
1157	40	720	39 x 39	176	180	41	40
1413	40	864	39 x 39	212	216	61	60
1728	45	1024	44 x 44	252	256	98	98

Complete Packaging Portfolio

The design and construction of LSI's multilayer laminate flip chip package provides superior electrical and thermal characteristics for a wide range of performance leading and high lead count applications in computing, networking and telecommunications.



Laminate Flip Chip Materials & Construction

LSI Logic's packaging portfolio offers a wide range of application focused packages ranging from low-cost packages for mainstream applications to Ball Grid Arrays optimized for the most demanding applications. These products are designed to meet a wide variety of thermal and electrical performance requirements with a focus on die size optimization, high I/O utilization, surface mount capability, and high reliability.

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Order No. B20022
599.1K.CM.L – Printed in USA