3-BIT SCANNABLE REGISTER

FEATURES

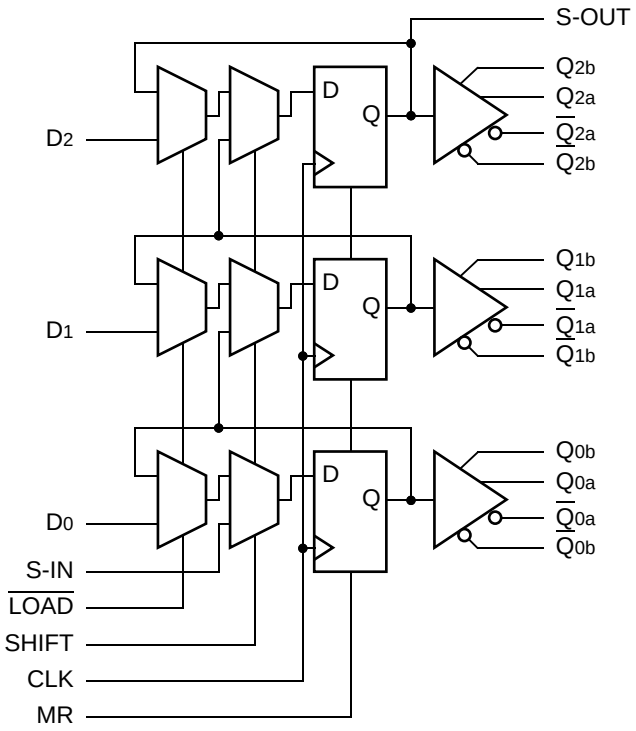
- **Scannable version E112 driver**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **1025ps max. CLK to Output**
- **Dual differential outputs**
- **Master Reset**
- **Internal 75KΩ input pull-down resistors**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Fully compatible with Motorola MC10E/100E212**
- **Available in 28-pin PLCC package**

DESCRIPTION

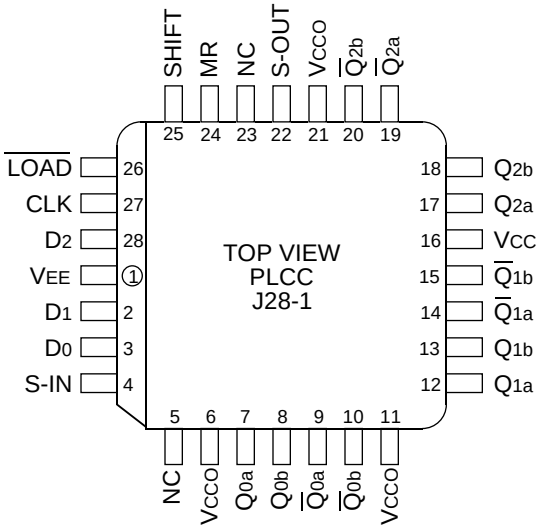
The SY10/100E212 are scannable registered ECL drivers typically used as fan-out memory address drivers for ECL cache driving. In a VLSI array-based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0 – D_2	Data Inputs
S-IN	Scan Input
$\overline{LOAD}$	LOAD/HOLD Control
SHIFT	Scan Control
CLK	Clock
MR	Master Reset
S-OUT	Scan Output
Q[0:2]a, Q[0:2]b	True Outputs
$\overline{Q}$[0:2]a, $\overline{Q}$[0:2]b	Inverting Outputs
V_{CCO}	V_{CC} to Output

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Issue Date: February, 1998

TRUTH TABLE

$\overline{\text{LOAD}}$	SHIFT	MR	Mode
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	80	96	—	80	96	—	80	96		
	100E	—	80	96	—	80	96	—	92	110		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	575	800	1025	575	800	1025	575	800	1025		
	MR	575	800	1025	575	800	1025	575	800	1025		
	CLK to S-OUT	575	800	1025	575	800	1025	575	800	1025		
t_S	Set-up Time										ps	—
	D	175	25	—	175	25	—	175	25	—		
	$\overline{\text{SHIFT}}$	150	–50	—	150	–50	—	150	–50	—		
	$\overline{\text{LOAD}}$	225	50	—	225	50	—	225	50	—		
	S-IN	150	–50	—	150	–50	—	150	–50	—		
t_H	Hold Time										ps	—
	D	250	25	—	250	25	—	250	25	—		
	$\overline{\text{SHIFT}}$	300	100	—	300	100	—	300	100	—		
	$\overline{\text{LOAD}}$	225	0	—	225	0	—	225	0	—		
	S-IN	300	100	—	300	100	—	300	100	—		
t_{RR}	Reset Recovery	600	350	—	600	350	—	600	350	—	ps	—
t_{skew}	Within-Device Skew	—	100	—	—	100	—	—	100	—	ps	1
t_{skew}	Within-Gate Skew	—	50	—	—	50	—	—	50	—	ps	2
t_r t_f	Rise/Fall Times 20% to 80%	275	425	650	275	425	650	275	425	650	ps	—

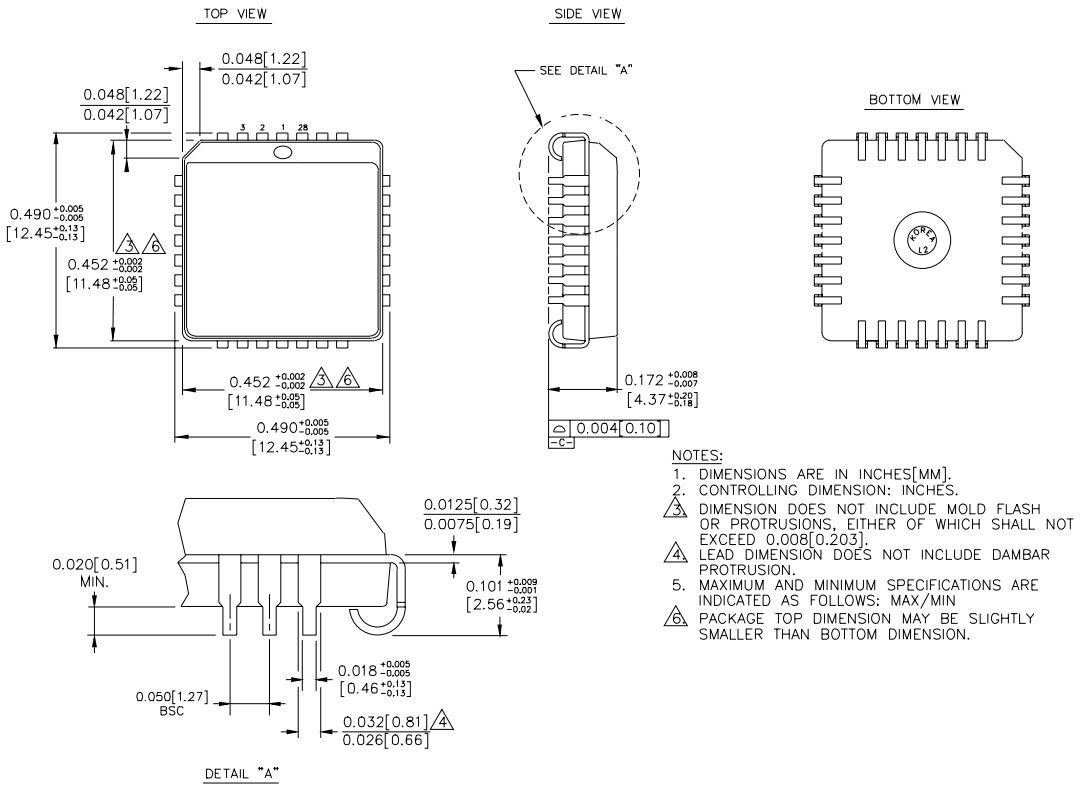
NOTES:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E212JC	J28-1	Commercial
SY10E212JCTR	J28-1	Commercial
SY100E212JC	J28-1	Commercial
SY100E212JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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