18Mb DDRII CIO SRAM 4-WORD BURST

MT57W2MH8J
MT57W1MH18J
MT57W512H36J

Features

- DLL circuitry for accurate output data placement
- Pipelined, double data rate operation
- Common data input/output bus
- Fast clock to valid data times
- Full data coherency, providing most current data
- Four-tick burst for reduced-address frequency
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two output clocks (C and C#) for precise flight time and clock skew matching—clock and data delivered together to receiving device
- Optional-use echo clocks (CQ and CQ#) for flexible receive data synchronization
- Simple control logic for easy depth expansion
- Internally self-timed, registered writes
- Core VDD = 1.8V (±0.1V); I/O VDDQ = 1.5V to VDD (±0.1V) HSTL
- Clock-stop capability with µs restart
- 13mm x 15mm, 1mm pitch, 11 x 15 grid FBGA package
- User-programmable impedance output
- JTAG boundary scan

Options

Options	Marking[1]
• Clock Cycle Timing	
3ns (333 MHz)	-3
3.3ns (300 MHz)	-3.3
4ns (250 MHz)	-4
5ns (200 MHz)	-5
6ns (167 MHz)	-6
7.5ns (133 MHz)	-7.5
• Configurations	
2 Meg x 8	MT57W2MH8J
1 Meg x 18	MT57W1MH18J
512K x 36	MT57W512H36J
• Package	
165-ball, 13mm x 15mm FBGA	F
• Operating Temperature Range	
Commercial (0°C ≤ T_A ≤ +70°C)	None

NOTE:

1. A Part Marking Guide for the FBGA devices can be found on Micron's Web site—http://www.micron.com/numberguide

Figure 1: 165-Ball FBGA

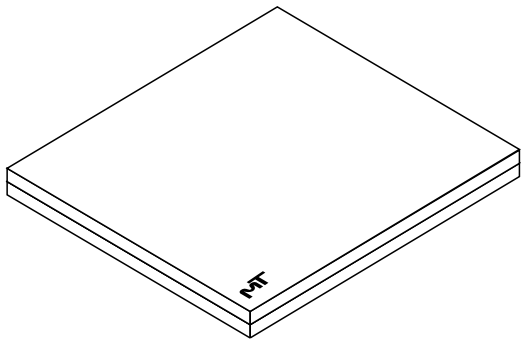


Table 1: Valid Part Numbers

PART NUMBER	DESCRIPTION
MT57W2MH8JF-xx	2 Meg x 8, DDRIIb4 FBGA
MT57W1MH18JF-xx	1 Meg x 18, DDRIIb4 FBGA
MT57W512H36JF-xx	512K x 36, DDRIIb4 FBGA

General Description

The Micron® DDRII synchronous, pipelined burst SRAM employs high-speed, low-power CMOS designs using an advanced 6T CMOS process.

The DDR SRAM integrates an SRAM core with advanced synchronous peripheral circuitry and a burst counter. All synchronous inputs pass through registers controlled by an input clock pair (K and K#) and are latched on the rising edge of K and K#. The synchronous inputs include all addresses, all data inputs, active LOW load (LD#), read/write (R/W#), and active LOW byte writes or nibble writes (BWx# or NWx#). Write data is registered on the rising edges of both K and K#. Read data is driven on the rising edge of C and C#, if provided, or on the rising edge of K and K# if C and C# are not provided.

Asynchronous inputs include impedance match (ZQ). Synchronous data outputs (Q, sharing the same physical balls as the data inputs D) are tightly matched

to the output data clocks C and C#, eliminating the need for separately capturing data from each individual DDR SRAM in the system design.

Additional write registers are incorporated to enhance pipelined WRITE cycles and reduce READ-to-WRITE turnaround time. WRITE cycles are self-timed.

Four balls are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK), and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use JEDEC-standard 1.8V I/O levels to shift data during this testing mode of operation.

The device can be used in HSTL systems by supplying an appropriate reference voltage (VREF). The device is ideally suited for applications requiring very rapid data transfer by operation in data-doubled mode. The device is also ideal in applications requiring the cost benefits of pipelined CMOS SRAMs and the reduced READ-to-WRITE turnaround times of Late Write SRAMs.

The SRAM operates from a 1.8V power supply, and all inputs and outputs are HSTL-compatible. The device is ideally suited for cache, network, telecom, DSP, and other applications that benefit from a very wide, high-speed data bus.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

DDR Operation

The DDR SRAM enables high performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation. At slower frequencies, the DDR SRAM requires a single no-operation (NOP) cycle when transitioning from a READ to a WRITE cycle. At higher frequencies, a second NOP cycle may be required to prevent bus contention. NOP cycles are not required when switching from a WRITE to a READ.

If a READ occurs after a WRITE cycle, address and data for the write are stored in registers. The write information must be stored because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next WRITE cycle occurs. On the first WRITE cycle after the READ(s), the stored data from the earlier WRITE will be written into the SRAM array. This is called a posted write.

A read can be made immediately to an address even if that address was written in the previous cycle. During this READ cycle, the SRAM array is bypassed, and data is read instead from the data register storing the recently written data. This is transparent to the user. This feature facilitates system data coherency.

The DDR SRAM differs in some ways from its predecessor, the Claymore DDR SRAM. Single data rate operation is not supported, hence, no SD/DD# ball is provided. Only bursts of four are supported. The need for echo clocks is reduced or eliminated by the two single-ended input clocks (C and C#), although tightly controlled echo clocks (CQ and CQ#) are provided. The SRAM synchronizes its output data to these data clock rising edges, if provided. No differential clocks are used in this device. This clocking scheme provides greater system tuning capability than Claymore SRAMs and reduces the number of input clocks required by the bus master.

PARTIAL WRITE Operations

BYTE WRITE operations are supported, except for x8 devices in which nibble write is supported. The active LOW write controls, BWx# (NWx#), are registered coincident with their corresponding data. This feature can eliminate the need for some READ-MODIFY-WRITE cycles, collapsing it to a single BYTE/NIBBLE WRITE operation in some instances.

Programmable Impedance Output Buffer

The DDR SRAM is equipped with programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ ball and VSS. The value of the resistor must be five times the desired impedance. For example, a 350Ω resistor is required for an output impedance of 70Ω. To ensure that output impedance is one-fifth the value of RQ (within 15 percent), the range of RQ is 175Ω to 350Ω. Alternately, the ZQ ball can be connected directly to VDDQ, which will place the device in a minimum impedance mode.

Output impedance updates may be required because, over time, variations may occur in supply voltage and temperature. The device samples the value of RQ. Impedance updates are transparent to the system; they do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set at 50Ω. To guarantee optimum output driver impedance after power-up, the SRAM needs 1,024 cycles to update the impedance. The user can operate the part with fewer than 1,024 clock cycles, but optimal output impedance is not guaranteed.

Clock Considerations

This device utilizes internal delay-locked loops for maximum output, data valid window. It can be placed into a stopped-clock state to minimize power with a modest restart time of 1,024 clock cycles. Circuitry automatically resets the DLL when the absence of input clock is detected. See Micron Technical Note TN-54-02 for more information on clock DLL start-up procedures.

Single Clock Mode

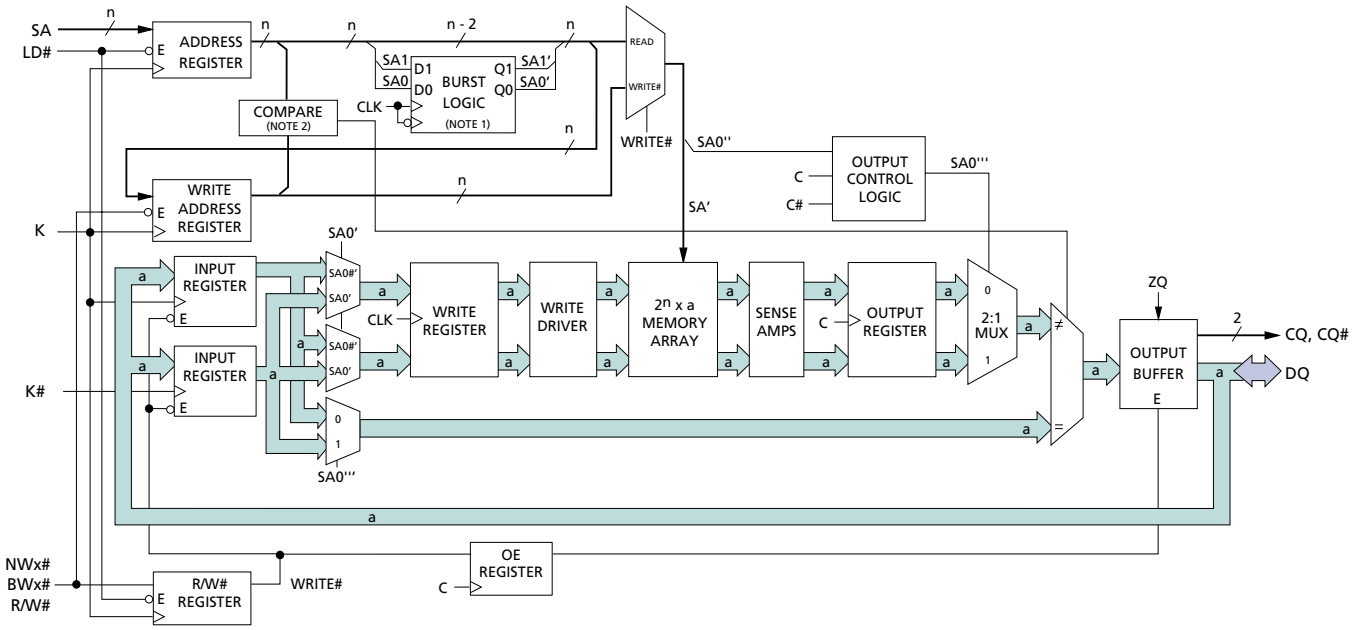
The SRAM can be used with the single K, K# clock pair by tying C and C# HIGH. In this mode, the SRAM will use K and K# in place of C and C#. This mode provides the most rapid data output but does not compensate for system clock skew and flight times.

The output echo clocks are precise references to output data. CQ and CQ# are both rising edge and falling edge accurate and are 180° out of phase. Either or both may be used for output data capture. K or C rising edge triggers CQ rising and CQ# falling edge. CQ rising edge indicates first data response for QDRI and DDRI (version 1, non-DLL) SRAM, while CQ# rising edge indicates first data response for QDRII and DDRII (version 2, DLL) SRAM.

Depth Expansion

Depth expansion requires replicating the LD# control signal for each bank. All other control signals can be common between banks as appropriate.

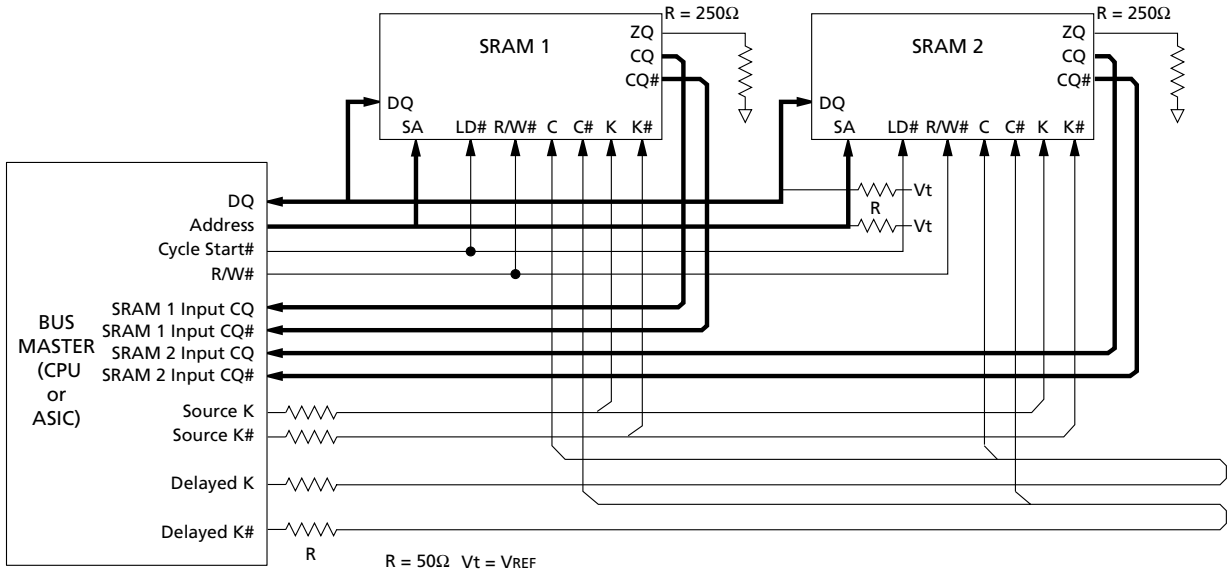
Figure 2: Functional Block Diagram
2 Meg x 8; 1 Meg x 18; 512K x 36



NOTE:

1. SA0 and SA1 are advanced in linear burst order at each K and K# rising edge.
2. The compare width is n – 2 bits. The compare is performed only if a WRITE is pending and a READ cycle is requested. If the address matches, data is routed directly to the device outputs, bypassing the memory array.
3. The functional block diagram illustrates simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.
4. For 2 Meg x 8, n = 21, a = 8; NWx# = 2 separate nibble writes.
   For 1 Meg x 18, n = 20, a = 18; BWx# = 2 separate byte writes.
   For 512K x 36, n = 19, a = 36; BWx# = 4 separate byte writes.

Figure 3: Application Example



NOTE:

1. In this approach, the second clock pair drives the C and C# clocks but is delayed such that return data meets setup and hold times at the bus master.
2. Consult Micron Technical Notes for more thorough discussions of clocking schemes.
3. Data capture is possible using only one of the two signals. CQ and CQ# clocks are optional use outputs.
4. For high frequency applications (200 MHz and faster) the CQ and CQ# clocks (for data capture) are recommended over the C and C# clocks (for data alignment). The C and C# clocks are optional use inputs.

Table 2: 2 Meg x 8 Ball Layout (Top View) 165-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	VSS/SA[1]	SA	R/W#	NW1#[2]	K#	NC[3]	LD#	SA	VSS/SA[4]	CQ
B	NC	NC	NC	SA	NC[5]	K	NW0#[6]	SA	NC	NC	DQ3
C	NC	NC	NC	VSS	SA	NC	SA	VSS	NC	NC	NC
D	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	NC	NC	NC
E	NC	NC	DQ4	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2
F	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
G	NC	NC	DQ5	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
H	DLL#	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ1	NC
K	NC	NC	NC	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	NC
L	NC	DQ6	NC	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ0
M	NC	NC	NC	VSS	VSS	VSS	VSS	VSS	NC	NC	NC
N	NC	NC	NC	VSS	SA	SA	SA	VSS	NC	NC	NC
P	NC	NC	DQ7	SA	SA	C	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

NOTE:
1. Expansion address: 2A for 72Mb
2. NW1# controls writes to DQ4:DQ7
3. Expansion address: 7A for 144Mb
4. Expansion address: 10A for 36Mb
5. Expansion address: 5B for 288Mb
6. NW0# controls writes to DQ0:DQ3

Note that the x8 does not permit random start address on the two least-significant address bits. SA and SA1 = 0 at the start of each address.

Table 3: 1 Meg x 18 Ball Layout (Top View) 165-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	Vss/SA[1]	SA	R/W#	BW1#[2]	K#	NC/SA[3]	LD#	SA	Vss/SA[4]	CQ
B	NC	DQ9	NC	SA	NC/SA[5]	K	BW0[6]#	SA	NC	NC	DQ8
C	NC	NC	NC	Vss	SA	SA0	SA1	Vss	NC	DQ7	NC
D	NC	NC	DQ10	Vss	Vss	Vss	Vss	Vss	NC	NC	NC
E	NC	NC	DQ11	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ6
F	NC	DQ12	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ5
G	NC	NC	DQ13	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	NC
H	DLL#	VREF	VDDQ	VDDQ	VDD	Vss	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	VDD	Vss	VDD	VDDQ	NC	DQ4	NC
K	NC	NC	DQ14	VDDQ	VDD	Vss	VDD	VDDQ	NC	NC	DQ3
L	NC	DQ15	NC	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ2
M	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	DQ1	NC
N	NC	NC	DQ16	Vss	SA	SA	SA	Vss	NC	NC	NC
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

NOTE:

1. Expansion address: 2A for 72Mb
2. BW1#controls writes to DQ9:DQ17
3. Expansion address: 7A for 144Mb
4. Expansions address: 10A for 36Mb
5. Expansion address: 5B for 288Mb
6. BW0# controls writes to DQ0:DQ8

Table 4: 512K x 36 Ball Layout (Top View) 165-Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	VSS/SA[1]	NC/SA[2]	R/W#	BW2#[3]	K#	BW1#[4]	LD#	SA	VSS/SA[5]	CQ
B	NC	DQ27	DQ18	SA	BW3#[6]	K	BW0#[7]	SA	NC	NC	DQ8
C	NC	NC	DQ28	VSS	SA	SA0	SA1	VSS	NC	DQ17	DQ7
D	NC	DQ29	DQ19	VSS	VSS	VSS	VSS	VSS	NC	NC	DQ16
E	NC	NC	DQ20	VDDQ	VSS	VSS	VSS	VDDQ	NC	DQ15	DQ6
F	NC	DQ30	DQ21	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ5
G	NC	DQ31	DQ22	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	DQ14
H	DLL#	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	DQ32	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ13	DQ4
K	NC	NC	DQ23	VDDQ	VDD	VSS	VDD	VDDQ	NC	DQ12	DQ3
L	NC	DQ33	DQ24	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	DQ2
M	NC	NC	DQ34	VSS	VSS	VSS	VSS	VSS	NC	DQ11	DQ1
N	NC	DQ35	DQ25	VSS	SA	SA	SA	VSS	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

NOTE:

1. Expansion address: 2A for 144Mb
2. Expansion address: 3A for 36Mb
3. BW2# controls writes to DQ18:DQ26
4. BW1# controls writes to DQ9:DQ17
5. Expansion address: 10A for 72Mb
6. BW3# controls writes to DQ27:DQ35
7. BW0# controls writes to DQ0:DQ8

Table 5: Ball Descriptions

SYMBOL	TYPE	DESCRIPTION
BW_# NW_#	Input	Synchronous Byte Writes (or Nibble Writes on x8): When LOW, these inputs cause their respective bytes or nibbles to be registered and written if W# had initiated a WRITE cycle. These signals must meet setup and hold times around the rising edges of K and K# for each of the four rising edges comprising the WRITE cycle. See Ball Layout figures for signal to data relationships.
C C#	Input	Output Clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of C# is used as the output timing reference for first and third output data. The rising edge of C is used as the output reference for second and fourth output data. Ideally, C# is 180 degrees out of phase with C. C and C# may be tied HIGH to force the use of K and K# as the output reference clocks instead of having to provide C and C# clocks. If tied HIGH, these inputs may not be allowed to toggle during device operation.
DLL#	Input	DLL Disable: When LOW, this input causes the DLL to be bypassed for stable, low-frequency operation.
K K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
LD#	Input	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of four data (two clock periods of bus activity).
R/W#	Input	Synchronous Read/Write Input: When LD# is LOW, this input designates the access type (READ when R/W# is HIGH; WRITE when R/W# is LOW) for the loaded address. R/W# must meet the setup and hold times around the rising edge of K.
SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. See Ball Layout figures for address expansion inputs. All transactions operate on a burst of four words (two clock periods of bus activity). SA0 and SA1 are used as the lowest two address bits for BURST READ and BURST WRITE operations, permitting a random burst start address on the x18 and x36 devices. These inputs are ignored when both ports are deselected.
TCK	Input	IEEE 1149.1 Clock Input: 1.8V I/O levels. This ball must be tied to VSS if the JTAG function is not used in the circuit.
TMS TDI	Input	IEEE 1149.1 Test Inputs: 1.8V I/O levels. These balls may be left as No Connects if the JTAG function is not used in the circuit.
VREF	Input	HSTL Input Reference Voltage: Nominally VDDQ/2. Provides a reference voltage for the HSTL input buffer trip points.
ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance are set to 0.2 x RQ, where RQ is a resistor from this ball to ground. Alternately, this ball can be connected directly to VDDQ to enable the minimum impedance mode. This ball cannot be connected directly to GND or left unconnected.
DQ_	Input/ Output	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K#. Output data is synchronized to the respective C and C# data clocks or to K and K#, if C and C# are tied HIGH. See Ball Layout figures for ball site location of individual signals. The x8 device uses DQ0-DQ7. Remaining signals are NC. The x18 device uses DQ0-DQ17. Remaining signals are NC. The x36 device uses DQ0-DQ35. Remaining signals are NC.
CQ#, CQ	Output	Synchronous Echo Clock Outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as data valid indication. These signals run freely and do not stop when DQ tri-states.
TDO	Output	IEEE 1149.1 Test Output: 1.8V I/O level.
VDD	Supply	Power Supply: 1.8V nominal. See DC Electrical Characteristics and Operating Conditions for range.
VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. 1.8V is also permissible. See DC Electrical Characteristics and Operating Conditions for range.
VSS	Supply	Power Supply: GND.

Table 5: Ball Descriptions (continued)

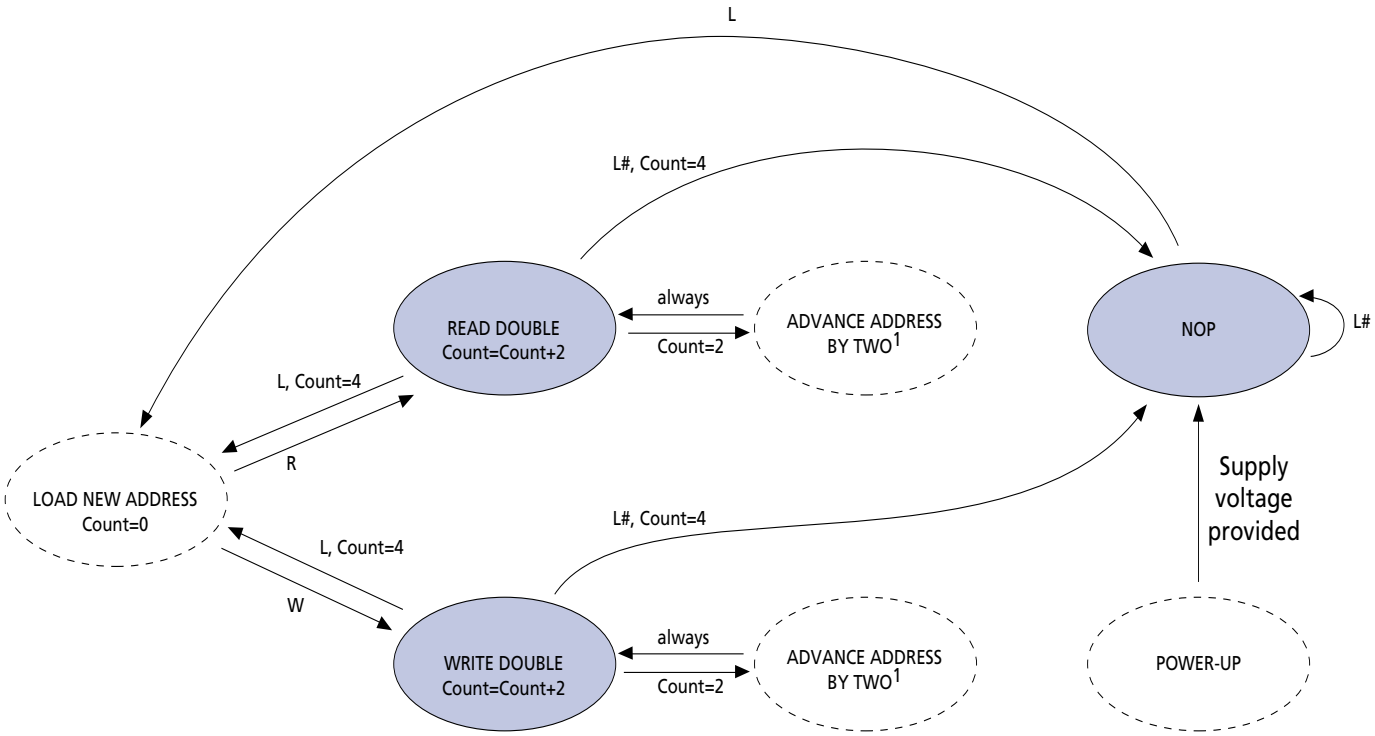
SYMBOL	TYPE	DESCRIPTION
NC	–	No Connect: These balls are internally connected to the die, but have no function and may be left not connected to the board to minimize ball count.

Table 6: Burst Address Table

x 18, x 36 only

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
X . . . X00	X . . . X01	X . . . X10	X . . . X11
X . . . X01	X . . . X10	X . . . X11	X . . . X00
X . . . X10	X . . . X11	X . . . X00	X . . . X01
X . . . X11	X . . .X00	X . . . X01	X . . . X10

Figure 4: Bus Cycle State Diagram



NOTE:

1. SA0 and SA1 are internally advanced in accordance with the burst order table. Bus cycle is terminated after burst count = 4.
2. State transitions: L = (LD# = LOW); L# = (LD# = HIGH); R = (R/W# = HIGH); W = (R/W# = LOW).
3. State machine, control timing sequence is controlled by K.

Table 7: Truth Table

Notes 1–6

OPERATION	LD#	R/W#	K	DQ	DQ	DQ	DQ
WRITE Cycle: Load address, input write data on two consecutive K and K# rising edges	L	L	L→H	DIN(A0) at K(t)↑	DIN(A0 + 1) at K#(t + 1)↑	DIN(A0 + 2) at K(t + 2)↑	DIN(A0 + 3) at K#(t + 3)↑
READ Cycle: Load address, read data on two consecutive C and C# rising edges	L	H	L→H	QOUT(A0) at C#(t)↑	QOUT(A0 + 1) at C(t + 1)↑	QOUT(A0 + 2) at C#(t + 2)↑	QOUT(A0 + 3) at C(t + 3)↑
NOP: No operation	H	X	L→H	High-Z	High-Z	High-Z	High-Z
STANDBY: Clock stopped	X	X	Stopped	Previous State	Previous State	Previous State	Previous State

Table 8: BYTE WRITE Operation

Notes 7, 8

OPERATION	K	K#	BW0#	BW1#
WRITE D0:17 at K rising edge	L→H		0	0
WRITE D0:17 at K# rising edge		L→H	0	0
WRITE D0:8 at K rising edge	L→H		0	1
WRITE D0:8 at K# rising edge		L→H	0	1
WRITE D9:17 at K rising edge	L→H		1	0
WRITE D9:17 at K# rising edge		L→H	1	0
WRITE nothing at K rising edge	L→H		1	1
WRITE nothing at K# rising edge		L→H	1	1

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW. ↑means rising edge; ↓ means falling edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges except if C and C# are HIGH, then data outputs are delivered at K and K# rising edges.
3. R/W# and LD# must meet setup and hold times around the rising edge (LOW to HIGH) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification. A0 + 1 refers to the address input during a WRITE or READ cycle. A0 + 2 refers to the next internal burst address in accordance with the burst sequence.
6. It is recommended that K = K# = C = C# when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.
8. This table illustrates operation for x18 devices. The x36 device operation is similar, except for the addition of BW2# (controls DQ18:DQ26) and BW3# (controls DQ27:DQ35). The x8 device operation is similar, except that NW0# controls DQ0:DQ3, and NW1# controls DQ4:DQ7.

Absolute Maximum Ratings

Voltage on VDD Supply
Relative to VSS ..... -0.5V to 2.8V
Voltage on VDDQ Supply
Relative to Vss ..... -0.5V to VDD
VIN..... -0.5V to VDD +0.5V
Storage Temperature..... -55°C to +125°C
Junction Temperature..... +125°C
Short Circuit Output Current ..... ±70mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Maximum Junction Temperature depends upon package type, cycle time, loading, ambient temperature, and airflow.

Table 9: DC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD = 1.8V ±0.1V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH(DC)	VREF + 0.1	VDDQ + 0.3	V	3, 4
Input Low (Logic 0) Voltage		VIL(DC)	-0.3	VREF - 0.1	V	3, 4
Clock Input Signal Voltage		VIN	-0.3	VDDQ + 0.3	V	3, 4
Input Leakage Current	0V ≤ VIN ≤ VDDQ	ILI	-5	5	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDDQ (Q)	ILO	-5	5	µA	
Output High Voltage	|IOH| ≤ 0.1mA	VOH (LOW)	VDDQ - 0.2	VDDQ	V	3, 5, 6
	Note 1	VOH	VDDQ/2 - 0.12	VDDQ/2 + 0.12	V	3, 5, 6
Output Low Voltage	IOL ≤ 0.1mA	VOL (LOW)	VSS	0.2	V	3, 5, 6
	Note 2	VOL	VDDQ/2 - 0.12	VDDQ/2 + 0.12	V	3, 5, 6
Supply Voltage		VDD	1.7	1.9	V	3
Isolated Output Buffer Supply		VDDQ	1.4	VDD	V	3, 7
Reference Voltage		VREF	0.68	0.95	V	3

Table 10: AC Electrical Characteristics and Operating Conditions

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD = 1.8V ±0.1V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH(AC)	VREF + 0.2	-	V	3, 4, 8
Input Low (Logic 1) Voltage		VIL(AC)	-	VREF - 0.2	V	3, 4, 8

Table 11: IDD Operating Conditions and Maximum Limits

Notes appear following parameter tables on page 17; 0°C ≤ T_A ≤ +70°C; VDD = 1.8V ±0.1V unless otherwise noted

				MAX							
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-3**	**-3.3**	**-4**	**-5**	**-6**	**-7.5**	**UNITS**	**NOTES**
Operating Supply Current: DDR	All inputs ≤ VIL or ≥ VIH; Cycle time ≥ ^{t}KHKH (MIN); Outputs open; x:1 ratio for READs to WRITEs; 50% address and data bits toggling on each clock cycle	IDD x8, x18 x36	TBD	 390 520	 355 475	 300 400	 250 330	 215 285	 180 240	mA	9, 10
Standby Supply Current: NOP	^{t}KHKH = ^{t}KHKH (MIN); Device in NOP state; All addresses/data static	ISB1 x8, x18 x36	TBD	 255 265	 235 245	 200 210	 170 180	 150 160	 125 135	mA	10, 11
Output Supply Current: DDR (Information only)	CL = 15pF	IDDQ x8 x18 x36	TBD	42 95 189	38 85 170	32 71 142	25 57 142	21 47 95	17 38 76	mA	12

Table 12: Capacitance

Note 13; notes appear following parameter tables on page 17

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	CI	4.5	5.5	pF
Input, Output Capacitance (DQ)		CO	6	7	pF
Clock Capacitance		CCK	5.5	6.5	pF

Table 13: Thermal Resistance

Note 13; notes appear following parameter tables on page 17

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ_{JA}	19.4	°C/W	14
Junction to Case (Top)		θ_{JC}	1.0	°C/W	
Junction to Balls (Bottom)		θ_{JB}	9.6	°C/W	15

Table 14: AC Electrical Characteristics and Recommended Operating Conditions

Notes 16-19; 22; notes appear following parameter tables on page 17; °C ≤ T_A ≤ +70°C; T_J ≤ +95°C; VDD = 1.8V ±0.1V

DESCRIPTION	SYM	-3		-3.3		-4		-5		-6		-7.5		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock															
Clock cycle time (K, K#, C, C#)	^{t}KHKH	3.00	3.47	3.30	4.20	4.00	5.25	5.00	6.30	6.00	7.80	7.50	8.40	ns	20
Clock phase jitter (K, K#, C, C#)	^{t}KC var		0.20		0.20		0.20		0.20		0.20		0.20	ns	21
Clock HIGH time (K, K#, C, C#)	^{t}KHKL	1.20		1.32		1.60		2.00		2.40		3.00		ns	
Clock LOW time (K, K#, C, C#)	^{t}KLKH	1.20		1.32		1.60		2.00		2.40		3.00		ns	
Clock to clock# (K↑→K#↑, C↑→C#↑) at ^{t}KHKH minimum	^{t}KHK#H	1.35		1.49		1.80		2.20		2.70		3.38		ns	
Clock# to clock (K#↑→K↑, C#↑→C↑)at ^{t}KHKH minimum	^{t}K#HKH	1.35		1.49		1.80		2.20		2.70		3.38		ns	
Clock to data clock (K↑→C↑, K#↑→C#↑)	^{t}KHCH	0.00	1.30	0.00	1.45	0.00	1.80	0.00	2.30	0.00	2.80	0.00	3.55	ns	
DLL lock time (K, C)	^{t}KC lock	1,024		1,024		1,024		1,024		1,024		1,024		cycles	22
K static to DLL reset	^{t}KC reset	30		30		30		30		30		30		ns	
Output Times															
C, C# HIGH to output valid	^{t}CHQV		0.45		0.45		0.45		0.45		0.50		0.50	ns	
C, C# HIGH to output hold	^{t}CHQX	-0.45		-0.45		-0.45		-0.45		-0.50		-0.50		ns	
C, C# HIGH to echo clock valid	^{t}CHCQV		0.45		0.45		0.45		0.45		0.50		0.50	ns	
C, C# HIGH to echo clock hold	^{t}CHCQX	-0.45		-0.45		-0.45		-0.45		-0.50		-0.50		ns	
CQ, CQ# HIGH to output valid	^{t}CQHQV		0.25		0.27		0.30		0.35		0.40		0.40	ns	23
CQ, CQ# HIGH to output hold	^{t}CQHQX	-0.25		-0.27		-0.30		-0.35		-0.40		-0.40		ns	23
C HIGH to output High-Z	^{t}CHQZ		0.45		0.45		0.45		0.45		0.50		0.50	ns	
C HIGH to output Low-Z	^{t}CHQX1	-0.45		-0.45		-0.45		-0.45		-0.50		-0.50		ns	
Setup Times															
Address valid to K rising edge	^{t}AVKH	0.40		0.40		0.50		0.60		0.70		0.70		ns	16

Table 14: AC Electrical Characteristics and Recommended Operating Conditions (continued)

DESCRIPTION	SYM	-3		-3.3		-4		-5		-6		-7.5		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Control inputs valid to K rising edge	^{t}IVKH	0.40		0.40		0.50		0.60		0.70		0.70		ns	16
Data-in valid to K, K# rising edge	^{t}DVKH	0.28		0.30		0.35		0.40		0.50		0.50		ns	16
Hold Times															
K rising edge to address hold	^{t}KHAX	0.40		0.40		0.50		0.60		0.70		0.70		ns	16
K rising edge to control inputs hold	^{t}KHIX	0.40		0.40		0.50		0.60		0.70		0.70		ns	16
K, K# rising edge to data-in hold	^{t}KHDX	0.28		0.30		0.35		0.40		0.50		0.50		ns	16

Notes

1. Outputs are impedance-controlled. |IOH| = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
2. Outputs are impedance-controlled. IOL = (VDDQ/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
3. All voltages referenced to VSS (GND).
4. Overshoot: VIH(AC) ≤ VDD + 0.7V for t ≤ ^{t}KHKH/2
   Undershoot: VIL(AC) ≥ -0.5V for t ≤ ^{t}KHKH/2
   Power-up: VIH ≤ VDDQ + 0.3V and VDD ≤ 1.7V and VDDQ ≤ 1.4V for t ≤ 200ms
   During normal operation, VDDQ must not exceed VDD. Control input signals may not have pulse widths less than ^{t}KHKL (MIN) or operate at cycle rates less than ^{t}KHKH (MIN).
5. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
6. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
7. The nominal value of VDDQ may be set within the range of 1.5V to 1.8V DC, and the variation of VDDQ must be limited to ±0.1V DC.
8. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, VIL(AC) or VIH(AC).
   b. Reach at least the target AC level.
   c. After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
9. IDD is specified with no output current. IDD is linear with frequency. Typical value is measured at 6ns cycle time.
10. Typical values are measured at VDD = 1.8V, VDDQ = 1.5V, and temperature = 25°C.
11. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
12. Average I/O current and power is provided for informational purposes only and is not tested. Calculation assumes that all outputs are loaded with CL (in farads), f = input clock frequency, half of outputs toggle at each transition (n = 18 for the x36), CO = 6pF, VDDQ = 1.5V and uses the equations: Average I/O Power as dissipated by the SRAM is: $P = 0.5 \times n \times f \times V_{DDQ}^2 \times (C_L + 2C_O)$.
    Average IDDQ = n × f × VDDQ x (CL + CO).
13. This parameter is sampled.
14. Average thermal resistance between the die and the case top surface per MIL SPEC 883 Method 1012.1.
15. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
16. This is a synchronous device. All addresses, data, and control lines must meet the specified setup and hold times for all latching clock edges.
17. Test conditions as specified with the output loading as shown in Figure 5 unless otherwise noted.
18. Control input signals may not be operated with pulse widths less than ^{t}KHKL (MIN).
19. If C and C# are tied HIGH, then K and K# become the references for C and C# timing parameters.
20. The device will operate at clock frequencies slower than ^{t}KHKH (MAX). See Micron Technical Note TN-54-02 for more information.
21. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
22. VDD slew rate must be less than 0.1V DC per 50ns for DLL lock retention. DLL lock time begins once VDD and input clock are stable.
23. Echo clock is tightly controlled to data valid/data hold. By design, there is a ±0.1ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.

AC Test Conditions

Input pulse levels	0.25V to 1.25V
Input rise and fall times	0.7ns
Input timing reference levels	0.75V
Output reference levels	VDDQ/2
ZQ for 50Ω impedance	250Ω
Output load	See Figure 5

Figure 5:
Output Load Equivalent

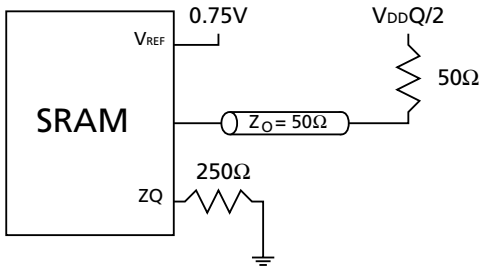
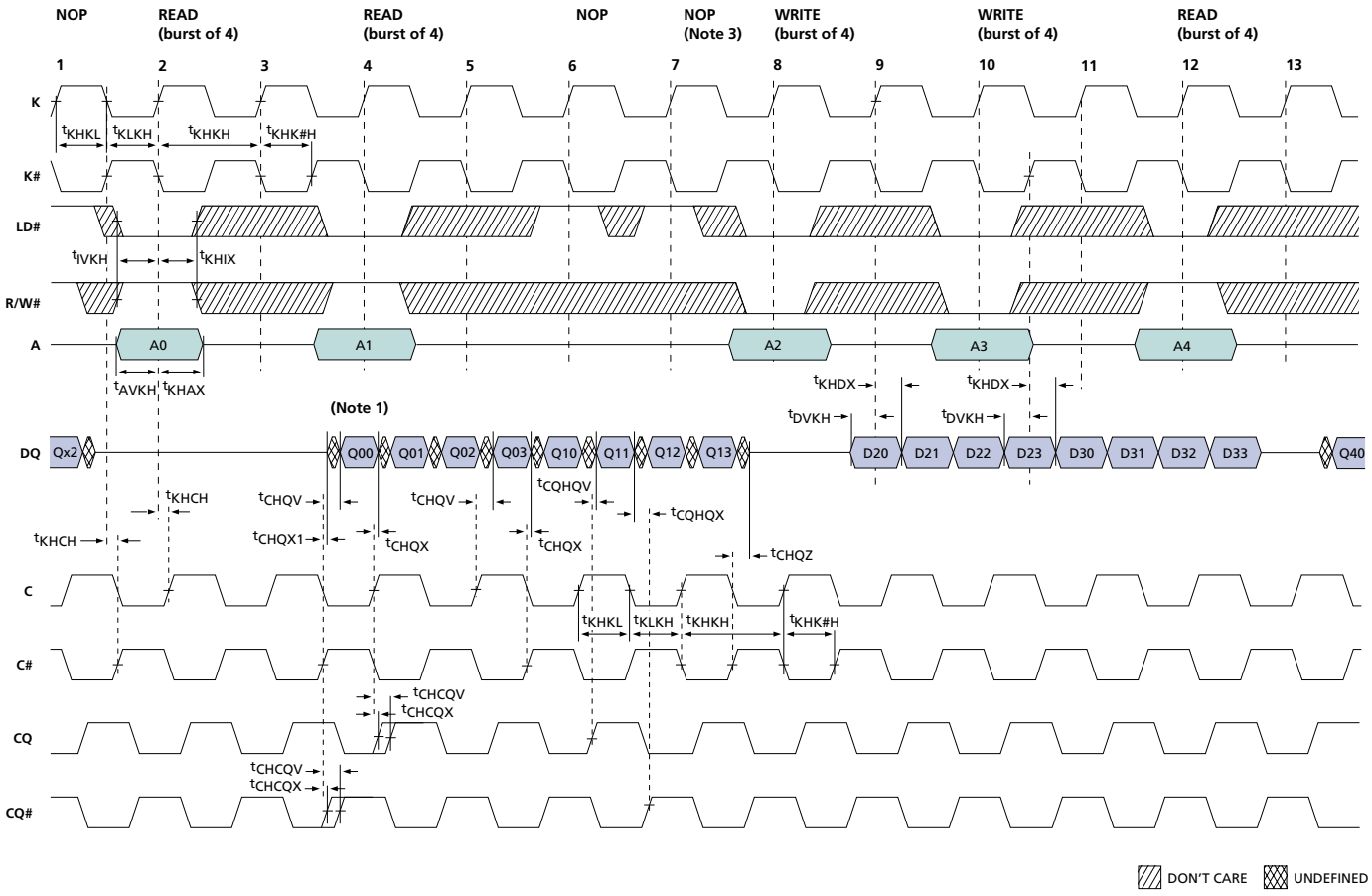


Figure 6:
READ/WRITE Timing



NOTE:

1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, i.e., A0 + 1.
2. Outputs are disabled (High-Z) one clock cycle after a NOP.
3. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.

IEEE 1149.1 Serial Boundary Scan (JTAG)

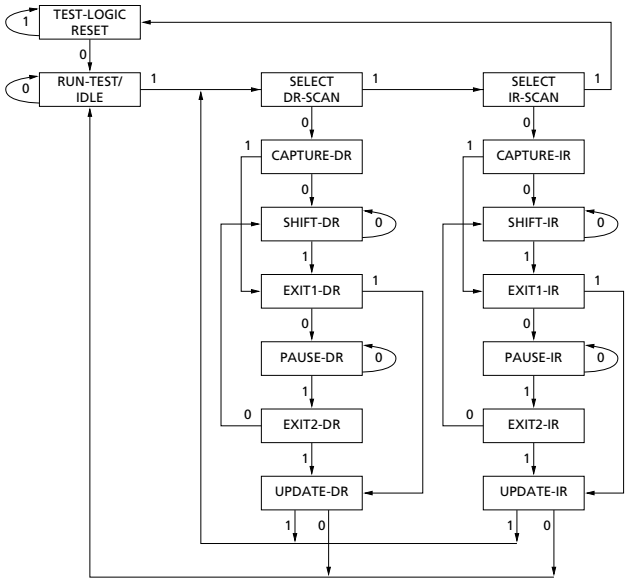
The SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully-compliant TAPs. The TAP operates using JEDEC-standard 1.8V I/O logic levels.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling The JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. Alternately, they may be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state, which will not interfere with the operation of the device.

Figure 7:
TAP Controller State Diagram



NOTE:

The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

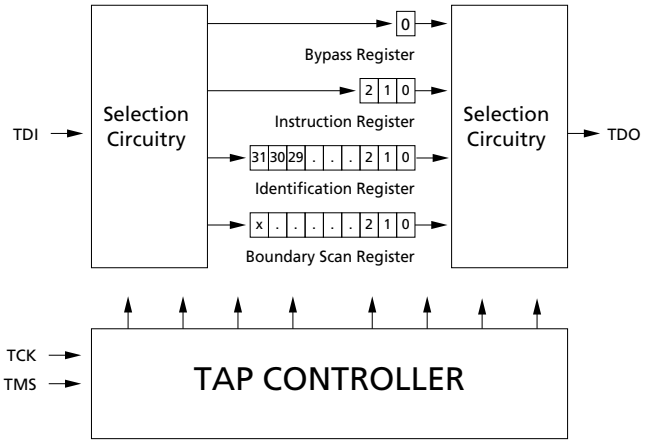
Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

Test Data-in (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 7. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register, as illustrated in Figure 8.

Figure 8:
TAP Controller Block Diagram



NOTE:

X = 106.

Test Data-out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine illustrated in Figure 7. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register, as depicted in Figure 8.

Performing a TAP RESET

A RESET is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register at a time can be selected through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls, as shown in Figure 8. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (Vss) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several no connect (NC) balls are also included in the scan register to reserve balls. The SRAM has a 107-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table shows the order in which the bits are connected. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the I/O ring when these instructions are executed.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller; therefore, this device is not 1149.1-compliant.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. EXTEST does not place the SRAM outputs (including CQ and CQ#) in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

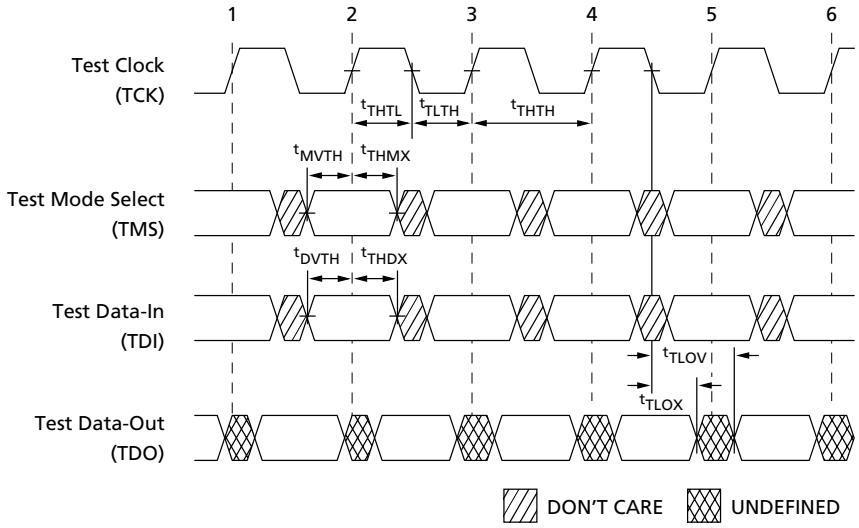
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 9: TAP Timing



NOTE:

Timing for SRAM inputs and outputs is congruent with TDI and TDO, respectively, as shown in Figure 9.

Table 15: TAP AC Electrical Characteristics

Notes 1, 2; 0°C ≤ T_A ≤ +70°C; VDD = 1.8V ±0.1V

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	$^{t}THTH$	100		ns
Clock frequency	^{f}TF		10	MHz
Clock HIGH time	$^{t}THTL$	40		ns
Clock LOW time	$^{t}TLTH$	40		ns
Output Times				
TCK LOW to TDO unknown	$^{t}TLOX$	0		ns
TCK LOW to TDO valid	$^{t}TLOV$		20	ns
TDI valid to TCK HIGH	$^{t}DVTH$	10		ns
TCK HIGH to TDI invalid	$^{t}THDX$	10		ns
Setup Times				
TMS setup	$^{t}MVTH$	10		ns
Capture setup	^{t}CS	10		ns
Hold Times				
TMS hold	$^{t}THMX$	10		ns
Capture hold	^{t}CH	10		ns

NOTE:

1. ^{t}CS and ^{t}CH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 10.

TAP AC Test Conditions

Input pulse levels ..... VSS to 1.8V
Input rise and fall times..... 1ns
Input timing reference levels 0.9V
Output reference levels.....0.9V
Test load termination supply voltage 0.9V

Figure 10:
TAP AC Output Load Equivalent

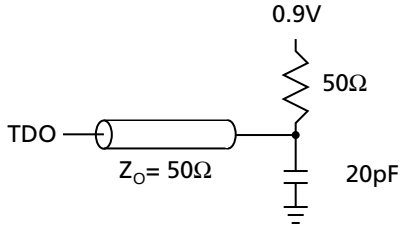


Table 16: TAP DC Electrical Characteristics and Operating Conditions

Note 2; 0°C ≤ T_A ≤ +70°C; VDD = 1.8V ±0.1V unless otherwise noted

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	1.3	VDD + 0.3	V	1, 2
Input Low (Logic 0) Voltage		VIL	-0.3	0.5	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ VDD	ILI	-5.0	5.0	µA	2
Output Leakage Current	Output(s) disabled, 0V ≤ VIN ≤ VDD	ILO	-5.0	5.0	µA	2
Output Low Voltage	IOLC = 100µA	VOL1		0.2	V	1, 2
Output Low Voltage	IOLT = 2mA	VOL2		0.4	V	1, 2
Output High Voltage	|IOHC| = 100µA	VOH1	1.6		V	1, 2
Output High Voltage	|IOHT| = 2mA	VOH2	1.4		V	1, 2

NOTE:

1. All voltages referenced to VSS (GND).
2. This table defines DC values for TAP control and data balls only. The DQ SRAM balls used in JTAG operation will have the DC values as defined in Table 9, “DC Electrical Characteristics and Operating Conditions,” on page 13.

Table 17: Identification Register Definitions

INSTRUCTION FIELD	ALL DEVICES	DESCRIPTION
REVISION NUMBER (31:29)	000	Revision number.
DEVICE ID (28:12)	00def0wx0t0q0b0s0	def = 010 for 36Mb density def = 001 for 18Mb density wx = 11 for x36 width wx = 10 for x18 width wx = 01 for x8 width t = 1 for DLL version t = 0 for non-DLL version q = 1 for QDR q = 0 for DDR b = 1 for 4-word burst b = 0 for 2-word burst s = 1 for separate I/O s = 0 for common I/O
MICRON JEDEC ID CODE (11:1)	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.

Table 18: Scan Register Size

REGISTER NAME	BIT SIZE
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

Table 19: Instruction Codes

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

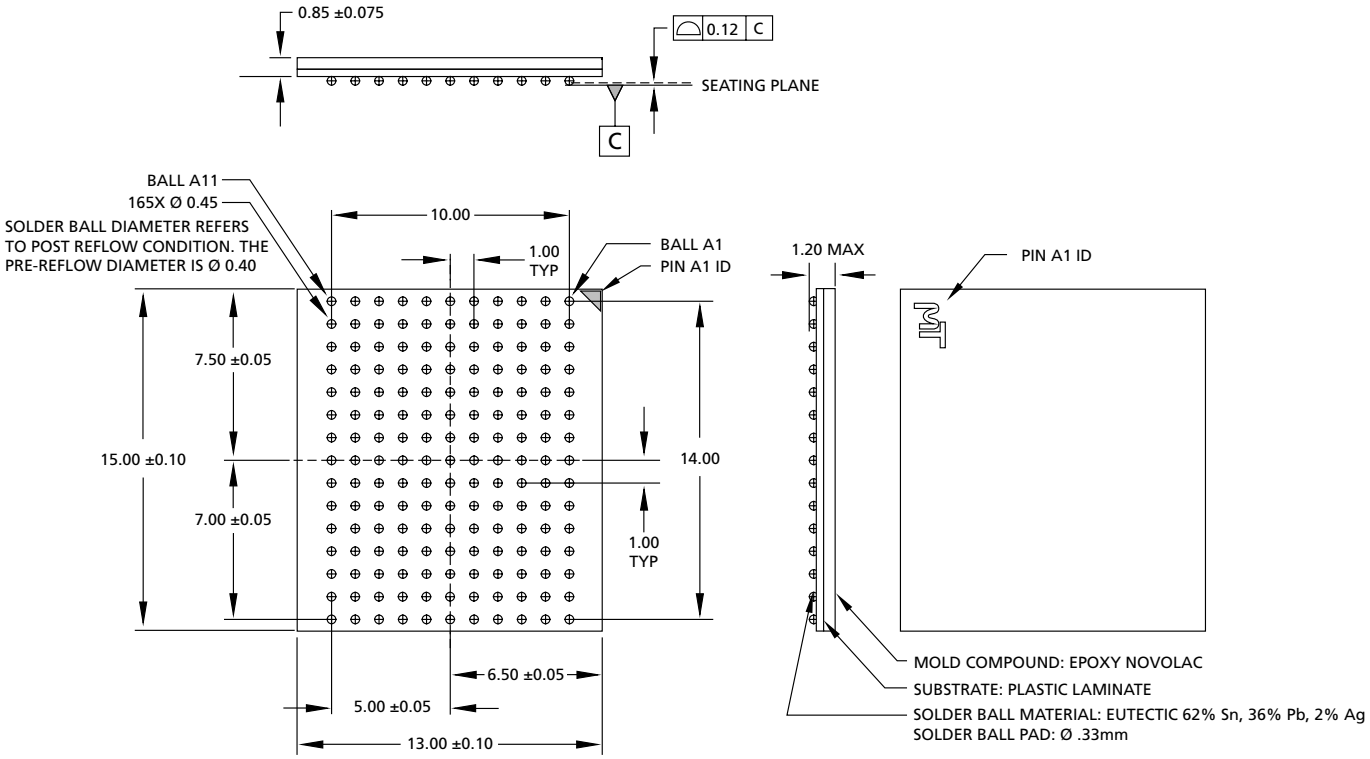
Table 20: Boundary Scan (Exit) Order

BIT#	FBGA BALL
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

BIT#	FBGA BALL
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

BIT#	FBGA BALL
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R

Figure 11:
165-Ball FBGA



NOTE:
1. All dimensions are in millimeters.

Data Sheet Designation

No Marking: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Document Revision History

Rev. H, Pub 3/03 ..... 3/03

- Updated JTAG Section
- Removed Preliminary Status

Rev. G, Pub 2/03 ..... 2/03

- Added definitive notes to Figure 3
- Added definitive note to Table 9
- Added definitive note concerning bit# 64 to Table 19
- Removed Errata specifications
- Updated AC timing values with new codevelopment values
- Updated JTAG description to reflect 1149.1 specification compliance with EXTEST feature
- Added definitive note concerning SRAM (DQ) I/O balls used for JTAG DC values and timing
- Changed process information in header to die revision indicator
- Updated Thermal Resistance Values to Table 12:
  C_I = 4.5 TYP; 5.5 MAX
  C_O = 6 TYP; 7 MAX
  C_{CK} = 5.5 TYP; 6.5 MAX
- Updated Thermal Resistance values to Table 12:
  J_A = 19.4 TYP
  J_C = 1.0 TYP
  J_B = 9.6 TYP
- Added $T_J \leq +95°C$ to Table 13
- Modified Figure 2 regarding depth, configuration, and byte controls
- Added definitive notes regarding I/O behavior during JTAG operation
- Added definitive notes regarding I_{DD} test conditions for read to write ratio
- Removed note regarding AC derating information for full I/O range
- Remove references to JTAG scan chain logic levels being at logic zero for NC pins in Tables 5 and 19
- Revised ball description for NC balls:
  These balls are internally connected to the die, but have no function and may be left not connected to the board to minimize ball count.

Rev. 6, Pub 9/02 ..... 9/02

- Reverted data sheet to PRELIMINARY designation

Rev. 5, Pub 9/02 ..... 9/02

- Added new Output Times values
- Added Errata to back of data sheet
- Removed ADVANCE designation
- Removed T_J references

Rev. 4, Pub 8/02, ADVANCE 8/02

- Update format

Rev. 3, Pub. 12/01, ADVANCE 12/01

- Changed AC Timing

Rev. 2, Pub. 11/01, ADVANCE 11/01

- New ADVANCE data sheet