



2Mb SYNCBURST™ SRAM

MT58L128L18P, MT58L64L32P, MT58L64L36P;
MT58L128V18P, MT58L64V32P, MT58L64V36P

3.3V V_{DD}, 3.3V or 2.5V I/O, Pipelined, Single-Cycle Deselect

FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (V_{DD})
- Separate +3.3V or +2.5V isolated output buffer supply (V_{DDQ})
- SNOOZE MODE for reduced-power standby
- Single-cycle deselect (Pentium® BSRAM-compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-pin TQFP package
- Low capacitive bus loading
- x18, x32, and x36 options available

OPTIONS

- Timing (Access/Cycle/MHz)
 - 3.5ns/5ns/200 MHz
 - 3.5ns/6ns/166 MHz
 - 4.0ns/7.5ns/133 MHz
 - 5ns/10ns/100 MHz

Configurations

3.3V I/O

128K x 18
64K x 32
64K x 36

MT58L128L18P
MT58L64L32P
MT58L64L36P

2.5V I/O

128K x 18
64K x 32
64K x 36

MT58L128V18P
MT58L64V32P
MT58L64V36P

Package

100-pin TQFP

T

Operating Temperature Range

Commercial (0°C to +70°C)

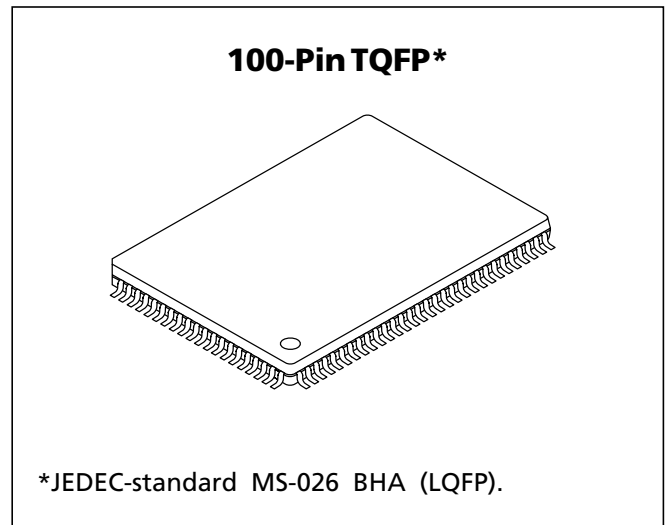
None

Part Number Example:

MT58L128L18PT-10

MARKING

-5
-6
-7.5
-10



GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 2Mb SyncBurst SRAMs integrate a 128K x 18, 64K x 32, or 64K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#), and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK), and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

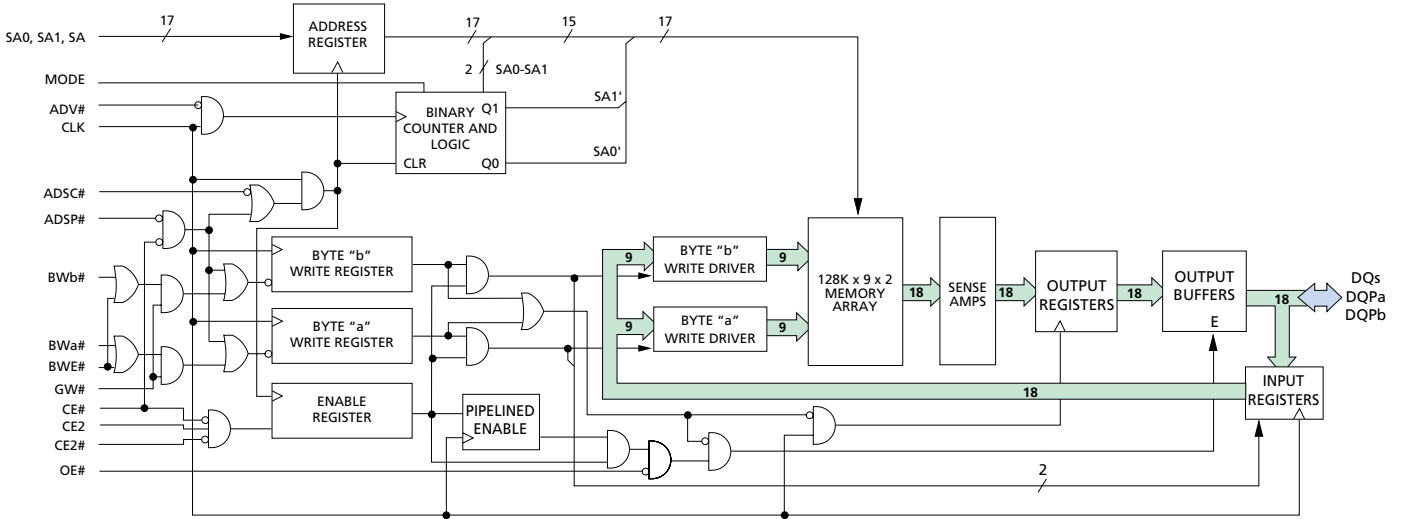
Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

NOT RECOMENDED FOR NEW DESIGNS

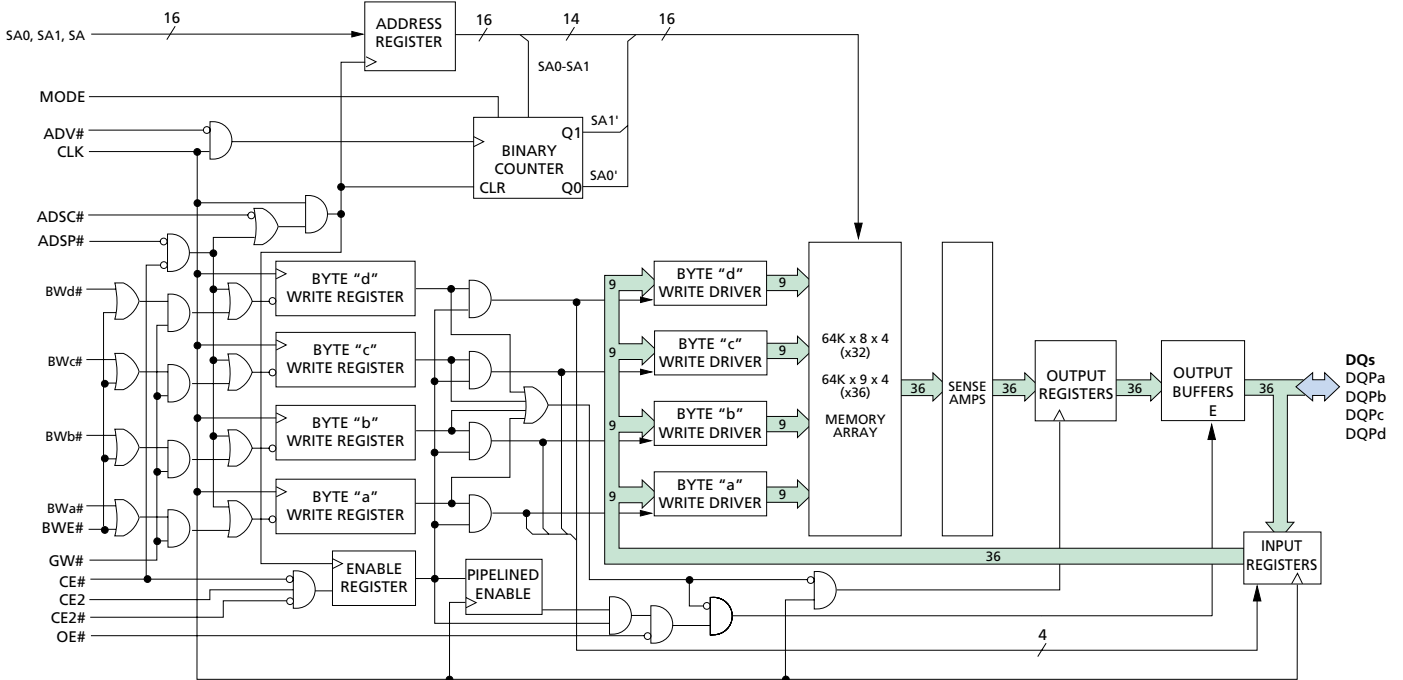


**2Mb: 128K x 18, 64K x 32/36
PIPELINED, SCD SYNCBURST SRAM**

**FUNCTIONAL BLOCK DIAGRAM
128K x 18**



**FUNCTIONAL BLOCK DIAGRAM
64K x 32/36**



NOTE: Functional block diagrams illustrate simplified device operation. See truth table, pin descriptions, and timing diagrams for detailed information.



GENERAL DESCRIPTION (continued)

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWA# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWA# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWC# controls DQc pins and DQPc; BWD# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity pins are only available on the x18 and x36 versions.

This device incorporates a single-cycle deselect feature during READ cycles. If the device is immediately

deselected after a READ cycle, the output bus goes to a High-Z state ^tKQHZ nanoseconds after the rising edge of clock.

Micron's 2Mb SyncBurst SRAMs operate from a +3.3V V_{DD} power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 3.3V or 2.5V I/O version. The device is ideally suited for Pentium and PowerPC pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64-, and 72-bit-wide applications.

Please refer to Micron's Web site (www.micron.com/sramds) for the latest data sheet.

TQFP PIN ASSIGNMENT TABLE

| PIN # | x18 | x32/x36 |
|-------|------------------|-----------|
| 1 | NC | NC/DQPa** |
| 2 | NC | DQc |
| 3 | NC | DQc |
| 4 | V _{DDQ} | |
| 5 | V _{SS} | |
| 6 | NC | DQc |
| 7 | NC | DQc |
| 8 | DQb | DQc |
| 9 | DQb | DQc |
| 10 | V _{SS} | |
| 11 | V _{DDQ} | |
| 12 | DQb | DQc |
| 13 | DQb | DQc |
| 14 | V _{DD} | |
| 15 | V _{DD} | |
| 16 | NC | |
| 17 | V _{SS} | |
| 18 | DQb | DQd |
| 19 | DQb | DQd |
| 20 | V _{DDQ} | |
| 21 | V _{SS} | |
| 22 | DQb | DQd |
| 23 | DQb | DQd |
| 24 | DQPa | DQd |
| 25 | NC | DQd |

| PIN # | x18 | x32/x36 |
|-------|------------------|-----------|
| 26 | V _{SS} | |
| 27 | V _{DDQ} | |
| 28 | NC | DQd |
| 29 | NC | DQd |
| 30 | NC | NC/DQPa** |
| 31 | MODE | |
| 32 | SA | |
| 33 | SA | |
| 34 | SA | |
| 35 | SA | |
| 36 | SA1 | |
| 37 | SA0 | |
| 38 | DNU | |
| 39 | DNU | |
| 40 | V _{SS} | |
| 41 | V _{DD} | |
| 42 | DNU | |
| 43 | DNU | |
| 44 | SA | |
| 45 | SA | |
| 46 | SA | |
| 47 | SA | |
| 48 | SA | |
| 49 | SA | |
| 50 | NC/SA* | |

| PIN # | x18 | x32/x36 |
|-------|------------------|-----------|
| 51 | NC | NC/DQPa** |
| 52 | NC | DQa |
| 53 | NC | DQa |
| 54 | V _{DDQ} | |
| 55 | V _{SS} | |
| 56 | NC | DQa |
| 57 | NC | DQa |
| 58 | DQa | |
| 59 | DQa | |
| 60 | V _{SS} | |
| 61 | V _{DDQ} | |
| 62 | DQa | |
| 63 | DQa | |
| 64 | ZZ | |
| 65 | V _{DD} | |
| 66 | NC | |
| 67 | V _{SS} | |
| 68 | DQa | DQb |
| 69 | DQa | DQb |
| 70 | V _{DDQ} | |
| 71 | V _{SS} | |
| 72 | DQa | DQb |
| 73 | DQa | DQb |
| 74 | DQPa | DQb |
| 75 | NC | DQb |

| PIN # | x18 | x32/x36 |
|-------|------------------|-----------|
| 76 | V _{SS} | |
| 77 | V _{DDQ} | |
| 78 | NC | DQb |
| 79 | NC | DQb |
| 80 | SA | NC/DQPa** |
| 81 | SA | |
| 82 | SA | |
| 83 | ADV# | |
| 84 | ADSP# | |
| 85 | ADSC# | |
| 86 | OE# | |
| 87 | BWE# | |
| 88 | GW# | |
| 89 | CLK | |
| 90 | V _{SS} | |
| 91 | V _{DD} | |
| 92 | CE2# | |
| 93 | BWA# | |
| 94 | BWb# | |
| 95 | NC | BWc# |
| 96 | NC | BWd# |
| 97 | CE2 | |
| 98 | CE# | |
| 99 | SA | |
| 100 | SA | |

*Pin 50 is reserved for address expansion.

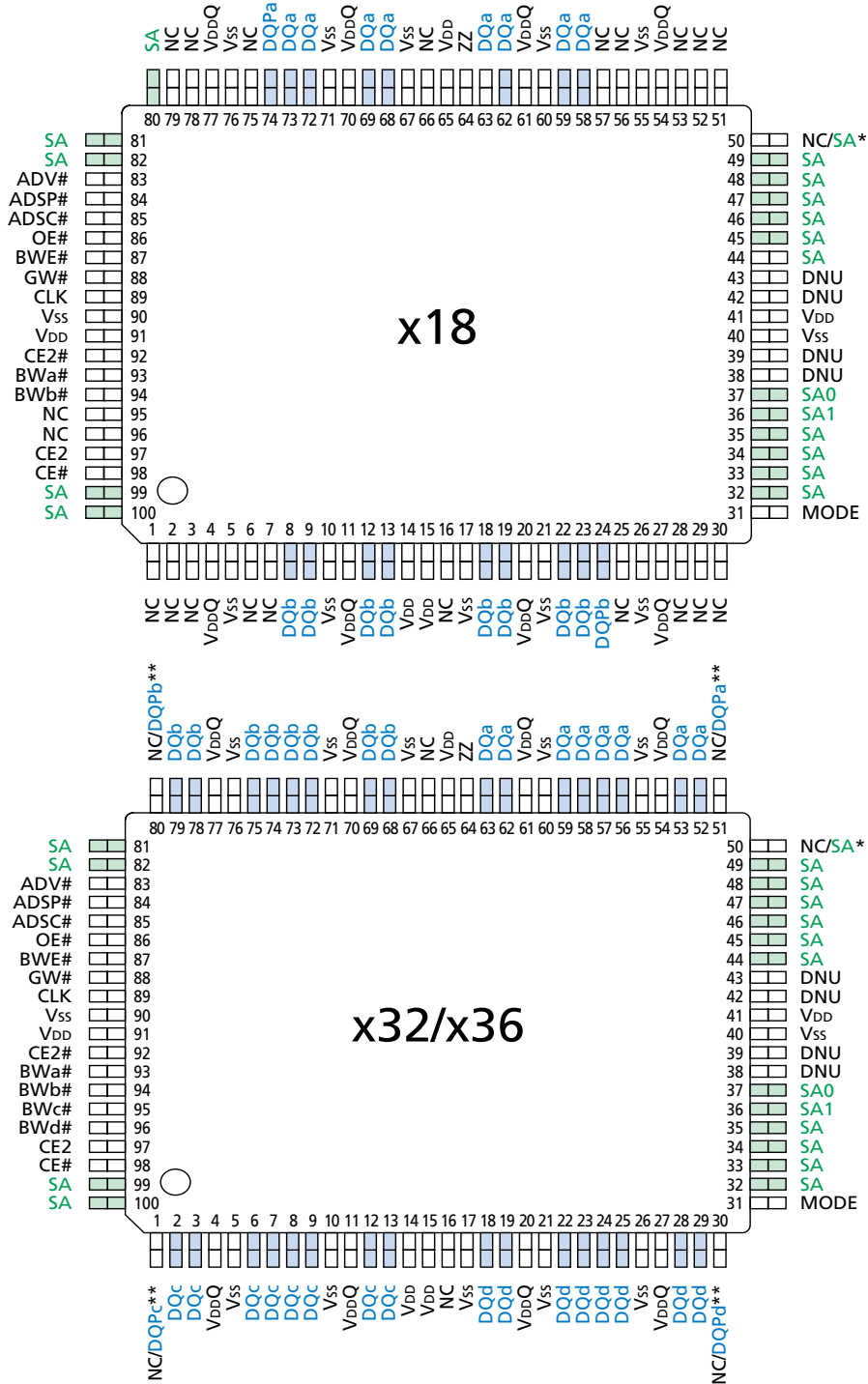
**No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

NOT RECOMMENDED FOR NEW DESIGNS



**2Mb: 128K x 18, 64K x 32/36
PIPELINED, SCD SYNCBURST SRAM**

**PIN ASSIGNMENT (Top View)
100-Pin TQFP**



*Pin 50 is reserved for address expansion.

**No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.



TQFP PIN DESCRIPTIONS

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|---|------------------------------|-------|---|
| 37 36 32-35, 44-49, 80-82, 99, 100 | 37 36 32-35, 44-49, 81, 82, 99, 100 | SA0 SA1 SA | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. |
| 93 94 – – | 93 94 95 96 | BWa# BWb# BWc# BWD# | Input | Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQP _a ; BWb# controls DQb pins and DQP _b . For the x32 and x36 versions, BWa# controls DQa pins and DQP _a ; BWb# controls DQb pins and DQP _b ; BWc# controls DQc pins and DQP _c ; BWD# controls DQd pins and DQP _d . Parity is only available on the x18 and x36 versions. |
| 87 | 87 | BWE# | Input | Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. |
| 88 | 88 | GW# | Input | Global Write: This active LOW input allows a full 18-, 32-, or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK. |
| 89 | 89 | CLK | Input | Clock: This signal registers the address, data, chip enable, byte write enables, and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| 98 | 98 | CE# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded. |
| 92 | 92 | CE2# | Input | Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded. |
| 97 | 97 | CE2 | Input | Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded. |
| 86 | 86 | OE# | Input | Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. |
| 83 | 83 | ADV# | Input | Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated. |
| 84 | 84 | ADSP# | Input | Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH. |

(continued)



TQFP PIN DESCRIPTIONS (continued)

| x18 | x32/x36 | SYMBOL | TYPE | DESCRIPTION |
|--|--|--|------------------|---|
| 85 | 85 | ADSC# | Input | Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH. |
| 31 | 31 | MODE | Input | Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating. |
| 64 | 64 | ZZ | Input | Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored. |
| (a) 58, 59, 62, 63, 68, 69, 72, 73 (b) 8, 9, 12, 13, 18, 19, 22, 23 | (a) 52, 53, 56-59, 62, 63 (b) 68, 69, 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29 | DQa DQb DQc DQd | Input/ Output | SRAM Data I/Os: For the x18 version, Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins. For the x32 and x36 versions, Byte "a" is associated with DQa pins; Byte "b" is associated with DQb pins; Byte "c" is associated with DQc pins; Byte "d" is associated with DQd pins. Input data must meet setup and hold times around the rising edge of CLK. |
| 74 24 – – | 51 80 1 30 | NC/DQPa NC/DQPb NC/DQPC NC/DQPD | NC/ I/O | No Connect/Parity Data I/Os: On the x32 version, these pins are No Connect (NC). On the x18 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb. On the x36 version, Byte "a" parity is DQPa; Byte "b" parity is DQPb; Byte "c" parity is DQPC; Byte "d" parity is DQPD. |
| 14, 15, 41, 65, 91 | 14, 15, 41, 65, 91 | V _{DD} | Supply | Power Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 4, 11, 20, 27, 54, 61, 70, 77 | 4, 11, 20, 27, 54, 61, 70, 77 | V _{DDQ} | Supply | Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range. |
| 5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90 | 5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90 | V _{SS} | Supply | Ground: GND. |
| 38, 39, 42, 43 | 38, 39, 42, 43 | DNU | – | Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation. |
| 1-3, 6, 7, 16, 25, 28-30, 51-53, 56, 57, 66, 75, 78, 79, 95, 96 | 16, 66 | NC | – | No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. |
| 50 | 50 | NC/SA | – | No Connect: This pin is reserved for address expansion. |



INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

| FIRST ADDRESS (EXTERNAL) | SECOND ADDRESS (INTERNAL) | THIRD ADDRESS (INTERNAL) | FOURTH ADDRESS (INTERNAL) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X00 | X...X11 | X...X10 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X10 | X...X01 | X...X00 |

LINEAR BURST ADDRESS TABLE (MODE = LOW)

| FIRST ADDRESS (EXTERNAL) | SECOND ADDRESS (INTERNAL) | THIRD ADDRESS (INTERNAL) | FOURTH ADDRESS (INTERNAL) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X10 | X...X11 | X...X00 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X00 | X...X01 | X...X10 |

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x18)

| FUNCTION | GW# | BWE# | BWa# | BWb# |
|-----------------|-----|------|------|------|
| READ | H | H | X | X |
| READ | H | L | H | H |
| WRITE Byte "a" | H | L | L | H |
| WRITE Byte "b" | H | L | H | L |
| WRITE All Bytes | H | L | L | L |
| WRITE All Bytes | L | X | X | X |

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x32/x36)

| FUNCTION | GW# | BWE# | BWa# | BWb# | BWc# | BWd# |
|-----------------|-----|------|------|------|------|------|
| READ | H | H | X | X | X | X |
| READ | H | L | H | H | H | H |
| WRITE Byte "a" | H | L | L | H | H | H |
| WRITE All Bytes | H | L | L | L | L | L |
| WRITE All Bytes | L | X | X | X | X | X |

NOTE: Using BWE# and BWa# through BWd#, any one or more bytes may be written.



TRUTH TABLE

| OPERATION | ADDRESS USED | CE# | CE2# | CE2 | ZZ | ADSP# | ADSC# | ADV# | WRITE# | OE# | CLK | DQ |
|-----------------------------|--------------|-----|------|-----|----|-------|-------|------|--------|-----|-----|--------|
| DESELECT Cycle, Power-Down | None | H | X | X | L | X | L | X | X | X | L-H | High-Z |
| DESELECT Cycle, Power-Down | None | L | X | L | L | L | X | X | X | X | L-H | High-Z |
| DESELECT Cycle, Power-Down | None | L | H | X | L | L | X | X | X | X | L-H | High-Z |
| DESELECT Cycle, Power-Down | None | L | X | L | L | H | L | X | X | X | L-H | High-Z |
| DESELECT Cycle, Power-Down | None | L | H | X | L | H | L | X | X | X | L-H | High-Z |
| SNOOZE MODE, Power-Down | None | X | X | X | H | X | X | X | X | X | X | High-Z |
| READ Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | L | L-H | Q |
| READ Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | H | L-H | High-Z |
| WRITE Cycle, Begin Burst | External | L | L | H | L | H | L | X | L | X | L-H | D |
| READ Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | L | L-H | Q |
| READ Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | H | L-H | High-Z |
| READ Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| READ Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L-H | High-Z |
| READ Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| READ Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L-H | High-Z |
| WRITE Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| WRITE Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| READ Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| READ Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L-H | High-Z |
| READ Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| READ Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L-H | High-Z |
| WRITE Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| WRITE Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

- NOTE:**
1. X means "Don't Care." # means active LOW. H means logic HIGH. L means logic LOW.
 2. For WRITE#, L means any one or more byte write enable signals (BWA#, BWB#, BWC# or BWD#) and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
 3. BWA# enables WRITES to DQa pins and DQP a. BWB# enables WRITES to DQb pins and DQP b. BWC# enables WRITES to DQc pins and DQP c. BWD# enables WRITES to DQd pins and DQP d. DQP a and DQP b are only available on the x18 and x36 versions. DQP c and DQP d are only available on the x36 version.
 4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
 5. Wait states are inserted by suspending burst.
 6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
 7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
 8. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

NOT RECOMMENDED FOR NEW DESIGNS



2Mb: 128K x 18, 64K x 32/36 PIPELINED, SCD SYNCBURST SRAM

ABSOLUTE MAXIMUM RATINGS*

| | |
|-------------------------------------|----------------------------------|
| Voltage on V _{DD} Supply | |
| Relative to V _{SS} | -0.5V to +4.6V |
| Voltage on V _{DDQ} Supply | |
| Relative to V _{SS} | -0.5V to +4.6V |
| V _{IN} | -0.5V to V _{DDQ} + 0.5V |
| Storage Temperature (plastic) | -55°C to +150°C |
| Junction Temperature** | +150°C |
| Short Circuit Output Current | 100mA |

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature, and airflow. See Micron Technical Note TN-05-14 for more information.

3.3V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD}, V_{DDQ} = +3.3V +0.3V/-0.165V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|-------------------------------|---|------------------|-------|-----------------------|-------|-------|
| Input High (Logic 1) Voltage | | V _{IH} | 2.0 | V _{DD} + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | | V _{IL} | -0.3 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DD} | I _{LI} | -1.0 | 1.0 | μA | 3 |
| Output Leakage Current | Output(s) disabled, 0V ≤ V _{IN} ≤ V _{DD} | I _{LO} | -1.0 | 1.0 | μA | |
| Output High Voltage | I _{OH} = -4.0mA | V _{OH} | 2.4 | – | V | 1, 4 |
| Output Low Voltage | I _{OL} = 8.0mA | V _{OL} | – | 0.4 | V | 1, 4 |
| Supply Voltage | | V _{DD} | 3.135 | 3.6 | V | 1 |
| Isolated Output Buffer Supply | | V _{DDQ} | 3.135 | 3.6 | V | 1, 5 |

- NOTE:**
- All voltages referenced to V_{SS} (GND).
 - Overshoot: V_{IH} ≤ +4.6V for t ≤ 1KC/2 for I ≤ 20mA
Undershoot: V_{IL} ≥ -0.7V for t ≤ 1KC/2 for I ≤ 20mA
Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V for t ≤ 200ms
 - MODE pin has an internal pull-up, and input leakage = ±10μA.
 - The load used for V_{OH}, V_{OL} testing is shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
 - V_{DDQ} should never exceed V_{DD}. V_{DD} and V_{DDQ} can be connected together for 3.3V I/O.



2.5V I/O DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V +0.3V/-0.165V; V_{DDQ} = +2.5V +0.4V/-0.125V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|-------------------------------|--|------------------|-------|------------------------|-------|-------|
| Input High (Logic 1) Voltage | Data bus (DQx) | V _{IHQ} | 1.7 | V _{DDQ} + 0.3 | V | 1, 2 |
| | Inputs | V _{IH} | 1.7 | V _{DD} + 0.3 | V | 1, 2 |
| Input Low (Logic 0) Voltage | | V _{IL} | -0.3 | 0.7 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{DD} | I _{LI} | -1.0 | 1.0 | μA | 3 |
| Output Leakage Current | Output(s) disabled, 0V ≤ V _{IN} ≤ V _{DDQ} (DQx) | I _{Lo} | -1.0 | 1.0 | μA | |
| Output High Voltage | I _{OH} = -2.0mA | V _{OH} | 1.7 | – | V | 1, 4 |
| | I _{OH} = -1.0mA | V _{OH} | 2.0 | – | V | 1, 4 |
| Output Low Voltage | I _{OL} = 2.0mA | V _{OL} | – | 0.7 | V | 1, 4 |
| | I _{OL} = 1.0mA | V _{OL} | – | 0.4 | V | 1, 4 |
| Supply Voltage | | V _{DD} | 3.135 | 3.6 | V | 1 |
| Isolated Output Buffer Supply | | V _{DDQ} | 2.375 | 2.9 | V | 1 |

- NOTE:**
- All voltages referenced to V_{SS} (GND).
 - Overshoot: V_{IH} ≤ +4.6V for t ≤ 'KC/2 for I ≤ 20mA
Undershoot: V_{IL} ≥ -0.7V for t ≤ 'KC/2 for I ≤ 20mA
Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V for t ≤ 200ms
 - MODE pin has an internal pull-up, and input leakage = ±10μA.
 - The load used for V_{OH}, V_{OL} testing is shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
 - V_{DDQ} should never exceed V_{DD}. V_{DD} and V_{DDQ} can be connected together for 3.3V I/O.



I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Note 1) (0°C ≤ T_A ≤ +70°C; V_{DD} = +3.3V +0.3V/-0.165V unless otherwise noted)

| DESCRIPTION | CONDITIONS | SYM | TYP | MAX | | | | UNITS | NOTES |
|---------------------------------|---|------------------|-----|-----|-----|------|-----|-------|---------|
| | | | | -5 | -6 | -7.5 | -10 | | |
| Power Supply Current: Operating | Device selected; All inputs ≤ V _{IL} or ≥ V _{IH} ; Cycle time ≥ ^t KC (MIN); V _{DD} = MAX; Outputs open | I _{DD} | 100 | 400 | 340 | 280 | 225 | mA | 2, 3, 4 |
| Power Supply Current: Idle | Device selected; V _{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V _{IH} ; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; Cycle time ≥ ^t KC (MIN) | I _{DD1} | 30 | 100 | 85 | 70 | 65 | mA | 2, 3, 4 |
| CMOS Standby | Device deselected; V _{DD} = MAX; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; All inputs static; CLK frequency = 0 | I _{SB2} | 0.5 | 10 | 10 | 10 | 10 | mA | 3, 4 |
| TTL Standby | Device deselected; V _{DD} = MAX; All inputs ≤ V _{IL} or ≥ V _{IH} ; All inputs static; CLK frequency = 0 | I _{SB3} | 6 | 25 | 25 | 25 | 25 | mA | 3, 4 |
| Clock Running | Device deselected; V _{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V _{IH} ; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; Cycle time ≥ ^t KC (MIN) | I _{SB4} | 30 | 100 | 85 | 70 | 65 | mA | 3, 4 |

TQFP CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | MAX | UNITS | NOTES |
|-------------------------------|---|-----------------|-----|-----|-------|-------|
| Control Input Capacitance | T _A = 25°C; f = 1 MHz; V _{DD} = 3.3V | C _I | 2.7 | 3.5 | pF | 5 |
| Input/Output Capacitance (DQ) | | C _O | 4 | 5 | pF | 5 |
| Address Capacitance | | C _A | 2.5 | 3.5 | pF | 5 |
| Clock Capacitance | | C _{CK} | 2.5 | 3.5 | pF | 5 |

- NOTE:**
1. V_{DDQ} = +3.3V +0.3V/-0.165V for 3.3V I/O configuration; V_{DDQ} = +2.5V +0.4V/-0.125V for 2.5V I/O configuration.
 2. I_{DD} is specified with no output current and increases with faster cycle times. I_{DDQ} increases with faster cycle times and greater output loading.
 3. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
 4. Typical values are measured at 3.3V, 25°C and 10ns cycle time.
 5. This parameter is sampled.

NOT RECOMENDED FOR NEW DESIGNS



**2Mb: 128K x 18, 64K x 32/36
PIPELINED, SCD SYNCBURST SRAM**

TQFP THERMAL RESISTANCE

| DESCRIPTION | CONDITIONS | SYMBOL | TYP | UNITS | NOTES |
|---|--|---------------|-----|-------|-------|
| Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | θ_{JA} | 40 | °C/W | 1 |
| Thermal Resistance (Junction to Top of Case) | | θ_{JC} | 8 | °C/W | 1 |

NOTE: 1. Typical values are measured at 3.3V, 25°C and 10ns cycle time.



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 1) ($0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$; $V_{DD} = +3.3\text{V} +0.3\text{V}/-0.165\text{V}$)

| DESCRIPTION | SYMBOL | -5 | | -6 | | -7.5 | | -10 | | UNITS | NOTES |
|---|------------|-----|-----|-----|-----|------|-----|-----|-----|-------|------------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Clock | | | | | | | | | | | |
| Clock cycle time | t_{KC} | 5.0 | | 6.0 | | 7.5 | | 10 | | ns | |
| Clock frequency | f_{KF} | | 200 | | 166 | | 133 | | 100 | MHz | |
| Clock HIGH time | t_{KH} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns | 2 |
| Clock LOW time | t_{KL} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns | 2 |
| Output Times | | | | | | | | | | | |
| Clock to output valid | t_{KQ} | | 3.5 | | 3.5 | | 4.0 | | 5.0 | ns | |
| Clock to output invalid | t_{KQX} | 1.0 | | 1.5 | | 1.5 | | 1.5 | | ns | 3 |
| Clock to output in Low-Z | t_{KQLZ} | 0 | | 1.5 | | 1.5 | | 1.5 | | ns | 3, 4, 5, 6 |
| Clock to output in High-Z | t_{KQHZ} | | 3.5 | | 3.5 | | 4.0 | | 5.0 | ns | 3, 4, 5, 6 |
| OE# to output valid | t_{OEQ} | | 3.5 | | 3.5 | | 4.0 | | 5.0 | ns | 7 |
| OE# to output in Low-Z | t_{OELZ} | 0 | | 0 | | 0 | | 0 | | ns | 3, 4, 5, 6 |
| OE# to output in High-Z | t_{OEHZ} | | 3.0 | | 3.5 | | 4.0 | | 4.5 | ns | 3, 4, 5, 6 |
| Setup Times | | | | | | | | | | | |
| Address | t_{AS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns | 8, 9 |
| Address status (ADSC#, ADSP#) | t_{ADSS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns | 8, 9 |
| Address advance (ADV#) | t_{AAS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns | 8, 9 |
| Write signals (BWA#-BWD#, BWE#, GW#) | t_{WS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns | 8, 9 |
| Data-in | t_{DS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns | 8, 9 |
| Chip enables (CE#, CE2#, CE2) | t_{CES} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns | 8, 9 |
| Hold Times | | | | | | | | | | | |
| Address | t_{AH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns | 8, 9 |
| Address status (ADSC#, ADSP#) | t_{ADSH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns | 8, 9 |
| Address advance (ADV#) | t_{AAH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns | 8, 9 |
| Write signals (BWA#-BWD#, BWE#, GW#) | t_{WH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns | 8, 9 |
| Data-in | t_{DH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns | 8, 9 |
| Chip enables (CE#, CE2#, CE2) | t_{CEH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns | 8, 9 |

- NOTE:**
1. Test conditions as specified with the output loading shown in Figure 1 for 3.3V I/O ($V_{DDQ} = +3.3\text{V} +0.3\text{V}/-0.165\text{V}$) and Figure 3 for 2.5V I/O ($V_{DDQ} = +2.5\text{V} +0.4\text{V}/-0.125\text{V}$) unless otherwise noted.
 2. Measured as HIGH above V_{IH} and LOW below V_{IL} .
 3. This parameter is measured with the output loading shown in Figure 2 for 3.3V I/O and Figure 4 for 2.5V I/O.
 4. This parameter is sampled.
 5. Transition is measured $\pm 500\text{mV}$ from steady state voltage.
 6. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
 7. OE# is a "Don't Care" when a byte write enable is sampled LOW.
 8. A WRITE cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ADSC# or ADV# LOW or ADSP# LOW for the required setup and hold times.
 9. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP# or ADSC# is LOW to remain enabled.



3.3V I/O AC TEST CONDITIONS

| | |
|-------------------------------------|--------------------------------|
| Input pulse levels | $V_{IH} = (V_{DD}/2.2) + 1.5V$ |
| | $V_{IL} = (V_{DD}/2.2) - 1.5V$ |
| Input rise and fall times | 1ns |
| Input timing reference levels | $V_{DD}/2.2$ |
| Output reference levels | $V_{DD}Q/2.2$ |
| Output load | See Figures 1 and 2 |

2.5V I/O AC TEST CONDITIONS

| | |
|-------------------------------------|----------------------------------|
| Input pulse levels | $V_{IH} = (V_{DD}/2.64) + 1.25V$ |
| | $V_{IL} = (V_{DD}/2.64) - 1.25V$ |
| Input rise and fall times | 1ns |
| Input timing reference levels | $V_{DD}/2.64$ |
| Output reference levels | $V_{DD}Q/2$ |
| Output load | See Figures 3 and 4 |

3.3V I/O Output Load Equivalentts

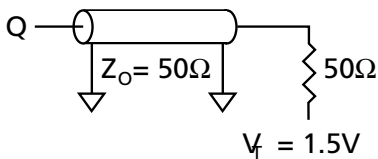


Figure 1

2.5V I/O Output Load Equivalentts

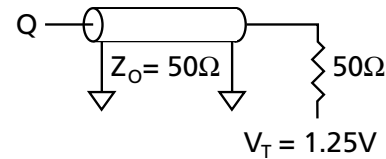


Figure 3

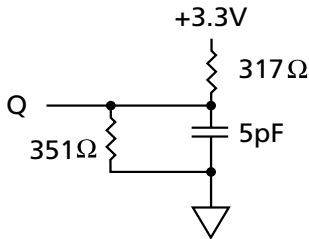


Figure 2

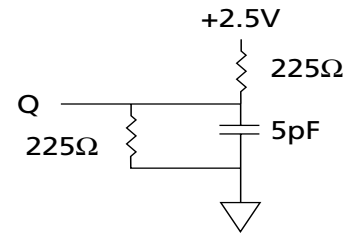


Figure 4

LOAD DERATING CURVES

The Micron 128K x 18, 64K x 32, and 64K x 36 SyncBurst SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.



SNOOZE MODE

SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to I_{SB2Z} . The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

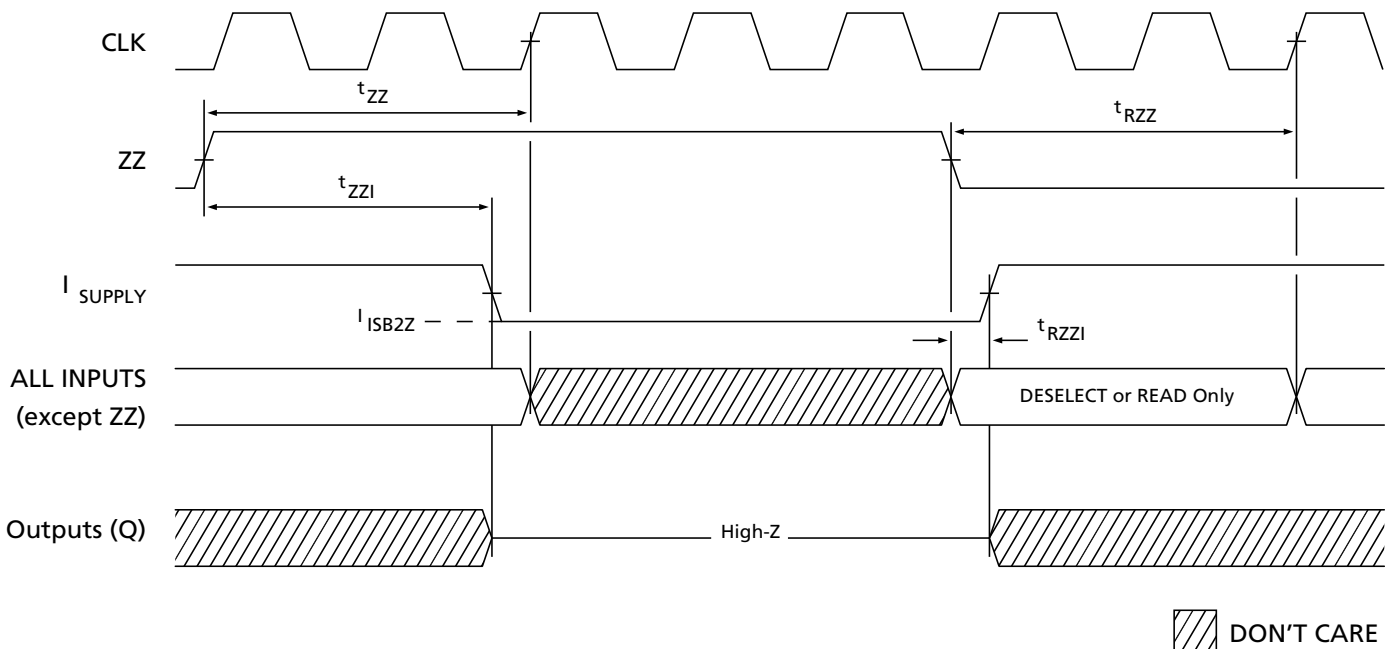
The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------------|------------------|------------|-------------|-------------|-------|-------|
| Current during SNOOZE MODE | $ZZ \geq V_{IH}$ | I_{SB2Z} | | 10 | mA | |
| ZZ active to input ignored | | t_{ZZ} | | $2(t_{KC})$ | ns | 1 |
| ZZ inactive to input sampled | | t_{RZZ} | $2(t_{KC})$ | | ns | 1 |
| ZZ active to snooze current | | t_{ZZI} | | $2(t_{KC})$ | ns | 1 |
| ZZ inactive to exit snooze current | | t_{RZZI} | 0 | | ns | 1 |

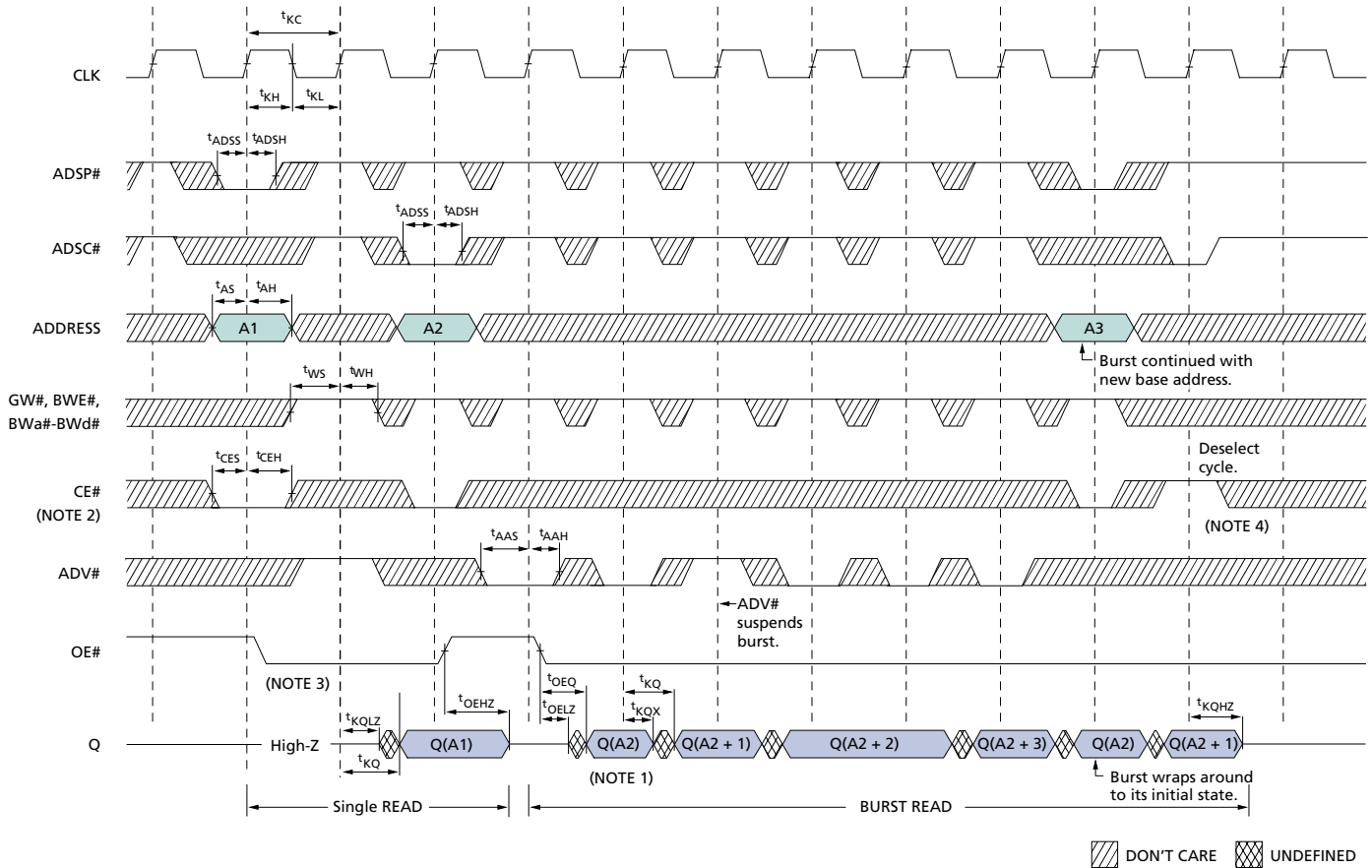
NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM





READ TIMING



READ TIMING PARAMETERS

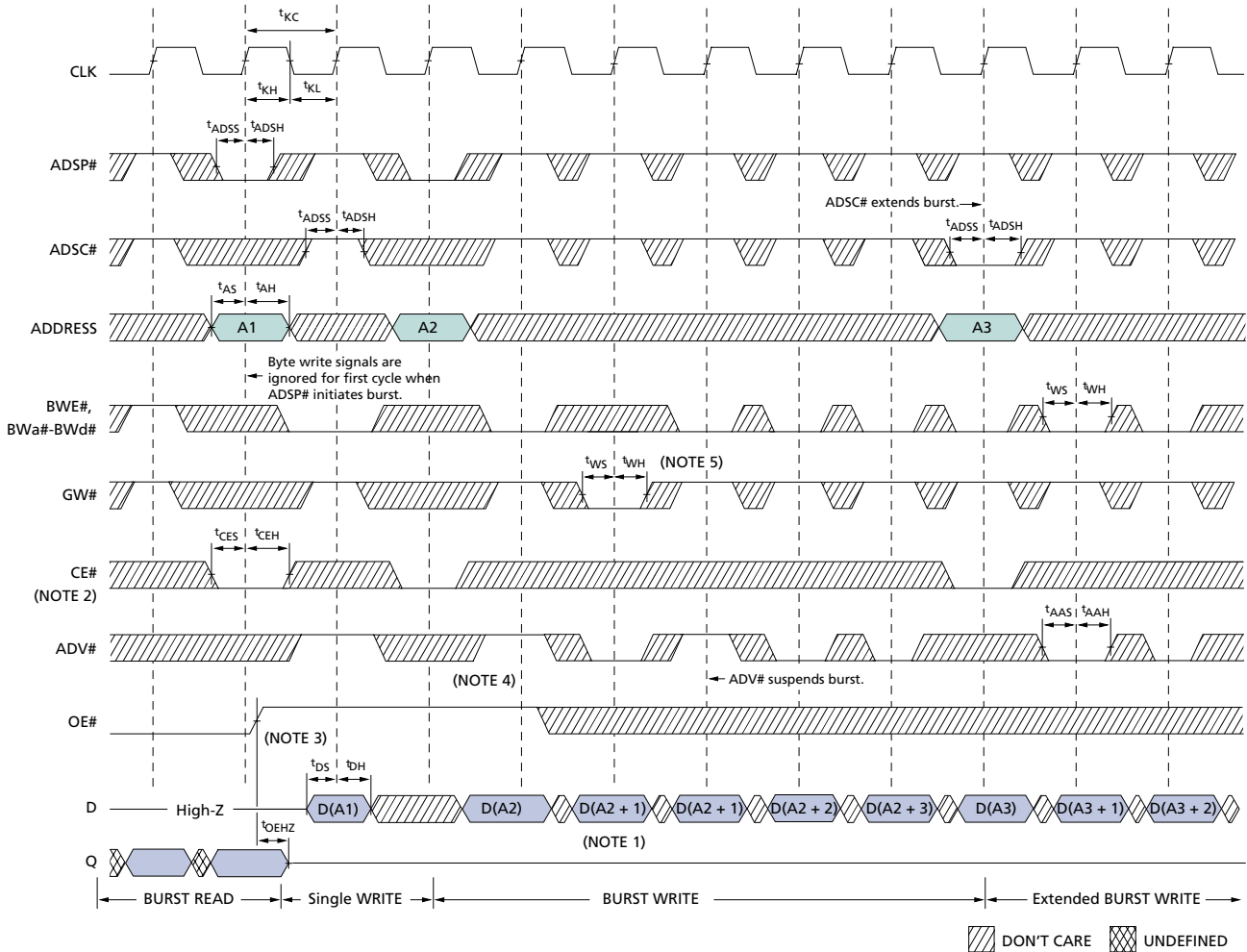
| SYMBOL | -5 | | -6 | | -7.5 | | -10 | | UNITS |
|-------------------|-----|-----|-----|-----|------|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{KC} | 5.0 | | 6.0 | | 7.5 | | 10 | | ns |
| f _{KF} | | 200 | | 166 | | 133 | | 100 | MHz |
| t _{KH} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns |
| t _{KL} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns |
| t _{KQ} | | 3.5 | | 3.5 | | 4.0 | | 5.0 | ns |
| t _{KQX} | 1.0 | | 1.5 | | 1.5 | | 1.5 | | ns |
| t _{KQLZ} | 0 | | 1.5 | | 1.5 | | 1.5 | | ns |
| t _{KQHZ} | | 3.5 | | 3.5 | | 4.0 | | 5.0 | ns |
| t _{OEQ} | | 3.5 | | 3.5 | | 4.0 | | 5.0 | ns |
| t _{OELZ} | 0 | | 0 | | 0 | | 0 | | ns |
| t _{OEHZ} | | 3.0 | | 3.5 | | 4.0 | | 4.5 | ns |

| SYMBOL | -5 | | -6 | | -7.5 | | -10 | | UNITS |
|-------------------|-----|-----|-----|-----|------|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{AS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{ADSS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{AAS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{WS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{CES} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{AH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{ADSH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{AAH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{WH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{CEH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

- NOTE:**
1. Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
 2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
 3. Timing is shown assuming that the device was not enabled before entering into this sequence. OE# does not cause Q to be driven until after the following clock rising edge.
 4. Outputs are disabled within one clock cycle after deselect.



WRITE TIMING



WRITE TIMING PARAMETERS

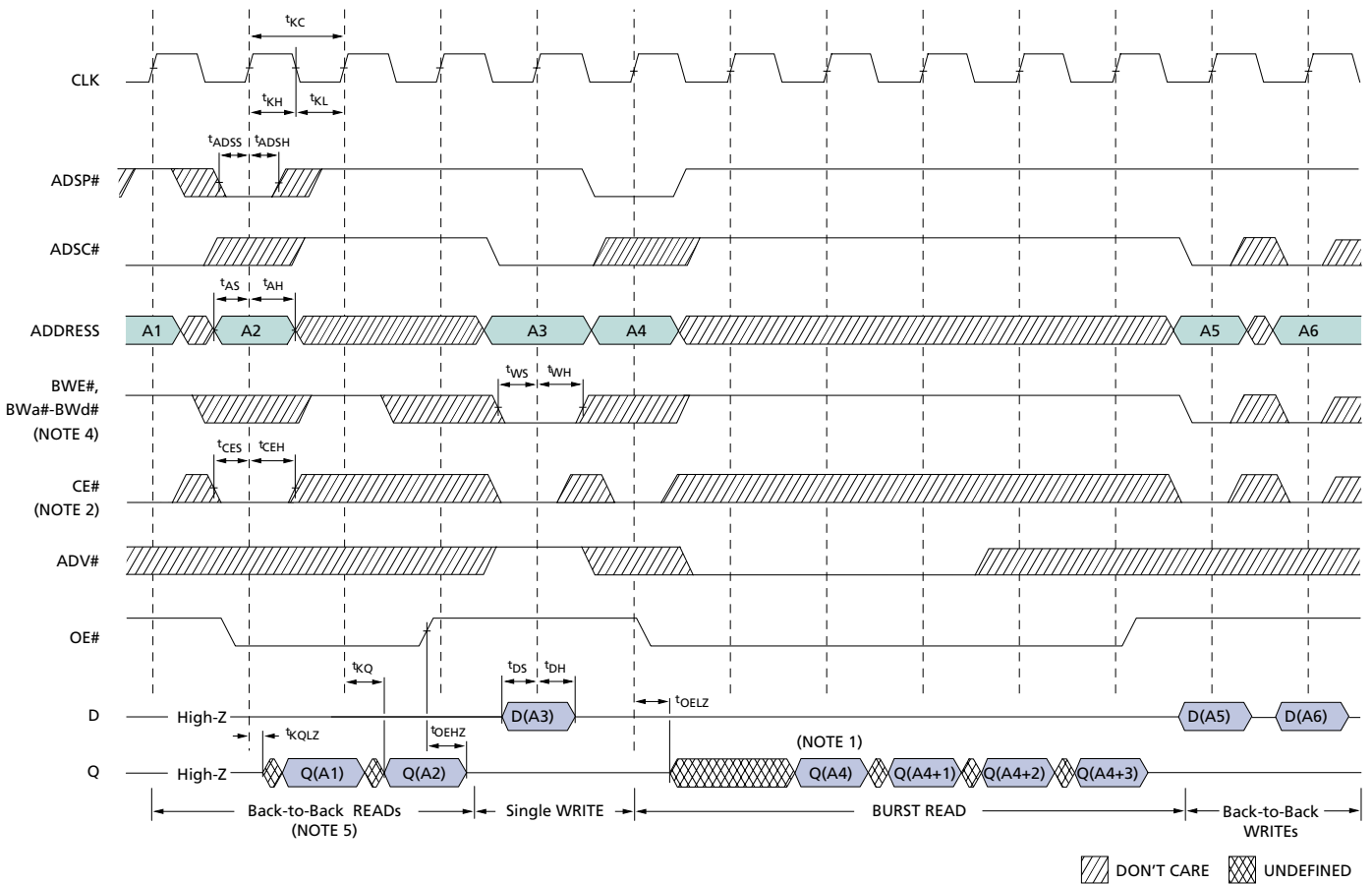
| SYMBOL | -5 | | -6 | | -7.5 | | -10 | | UNITS |
|-------------------|-----|-----|-----|-----|------|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{KC} | 5.0 | | 6.0 | | 7.5 | | 10 | | ns |
| t _{KF} | | 200 | | 166 | | 133 | | 100 | MHz |
| t _{KH} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns |
| t _{KL} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns |
| t _{OEHZ} | | 3.0 | | 3.5 | | 4.0 | | 4.5 | ns |
| t _{AS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{ADSS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{AAS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{WS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |

| SYMBOL | -5 | | -6 | | -7.5 | | -10 | | UNITS |
|-------------------|-----|-----|-----|-----|------|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{DS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{CES} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{AH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{ADSH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{AAH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{WH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{DH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{CEH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

- NOTE:**
1. D(A2) refers to input for address A2. Q(A2 + 1) refers to input for the next internal burst address following A2.
 2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
 3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
 4. ADV# must be HIGH to permit a WRITE to the loaded address.
 5. Full-width WRITE can be initiated by GW# LOW; or GW# HIGH and BWE#, BWA# and BWD# LOW for x18 device; or GW# HIGH and BWE#, BWA#-BWD# LOW for x32 and x36 devices.



READ/WRITE TIMING



READ/WRITE TIMING PARAMETERS

| SYMBOL | -5 | | -6 | | -7.5 | | -10 | | UNITS |
|-------------------|-----|-----|-----|-----|------|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{KC} | 5.0 | | 6.0 | | 7.5 | | 10 | | ns |
| t _{KF} | | 200 | | 166 | | 133 | | 100 | MHz |
| t _{KH} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns |
| t _{KL} | 1.6 | | 1.7 | | 1.9 | | 3.2 | | ns |
| t _{KQ} | | 3.5 | | 3.5 | | 4.0 | | 5.0 | ns |
| t _{KQLZ} | 0 | | 1.5 | | 1.5 | | 1.5 | | ns |
| t _{OELZ} | 0 | | 0 | | 0 | | 0 | | ns |
| t _{OEHZ} | | 3.0 | | 3.5 | | 4.0 | | 4.5 | ns |
| t _{AS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |

| SYMBOL | -5 | | -6 | | -7.5 | | -10 | | UNITS |
|-------------------|-----|-----|-----|-----|------|-----|-----|-----|-------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{ADSS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{WS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{DS} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{CES} | 1.5 | | 1.5 | | 1.5 | | 2.2 | | ns |
| t _{AH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{ADSH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{WH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{DH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |
| t _{CEH} | 0.5 | | 0.5 | | 0.5 | | 0.5 | | ns |

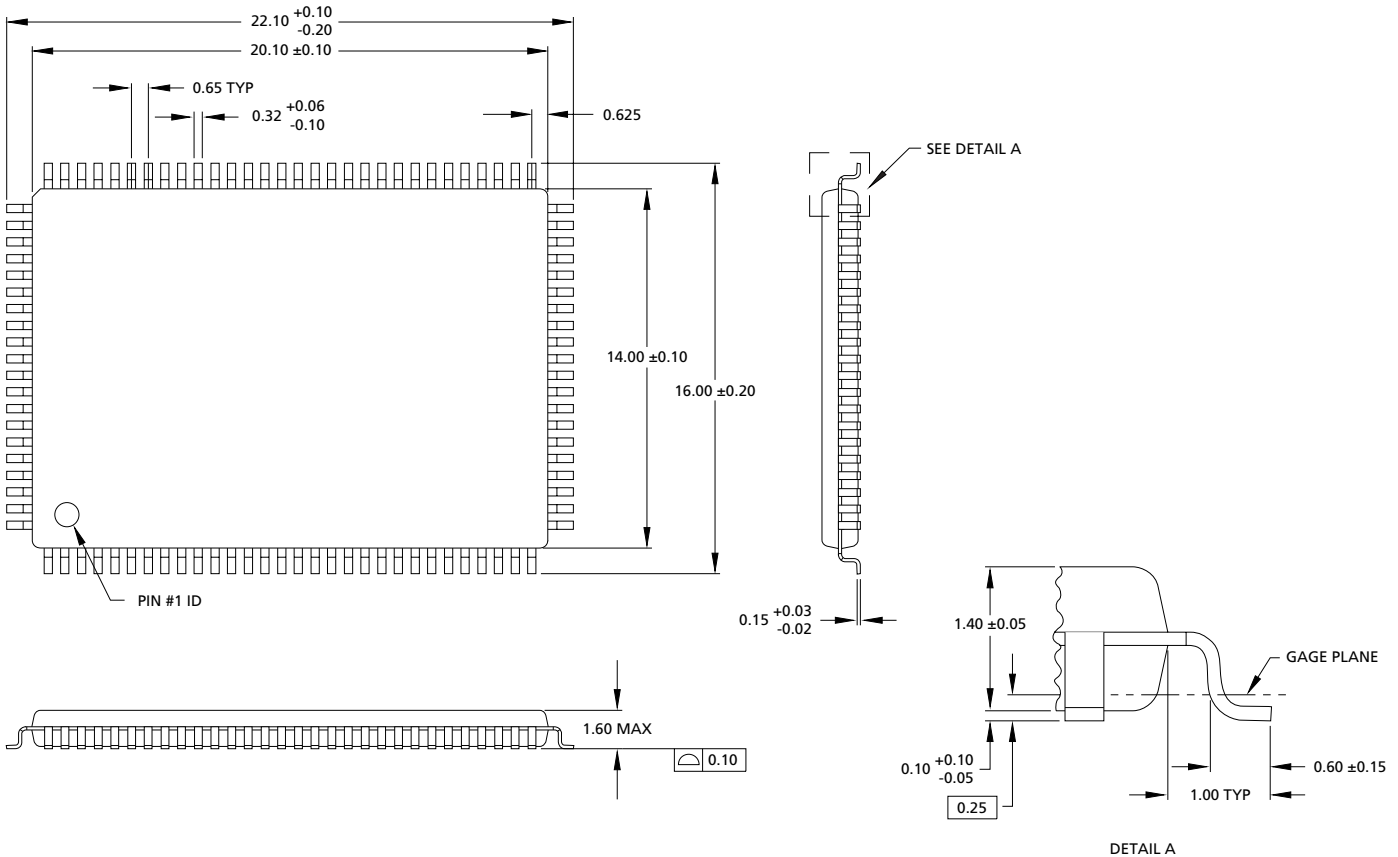
- NOTE:**
1. Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
 2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
 3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC# or ADV# cycle is performed.
 4. GW# is HIGH.
 5. Back-to-back READs may be controlled by either ADSP# or ADSC#.

NOT RECOMENDED FOR NEW DESIGNS



**2Mb: 128K x 18, 64K x 32/36
PIPELINED, SCD SYNCBURST SRAM**

100-PIN PLASTIC TQFP (JEDEC LQFP)



- NOTE:**
1. All dimensions in millimeters MAX or typical here noted.
MIN
 2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

DATA SHEET DESIGNATIONS

No Marking: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

E-mail: prodmktg@micron.com, Internet: <http://www.micron.com>, Customer Comment Line: 800-932-4992

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REVISION HISTORY

- Added “NOT RECOMENDED FOR NEW DESIGNS,” REV. C, Pub. 11/02, FINAL November/22/02
- Removed 165-pin FBGA package, Rev. 6/01 June/7/01
- Removed FBGA Part Marking Guide, REV 8/00, FINAL August/22/00
- Changed FBGA capacitance values, REV 8/00, FINAL August/7/00
Ci; TYP 2.5pF from 4pF; MAX. 3.5pF from 5pF
Co; TYP 4pF from 6pF; MAX. 5pF from 7pF
Cck; TYP 2.5pF from 5pF; MAX. 3.5pF from 6pF
- Removed IT References, REV 7/00, FINAL July/14/00
Added FBGA Part Marking Guide
Added Revision History to Datasheet
- Removed IT from Part Number Example, REV 6/00, FINAL June/21/00
Added # of datalines to the databus in x32/36 Block Diagram
Added Note - “Preliminary Package Data” to FBGA Capacitance and Thermal Resistance Tables
Changed heading on Mechanical Drawing from BGA to FBGA
- Added 165-Pin FBGA package, REV 3/00, FINAL March/3/00
Added PRELIMINARY PACKAGE DATA to diagram