CX28224/5/9
Inverse Multiplexing for ATM (IMA) Family

Data Sheet

28229-DSH-001-B
January 2003

MINDSPEED™

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX28224	28224-14	D	256-pin, 17 mm BGA	–40 °C to 85 °C
CX28225	28225-14	D	256-pin, 17 mm BGA	–40 °C to 85 °C
CX28229	28229-14	D	256-pin, 17 mm BGA	–40 °C to 85 °C

Revision History

Revision	Level	Date	Description
A	Preliminary	July 2001	Preliminary A version. Note that this document was also released as a preliminary version under the document numbers 101265P1 and 101265P2.
B	Preliminary	September 2001	Preliminary B version.
C	Preliminary	September 2001	Removed all references to PLCP and updated some of the bit descriptions.
D	Preliminary	April 2002	Restructured and enhanced document to include more IMA related information.
E	Preliminary	May 2002	Updated Ordering Information and a few register descriptions to reflect the CX28229-13 part.
F	Preliminary	September 2002	Updated to reflect the -14 part. Section 8, Electrical and Mechanical Specifications, improved and noted with change bars.
A	Released	January 2003	Revised document number to reflect new numbering system: new document number is 28229-DSH-001-B. Removed Prelimary document designations. Replaced hysteresis references with TTL levels in Table 8-16.

CX28224/5/9

Inverse Multiplexing for ATM (IMA) Family

The CX2822x family of devices provides system designers with a complete integrated IMA solution for up to 32 ports. All devices include a Transmission Convergence block to perform cell delineation, on-board RAM to meet ATM forum requirements for differential delay compensation and a dual mode (UTOPIA or Serial) PHY layer interface.

Source code for all required software functions is available from Mindspeed. Since all processing intensive functions are performed in hardware, they require only minimal overhead from the system processor.

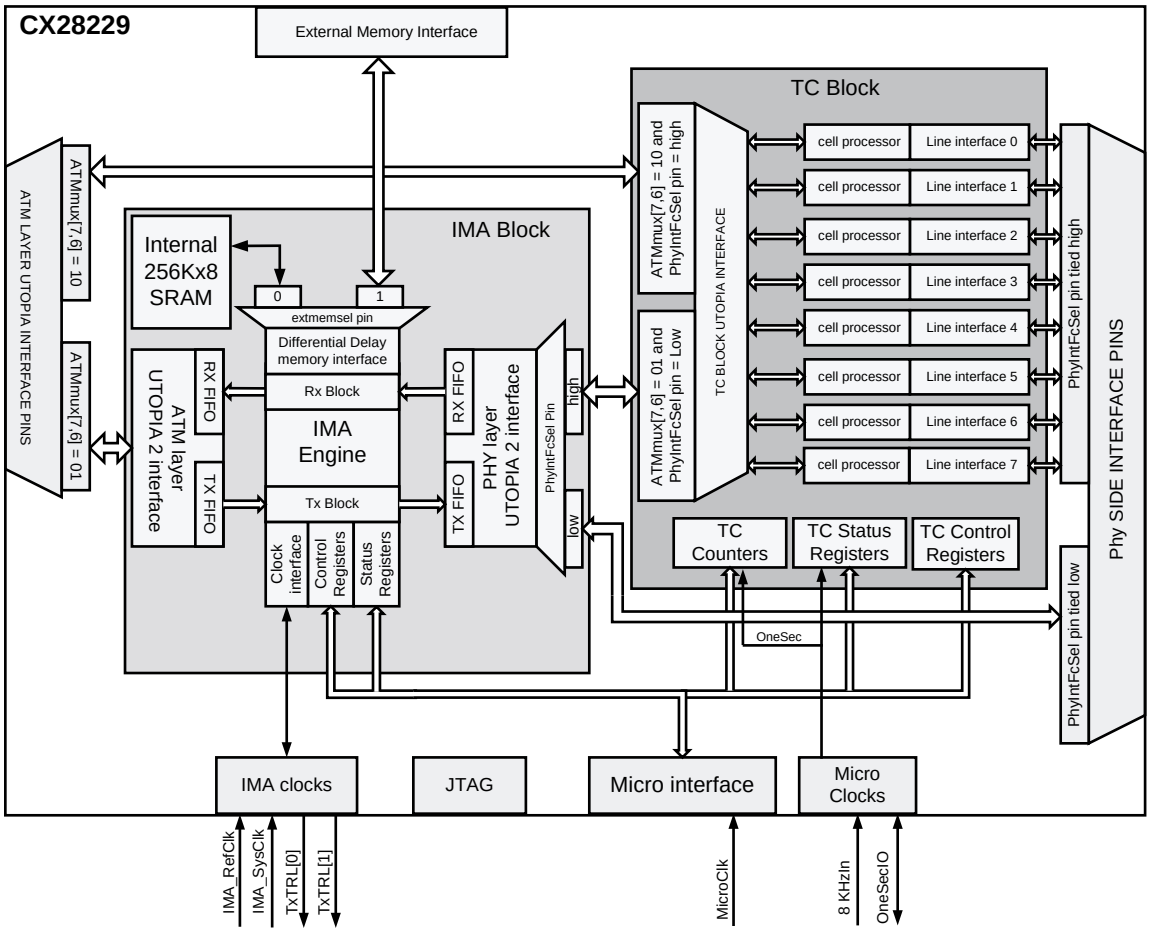
The TC block is capable of bit level cell delineation, which allows for direct connection DSL serial data streams without a frame sync pulse. Individual ports can be operated in a 'pass thru' mode without the IMA overhead.

The CX28229 provides direct connection to 8 serial links or can be expanded to a 32 port IMA using the PHY side UTOPIA bus and external TC devices such as the RS8228. In addition, an external memory bus allows the differential delay memory to access up to 2 Mbytes of external RAM.

Distinguishing Features

- Complete IMA solution in a single package
  - 2 port, CX28224, 17mm BGA
  - 4 port, CX28225, 17mm BGA
  - 8/32 port, CX28229, 17mm BGA
- Field tested software available
- Supports up to 32 ports using external TC PHYs
- Up to 16 IMA groups
- Supports the IMA standard requirements for 25 ms differential delay with 256K Internal memory
- Memory expandable to 2 M bytes via external bus (CX28229 only)
- UTOPIA level 2 interfaces
- Glueless interface to Mindspeed Framers
- Octet or Bit level cell delineation
- Variable link data rates (64K–3.072 Mb/s)

Functional Block Diagram



IMA Features

- Field proven design
- All software available
- Supports variable link data rates (64K–3.072 Mb/s)
- Internal memory
- Connects directly to the Mindspeed SARs for inexpensive CPE solutions
- CX28224 2 ports
- CX28225 4 ports
- CX28229 32 ports
  - Memory expandable to 2 M bytes via external bus
  - Up to 16 independent groups (using external PHYs):
    Each group can have up to 8 links.
- Supports IMA versions 1.0 and 1.1
- Fractional T1/E1

Cell Delineation Section

- Supports ATM cell interface for:
  - Circuit-based physical layer
  - Cell-based physical layer
- Performs single-bit HEC correction and single- or multiple-bit detection
- Inserts headers and generates HEC
- Direct connection to external Mindspeed components for:
  - T1/E1
  - xDSL
  - General purpose mode
- Byte-level or bit-level cell delineation

Control and Status

Microprocessor Interface

- Asynchronous SRAM-like interface mode
- Synchronous, glueless Bt8233/RS8234 SAR interface mode
- 8-bit data bus
- Open-drain interrupt output
- Open-drain ready output
- 8–33 MHz operation
- All control registers are read/write

UTOPIA Interfaces

- UTOPIA Level 2 Interface to ATM Layer:
  - 8/16 bit operation
  - 50 MHz
- PHY-side UTOPIA Interface:
  - 8-bit UTOPIA Level 2
  - Supports 32 ports via dual CLAV and Enable lines

Counters/Status Register Section

- Summary interrupt indications
- Configuration of interrupt enables
- One-second counter latching
- Counters for:
  - LOCD events
  - Corrected HEC errors
  - Uncorrected HEC errors
  - Transmitted cells
  - Matching received cells
  - Non-matching received cells

Contents

Figures

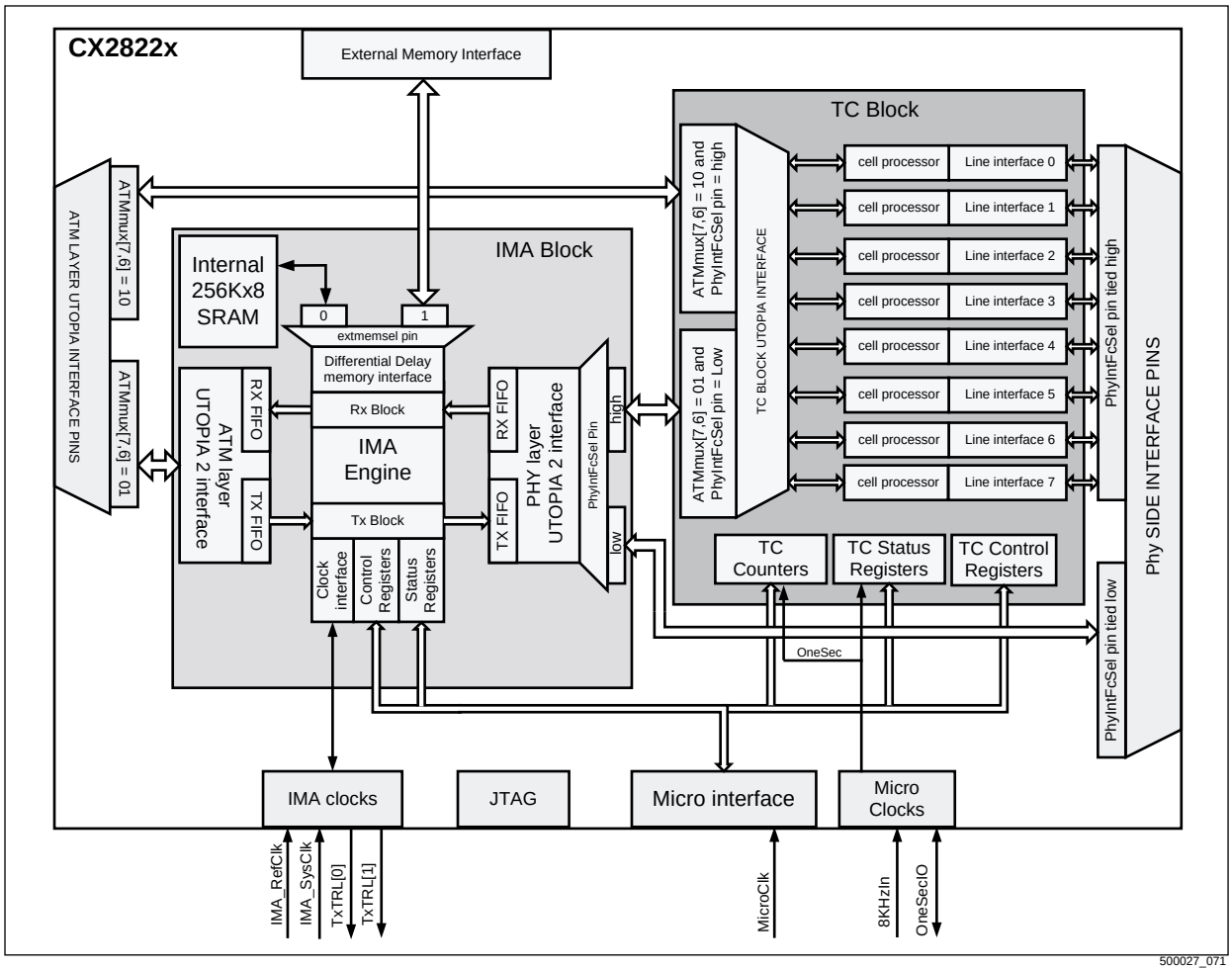
Tables

1 Introduction to IMA

This chapter provides a basic introduction to IMA. It will introduce common terminology, the IMA frame format and IMA Cell structure. It will also address one of the challenges of IMA: differential delay between links. For detailed coverage of these topics the reader should refer to the ATM forum's standard for IMA.

The CX2822x is composed of the following major functional blocks as shown in Figure 1-1.

Figure 1-1. Block DIagram



1.1 Introduction To Inverse Multiplexing for ATM

Bandwidth, or the lack thereof, has always been the main challenge of telecommunications. While numerous standards for high speed connections have been around for years, the cost of these higher speed connections often prohibit users from deploying them. For example, users who need a data rate higher than the standard T1, (1.544 Mbps) must pay for an entire DS3 (44 Mbps). Often the extra cost cannot be justified.

IMA solves this problem by allowing users to purchase bandwidth in smaller increments and combine these smaller 'pipes' into one high speed connection. An example is given in Figure 1-2 where 3 T1 lines are combined into one 4.6 Mbps data link.

At first glance, the concept of IMA is deceptively simple: spread the ATM cells out evenly over the available individual lines. However, many serious technical issues must be dealt with and a wide range of functions must be supported. These include IMA framing, differential delay accommodation, link/group state machines, IMA clocking, and maintenance. Several terms must be defined:

IMA Engine — The logic that performs the actual IMA function. This sits between the ATM layer and the individual links (see Figure 1-2). An IMA engine can control multiple independent groups.

Link — Refers to an individual physical connection such as a T1 or DSL line. Each link has an individual UTOPIA address or serial connection to the IMA engine.

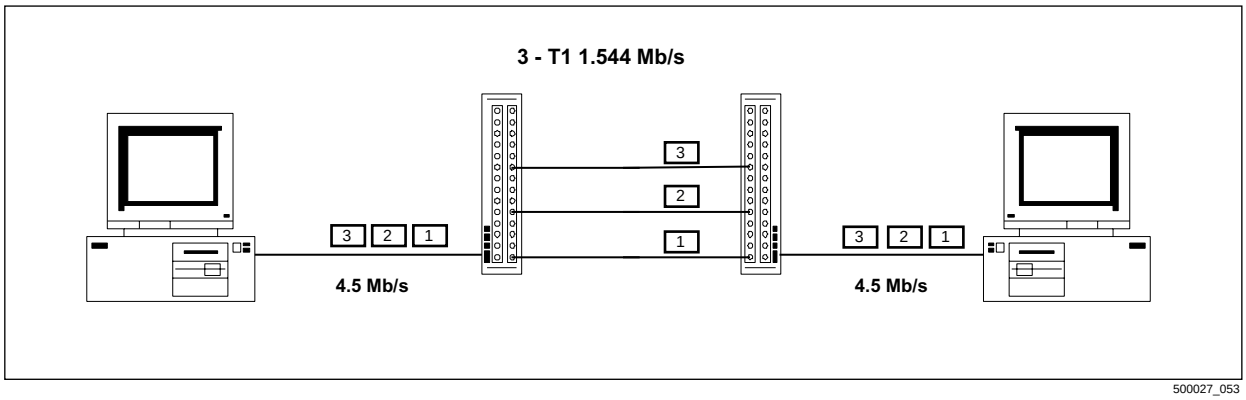
Group — An IMA group is composed of links. A group appears as a single UTOPIA address to the ATM layer. Thus an IMA-4 group would have 4 individual links.

Group State Machine — The operation of the IMA group is governed by the Group State Machine (GSM), the Group Traffic State Machine (GTSM), and the Link Addition and Slow Recovery (LASR) procedure. These three processes ensure reliable transmission and reception of ATM layer cells across all links in the Active state. This includes the negotiation of group parameters (i.e., symmetry and M values), the bringing up of the IMA group, and the graceful addition/recovery and deletion of links to and from the group. For the CX28229, this function is performed in the host software. The software itself is available from Mindspeed.

Link State Machine

A Link State Machine (LSM) is defined for the transmit and receive directions of each IMA link. The IMA protocol is defined to allow symmetric or asymmetric cell rate transfer over the IMA virtual link. It allows for smooth introduction of each link in the group. It also allows graceful handling of error conditions and removal of a link. This function is performed internally by the CX28229.

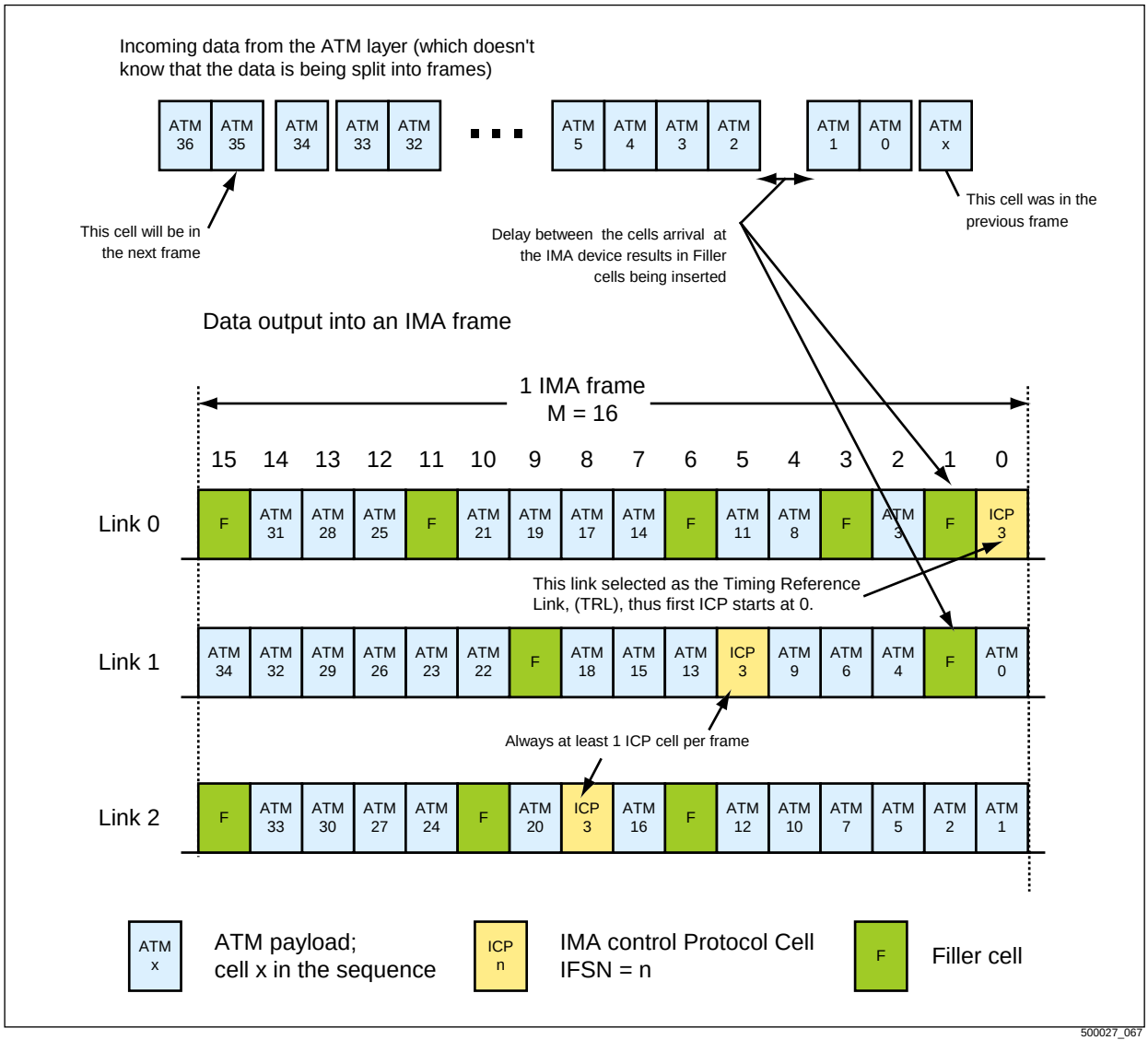
Figure 1-2. IMA Overview



1.1.1 IMA Framing

The IMA protocol employs a simple frame structure as shown in Figure 1-3. It consists of a single IMA overhead cell (ICP) and M – 1 ATM layer cells, where M is the IMA frame length. Valid frame lengths are 32, 64, 128 (default), or 256. This example shows a group composed of three links and an IMA frame length of 16. (An invalid frame length of 16 is used for brevity, the default frame length is 128.)

Figure 1-3. IMA Frame; Length = 16; Number of links = 3



Since the ATM layer data rate is often less than the bandwidth available across the links in the IMA group, the IMA engine generates IMA Filler cells when no ATM layer cells are available. (The IMA Filler cells perform the same basic function as Idle cells in a non-IMA ATM system and are discarded by the IMA receiver.)

The IMA frame rate is intentionally set slightly below the available payload bandwidth of the IMA link. To allow for timing differences between the links in a group, the IMA standard requires that the system insert an extra ICP cell every 2049

cells. This cell is called the SICP cell and is inserted immediately after the normal ICP cell for that link and results in the frame being M+1 cells long. Information in the ICP cell payload signals the insertion of these cells so that the receiver does not lose framing and can identify and discard these cells. For further details consult the IMA standard.

One link in each group is designated the Timing Reference Link (TRL). All timing issues for the group are relative to this link.

1.1.2 IMA Control Protocol Cells

The IMA Standard defines three types of IMA cells: IMA Control Protocol (ICP) cells, Filler cells, and ATM layer cells. ICP cells are the IMA overhead cells that carry the IMA control and status information between both ends of the link, assuring synchronization and configuration. The purpose of filler cells is rate decoupling; they are inserted into the IMA stream if no ATM layer cells are available.

NOTE: Standard ATM 'idle' cells are never transmitted over an IMA link.

ATM layer cells are the data “payload” carried by the IMA group. These are the standard ATM cells being sent from the ATM layer.

Table 1-1 describes the IMA Overhead Cell definition, and Table 1-2 lists format of the IMA Overhead Stuff Cell.

Table 1-1. IMA Overhead Cell Definition *(1 of 3)*

Octet	Field	Description
1-5	ATM Cell Header	OAM cell type: Octet 1 = 0000 0000 Octet 2 = 0000 0000 Octet 3 = 0000 0000 Octet 4 = 0000 1011 Octet 5 = 0110 0100 (valid HEC with Coset)
6	IMA Label	OAM type field: 0000 0001—IMA Version 1.0 0000 0011—IMA Version 1.1
7	Cell ID Link ID	Bit 7 Set to 1 for ICP cell Bits 6–5 Unused and set to 0 Bits 4–0 Logical ID for physical link range (0... 31)
8	Frame Sequence Number	Cyclical counter: 0 to 255
9	ICP Cell Offset	Indicates position of ICP cell within the IMA frame of size *M* cells. Range: (0... *M* – 1)

Table 1-1. IMA Overhead Cell Definition *(2 of 3)*

Octet	Field	Description
10	Link Stuff Indication (LSI)	Stuff Indication code for link on which ICP cell is being sent Bits 7–3 Unused and set to 0 Bits 2–0 111: no imminent stuff (default) 100: stuff event in 4 ICP cell locations (optional) 011: stuff event in 3 ICP cell locations (optional) 010: stuff event in 2 ICP cell locations (optional) 001: stuff event at the next ICP cell location (mandatory) 000: This is one out of the 2 ICP cells comprising the stuff event (mandatory)
11	Status / Control Change Indication (SCCI)	Status and Control Change Indication: 0 to 255 and cycling (count to be incremented every time there is a change to octets 12 to 49).
12	IMA ID	Logical IMA group ID
13	Group Status & Control	Bits 7–4 Group Status 0000: Start-up 0001: Start-up-Ack 0010: Config-Aborted: Unsupported M 0011: Config-Aborted: Incompatible Symmetry 0100: Config-Aborted: Unsupported IMA version 01xx: Available for other Config Abort reasons 1000: Insufficient-Links 1001: Blocked 1010: Operational Bits 3–2 Others: Reserved Symmetry of Group 00: Symmetrical configuration and operation 01: Symmetrical configuration and asymmetric operation 10: Asymmetrical configuration and operation Bits 1–0 11: Reserved IMA Frame Length 00: M=32 01: M=64 10: M=128 11: M=256
14	Transmit Timing Information	Transmit Clock Information Bits 7–6 Unused, set to 00 Bit 5 Transmit Clock Mode (0: ITC mode, 1: CTC mode) Bits 4–0 Tx LID of the timing reference link (TRL)—Range: 0 to 31

***Table 1-1. IMA Overhead Cell Definition** (3 of 3)*

Octet	Field	Description
15	Tx Test Control	Test Pattern Command Bits 7–6 Unused, set to 00 Bit 5 Test Link Command (0: inactive, 1: active) Bits 4–0 Tx LID of test link—Range: 0 to 31
16	Tx Test Pattern	Value from 0 to 255
17	Rx Test Pattern	Value from 0 to 255
18	Link 0 Information	Link State Machine and Defect Information for link with LID = 0 Bits 7–5 Transmit LSM state Bits 4–2 Receive LSM state Bits 1–0 Rx Link defect status 00: no errors 01: Physical Link defect (e.g., LOS, OOF/LOF, LCD) 10: LIF 11: LODS
19–49	Link 1–31 Info	Status and control of link with LID in the range 1–31
50	Unused	Set to 0x6A (as defined in ITU-T I.432)
51	End-to-end channel	Proprietary channel (set to 0 if unused). The CX2822x does not support this octet.
52–53	CRC Error Control	Bits 15-10 Reserved field for future use—default value is all zeros Bits 9-0 CRC-10 as defined in ITU-T Recommendation I.610

Table 1-2. IMA Overhead Filler Cell Format

Octet	Field	Description
1–5	ATM Cell Header	OAM cell type: Octet 1 = 0000 0000 Octet 2 = 0000 0000 Octet 3 = 0000 0000 Octet 4 = 0000 1011 Octet 5 = 0110 0100 (valid HEC)
6	IMA Label	OAM type field: 0000 0001—IMA Version 1.0 0000 0011—IMA Version 1.1
7	Cell ID Link ID	Bit 7 Set to 0 for IMA Filler cell Bits 6–0 Unused and set to 0
8–51	Unused	Set to 0x6A (as defined in ITU-T I.432)
52–53	CRC Error Control	Bits 15-10 Reserved field for future use—default value is all zeros Bits 9-0 CRC-10 as defined in ITU-T Recommendation I.610

1.1.3 Link State Machine

Management of the individual links is performed by two state machines: the Transmit Link State Machine and the Receive Link State Machine. Four possible states are available for each link as shown in Table 1-3.

Table 1-3. Link States

State	Description
Not in Group	this link has not been added to an IMA group
Unusable	the link is in a group but cannot be used due to line fault etc.
Usable	assigned to a group and ready but is waiting for the other end
Active	fully configured and carrying traffic

The Link State Machines are responsible for handling the transition from one state to another. All functions of the LSM's are performed internally by the CX2822x. Further details are covered in Chapter 3 and in the ATM standard on IMA.

1.1.4 Transmit Clocks

The IMA standard provides two options regarding the transmit clocks. The default mode, and most common IMA application, is Common Transmit Clock (CTC) mode, where all links in the IMA group are generated from the same source. Thus they are in phase and have the same rate of SICP insertion (1/2049) as the designated TRL link.

The Independent Transmit Clock (ITC) mode is available as an optional feature of the IMA protocol (of course, it is fully supported by the CX2822x family). In this mode, each link runs off of an independent clock at the nominal line rate. To support these asynchronous links within an IMA group, the rate of SICP insertion is allowed to vary on the non-TRL links.

The IMA group frame rate for each IMA group must be re-created at the receive end. This regeneration is necessary to implement the IMA Data Cell Clock and smoothing buffer functionality of the IMA protocol. One method for generating the Receive IMA group frame rate is to use the line or payload clock recovered from the receive TRL physical port interface. This clock is a frequency locked reference of the far-end Transmit IMA group frame rate. Equivalently, the rate of cell transfers (i.e., payload bandwidth) from the TRL link can be used as the reference for generating the Receive IMA group frame rate. Both methods are available for use by the CX2822x device, depending on the application and configuration.

1.1.5 Differential Delay

When dealing with multiple facilities, there is no guarantee that the individual links within a group will take the same physical path between the terminating equipment. This variation is referred to as Differential Delay. The ATM Forum specification requires an IMA implementation to absorb a minimum of 25 ms of differential delay between the links. Each port requires 8 K of memory for every 27.5 ms of delay (at E1; 8 K provides for 34.375 ms at T1 rates). The CX28229 provides 256K bytes of on-board memory for the buffering necessary to re-align the links within an IMA group. This is sufficient to support the 25 ms delay for 32 IMA ports. In addition, an external memory bus allows this to be expanded to 2 MB, which supports up to 200 ms of delay. Table 1-4 shows the memory requirements for differential delay.

Table 1-4. Memory Requirements for Differential Delay (in bytes)

Number of ports	E1	27.5 ms	55 ms	110 ms	220 ms
	T1	34.375 ms	68.75 ms	137.5 ms	275 ms
1	8 K		16 K	32 K	64 K
2	16 K		32 K	64 K	128 K
4	32 K		64 K	128 K	256 K
8	64 K		128 K	256 K	512 K
16	128 K		256 K	512 K	1024 K
32	256 K		512 K	1024 K	2048 K

GENERAL NOTE: Shaded areas can be supported by internal memory. Internal memory is disabled when the external bus is used.

The magnitude of the differential delay can be quite large when dealing with T1/E1 links; whereas DSL links generally follow the same path and have nearly identical delays.

1.2 Software Overview

NOTE: Mindspeed's software supports both TC and IMA; however, this section only describes IMA software support.

All IMA devices require a software driver to interface to the system host. Since the GSM's primary function only occurs during startup; the CX2822x family relies on the IMA driver to perform these functions. This allows for maximum flexibility; simpler device design and requires very little overhead from the host.

Mindspeed provides a complete IMA and device driver in ANSI C to simplify system development. This software has been field tested and can be ported to virtually all systems. This is also covered in chapter 3, the IMA engine and the CX28229TAP IMA Software Programming Guide.

Table 1-5 summarizes the API of the CX28224/5/9 software. All functions require a pointer to the structure IMA_DEV. The additional parameters for each function are listed in the following sections. The functions named **IMA_xxxx()** are function calls to the CX28224/5/9. The functions named **USER_xxxx()** are user defined functions called by the CX28224/5/9. The pointers to the user defined functions are passed to CX28224/5/9 during initialization as fields in the DRV initialization structure or after initialization using the **IMA_subsys_set()** function.

Table 1-5. Software Function Summary *(1 of 2)*

Class	Function	Short Description
Initialization	IMA_init_default ()	Initializes the fields of the CX28224/5/9 initialization structure to default values.
	IMA_init ()	This function initializes the IMA software driver and the IMA device.
Interrupts	IMA_tick ()	This function polls the error counters and failure monitoring registers of the IMA device and must be called at a regular periodic interval.
	IMA_intr ()	This function should be called when the device interrupt line has been asserted.
IMA Subsystem	IMA_read ()	This function provides a direct interface to read the registers within the IMA device.
	IMA_write ()	This function provides a direct interface to write the registers within the IMA device.
	IMA_subsys_set ()	This function provides a direct interface to set the CX28224/5/9 Subsystem parameters.
	IMA_subsys_get ()	This function provides a direct interface to retrieve the CX28224/5/9 Subsystem parameters.
	IMA_test ()	This function executes a specified IMA diagnostic test.
	IMA_facility_set()	This function provides a direct interface to set the CX28224/5/9 Facility parameters.
	IMA_facility_get()	This function provides a direct interface to retrieve the CX28224/5/9 Facility parameters.

***Table 1-5. Software Function Summary** (2 of 2)*

Class	Function	Short Description
Group Interface	IMA_group_set ()	This function provides a direct interface to set the CX28224/5/9 Group parameters.
	IMA_group_get ()	This function provides a direct interface to retrieve the CX28224/5/9 Group parameters.
	IMA_group_FM_status ()	This function retrieves the current state of the parameters monitored by the Facility Monitoring subsystem for the IMA Group layer.
	IMA_group_PM_preset ()	This function allows the user to initialize the IMA Group PM statistics to arbitrary values for the current interval of the 15 minute accumulation period.
	IMA_group_PM_status ()	This function retrieves the states (from either the current or previous 15 minute accumulation interval) of the IMA Group Performance Monitoring parameters.
Link Interface	IMA_link_set ()	This function provides a direct interface to set the CX28224/5/9 Link parameters.
	IMA_link_get ()	This function provides a direct interface to retrieve the CX28224/5/9 Link parameters.
	IMA_link_FM_status ()	This function retrieves the current state of the parameters monitored by the Facility Monitoring subsystem for the IMA Link layer.
	IMA_link_PM_preset ()	This function allows the user to initialize the IMA Link PM statistics to arbitrary values for the current interval of the 15 minute accumulation period.
	IMA_link_PM_status ()	This function retrieves the states (from either the current or previous 15 minute accumulation interval) of the IMA Link Performance Monitoring parameters.
PHY Interface	IMA_phy_link_set ()	This function provides a direct interface to set the CX28224/5/9 Link parameters, per facility.
	IMA_phy_link_get ()	This function provides a direct interface to retrieve the CX28224/5/9 Link parameters, per facility.
	IMA_phy_link_FM_status ()	This function retrieves the current state of the parameters monitored by the Failure Monitoring subsystem for the IMA Link layer, per facility.
	IMA_phy_link_PM_preset ()	This function allows the user to initialize the IMA Group PM statistics to arbitrary values for the current interval of the 15 minute accumulation period.
	IMA_phy_link_PM_status ()	This function retrieves the states (from either the current or previous 15 minute accumulation interval) of the IMA Link Performance Monitoring parameters, per facility.
Monitor	IMA_mon()	This function is called to control the CX28224/5/9 debugger.
User Defined	*USER_intr_disable()	This is an application defined function that disables interrupts from the IMA hardware device.
	*USER_intr_enable()	This is an application defined function that enables interrupts from the IMA hardware device.
	* USER_event ()	This is an application defined function that accepts asynchronous event messages from the CX28224/5/9 software.

1.2.1 Software Subsystems

The internal architecture of the CX28229TAP software is composed of five logical subsystems: Configuration (CF), Diagnostics (DG), IMA Group (GRP), Failure Monitoring (FM), and Performance Monitoring (PM).

The following sections summarize the interfaces of the CX28224/5/9 IMA software device driver. It is important to point out that the CX28224/5/9 products can be configured to run in different operating environments. As such, not all the interfaces described below are used in a given application.

1.2.2 Configuration (CF)

The CF subsystem is responsible for setting the operating parameters of the IMA device that are associated with the IMA Link and IMA Group termination entities. Additionally, some of the application specific configurations of the device are set by this subsystem. The default value for each parameter is used to initialize and set the operating mode of the device.

1.2.3 Diagnostics (DG)

The DG subsystem performs control and testing functions on the IMA device and its environment. One role of the DG subsystem is configuration, very similar to the CF subsystem but with different parameters. Similar in function to the Configuration subsystem, the default value for each DG parameter is used to initialize and set the operating mode of the device. The DG subsystem parameters are typically exercised only during test or maintenance conditions, and may affect ATM transmission through the device.

1.2.4 Failure Monitoring (FM)

The Failure Monitoring (FM) subroutine is responsible for monitoring the IMA links and groups for defects and anomalies and integrating the defects into failures. The primary role performed by this subsystem is alarm integration. The CX28229TAP program is aware of changes in the state of the underlying defects and anomalies through periodic polling. The user has control over which Failure indicators are monitored and the length of both the activation and decay times.

Upon initializing the CX28229TAP, the Failure indications required by the ATM MIB are enabled and the activation and decay times are set at 2.5 and 10 seconds, respectively.

1.2.5 Performance Monitoring (PM)

This is the set of functions and capabilities necessary for a Network Element (NE) to gather, store, and report performance data associated with its monitored digital transmission entities In contrast with alarm/status indications, performance parameters are quantitative, not binary, in nature. These performance parameters are gathered over programmable, predetermined accumulation periods. The CX28229TAP calculates these statistics over 15 minute intervals. The PM data is available to the application grouped in a structure encompassing one of the two accumulation sets: the current 15 minute interval or the previous 15 minute interval. The PM subsystem uses the raw anomaly and defect information obtained by the FM subsystem to calculate its performance statistics.

Upon initialization, the PM subsystem is basically disabled: none of the monitored statistics are calculated.

1.2.6 Group State Machine

Overall management of each Group is the responsibility of the Group State Machine. This actually involves three interrelated processes: the Group State Machine (GSM), the Group Traffic State Machine (GTSM), and the Link Addition and Slow Recovery (LASR) procedure. These three processes are used to ensure reliable transmission and reception of ATM layer cells across all links in the Active state. This includes the negotiation of group parameters (i.e., symmetry and M values), the bringing up of the IMA group, and the graceful addition/recovery and deletion of links to and from the group. The seven possible states are shown in Table 1-6. Again, this will be covered in more detail in Chapter 3 and in the ATM standard on IMA.

Table 1-6. Group State Machine

State	Description
Not Configured	no groups configured
Start up	Waiting to establish communications with the other end
Start up Ack	Start Up acknowledge; has recognized the far end and waiting to enter the Insufficient links state
Config Aborted	results when the Far End doesn't comply with the requested configuration parameters
Insufficient links	Both ends have accepted the group parameters and are waiting for the LSM to provide active links
Blocked	The host controller has inhibited the group (probably for maintenance reasons)
Operational	Fully operational and able to pass data

2 CX2822x Hardware Description

Three versions of Mindspeed's IMA solution are available: CX28224, CX28225, and the CX28229. All use the same software drivers and are basically pin compatible. Table 2-1 provides a quick comparison of the three devices.

Table 2-1. Available Parts

Device	Internal memory	External memory interface	UTOPIA addresses (PHY side)	Serial ports
CX28224	128 Kbytes	None	0, 1, 31 (NULL)	2
CX28225	256 Kbytes	None	0–3, 31 (NULL)	4
CX28229	256 Kbytes	2 Mbyte(1)	0–31(2)	8

FOOTNOTE:
(1) Internal memory is disabled when the external bus is used.
(2) Normally, 0x31 is the NULL address; however, the CX28229 can be configured to treat it as a valid port address.

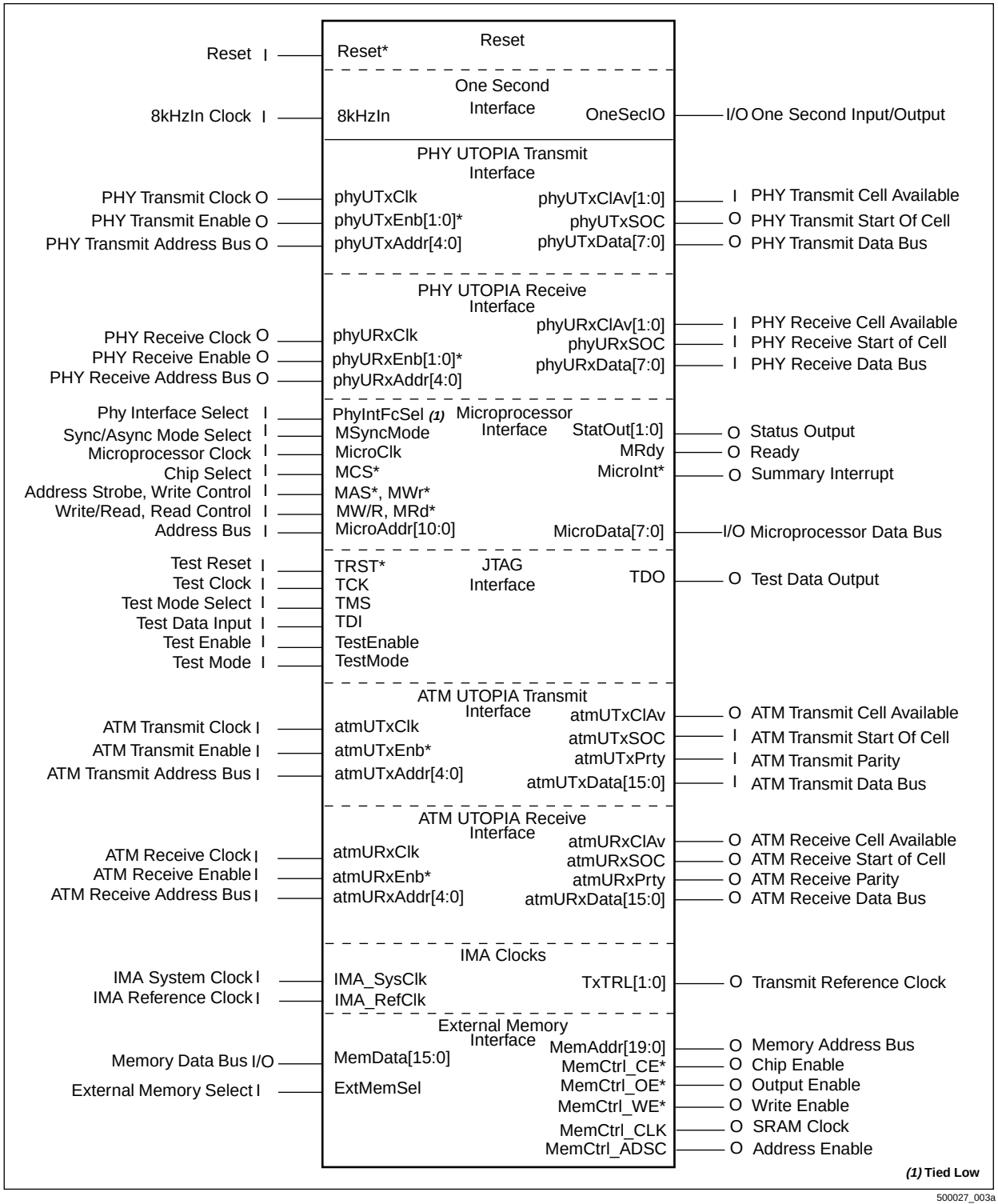
The following three configurations are available:

- UTOPIA-to-Serial
- UTOPIA-to-UTOPIA
- Stand-alone Cell Delineation only

2.1 Logic Diagram

Figures 2-1 and 2-4 illustrate the logic diagrams of the CX2822x's functional modules. Pin descriptions are listed in Table 2-10.

Figure 2-1. CX28229 Logic Diagram (UTOPIA-to-UTOPIA)



2.2 Pin Diagram and Definitions (UTOPIA-to-UTOPIA Configuration)

Figure 2-3 is the pinout diagram for the CX28229 when operating in the UTOPIA-to-UTOPIA mode. It is a single CMOS integrated circuit packaged in a 256-pin BGA. All unused input pins should be connected to ground or power. Unused outputs should be left unconnected.

NOTE: UTOPIA-to-UTOPIA configuration is selected by tying the PhyIntFcSel pin low.

Figure 2-2 is a block diagram of a 32 port IMA solution using the device in the UTOPIA-to-UTOPIA mode. In this case, the Cell Delineation and the interface to the framers is performed by RS8228's. The framers could be T1/E1 or DSL. Further details can be found in the Mindspeed reference designs available online. Configuration information is shown in Table 2-2.

Figure 2-2. IMA Block Diagram

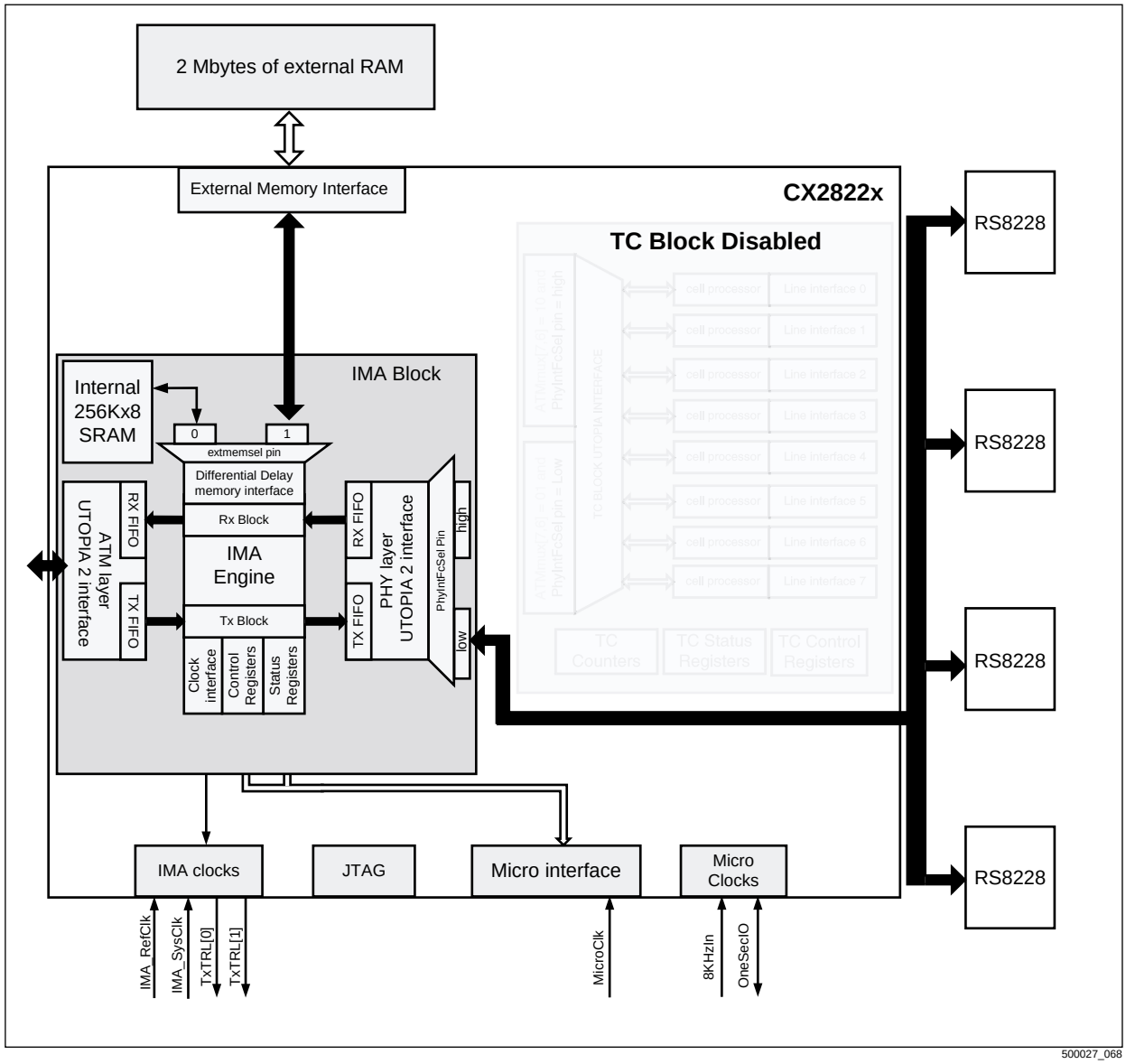


Table 2-2. UTOPIA-to-UTOPIA Configuration Information

ATMMux [7,6] (ATMINTFC, 0x202)	PhyIntFcSel (Pin R4)	Description
01	Low	IMA UTOPIA using the PHY Side UTOPIA; Internal TC block and serial ports not used.
GENERAL NOTE: Use of external memory is optional.		

Figure 2-3. CX28229 Pinout Diagram UTOPIA-to-UTOPIA (Top View)

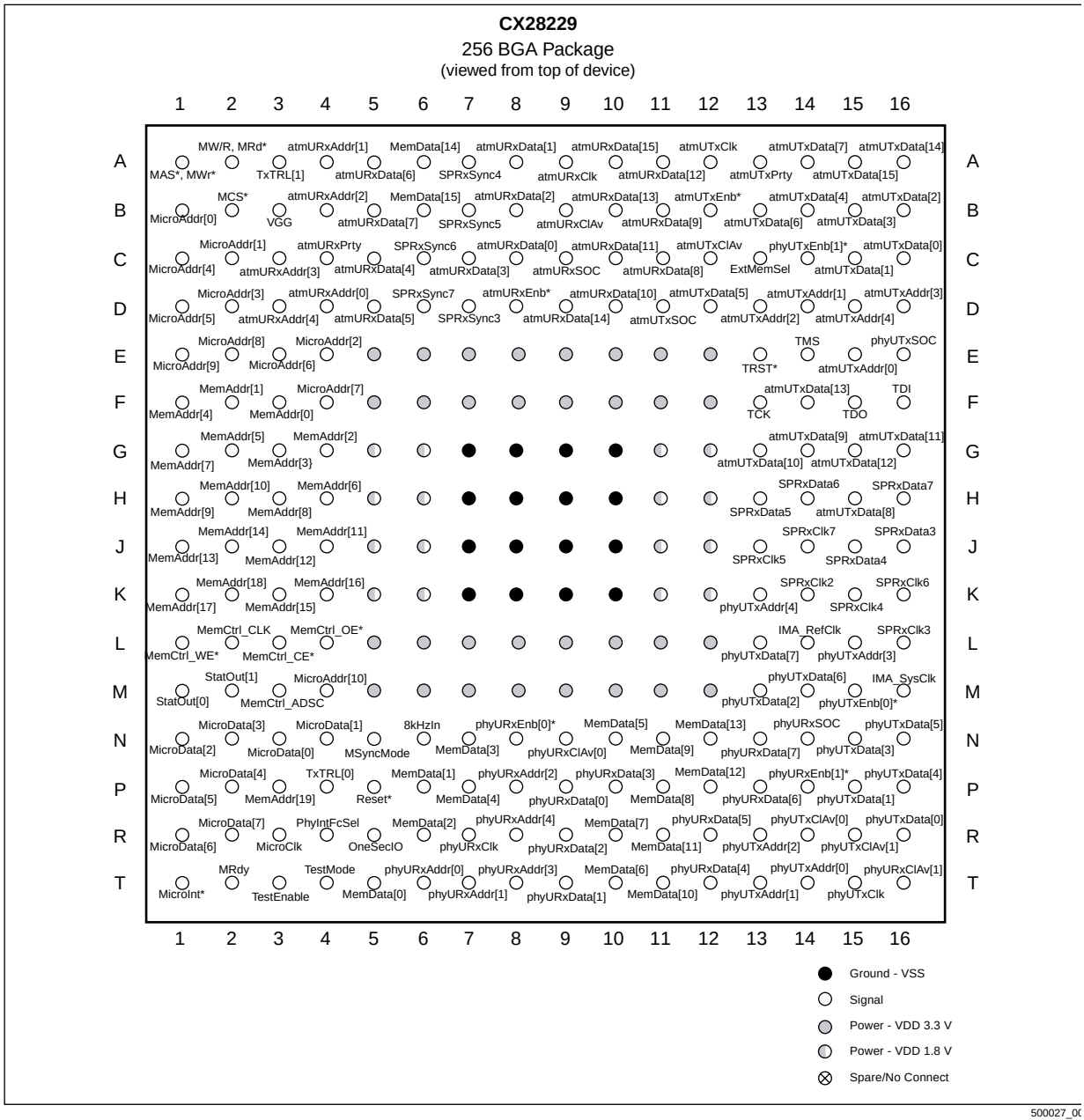


Table 2-3. CX2822x Pin Descriptions *(1 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Micro Interface	StatOut[0]	Status Output	M1	O	General purpose output pins under software control.
	StatOut[1]		M2		
	MSyncMode	Microprocessor Synchronous/ Asynchronous Bus Mode Select	N5	I	Selects synchronous or asynchronous bus mode, which determines the functions of two pins, MW/R, MRd* (pin A2) and MAS*,MWr* (pin A1). A logic 1 selects the synchronous bus mode, compatible with Bt8230 and Bt8233. In this mode, these pins are defined as follows: MW/R (A2) and MAS* (A1). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MRd* (A2) and MWr* (A1).
	Reset*	Device Reset	P5	I	When asserted low, resets the device. The microprocessor clock must be present before reset is released.
	8kHzIn	8 kHz Input	N6	I	A clock input used to derive OneSecIO. Typically operates at a frequency of 8 kHz.
	OneSecIO	One-Second Input/ Output	R5	I/O	Software can configure this pin as an output that equals the input from the 8kHzIn divided by 8000. When configured as an input, status registers and counters may be latched on the rising edge of this input. See Bit 0 of the Mode register (0x200).
	MW/R, MRd*	Microprocessor Write/Read	A2	I	When MSyncMode is asserted high, this pin is a read/write control pin. In this mode, when MW/R is asserted high, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[10:0] pins. Also, when MW/R is asserted low in this mode, a read access is enabled and the memory location indicated by the MicroAddr[10:0] pins is read. Its value is placed on the MicroData[7:0] pins. Both read and write accesses assume the device is chip selected (MCS* = 0), the address is valid (MAS* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is asserted low, this pin is a read control pin. In this mode, when MRd* is asserted low, a read access is enabled and the memory location indicated by the MicroAddr[10:0] pins is read. Its value is placed on the MicroData[7:0] pins.
	MCS*	Microprocessor Chip Select	B2	I	When asserted low, the device is selected for read and write accesses. When asserted high, the device will not respond to input signal transitions on MicroClk, MW/R, MRd*, or MAS*, MWr*. Additionally, when MCS* is asserted high, the MicroData[7:0] pins are in a high-impedance state but the MicroInt* pin remains operational.

Table 2-3. CX2822x Pin Descriptions *(2 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Micro Interface	MAS*, MWr*	Microprocessor Address Strobe	A1	I	When MSyncMode is asserted high, this pin is an address strobe pin. When the MAS* pin is asserted low, it indicates a valid address, MicroAddr[10:0]. This signal is used to qualify read and write accesses. When MSyncMode is asserted low, this pin is a write control pin. When MWr* is asserted low, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[10:0] pins. The write access assumes the device is chip selected (MCS* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1).
	MicroAddr[0]	Microprocessor Address Bus	B1	I	These 11 bits are an address input for identifying the register to access.
	MicroAddr[1]		C2		
	MicroAddr[2]		E4		
	MicroAddr[3]		D2		
	MicroAddr[4]		C1		
	MicroAddr[5]		D1		
	MicroAddr[6]		E3		
	MicroAddr[7]		F4		
	MicroAddr[8]		E2		
	MicroAddr[9]		E1		
	MicroAddr[10]		M4		
	MicroData[0]	Microprocessor Data Bus	N3	I/O	A bi-directional data bus for reading and writing data to internal registers.
	MicroData[1]		N4		
	MicroData[2]		N1		
	MicroData[3]		N2		
	MicroData[4]		P2		
	MicroData[5]		P1		
	MicroData[6]		R1		
	MicroData[7]		R2		
	MicroInt*	Microprocessor Interrupt Request	T1	O	When active low, the device needs servicing. It remains active until the pending interrupt is processed by the Interrupt Service Routine. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin.

***Table 2-3. CX2822x Pin Descriptions** (3 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Micro Interface	MRdy	Microprocessor Ready	T2	O	When active high, the current read or write transaction has been completed. For a read transaction, the data is ready to be transferred to the microprocessor. For a write transaction, the data provided by the microprocessor has been written. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin.
	MicroClk	Microprocessor Clock	R3	I	An 8–50 MHz clock signal input. The device samples the microprocessor interface pins (MCS*, MW/R, MRd*, MAS*, MicroAddr[10:0], and MicroData[7:0]) on the rising edge of this signal. The microprocessor interface output pins (MicroData[7:0], MicroInt*) are clocked on the rising edge of MicroClk. Note that this clock is required for both synchronous and asynchronous operations. See note in Section 6.1.
External Memory(1)	ExtMemSel	External Memory Enable	C13	I/PD	When this pin is pulled high, it enables the external differential delay SRAM bus. This pin is internally pulled low on the CX28224/5.
	MemData[0](1)	Differential Delay Memory Data Bus	T5	I/O/PD	Differential delay SRAM Data Bus. ATM cells extracted from the Receive data stream are stored in the SRAM for the purpose of differential delay compensation.
	MemData[1](1)		P6		
	MemData[2](1)		R6		
	MemData[3](1)		N7		
	MemData[4](1)		P7		
	MemData[5](1)		N10		
	MemData[6](1)		T10		
	MemData[7](1)		R10		
	MemData[8](1)		P11		
	MemData[9](1)		N11		
	MemData[10](1)		T11		
	MemData[11](1)		R11		
	MemData[12](1)		P12		
	MemData[13](1)		N12		
	MemData[14](1)		A6		
	MemData[15](1)		B6		

Table 2-3. CX2822x Pin Descriptions *(4 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
External Memory[1]	MemAddr[0][1]	Differential Delay Memory Address Bus	F3	O	Receive SRAM Address Bus. These signals are enabled by tying the ExtMemSel pin high.
	MemAddr[1][1]		F2		
	MemAddr[2][1]		G4		
	MemAddr[3][1]		G3		
	MemAddr[4][1]		F1		
	MemAddr[5][1]		G2		
	MemAddr[6][1]		H4		
	MemAddr[7][1]		G1		
	MemAddr[8][1]		H3		
	MemAddr[9][1]		H1		
	MemAddr[10][1]		H2		
	MemAddr[11][1]		J4		
	MemAddr[12][1]		J3		
	MemAddr[13][1]		J1		
	MemAddr[14][1]		J2		
	MemAddr[15][1]		K3		
	MemAddr[16][1]		K4		
	MemAddr[17][1]		K1		
	MemAddr[18][1]		K2		
	MemAddr[19][1]		P3		
	MemCtrl_CE*[1]	Chip Enable	L3	O	Receive SRAM Device Select (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high.
	MemCtrl_OE*[1]	Output Enable	L4	O	Receive SRAM Device Output (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high.
	MemCtrl_WE*[1]	Write Enable	L1	O	Receive SRAM write enable (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high.
	MemCtrl_CLK[1]	SRAM Clock	L2	O	Receive SRAM clock signal. This signal is enabled by pulling the ExtMemSel pin high.
	MemCtrl_ADSC[1]	Address Enable	M3	O	Receive SRAM address enable (active low) address strobe. This signal is enabled by pulling the ExtMemSel pin high.

Table 2-3. CX2822x Pin Descriptions *(5 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
JTAG	TRST*	Test Reset	E13	I/PU	When asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor. Do not assert this reset unless a clock is provided on TCK.
	TCK	Test Clock	F13	I	Samples the value of TMS and TDI on its rising edge to control the boundary scan operations.
	TMS	Test Mode Select	E14	I/PU	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor.
	TDI	Test Data Input	F16	I/PU	The serial test data input. This pin has a pull-up resistor.
	TDO	Test Data Output	F15	O	The serial test data output.
Test	TestEnable		T3	I	Factory test use only, tie to VSS.
	TestMode		T4	I	Factory test use only, tie to VSS.
PHY Side Interface	PhyIntFcSel	PHY Interface Select	R4	I	If this pin is tied low, the PHY UTOPIA Interface mode is selected. This table shows pin configurations with this pin tied low. If this pin is tied high, the PHY Serial mode is selected.
	phyURxClk	UTOPIA Receive Clock	R7	O	IMA_SysClk/2
	phyURxEnb[0]*	PHY UTOPIA Receive Enable	N8	O	Data transfer and output enable for Receive PHY cells (active low). To support multiple PHY devices, separate enable signals are provided. Depending on the software configuration, some of the enable signals may not be available and will be replaced by additional PHY cell bus address bits. PhyURxEnb[1] is a No Connect on the CX28224/5 devices.
	phyURxEnb[1]*		P14		
	phyURxAddr[0]	PHY UTOPIA Receive Address	T6	O	Receive PHY Cell Bus address. The following limitations apply: **Device** / **Addresses** CX28224: 0, 1, 31 CX28225: 0–3, 31 CX28229: 0–31
	phyURxAddr[1]		T7		
	phyURxAddr[2]		P8		
	phyURxAddr[3]		T8		
	phyURxAddr[4]		R8		
	phyURxClAv[0]	PHY UTOPIA Receive Cell Available	N9	I	Cell Available signals for Receive PHY interfaces. phyURxClAv{n] is active when one or more complete cells can be transferred. To support different PHY devices, separate cell available signals are provided. This allows expansion to 32 points. PhyURxClAv[1] is a No Connect on the CX28224/5 devices.
	phyURxClAv[1]		T16	I/PD	

Table 2-3. CX2822x Pin Descriptions *(6 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
PHY Side Interface (Continued)	phyURxData[0]	PHY UTOPIA Receive Data	P9	I	Received 8 bit PHY Cell Data. All received cells are passed to the internal IMA processor.
	phyURxData[1]		T9	I	
	phyURxData[2]		R9	I	
	phyURxData[3]		P10	I	
	phyURxData[4]		T12	I	
	phyURxData[5]		R12	I	
	phyURxData[6]		P13	I	
	phyURxData[7]		N13	I	
	phyURxSOC	PHY UTOPIA Start of Cell	N14	I	Start of Cell synchronization signal for Receive PHY cells (active high). Indicates that the first byte of the cell is being placed on the PhyURxData[7:0] bus.
	phyUTxAddr[0]	PHY UTOPIA Transmit Address	T14	O	Transmit PHY Cell Bus address. The following limitations apply: **Device** / **Addresses** CX28224: 0, 1, 31 CX28225: 0–3, 31 CX28229: 0–31
	phyUTxAddr[1]		T13		
	phyUTxAddr[2]		R13		
	phyUTxAddr[3]		L15		
	phyUTxAddr[4]		K13		
	phyUTxClAv[0]	PHY UTOPIA Transmit Cell Available	R14	I	Cell Available signals for Transmit ATM cells. When phyUTxClAv[n] is active high, the PHY has space available for one or more complete cells. To support different PHY devices, separate cell available signals are provided. PhyUTxClAv[1] is a No Connect on the CX28224/5 devices.
	phyUTxClAv[1]		R15	I/PD	
	phyUTxClk	PHY UTOPIA Transmit Clock	T15	O	IMA_SysClk divided by two.
	phyUTxData[0]	PHY UTOPIA Transmit Data	R16	O	8 bit PHY Cell Data to be sent out the PHY facility. 8 bit UTOPIA interface used to transmit data to the external TC devices.
	phyUTxData[1]		P15	O	
	phyUTxData[2]		M13	O	
	phyUTxData[3]		N15	O	
	phyUTxData[4]		P16	O	
	phyUTxData[5]		N16	O	
	phyUTxData[6]		M14	O	
	phyUTxData[7]		L13	O	
	phyUTxEnb[0]*	PHY UTOPIA Transmit Enable	M15	O	Data transfer enable for Transmit PHY cells (active low signal). To support different PHY devices, separate enable signals are provided.
	phyUTxEnb[1]*		C14		
	phyUTxSOC	PHY UTOPIA Transmit Start of Cell	E16	O	Start of Cell synchronization signal for Transmit PHY cells (active high). Indicates that the first byte of a cell is being placed on the phyUTxData[7:0] bus.

***Table 2-3. CX2822x Pin Descriptions** (7 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
IMA Clocks	IMA_SysClk	IMA Subsystem Clock	M16	I	Most of the IMA logic circuits use this clock (or a derivative of it). It can also be used as a T1/E1 reference clock. Refer to Chapter 3.
	IMA_RefClk	IMA Reference Clock	L14	I	If this is to be used as a reference clock, set the frequency as shown in Chapter 3.
	TxTRL[0]	Transmit Reference Clock	P4	O	Transmit Reference Clocks.
	TxTRL[1]		A3		
Serial Line Interface	SPRxSync3	Frame Sync Input	D7	I/PD	When using the PHY UTOPIA mode, this pin is a no-connect.
	SPRxSync4		A7		
	SPRxSync5		B7		
	SPRxSync6		C6		
	SPRxSync7		D6		
	SPRxClk2	Receive Line Clock Input	K14	I/PD	When using the PHY UTOPIA mode, this pin is a no-connect.
	SPRxClk3		L16		
	SPRxClk4		K15		
	SPRxClk5		J13		
	SPRxClk6		K16		
	SPRxClk7		J14		
	SPRxData3	Receive Line Data Input	J16	I/PD	When using the PHY UTOPIA mode, this pin is a no-connect.
	SPRxData4		J15		
	SPRxData5		H13		
	SPRxData6		H14		
	SPRxData7		H16		

Table 2-3. CX2822x Pin Descriptions *(8 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
ATM Layer UTOPIA Interface	atmUTxAddr[0]	ATM UTOPIA Transmit Address	E15	I	Transmit ATM Cell Bus address.
	atmUTxAddr[1]		D14		
	atmUTxAddr[2]		D13		
	atmUTxAddr[3]		D16		
	atmUTxAddr[4]		D15		
	atmUTxData[0]	ATM UTOPIA Transmit Data	C16	I	Transmit direction ATM side cell data. CX28224 only supports an 8 bit data path. Thus atmUTxData[8:15] are no-connects.
	atmUTxData[1]		C15	I	
	atmUTxData[2]		B16	I	
	atmUTxData[3]		B15	I	
	atmUTxData[4]		B14	I	
	atmUTxData[5]		D12	I	
	atmUTxData[6]		B13	I	
	atmUTxData[7]		A14	I	
	atmUTxData[8]		H15	I/PD	
	atmUTxData[9]		G14	I/PD	
	atmUTxData[10]		G13	I/PD	
	atmUTxData[11]		G16	I/PD	
	atmUTxData[12]		G15	I/PD	
	atmUTxData[13]		F14	I/PD	
	atmUTxData[14]		A16	I/PD	
	atmUTxData[15]		A15	I/PD	
	atmUTxPrty	ATM UTOPIA Transmit Parity	A13	I	Parity status signal. In 8 bit Utopia mode, a parity calculation is performed over atmUTxData[7:0] for each clock cycle of atmUTxClk. Odd parity is used. In 16 bit Utopia mode, this signal is the parity of atmUTxData[15:0]. This signal is optional.

Table 2-3. CX2822x Pin Descriptions *(9 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
ATM Layer UTOPIA Interface	atmUTxClAv	ATM UTOPIA Transmit Cell Available	C12	O	Cell Available signal for transmit ATM cells (active high).
	atmUTxSOC	ATM UTOPIA Transmit Start of Cell	D11	I	Start of Cell synchronization signal for transmit ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus.
	atmUTxEnb*	ATM UTOPIA Transmit Enable	B12	I	Data transfer enable for transmit ATM cells (active low). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus.
	atmUTxClk	ATM UTOPIA Transmit Clock	A12	I	Clock signal used for transfer of transmit ATM cells from the ATM Layer. The maximum clock rate is 33 MHz.
	atmURxSOC	ATM UTOPIA Receive Start of Cell	C9	O	Start of Cell synchronization signal for receive ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmURxData bus.
	atmURxClk	ATM UTOPIA Receive Clock	A9	I	Clock signal used for transfer of receive ATM cells from the ATM Layer. The maximum clock rate 33 MHz.
	atmURxClAv	ATM UTOPIA Receive Cell Available	B9	O	Cell Available signal for receive ATM cells (active high). As a software option in the IMA16 application, the pin atmURxAdr[4] will function as a cell available status signal (atmURxClAv[1]) for ATM Utopia addresses 8–15 only. In this mode, atmURxClAv[1] will threestate for addresses 0–7.
	atmURxEnb*	ATM UTOPIA Receive Enable	D8	I	Data transfer and output enable for receive ATM cells (active low).

Table 2-3. CX2822x Pin Descriptions *(10 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
ATM Layer UTOPIA Interface	atmURxData[0]	ATM UTOPIA Receive Data	C8	O	Receive direction ATM side cell data. CX28224 only supports an 8 bit data path. Thus atmURxData[8:15] are no-connects.
	atmURxData[1]		A8		
	atmURxData[2]		B8		
	atmURxData[3]		C7		
	atmURxData[4]		C5		
	atmURxData[5]		D5		
	atmURxData[6]		A5		
	atmURxData[7]		B5		
	atmURxData[8]		C11		
	atmURxData[9]		B11		
	atmURxData[10]		D10		
	atmURxData[11]		C10		
	atmURxData[12]		A11		
	atmURxData[13]		B10		
	atmURxData[14]		D9		
	atmURxData[15]		A10		
	atmURxPrty	ATM UTOPIA Receive Parity	C4	O	Parity status signal. In 8 bit Utopia mode, a parity calculation is performed over atmURxData[7:0] for each clock cycle of atmUTxClk. Odd parity is used. In 16 bit Utopia mode, this signal is the parity of atmURxData[15:0]. This signal is optional.
	atmURxAddr[0]	ATM UTOPIA Receive Address	D4	I	Receive ATM Cell Bus address. This address determines the source channel of the Receive ATM cells output from the IMA subsystem and also selects the channel sourcing the atmURxClAv signal.
	atmURxAddr[1]		A4		
	atmURxAddr[2]		B4		
	atmURxAddr[3]		C3		
	atmURxAddr[4]		D3		

Table 2-3. CX2822x Pin Descriptions *(11 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Power Supply	V_{DD} (1.8 V)	Supply Voltage (1.8 V)	G5 G6 G11 G12 H5 H6 H11 H12 J5 J6 J11 J12 K5 K6 K11 K12		Power supply connections. (1.8 V)
	V_{DD} 3.3 V)	Supply Voltage (3.3 V)	E5 E6 E7 E8 E9 E10 E11 E12 F5 F6 F7 F8 F9 F10 F11 F12 L5 L6 L7 L8 L9 L10 L11 L12 M5 M6 M7 M8 M9 M10 M11 M12		Power supply connections. (3.3 V)

Table 2-3. CX2822x Pin Descriptions *(12 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Power Supply	V_{SS} GND	Ground	G7 G8 G9 G10 H7 H8 H9 H10 J7 J8 J9 J10 K7 K8 K9 K10		Ground connections.
	VGG	Electrostatic Discharge (ESD) Supply Voltage	B3		Provides ESD protection when interfacing with 5 V systems. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using 3.3 V system, connect to 3.3 V.

FOOTNOTE:

(1) This bus is enabled by pulling the ExtMemSel pin high. External Memory is disabled on the CX28224 and CX28225 versions of the device.

2.3 Pin Diagram and Definitions (UTOPIA-to-Serial Configuration)

Figure 2-6 illustrates a pinout diagram for the CX28229 when operating in UTOPIA-to-Serial mode. It is a single CMOS integrated circuit packaged in a 256-pin BGA. All unused input pins should be connected to ground or power. Unused outputs should be left unconnected.

NOTE: UTOPIA-to-Serial configuration is selected by tying the PhyIntFcSel pin high.

Figure 2-5 is a block diagram of an 8 link IMA solution using the device in the UTOPIA-to-serial mode to take advantage of the internal serial ports. Cell Delineation is performed internally and the CX2822x interfaces directly to the framers. These framers could be T1/E1 or DSL. Further details can be found in the Mindspeed reference design available online. Configuration information is shown in Table 2-4.

Figure 2-4. CX28229 Logic Diagram (UTOPIA-to-Serial)

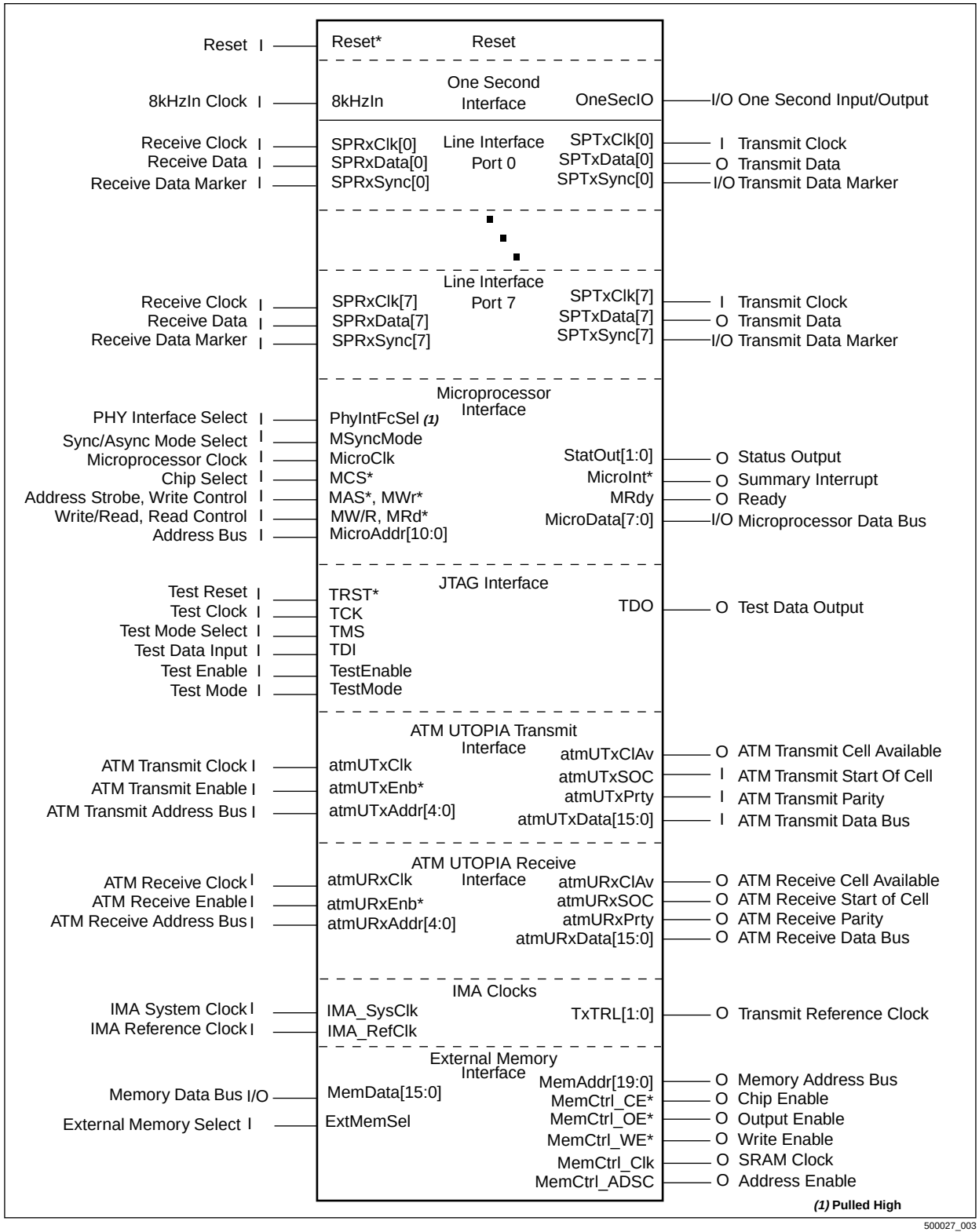


Figure 2-5. CX28229 UTOPIA-to-Serial Mode

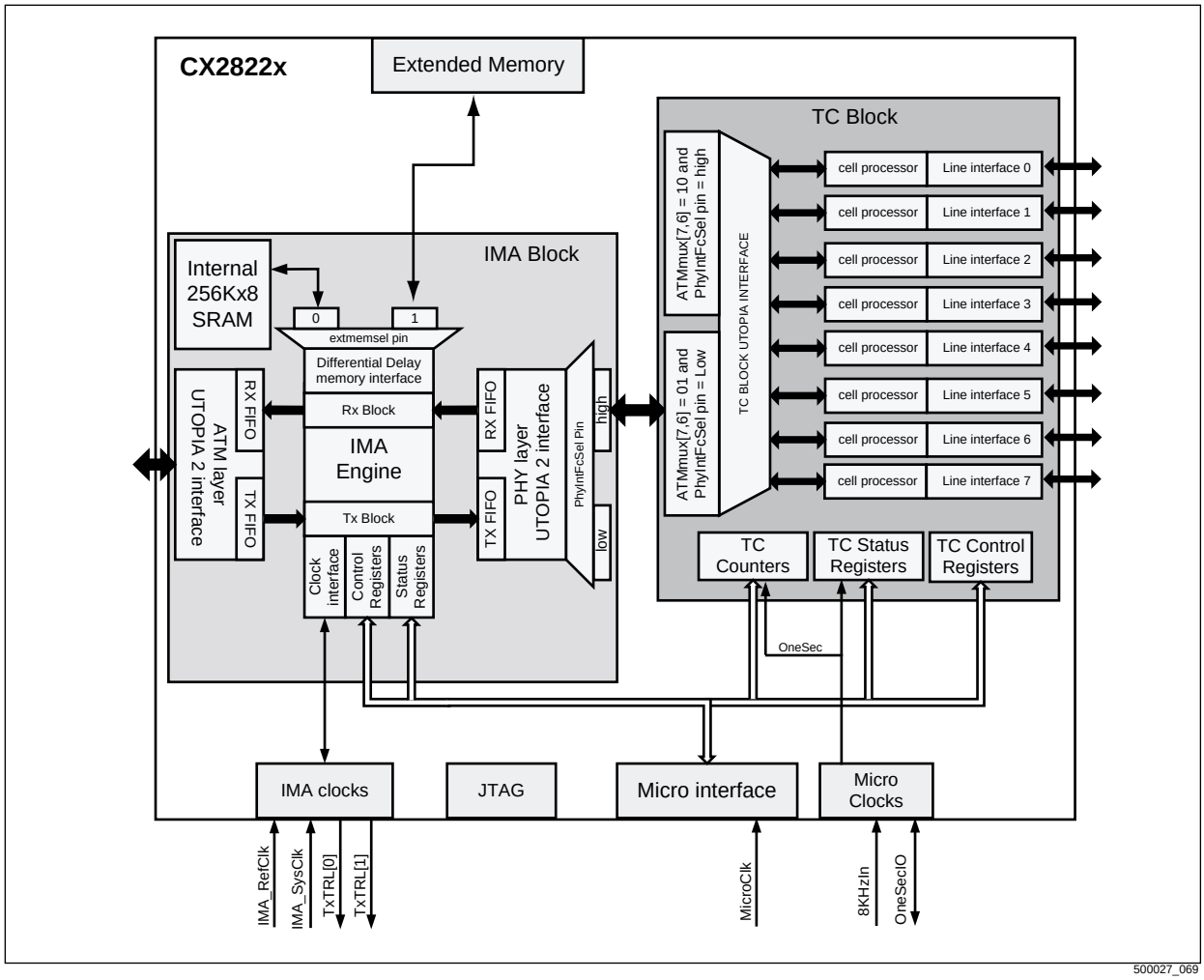


Table 2-4. CX28229 UTOPIA-to-Serial Mode

ATMMux [7,6] (ATMINTFC, 0x202)	PhyIntFcSel (Pin R4)	Description
01	High	IMA UTOPIA using Internal TC block; UTOPIA-to-Serial mode using 8 internal serial ports.
GENERAL NOTE: External memory could be used if desired (CX28229).		

Figure 2-6. CX28229 Pinout Diagram, UTOPIA-to-Serial (Top View)

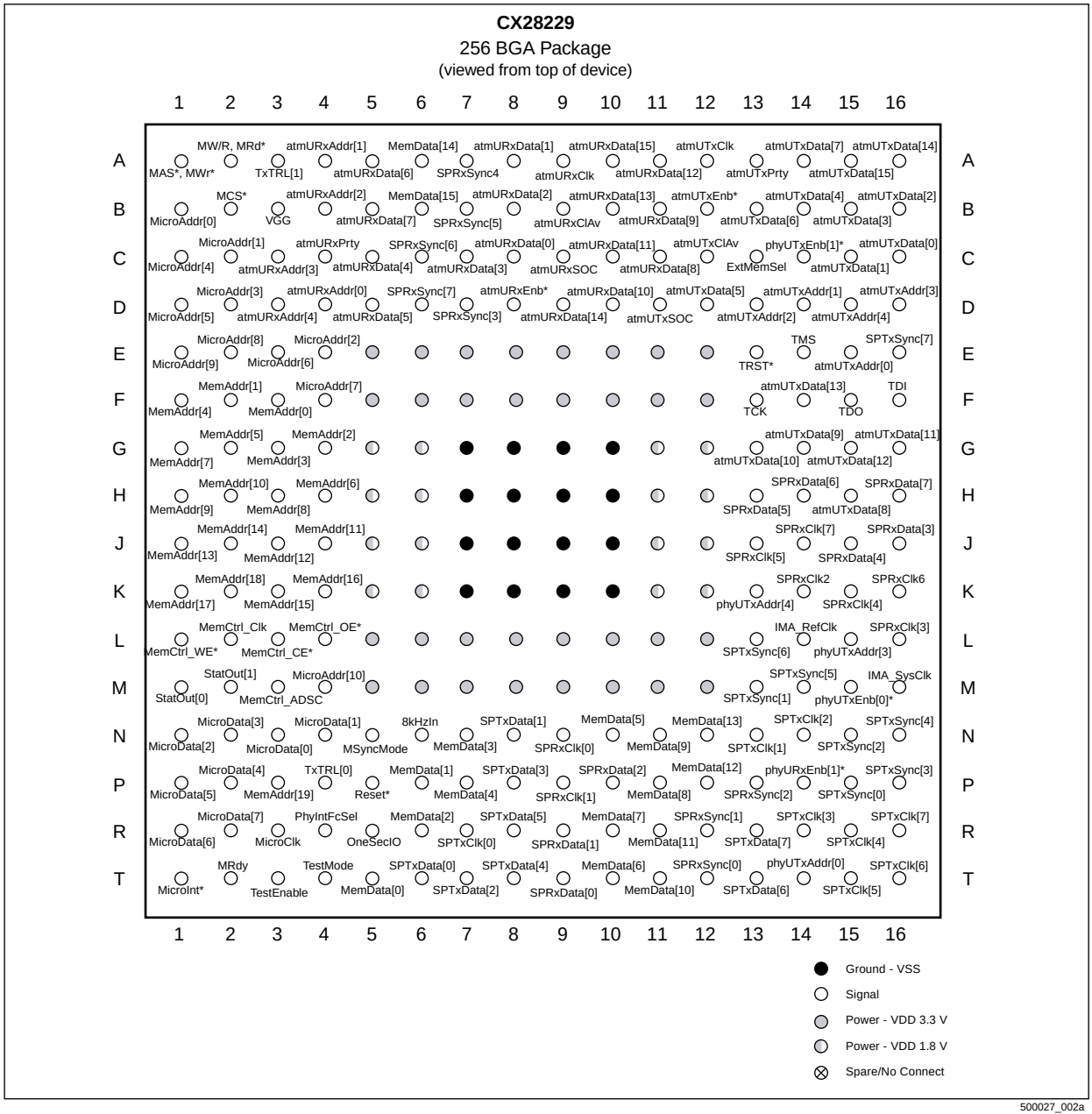


Table 2-5. CX28229 Pin Descriptions *(1 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Micro Interface	StatOut[0]	Status Output	M1	O	General purpose output pins under software control.
	StatOut[1]		M2		
	MSyncMode	Microprocessor Synchronous/ Asynchronous Bus Mode Select	N5	I	Selects synchronous or asynchronous bus mode, which determines the functions of two pins, MW/R,MRd* (pin A2) and MAS*,MWr* (pin A1). A logic 1 selects the synchronous bus mode, compatible with Bt8230 and Bt8233. In this mode, these pins are defined as follows: MW/R (A2) and MAS* (A1). A logic 0 selects the asynchronous SRAM-type bus mode. In this mode, the pins are defined as follows: MRd* (A2) and MWr* (A1).
	Reset*	Device Reset	P5	I	When asserted low, resets the device. The microprocessor clock must be present before reset is released.
	8kHzIn	8 kHz Input	N6	I	A clock input used to derive OneSecIO. Typically operates at a frequency of 8 kHz.
	OneSecIO	One-Second Input/ Output	R5	I/O	Software can configure this pin as an output that equals the input from the 8kHzIn divided by 8000. When configured as an input, status registers and counters may be latched on the rising edge of this input. See Bit 0 of the Mode register (0x200).
	MW/R, MRd*	Microprocessor Write/Read	A2	I	When MSyncMode is asserted high, this pin is a read/write control pin. In this mode, when MW/R is asserted high, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[10:0] pins. Also, when MW/R is asserted low in this mode, a read access is enabled and the memory location indicated by the MicroAddr[10:0] pins is read. Its value is placed on the MicroData[7:0] pins. Both read and write accesses assume the device is chip selected (MCS* = 0), the address is valid (MAS* = 0), and the device is not being reset (Reset* = 1). When MSyncMode is asserted low, this pin is a read control pin. In this mode, when MRd* is asserted low, a read access is enabled and the memory location indicated by the MicroAddr[10:0] pins is read. Its value is placed on the MicroData[7:0] pins.
	MCS*	Microprocessor Chip Select	B2	I	When asserted low, the device is selected for read and write accesses. When asserted high, the device will not respond to input signal transitions on MicroClk, MW/R, MRd*, or MAS*, MWr*. Additionally, when MCS* is asserted high, the MicroData[7:0] pins are in a high-impedance state but the MicroInt* pin remains operational.

Table 2-5. CX28229 Pin Descriptions *(2 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Micro Interface	MAS*, MWr*	Microprocessor Address Strobe	A1	I	When MSyncMode is asserted high, this pin is an address strobe pin. When the MAS* pin is asserted low, it indicates a valid address, MicroAddr[10:0]. This signal is used to qualify read and write accesses. When MSyncMode is asserted low, this pin is a write control pin. When MWr* is asserted low, a write access is enabled and the MicroData[7:0] pin values will be written to the memory location indicated by the MicroAddr[10:0] pins. The write access assumes the device is chip selected (MCS* = 0), a read access is not being requested (MRd* = 1), and the device is not being reset (Reset* = 1).
	MicroAddr[0]	Microprocessor Address Bus	B1	I	These 11 bits are an address input for identifying the register to access.
	MicroAddr[1]		C2		
	MicroAddr[2]		E4		
	MicroAddr[3]		D2		
	MicroAddr[4]		C1		
	MicroAddr[5]		D1		
	MicroAddr[6]		E3		
	MicroAddr[7]		F4		
	MicroAddr[8]		E2		
	MicroAddr[9]		E1		
	MicroAddr[10]		M4		
	MicroData[0]	Microprocessor Data Bus	N3	I/O	A bi-directional data bus for reading and writing data to internal registers.
	MicroData[1]		N4		
	MicroData[2]		N1		
	MicroData[3]		N2		
	MicroData[4]		P2		
	MicroData[5]		P1		
	MicroData[6]		R1		
	MicroData[7]		R2		
	MicroInt*	Microprocessor Interrupt Request	T1	O	When active low, the device needs servicing. It remains active until the pending interrupt is processed by the Interrupt Service Routine. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin.

***Table 2-5. CX28229 Pin Descriptions** (3 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Micro Interface	MRdy	Microprocessor Ready	T2	O	When active high, the current read or write transaction has been completed. For a read transaction, the data is ready to be transferred to the microprocessor. For a write transaction, the data provided by the microprocessor has been written. This pin is an open drain output for an external wired OR logic implementation. An external pull-up resistor is required for this pin.
	MicroClk	Microprocessor Clock	R3	I	An 8–50 MHz clock signal input. The device samples the microprocessor interface pins (MCS*, MW/R, MAS*, MicroAddr[10:0], and Microdata[7:0]) on the rising edge of this signal. The microprocessor interface output pins (Microdata[7:0], MicroInt*) are clocked on the rising edge of MicroClk. Note that this clock is required for both synchronous and asynchronous operations. See note in Section 6.1.
External Memory	ExtMemSel	External Memory Enable	C13	I/PD	When this pin is pulled high, it enables the external differential delay SRAM bus.
	MemData[0]	Differential Delay Memory Data Bus	T5	I/O/PD	Differential delay SRAM Data Bus. ATM cells extracted from the Receive data stream are stored in the SRAM for the purpose of differential delay compensation. This bus is enabled by pulling the ExtMemSel pin high.
	MemData[1]		P6		
	MemData[2]		R6		
	MemData[3]		N7		
	MemData[4]		P7		
	MemData[5]		N10		
	MemData[6]		T10		
	MemData[7]		R10		
	MemData[8]		P11		
	MemData[9]		N11		
	MemData[10]		T11		
	MemData[11]		R11		
	MemData[12]		P12		
	MemData[13]		N12		
	MemData[14]		A6		
	MemData[15]		B6		

***Table 2-5. CX28229 Pin Descriptions** (4 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
External Memory	MemAddr[0]	Differential Delay Memory Address Bus	F3	O	Receive SRAM Address Bus - msb. This signal is enabled by pulling the ExtMemSel pin high.
	MemAddr[1]		F2		
	MemAddr[2]		G4		
	MemAddr[3]		G3		
	MemAddr[4]		F1		
	MemAddr[5]		G2		
	MemAddr[6]		H4		
	MemAddr[7]		G1		
	MemAddr[8]		H3		
	MemAddr[9]		H1		
	MemAddr[10]		H2		
	MemAddr[11]		J4		
	MemAddr[12]		J3		
	MemAddr[13]		J1		
	MemAddr[14]		J2		
	MemAddr[15]		K3		
	MemAddr[16]		K4		
	MemAddr[17]		K1		
	MemAddr[18]		K2		
	MemAddr[19]		P3		
	MemCtrl_CE*	Chip Enable	L3	O	Receive SRAM Device Select (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high.
	MemCtrl_OE*	Output Enable	L4	O	Receive SRAM Device Output (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high.
	MemCtrl_WE*	Write Enable	L1	O	Receive SRAM write enable (active low) control signal. This signal is enabled by pulling the ExtMemSel pin high.
	MemCtrl_CLK	SRAM Clock	L2	O	Receive SRAM clock signal. This signal is enabled by pulling the ExtMemSel pin high.
External Memory	MemCtrl_ADSC	Address Enable	M3	O	Receive SRAM address enable (active low) address strobe. This signal is enabled by pulling the ExtMemSel pin high.

***Table 2-5. CX28229 Pin Descriptions** (5 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
JTAG	TRST*	Test Reset	E13	I/PU	When asserted, the internal boundary-scan logic is reset. This pin has a pull-up resistor. Do not assert this reset unless a clock is provided on TCK.
	TCK	Test Clock	F13	I	Samples the value of TMS and TDI on its rising edge to control the boundary scan operations.
	TMS	Test Mode Select	E14	I/PU	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin has a pull-up resistor.
	TDI	Test Data Input	F16	I/PU	The serial test data input. This pin has a pull-up resistor.
	TDO	Test Data Output	F15	O	The serial test data output.
Factory Test	TestEnable		T3	I	Factory test use only, tie to VSS.
	TestMode		T4	I	Factory test use only, tie to VSS.
PHY Side Interface	PhyIntFcSel	PHY Interface Select	R4	I	If this pin is tied low, the PHY UTOPIA Interface mode is selected. If this pin is tied high, the PHY Serial mode is selected (as shown in this table).
	phyURxEnb[1]*	PHY UTOPIA Receive Enable	NC	O	This pin is a No Connect when PhyIntFcSel is tied high.
	phyUTxAddr[0]	PHY UTOPIA Transmit Address	NC	O	These pins are a No Connect when PhyIntFcSel is tied high.
	phyUTxAddr[3]		NC		
	phyUTxAddr[4]		NC		
	phyUTxEnb[0]*	PHY UTOPIA Transmit Enable	NC	O	These pins are a No Connect when PhyIntFcSel is tied high.
	phyUTxEnb[1]*		NC		
IMA Clocks	IMA_SysClk	IMA Subsystem Clock	M16	I	Most of the IMA logic circuits use this clock (or a derivative of it). It can also be used as a T1/E1 reference clock. Refer to Chapter 3.
	IMA_RefClk	IMA Subsystem Clock	L14	I	If Ref_Xclk is to be used as a reference clock, set the frequency as shown in Chapter 3.
	TxTRL[0]	Transmit Reference Clock	P4	O	Transmit Reference Clocks.
	TxTRL[1]		A3		

Table 2-5. CX28229 Pin Descriptions *(6 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Serial Line Interface	SPRxSync[0]	Frame Sync Input	T12	I/PD	When the PHY serial interface is enabled, this is the frame sync input.
	SPRxSync[1]		R12		
	SPRxSync[2]		P13		
	SPRxSync[3]		D7		
	SPRxSync[4]		A7		
	SPRxSync[5]		B7		
	SPRxSync[6]		C6		
	SPRxSync[7]		D6		
	SPRxClk[0]	Receive Line Clock Input	N9	I	When the PHY serial interface is enabled, this is the receive line clock input. Note that Ports 2–7 are no-connects in the CX28224 and ports 4–7 are no-connects in the CX28225.
	SPRxClk[1]		P9	I	
	SPRxClk[2]		K14	I/PD	
	SPRxClk[3]		L16	I/PD	
	SPRxClk[4]		K15	I/PD	
	SPRxClk[5]		J13	I/PD	
	SPRxClk[6]		K16	I/PD	
	SPRxClk[7]		J14	I/PD	

***Table 2-5. CX28229 Pin Descriptions** (7 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Serial Line Interface	SPRxData[0]	Receive Line Data Input	T9	I/PD	When the PHY serial interface is enabled, this is the receive line data input.
	SPRxData[1]		R9		
	SPRxData[2]		P10		
	SPRxData[3]		J16		
	SPRxData[4]		J15		
	SPRxData[5]		H13		
	SPRxData[6]		H14		
	SPRxData[7]		H16		
	SPTxSync[0]	Frame Sync Input/ Output	P15	I/O	When the PHY serial interface is enabled, this is the frame sync. SPTxSync is input only for all port modes except DSL mode. In DSL Mode, SPTxSync is output only.
	SPTxSync[1]		M13		
	SPTxSync[2]		N15		
	SPTxSync[3]		P16		
	SPTxSync[4]		N16		
	SPTxSync[5]		M14		
	SPTxSync[6]		L13		
	SPTxSync[7]		E16		
	SPTxData[0]	Transmit Line Data Output	T6	O	When the PHY serial interface is enabled, this is the transmit line data output.
	SPTxData[1]		N8		
	SPTxData[2]		T7		
	SPTxData[3]		P8		
	SPTxData[4]		T8		
	SPTxData[5]		R8		
	SPTxData[6]		T13		
	SPTxData[7]		R13		
	SPTxClk[0]	Transmit Line Clock Input	R7	I	When the PHY serial interface is enabled, this is the transmit line clock input.
	SPTxClk[1]		N13		
	SPTxClk[2]		N14		
	SPTxClk[3]		R14		
	SPTxClk[4]		R15		
	SPTxClk[5]		T15		
	SPTxClk[6]		T16		
	SPTxClk[7]		R16		

Table 2-5. CX28229 Pin Descriptions *(8 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
ATM Layer UTOPIA Interface	atmUTxAddr[0]	ATM UTOPIA Transmit Address	E15	I	Transmit ATM Cell Bus address.
	atmUTxAddr[1]		D14		
	atmUTxAddr[2]		D13		
	atmUTxAddr[3]		D16		
	atmUTxAddr[4]		D15		
	atmUTxData[0]	ATM UTOPIA Transmit Data	C16	I	Transmit direction ATM side cell data.
	atmUTxData[1]		C15	I	
	atmUTxData[2]		B16	I	
	atmUTxData[3]		B15	I	
	atmUTxData[4]		B14	I	
	atmUTxData[5]		D12	I	
	atmUTxData[6]		B13	I	
	atmUTxData[7]		A14	I	
	atmUTxData[8]		H15	I/PD	
	atmUTxData[9]		G14	I/PD	
	atmUTxData[10]		G13	I/PD	
	atmUTxData[11]		G16	I/PD	
	atmUTxData[12]		G15	I/PD	
	atmUTxData[13]		F14	I/PD	
	atmUTxData[14]		A16	I/PD	
	atmUTxData[15]		A15	I/PD	
	atmUTxPrty	ATM UTOPIA Transmit Parity	A13	I	Parity status signal. In 8 bit Utopia mode, a parity calculation is performed over atmUTxData[7:0] for each clock cycle of atmUTxClk. Odd parity is used. In 16 bit Utopia mode, this signal is the parity of atmUTxData[15:0]. This signal is optional.

Table 2-5. CX28229 Pin Descriptions *(9 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
ATM Layer UTOPIA Interface	atmUTxClAv	ATM UTOPIA Transmit Cell Available	C12	O	Cell Available signal for Transmit ATM cells (active high).
	atmUTxSOC	ATM UTOPIA Transmit Start of Cell	D11	I	Start of Cell synchronization signal for transmit ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus.
	atmUTxEnb*	ATM UTOPIA Transmit Enable	B12	I	Data transfer enable for transmit ATM cells (active low). Indicates that the first byte/word of the 53 byte cell is being placed on the atmUTxData bus.
	atmUTxClk	ATM UTOPIA Transmit Clock	A12	I	Clock signal used for transfer of transmit ATM cells from the ATM Layer. The maximum clock rate is 33 MHz.
	atmURxSOC	ATM UTOPIA Receive Start of Cell	C9	O	Start of Cell synchronization signal for receive ATM cells (active high). Indicates that the first byte/word of the 53 byte cell is being placed on the atmURxData bus.
	atmURxClk	ATM UTOPIA Receive Clock	A9	I	Clock signal used for transfer of receive ATM cells from the ATM Layer. The maximum clock rate is 33 MHz.
	atmURxClAv	ATM UTOPIA Receive Cell Available	B9	O	Cell Available signal for receive ATM cells (active high). As a software option in the IMA16 application, the pin atmURxAdr[4] will function as a cell available status signal (atmURxClAv[1]) for ATM Utopia addresses 8–15 only. In this mode, atmURxClAv[1] will threestate for addresses 0–7.
	atmURxEnb*	ATM UTOPIA Receive Enable	D8	I	Data transfer and output enable for Receive ATM cells (active low).

Table 2-5. CX28229 Pin Descriptions *(10 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
ATM Layer UTOPIA Interface	atmURxData[0]	ATM UTOPIA Receive Data	C8	O	Receive direction ATM side cell data.
	atmURxData[1]		A8		
	atmURxData[2]		B8		
	atmURxData[3]		C7		
	atmURxData[4]		C5		
	atmURxData[5]		D5		
	atmURxData[6]		A5		
	atmURxData[7]		B5		
	atmURxData[8]		C11		
	atmURxData[9]		B11		
	atmURxData[10]		D10		
	atmURxData[11]		C10		
	atmURxData[12]		A11		
	atmURxData[13]		B10		
	atmURxData[14]		D9		
	atmURxData[15]		A10		
	atmURxPrty	ATM UTOPIA Receive Parity	C4	O	Parity status signal. In 8 bit Utopia mode, a parity calculation is performed over atmURxData[7:0] for each clock cycle of atmURxClk. Odd parity is used. In 16 bit Utopia mode, this signal is the parity of atmURxData[15:0]. This signal is optional.
	atmURxAddr[0]	ATM UTOPIA Receive Address	D4	I	Receive ATM Cell Bus address. This address determines the source channel of the Receive ATM cells output from the IMA subsystem and also selects the channel sourcing the atmURxClAv signal. All 5 bits are not required in every application.
	atmURxAddr[1]		A4		
	atmURxAddr[2]		B4		
	atmURxAddr[3]		C3		
	atmURxAddr[4]		D3		

***Table 2-5. CX28229 Pin Descriptions** (11 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Power Supply	V_{DD} (1.8 V)	Supply Voltage (1.8 V)	G5 G6 G11 G12 H5 H6 H11 H12 J5 J6 J11 J12 K5 K6 K11 K12		Power supply connections. (1.8 V)
	V_{DD} (3.3 V)	Supply Voltage (3.3 V)	E5 E6 E7 E8 E9 E10 E11 E12 F5 F6 F7 F8 F9 F10 F11 F12 L5 L6 L7 L8 L9 L10 L11 L12 M5 M6 M7 M8 M9 M10 M11 M12		Power supply connections. (3.3 V)

Table 2-5. CX28229 Pin Descriptions *(12 of 12)*

	Pin Label	Signal Name	No.	I/O	Description
Power Supply	V_{SS} GND	Ground	G7 G8 G9 G10 H7 H8 H9 H10 J7 J8 J9 J10 K7 K8 K9 K10		Ground connections.
	VGG	Electrostatic Discharge (ESD) Supply Voltage	B3		Provides ESD protection when interfacing with 5 V systems. If using this device in a system with 5 V logic, this pin must be connected to 5 V. If using 3.3 V system, connect to 3.3 V.

FOOTNOTE:

(1) This bus is enabled by pulling the ExtMemSel pin high. External Memory is disabled on the CX28224 and CX28225 versions of the device.

2.4 Stand Alone Cell Delineation

Figure 2-7 is an example of a non-IMA application. The CX28229 is being used as a stand alone Cell Delineator. Cell Delineation is performed internally and the CX2822x interfaces directly to the framers. These framers could be T1/E1 or DSL.

NOTE: Most applications would use the less expensive RS8228 or M28228 Cell delineator. However, there may be applications that require the flexibility of the CX28229. This mode is also useful for troubleshoot during development since the IMA software drivers are not required. Configuration information is shown inTable 2-6.

Figure 2-7. Non-IMA Application

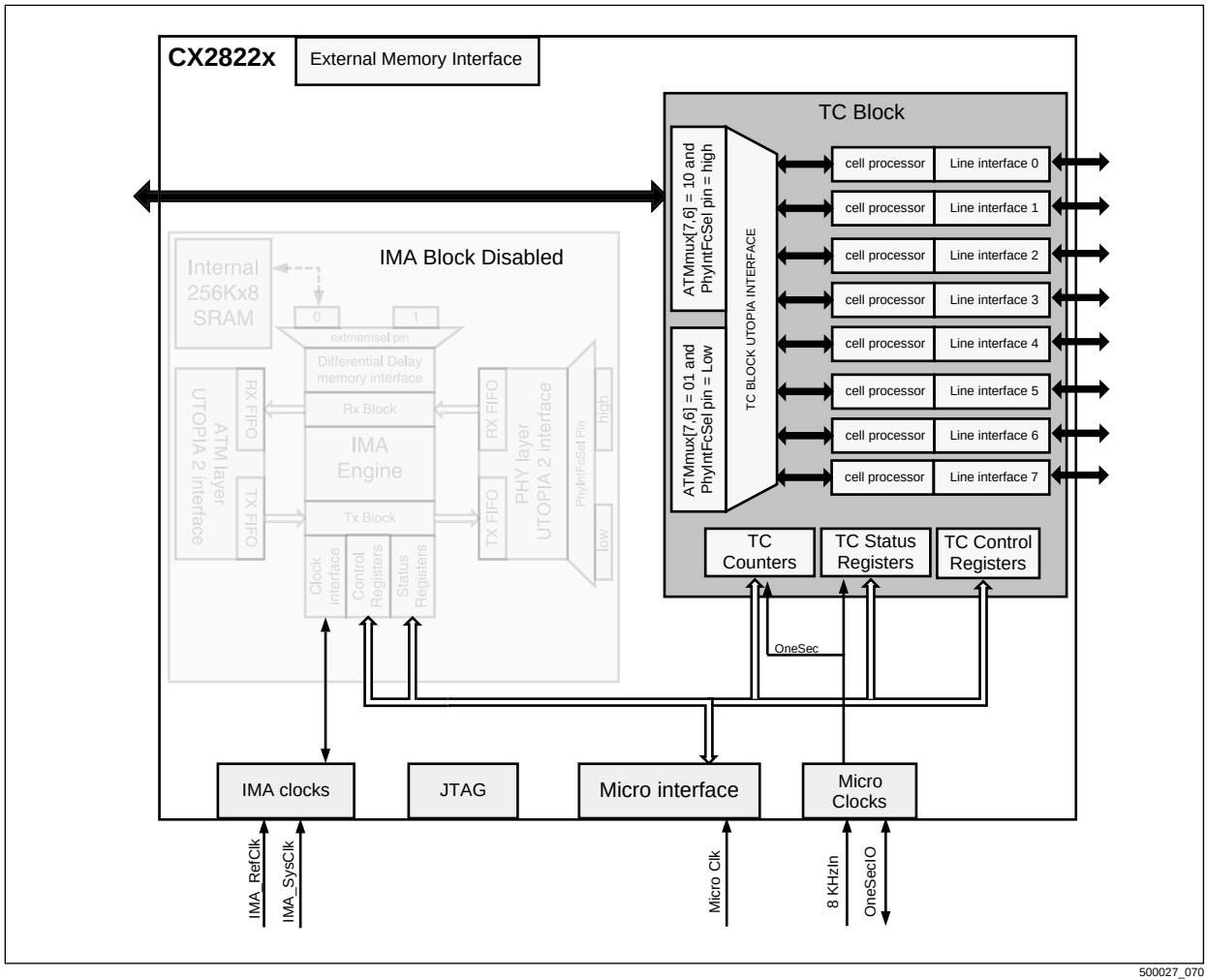


Table 2-6. Cell Delineation Configuration Information

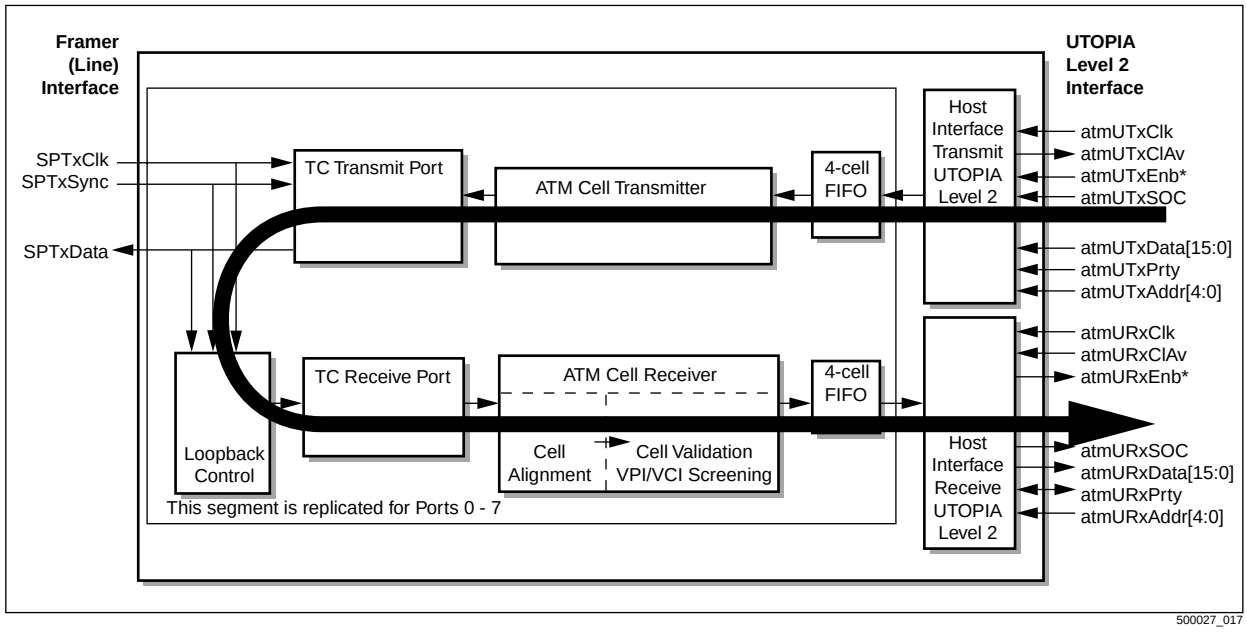
ATMMux [7,6] (ATMINTFC, 0x202)	PhyIntFcSel (Pin R4)	Description
10	High	TC Block Direct; Device used as Stand-alone cell delineator with 8 serial ports; IMA block not used.

2.5 Source Loopback (UTOPIA-to-Serial Configuration Only)

Source loopback checks that the host (the ATM layer) is communicating with the PHY. It is enabled and disabled in bit 5 of the PMODE register (0x04). When source loopback is enabled for a given port, all data transmitted by the CX2822x on that port is also looped back through the Receive Line Interface. Data from the framer interface is ignored.

NOTE: During Source loopback, the port is automatically placed in General Purpose mode and MicroClk used as the clock to loop back cells. As a result of the automatic mode switch and clock used, the data on the Tx serial lines will be corrupted.

Figure 2-8. Source Loopback Diagram (This only shows the TC Block. IMA Block in pass-through mode.)

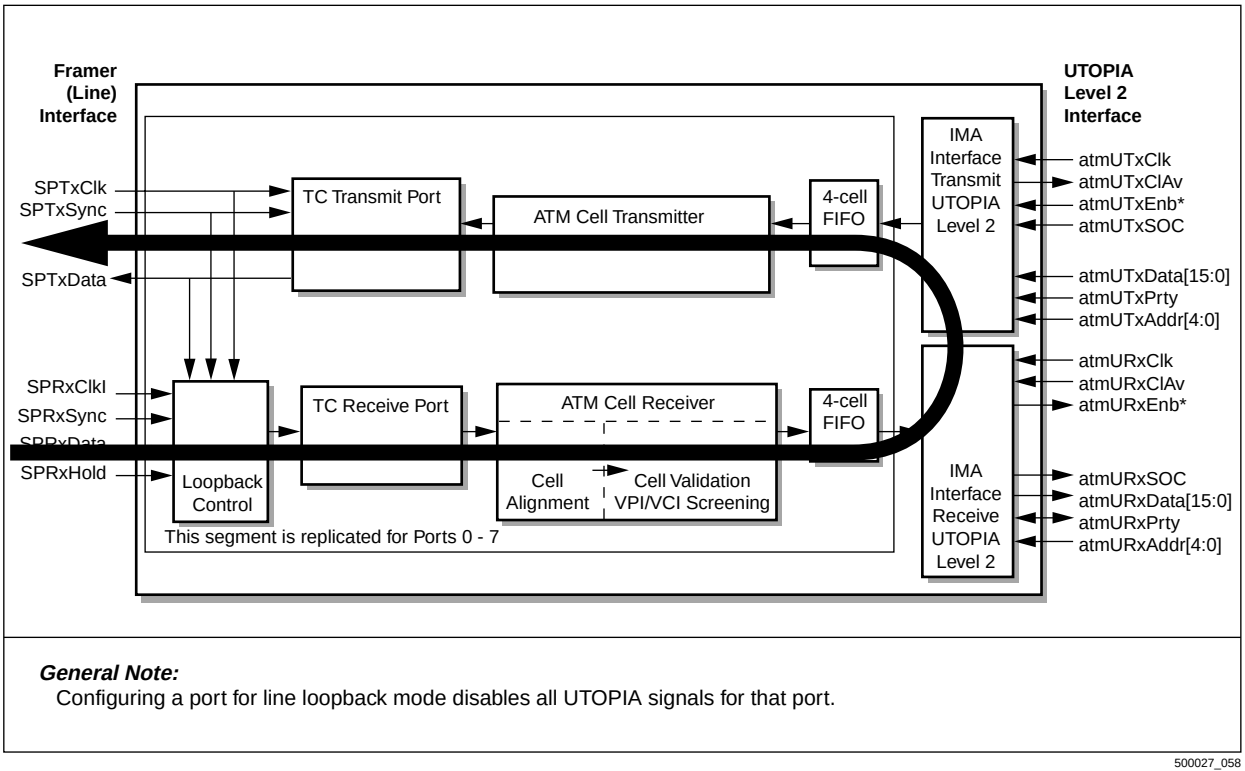


2.6 Far-End Line Loopback (Serial Configuration Only)

Far-End Line loopback verifies Line interface is communicating with the PHY. It is enabled by bit 4 of the PMODE register (0x04). When line loopback is enabled for a given port, all data received by the CX2822x on that port is processed by the Receive Line Interface and transmitted out the line interface. Data from the Transmit UTOPIA bus is ignored.

NOTE: SPTxClk, SPRxClk, SPTxSync, and SPRxSync must be present for the loopback mode to function properly for a given port.

Figure 2-9. Far-End Line Loopback (This only shows the TC Block.)



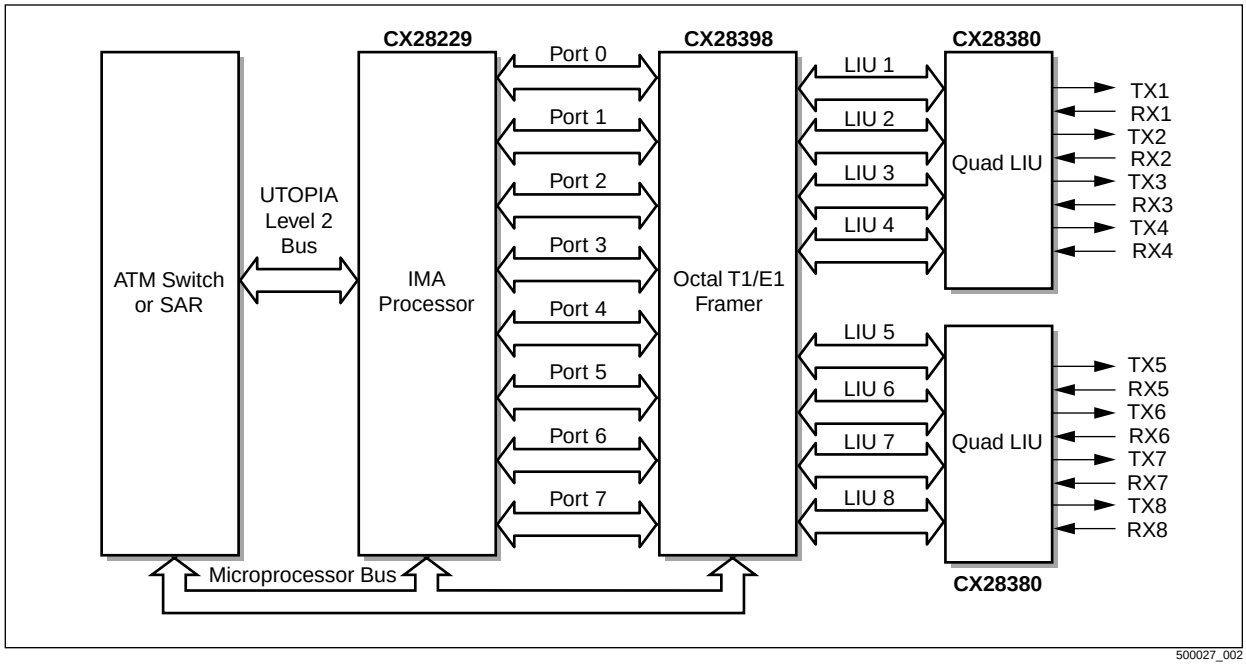
General Note:
Configuring a port for line loopback mode disables all UTOPIA signals for that port.

500027_058

2.7 Application Overview

The CX2822x is typically used with line framer devices like the CX28398 T1/E1 octal transceiver, the Bt8970 Zip Wire or the CX28398 HDLC Framer. Figure 2-10 illustrates a typical application.

Figure 2-10. CX2822x Connected to a CX28398 Transceiver



2.8 Reference Designs

Please contact Mindspeed for information on reference designs and schematic examples.

3 IMA Clocks

In order to maintain transmit frame synchronization the IMA engine must know the exact cell rate of each group. This is provided by the Transmit IMA Data Cell Rate clock (Tx IDCR). In addition, to operate the Receive Cell Smoothing buffer the device must know the Receive IMA Data Cell Rate (Rx IDCR). There is a Tx IDCR and Rx IDCR for each of the 16 groups that the CX29229 supports.

The CX29229 provides for tremendous flexibility with regard to these clocks. An oveview of the clocking circuitry is shown in Figure 3-1. While this can appear to be overwhelming at first glance, most applications are actually quite straightforward. The situation is also simplified by the software driver; it will calculate and program most of the control registers automatically. The hardware designer only needs to ensure that the proper clocks are available for the architecture desired.

In addition, two clock outputs are also provided: Tx_TRL[1] and Tx_TRL[0]. These can be used to output one of the reference clock inputs or generate an 8 kHz reference that is phase locked to IMA_SysClk or IMA_RefClk (whichever is used as a timing reference).

The IDCR Clocks can be derived from one of four input sources:

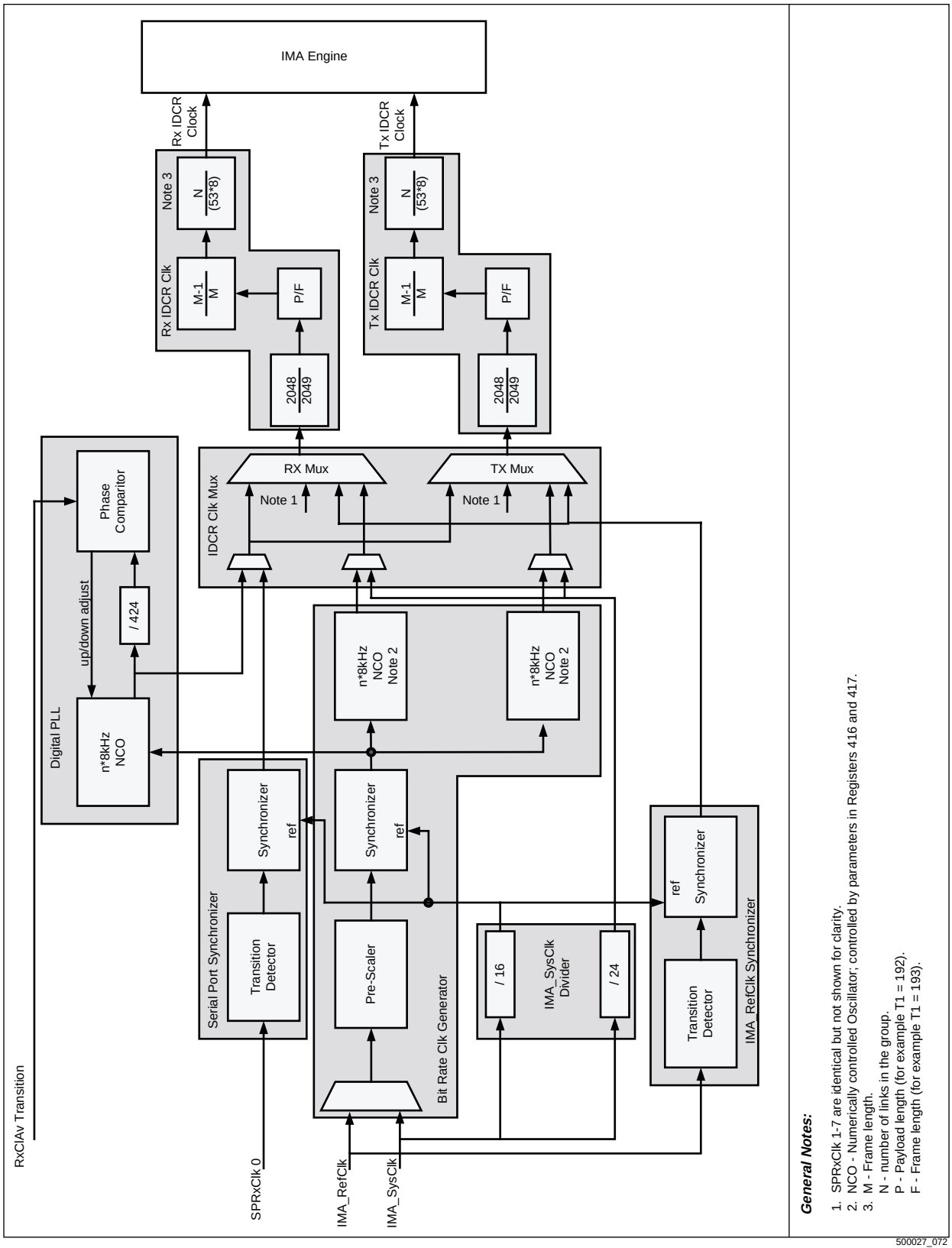
1. IMA_SysClk: This is the primary IMA system clock and is used by most of the internal IMA logic. It is also used to generate the PHY side UTOPIA Rx and Tx clocks (phyURxClk and phyUTxClk).
2. IMA_RefClk: This is used with applications where multiple Transmit references are available and/or when it is possible or necessary to run asynchronously relative to IMA_SysClk. This signal is either a line or payload rate reference clock or is a high speed (*n* x 8 kHz) reference clock from which nominal Transmit and Receive payload rates can be derived.
3. Receive bit clock: When operating in the UTOPIA-to-Serial mode the CX2822x can select any of the Rx bit clocks to use as the reference clock. The receive direction timing is used for recovering the IMA frame rate of the received IMA group. Using this option for the Transmit IMA group frame rate results in a 'line timed' configuration.
4. phyURxClAv: This is the PHY side UTOPIA Rx Cell Available signal, which tracks the actual cell data rate being transferred from an individual port. Internal synthesizers can use this signal in place of the serial Rx bit clocks to derive the payload rate for each Receive port. The receive direction timing is used for recovering the IMA frame rate of the received IMA group. Using this option for the Transmit IMA group frame rate results in a 'line timed' configuration.

Figure 3-1 shows the details of the CX28229's IMA clock block from Figure 1-1. This block is responsible for generating all clocks required by the IMA engine. It can be further divided into 8 sections, as shown in Table 3-1:

Table 3-1. IMA Block Clock Sections

Clock Section	Description
Serial Port Synchronizer	This block contains a transition detector and a synchronizer. It synchronizes the clocks from the TC block Serial ports to the IMA_SysClk divided by 16. It handles all 8 internal serial ports independently.
IMA_SysClk Dividers	This block contains two dividers: a divide by 16 and a divide by 24. The divide_16 is used to synchronize external clocks to internal logic. The divide_24 allows the IMA_SysClk to be used to generate both the Rx IDCR and the Tx IDCR clocks (provided that IMA_SysClk is 24 times the bit rate).
IMA_RefClk Synchronizer	This block contains a transition detector and a synchronizer. It synchronizes the IMA_RefClk to the IMA_SysClk divided by 16.
IDCR Source Mux	This software controlled mux selects which clock sources are feed to the appropriate IDCR clock dividers.
Rx IDCR Clock	This block divides the bit rate clock down to a link cell data rate clock based on the values of frame length (M), number of links in the group (N), frame payload (P) and frame bit (F). (The 2048/2049 factor results from the IMA standards requirement of inserting a stuff event every 2048 cells.) This block can generate 16 independent Rx IDCR clock outputs (one per group).
Tx IDCR Clock	This block divides the bit rate clock down to a Link cell data rate clock based on the values of frame length (M), number of links in the group (N), frame payload (P) and frame bit (F). (The 2048/2049 factor results from the IMA standards requirement of inserting a stuff event every 2048 cells.) This block can generate 16 independent Rx IDCR clock outputs (one per group).
Bit Rate Clock Generator	This block generates a clock that represents the link data rate. It can generate 16 independent Tx and 16 independent Rx clocks. In normal operation, all parameters are configured automatically by the software driver. It contains the following blocks: • Pre-scaler—This block divides the selected input (either IMA_RefClk or IMA_SysClk) by the factor of Pnum divided by Pden. • Synchronizer—Synchronizes the Pre-Scaler output to the internal logic using the IMA_SysClk divided by 16. • Numerically Controlled Oscillator—This clock circuit generates the link bit rate.
Digital Phase Locked Loop	This block generates a bit rate clock that is phase locked to the PHY side RxClAv signal. It can monitor all 32 ports on the bus. Any port can be selected as the group timing reference.

Figure 3-1. CX28229 Clock Diagram



3.1 Common Applications

The solution for high port count and variable rate DSL applications is to use internal counters and frequency synthesizers referenced from a common (n x 8 kHz) clock input with feedback from the cell available signal from the PHY side UTOPIA bus.

For low port count, single rate applications that take advantage of the embedded ATM Cell Processor, the use of receive bit clock inputs is the most straight-forward solution.

Several of the most common applications follow.

3.1.1 T1/E1 Using Internal Serial Ports

3.1.1.1 Using IMA_SysClk as the Transmit Clock

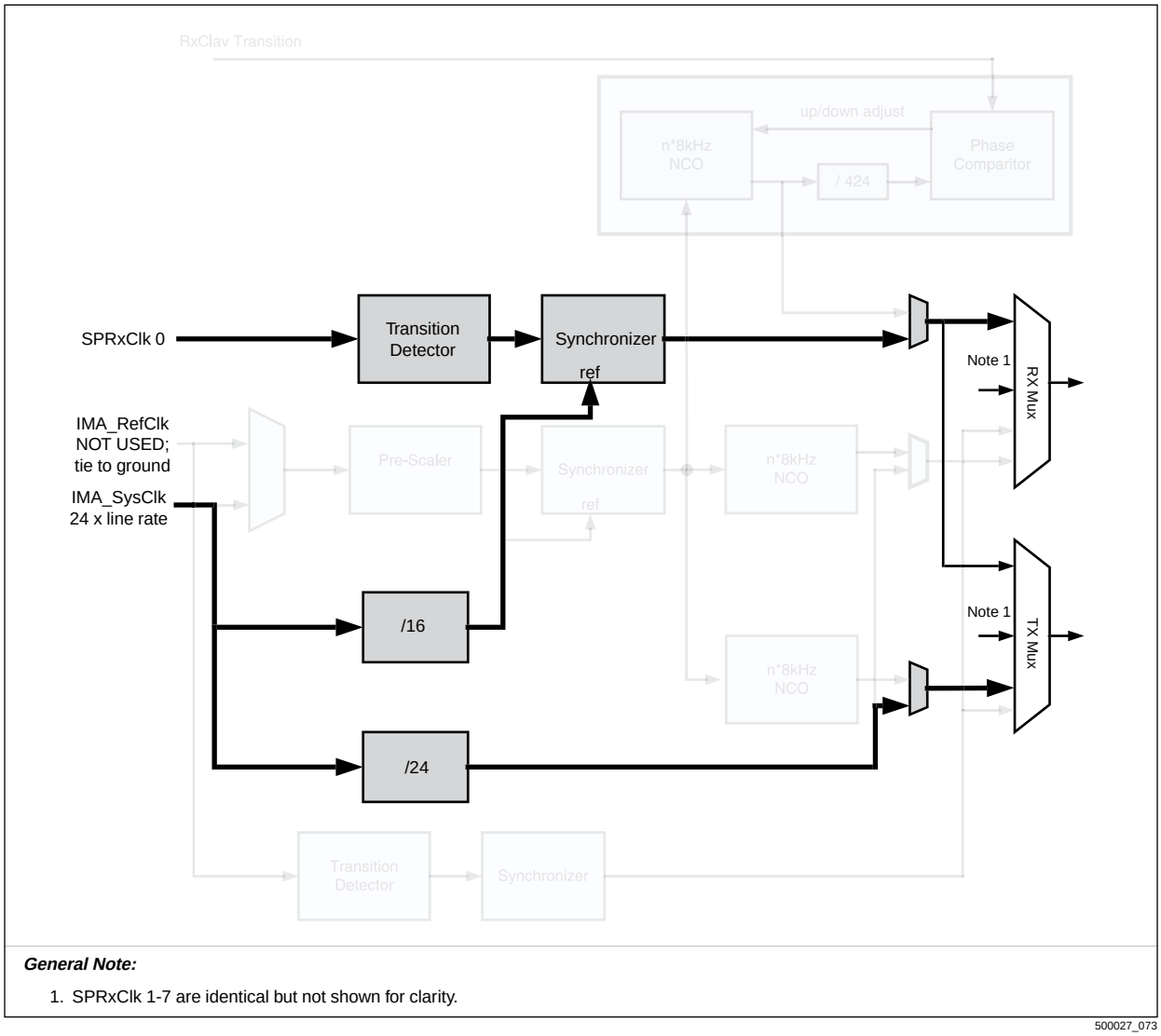
Figure 3-2 illustrates T1/E1 with internal serial ports, using IMA_SysClk equal to 24 times the line rate. This is one of the simplest implementation of IMA when a clock equal to 24 times the line rate is available. Several issues are worth noting:

- The IMA_RefClk input is unused and should be tied to ground. The CX28229 is deriving all required clocks from the Serial port clocks and the IMA_SysClk.
- The IMA_SysClk is used to synchronize the SPRxClk inputs to internal logic (via the divide by 16 block).
- The SPRxClk is being used to generate the Rx IDCR clock. Also note that the receive clock from any link within a group could be used to generate the Rx IDCR for that group.
- The IMA_SysClk is being used to derive the TX IDCR clock.

The device is configured using a software driver. The following code is an example of calls to the driver:

```
IMA_LINK_TYPE = IMA_DS1
IMA_DSL_USE_REF_CLK2 = IMA_INACTIVE
IMA_DSL_REF_GENERATOR = IMA_INACTIVE
IMA_ALT_RX_TRL = IMA_INACTIVE
IMA_GRP_TX_TRL_SRC = IMA_REF_XCLK (grp#)
IMA_GRP_RX_TRL_SRC = IMA_RX_TRL_(x) (grp#)
```

Figure 3-2. T1/E1 using Internal Serial ports; IMA_SysClk equals 24x line rate



General Note:

1. SPRxClk 1-7 are identical but not shown for clarity.

500027_073

3.1.1.2 Using IMA_RefClk as the Transmit Clock

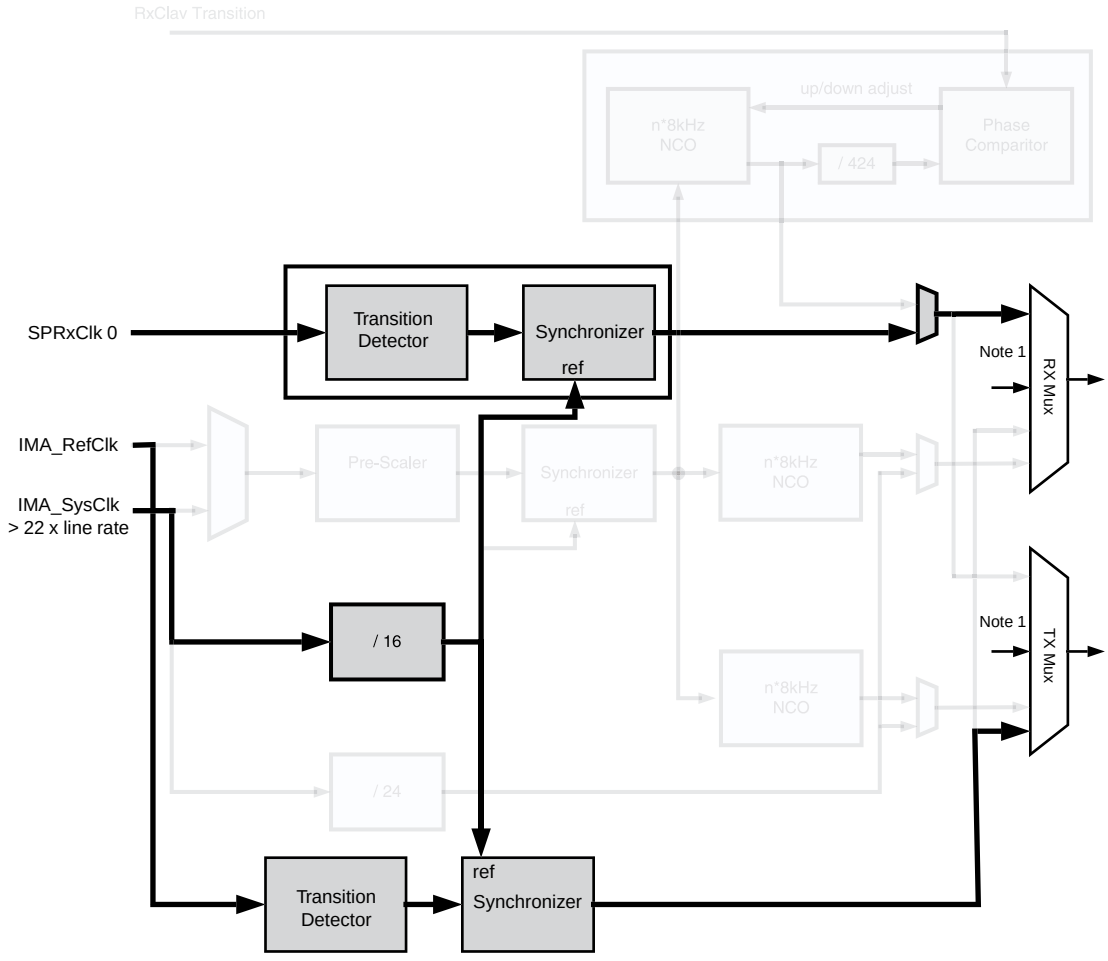
Figure 3-3 illustrates T1/E1 with internal serial ports, using IMA_RefClk. There are several important differences from the first example:

- In this case, IMA_SysClk is only used by internal logic. It must be greater than or equal to 22 times the line rate to ensure that internal logic can keep up with the data.
- Again, the SPRxClk is used to generate the RxIDCR clock.
- The TX IDCR clocks are generated from the IMA_RefClk. Thus IMA_RefClk must equal 1.544, 1.536, 2.028, or 1.920 MHz depending of the frame format used.

The device is configured using a software driver. The following code is an example of calls to the driver:

```
IMA_LINK_TYPE = IMA_DS1
IMA_DSL_USE_REF_CLK2 = IMA_INACTIVE
IMA_DSL_REF_GENERATOR = IMA_INACTIVE
IMA_ALT_RX_TRL = IMA_INACTIVE
IMA_GRP_TX_TRL_SRC = IMA_REF_CLK1 (grp#)
IMA_GRP_RX_TRL_SRC = IMA_RX_TRL_(x) (grp#)
```

Figure 3-3. T1/E1 using Internal Serial ports; IMA_RefClk equals line rate



General Note:

1. SPRxClk 1-7 are identical but not shown for clarity.

500027_074

3.1.2 DSL/T1/E1 Using UTOPIA-to-UTOPIA Interfaces

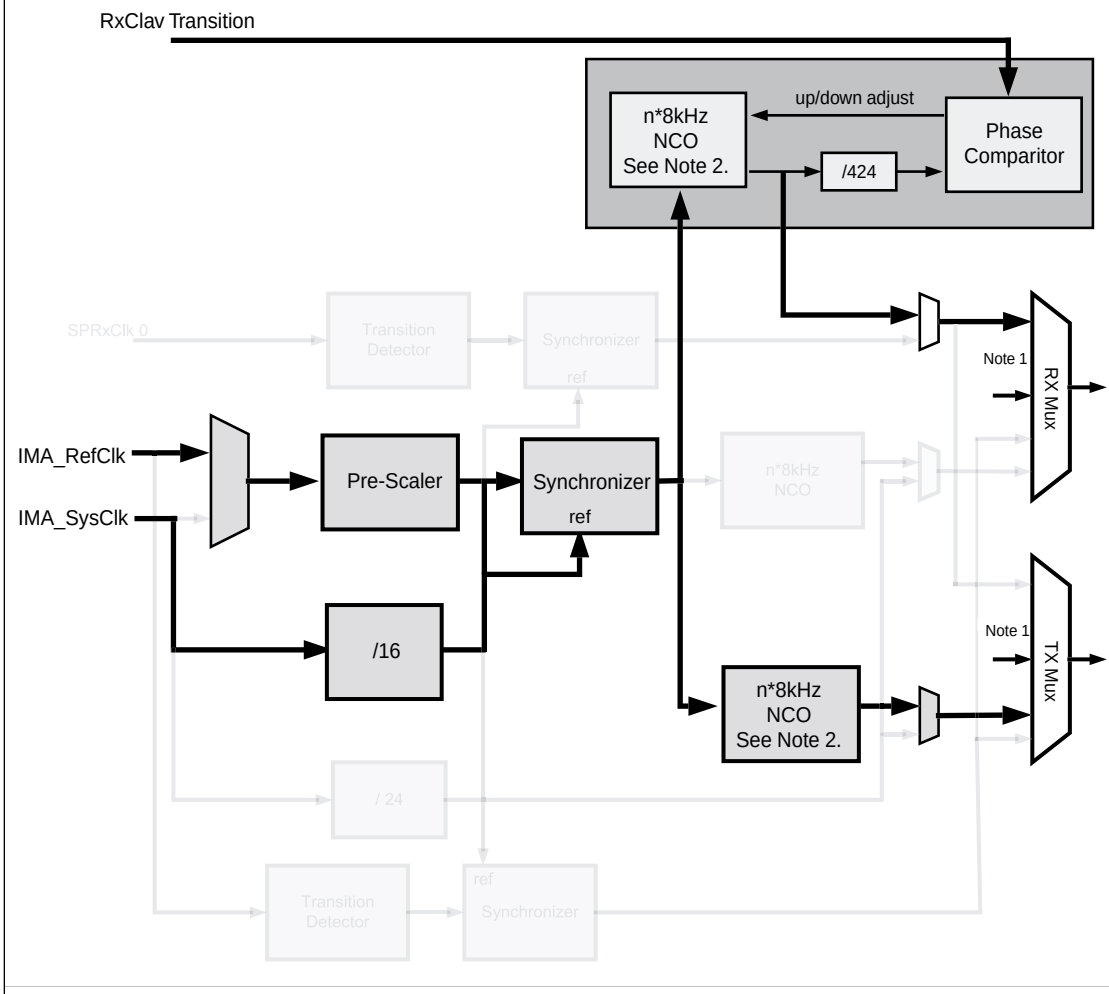
Figure 3-4 illustrates the configuration most commonly used with applications that require more than 8 ports. Up to 32 links and 16 groups can be supported using external Cell Delineators such as the RS8228.

- The Rx IDCR clock is synthesized using the RxClAv input from the PHY side UTPOIA bus. This is performed on a per group basis; that is, one link in each group is selected (via software) to provide the Rx IDCR for that group.
- IMA_SysClk must be greater than or equal to 40.96 MHz (less than 24 ports) and be greater than or equal to 49.152 MHz if there are more than 24 ports.
- Either IMA_SysClk or IMA_RefClk can be used as the Tx IDCR clock:
  - IMA_SysClk may be used if it is an 8 kHz multiple of the bit rate.
  - IMA_RefClk may be used if it is an 8 kHz multiple of the bit rate and greater than or equal to 4.64 MHz.

The device is configured using a software driver. The following code is an example of calls to the driver:

```
IMA_LINK_TYPE = IMA_VAR_RATE
IMA_DSL_REF_CLK_FREQUENCY = 40960000
IMA_DSL_USE_REF_CLK2 = IMA_INACTIVE
IMA_DSL_REF_GENERATOR = IMA_ACTIVE
IMA_ALT_RX_TRL = IMA_ACTIVE
IMA_GRP_LINK_BANDWIDTH = 2304 (grp#)
IMA_GRP_CLK_REF_FACTOR = IMA_NO_DIV (grp#)
IMA_GRP_TX_TRL_SRC = IMA_REF_XCLK (grp#)
IMA_GRP_RX_TRL_SRC = IMA_RX_TRL_(x) (grp#)
```

Figure 3-4. DSL—UTOPIA-to-UTOPIA



General Notes:

1. SPRxClk 1-7 are identical but not shown for clarity.
2. NCO - Numerically controlled oscillator; controlled by parameters in Register 416 and 417.

500027_075

4 UTOPIA Interfaces

The CX2822x supports multi-PHY operation as described in the UTOPIA Level specification (AF-PHY-0039.000, see www.atmforum.com). This standard allows up to 31 ports to interface to one ATM layer device. The interface uses either 8-bit or 16-bit wide data buses, and cell-level handshaking. The 16-bit mode, which can run at 50 MHz, supports data rates up to 800 Mbps. The Cx2822x implementation does not support octet level handshaking or UTOPIA parity.

Each of the CX2822x's UTOPIA blocks has two sections, transmit and receive, each of which has a 4-cell FIFO buffer. ATM cell data is placed in the transmit FIFOs where it can then be passed to the ATM cell processing block. On the receive side of the UTOPIA interface, incoming cells are placed in the receive FIFO until sent.

With regard to IMA, each IMA group is considered one logical port and will only take up one UTOPIA address. For example, a group with 8 T1 links could be assigned to address 0; the IMA engine handles the translation between the ATM layer and the physical links. In addition, each pass-though connection also requires one address.

NOTE: By convention, data being transferred from the PHY to the ATM layer is considered received data, while data from the ATM layer to the PHY is called transmitted data.

To provide maximum flexibility for system design the CX28229 has 3 UTOPIA Level 2 interfaces. This allows the CX28229 to be used in either UTOPIA-to-UTOPIA or UTOPIA-to-Serial IMA applications or it can function as a stand-alone cell delineator block. These interfaces are shown in Figure 4-1 and described below.

1. IMA direct—This interface allows the ATM layer to interface directly to the IMA engine. This would be the normal mode for all IMA applications. It is controlled by registers in the IMA section.
2. TC block direct—This interface is selected when the IMA engine is disabled and the device is being used as a stand-alone cell delineator. It may also be invoked during troubleshooting to verify serial port operation without having to run the IMA drivers. It is configured by registers in the TC section.
3. PHY side UTOPIA—This interface is selected when the TC block is disabled and the designer wishes to interface to a device via an UTOPIA interface. This allows the CX28229 IMA engine to address up to 32 ports on the line side.

4.1 General UTOPIA Operation

Three primary functions are performed by the UTOPIA controller: polling, selection, and data transfer. These functions are basically the same for both the transmit and receive sides of the UTOPIA bus. The following example describes the transmit functions. Refer to Figure 4-1.

The ATM layer UTOPIA controller polls the connected PHY ports by transmitting the port addresses on the UTxAddr lines. If a port is ready to transfer data, it asserts UTxClAv. Note that the process of polling a port does NOT result in that port being selected to transfer data! Polling allows the controller to determine which port is ready for data; it must then select that port before sending data. It does so by reasserting the desired address and then asserting UtxEnb*. The PHY will then be ready to transfer data on the UTxData lines. UTxEnb* is deasserted when the transfer is completed. Polling can continue during the data transfer process but not during port selection. It operates independently of the state of UTxEnb*.

To pause the data transfer, UTxEnb* can be deasserted. To continue the transfer, the controller must reselect the port by transmitting its address one clock cycle before asserting UTxEnb*. The controller must ensure that the cell transfer from this port has been completed, to avoid a start-of-cell error.

4.2 UTOPIA 8-bit and 16-bit Bus Widths

The CX2822x has two bus width options, 8-bit or 16-bit, which are selected in BusWidth, bit 2, of the MODE register (0x0202). The protocols and timing are the same in both modes, except that 8-bit mode uses only the lower half of the data bus (TxData[7:0] and RxData[7:0]) and parity is only generated or checked over those bits. UTOPIA Level 2 8-bit operates up to 33 MHz and Level 2 16-bit up to 50MHz.

NOTE: CX28224 only supports 8 bit UTOPIA.

In 8-bit mode, each ATM cell consists of 53 bytes, as listed in Table 10-8. The first five bytes are used for header information. The remaining bytes are used for payload.

In 16-bit mode, the cell consists of 54 bytes, as listed in Table 10-9. The first five bytes contain header information. The sixth byte, UDF2, is required to maintain alignment but is not read by the CX2822x. The remaining bytes are used for payload.

4.3 IMA UTOPIA

This is the normal interface for IMA applications and is selected as shown in Table 4-1.

It is intended to interface to a single ATM Layer device and appear as a multi-port PHY device. Figure 4-1 illustrates the connections to/from the ATM Layer device. The number of "ports" or channels on the IMA Subsystem is the sum of the number of configured IMA groups plus the number of pass-through facilities. The IMA CX28229 requires a unique Utopia address for each channel (IMA group or pass-through). There are no restrictions placed on the address assignment and not all 32 locations are normally used.

If only one channel is programmed, (a single IMA group and no pass-through facilities), then the CX28229 can be compatible with UTOPIA Level 1 by fixing the address lines to a specific value and setting the IMA group's ATM address (through the software driver) to that value.

The CX28229 provides numerous options to match non-standard UTOPIA controllers. See the IMA_ATM_UTOPIA_BUS_CTL register, 0x413, for more information.

NOTE: 0x1F can be assigned as a valid port address to enable 32 port bypass.

4.4 TC Block UTOPIA

This interface is selected when using the device as a stand-alone cell delineator. See Table 4-1 and Section 2.4. It interfaces to the ATM layer as a normal UTOPIA Level 2 interface with the following enhancements.

UDF2 Programmability

The user can program the contents of the UDF2 byte when operating in 16-bit UTOPIA mode. Be default, the contents of the UDF2 byte (detailed in Table 10-9) on the receive interface will match the default value of the UTOPIA port address. This can be changed by writing the desired value to the corresponding UDF2 control register, 0x0F. Bus width is controlled by bit 5 of the ATMINTFC register.

Port Number Assignment

The UTOPIA address for each port is stored in bits 0–4 of the UTOP2 register (0x0E). The default for this value is the port number. For example, the UTOP2 register for port 4 (0x10E [with the offset]) defaults to 04 hex. However, the value can be changed to any value from 00–1E hex by programming the register to accommodate multiple devices on the same UTOPIA bus. The value 1F hex is reserved for the null address. The UTOPIA address should be changed only when the device or port is in the reset state.

UTOPIA Receive Disable

The CX2822x has a UTOPIA receiver output disable feature which allows the user to set up redundant or back-up PHYs with the same UTOPIA address on the same UTOPIA bus. In this setup, both PHYs' transmitters are enabled, sending out identical data streams. Both PHYs' receivers are enabled, but only one is transferring data to the ATM device. The receiver output is disabled in the backup PHY by writing the UtopRxDis, bit 5, in the UTOP2 register (0x0E) to a logical 1. This disable places five of the backup PHY's signals, URxData, URxPrty, URxSOC, URxClAv, and UTxClAv, in a high-impedance state, preventing data and control signals from being passed to the ATM layer device. The disabled receiver will flush its FIFOs at the same rate as the enabled one, but all data it has received, except the last four cells, will be lost. Should the primary PHY device encounter an unacceptable error rate, software can quickly enable the backup PHY and disable the primary PHY, reducing cell loss in the transition.

HEC Override

In normal operation, the HEC is calculated by the TC layer and put in byte 5, UDF1. This may be overridden by setting bit 7 of the CGEN register (0x08) to a 1. In this case, data inserted by the ATM layer into byte 5 is transmitted unchanged by the device.

Table 4-1. Device Configuration Options

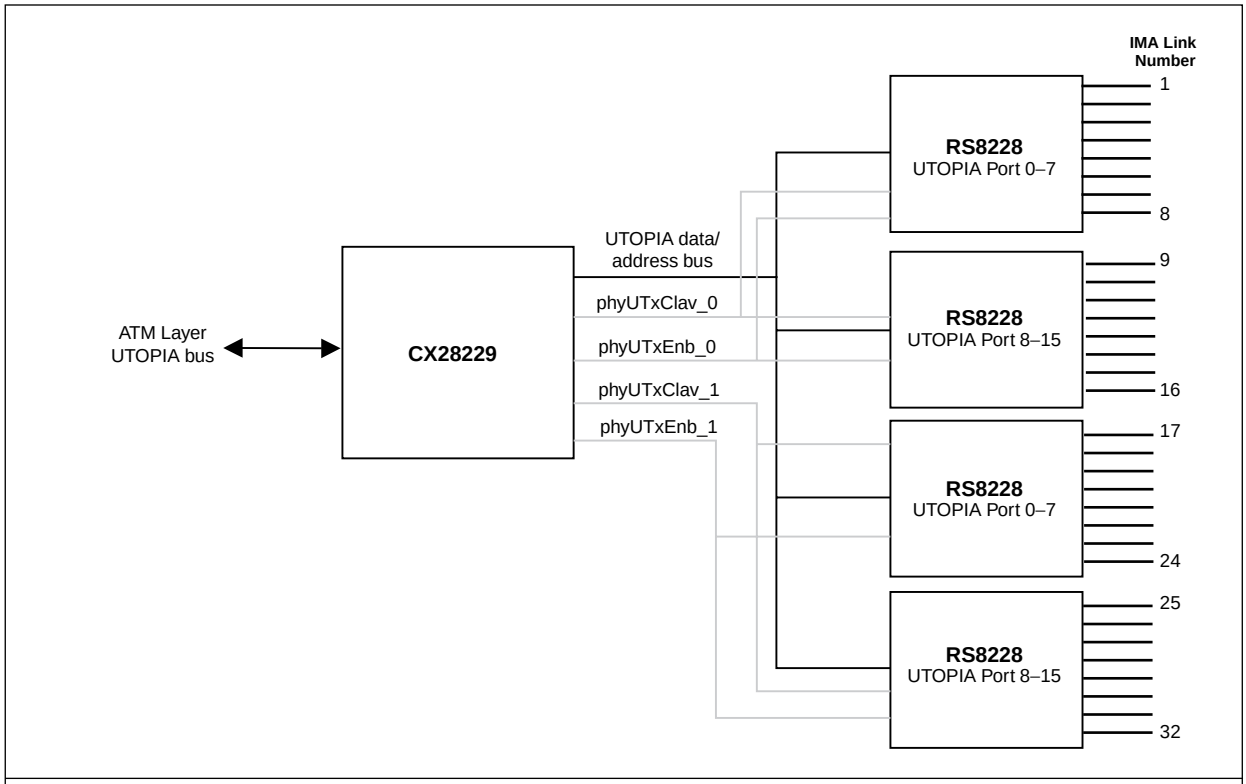
ATMMux [7,6] (ATMINTFC, 0x202)	PhyIntFcSel (Pin R4)	Description
01	Low	IMA UTOPIA using the PHY Side UTOPIA; UTOPIA-to-UTOPIA; TC block/serial ports not used.
01	High	IMA UTOPIA using Internal TC block; UTOPIA-to-Serial mode; 8 internal serial ports
10	High	TC only; Device used as Stand-alone cell delineator with 8 serial ports; IMA block not used.

4.5 PHY Side UTOPIA

An ATM forum compliant UTOPIA interface is provided for interfacing to PHY layer devices. Several unique features should be noted:

1. It is only UTOPIA level 2.
2. This bus only supports an 8 bit wide data path. This was done to simplify routing issues and reduce pin count.
3. The UTOPIA interface has a second set of control lines, which allow 32 addresses. These can be connected as shown in Figure 4-1. This effectively provides two buses with 16 devices each, all sharing common address and data lines but with separate control lines. (Remember, UTOPIA uses address 0x31 as the null address thus limiting the bus to 31 ports. However, the standard also allows for multiple ClAv and Enable lines.)

Figure 4-1. CX28229 Multiple UTOPIA Control Lines



General Note:

Only the Transmit side is shown for clarity. The Receive side is identical.

500027_056

5 Transmission Convergence Block

The CX2822x's ATM Transmission Convergence (TC) block is responsible for recovering cell alignment using the HEC octet, performing detection/correction, and descrambling the payload octets. The resulting ATM cells are then passed to the ATM layer via the UTOPIA interface. Simultaneously, the ATM transmitter block is receiving data from the ATM layer, optionally inserting header fields, optionally calculating the HEC, and sending the cells to the framers. If no data is being received from the ATM layer, the cell processor generates idle cells based on the data programmed into the associated registers.

NOTE: When operating in the UTOPIA-to-UTOPIA mode, the ATM Cell processor block is disabled.

5.1 ATM Cell Transmitter

The ATM cell transmitter controls the generation and formatting of 53-octet ATM cells that are sent to the Framer (Line) Transmit Ports. This block formats an octet stream containing ATM data cells from the ATM layer device when those cells are available. All 53 octets of the data cells may be obtained from the external data source and formatted into the outgoing octet stream.

This block calculates the HEC octet in the outgoing cell from the header field. The calculated HEC octet can be inserted in place of the incoming data octet by writing DisHEC (bit 7) in the CGEN register (0x08) to a logic 0. For testing purposes, this HEC octet can be corrupted by XORing the calculated value with a specific error pattern input set in the ERRPAT register (0x0B). This HEC error is achieved by writing ErrHEC (bit 4) in the CGEN register (0x08) to a logic 1. The remaining 48-octet payload field of the outgoing cell is obtained from the external data source. The payload can be scrambled.

When there is no data from the ATM layer device, the TC Block inserts idle cells automatically in the outgoing octet stream. The 4-octet header field for these idle cells comes from the TXIDL1–4 registers (0x14–17). The HEC octet is calculated and inserted automatically. The payload field is filled with the octet contained in the IDLPAY register (0x0A).

In normal operation, the 4-octet header field in the outgoing cell is passed on from the ATM layer device. Header patterns can be modified in the TXHDR1–4 registers (0x10–13) and inserted into outgoing cells in place of header bytes received from the ATM layer. Whether the original header cells or replacement cells are sent is controlled by bits 0–4 in the HDRFIELD (0x09) register.

5.1.1 HEC Generation

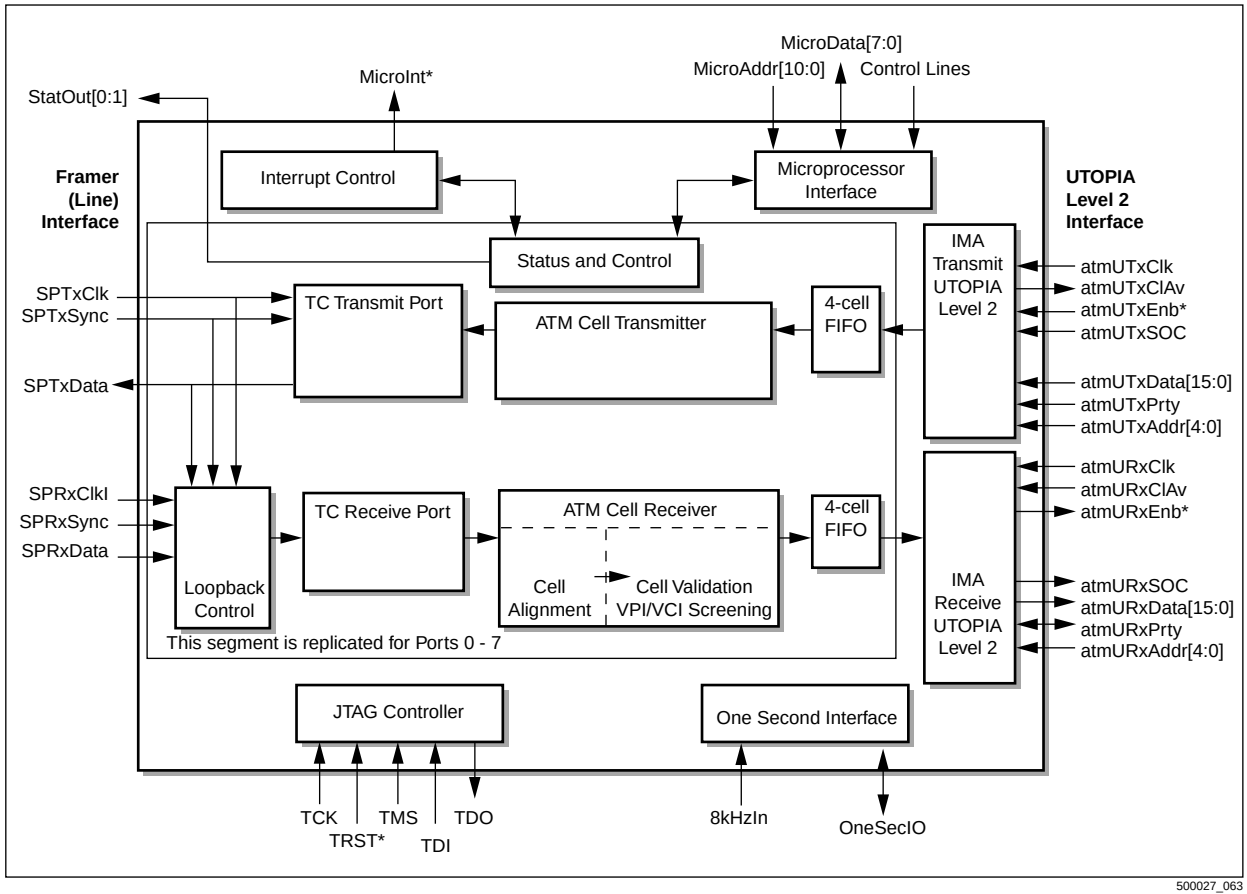
In normal operation, the CX2822x calculates the HEC for the four header bytes of each cell coming from the ATM layer. It then adds the HEC coset (55 hex, by ATM standards) and inserts the result in octet 5 of the outgoing cell. HEC calculation can be disabled by setting bit 7 of CGEN (0x08) to a 1. When HEC is disabled, the CX2822x leaves the contents of the HEC field unchanged and transmits whatever data is placed in that field by the ATM layer.

The HEC coset is used to maintain a value other than zero in the HEC field. If the first four bytes in the header are zero, the HEC derived from these bytes is also zero. When this occurs and there are strings of zeros in the data, the receiver cannot determine cell boundaries. Therefore, it is recommended that the value 55 hex be added to the HEC before transmission. To enable the HEC coset on the transmit side, set bit 6 in register CGEN (0x08) to one. To enable the receive HEC coset, set bit 5 in register CVAL (0x0C) to one.

5.2 ATM Cell Receiver

The ATM cell receiver performs cell delineation on incoming data cells by searching for the position of a valid HEC field within the cell. The HEC coset can be either active or inactive; this is determined in bit 5 in the CVAL (0x0C) register.

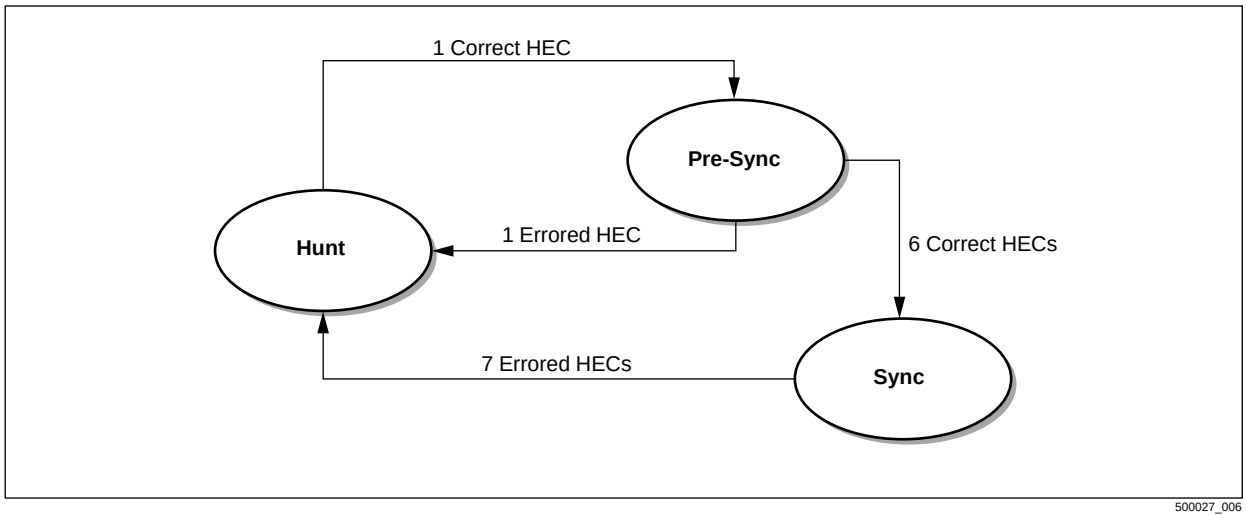
Figure 5-1. Details of the TC Block (Bits 7 and 6 in ATMINTFC, address 0x202)



5.2.1 Cell Delineation

The ATM block receives octets from the framers and recovers ATM cells by means of cell delineation. Cell delineation is achieved by aligning ATM cell boundaries using the HEC algorithm. Four consecutive bytes are chosen and the HEC value is calculated. The result is compared with the value of the following byte. This “hunt” is continued by shifting this four-byte window, one byte at a time, until the calculated HEC value equals the received HEC value. When this occurs, a pre-sync state is declared and the next 48 bytes are assumed to be payload. The ATM block calculates HEC on the four bytes following this payload, assuming that a new cell has begun. If seven consecutive header blocks are found, synchronization is declared. If any HEC calculation fails in the pre-sync state, the process begins again (see Figure 5-2). Synchronization will be held until seven consecutive incorrect HECs are received. At this time, the “hunt” state is reinitiated.

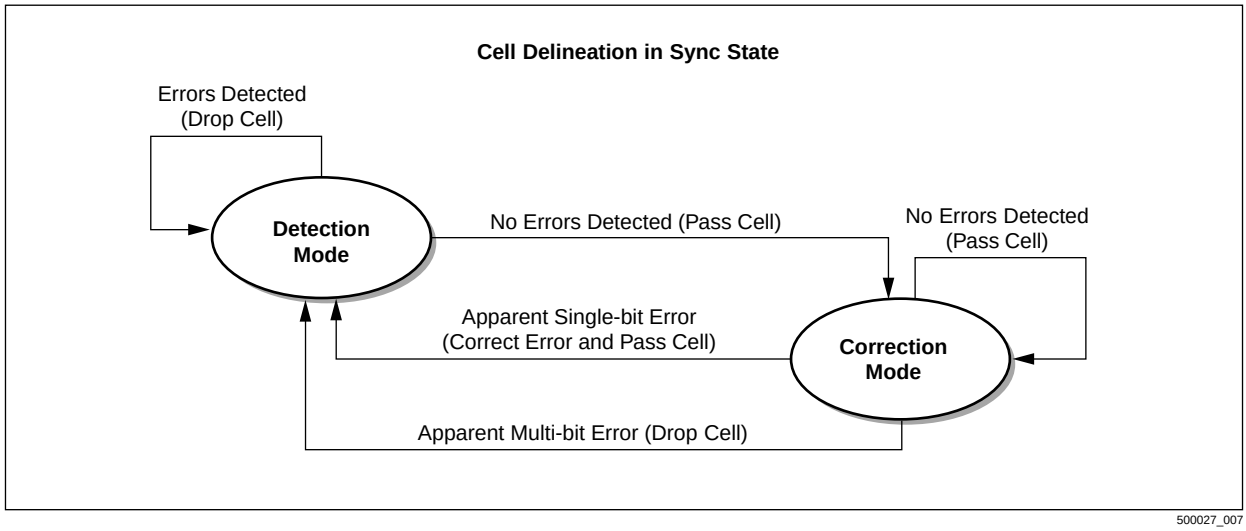
Figure 5-2. Cell Delineation Process



During the sync state of cell delineation, cells are passed to the UTOPIA interface if the HEC is valid. If a single-bit error in the header is detected, the error is corrected (optionally), and the cell is passed to the UTOPIA interface. If HEC checking is enabled and HEC correcting is disabled (bit 3 in the CVAL register [0x0C]), cells with single-bit HEC errors are discarded. If a multi-bit error is detected, the cell is dropped. Once either type of error is noted, all subsequent errored cells are dropped until a valid cell is received. This rule applies even for single-bit errors that could be corrected. Once a valid cell is detected, the process begins again. (See Figure 5-3.)

When loss-of-cell delineation (LOCD) occurs, an interrupt is generated and the CX2822x automatically enters the “hunt” mode. However, the cell is still being scrambled by the far-end transmitter, leaving only the headers (or just the HEC byte in Distributed Sample Scrambler [DSS]) unscrambled. This means that the only repetitive byte patterns in the data stream that meet the cell delineation criteria are valid headers (or just the HEC bytes in DSS).

Figure 5-3. Header Error Check Process



When the CX2822x is in general purpose mode, a synchronization pulse from the framer interface is not always available. In this mode, the CX2822x performs a bit serial search to find byte and cell alignment. The CX2822x selects a starting window of 32 sequential bits and calculates the HEC over this window. This HEC is then compared to the next eight incoming bits. If they do not match, the CX2822x shifts the 32-bit window by 1 bit and recalculates the HEC until a valid HEC position is found. Once byte-alignment is achieved, cell delineation is performed.

5.2.2 Processing Non-Standard Traffic Using the CX28229

The CX28229 contains two independent "HEC Check" state machines. The Cell Delineator (CD) State Machine is used to find Cell Delineation and, conversely, to declare loss of cell delineation (LOCD). The other is the Cell Valid (CV) State Machine, which is used to validate the cells to pass to the UTOPIA FIFOs.

These state machines are controlled by two register bits, (CVAL register, 0x0C), that allow the CX28229 to be programmed for special applications. Table 5-1 shows the control bits function.

Table 5-1. Control Bit Functions

DisLOCD	DisHECChk	Description
0	0	Normal operation; used for standard ATM traffic. Cells are output to the UTOPIA FIFO only after cell delineation is found. Only cells with valid HECs are passed (this includes cells with single bit errors that have been corrected).
0	1	Ignore HEC Errors Mode; used for IMA applications. The Cell Delineator state machine is active and looking for valid ATM cells. It will follow the ATM Forum's Cell Delineation process. However, since the Cell Valid State machine is turned off, the CX28229 will pass all cells, including those with HEC errors, to the UTOPIA FIFOs. The CX28229 will not transfer cells during LOCD.
1	0	The cell delineation function is disabled and every 53 bytes of incoming data is treated as a 'cell'. However, since the CV machine is still active, only cells with valid HECs will be output. As a result, almost all data will be dropped. Occasionally, random data will have what appears to be a valid HEC and will be output. Mindspeed is not aware of any use for this mode.
1	1	Raw Data mode; allows the CX28229 to be used as a generic 'serial to parallel' convertor. All data received will be passed across the UTOPIA bus in blocks of 53 bytes. No attempt is made to find ATM cells.

GENERAL NOTE:

1. The HEC Error Correction circuit is independent of the DisHECChk control bit. The CX28229 will correct single bit errors even when the DisHECChk is enabled (assuming that the EnHECCor bit is set to 1).

5.2.3 Cell Screening

The CX2822x provides two optional types of cell screening. The first type, idle cell rejection, prevents idle cells from being passed on. The second type, user traffic screening, compares incoming bits to the values in the receive cell header registers. Cells are rejected or accepted based on the bit patterns of their headers.

Idle cell rejection is enabled in bit 6 of the CVAL register (0x0C). If this bit is set to 1, all incoming cells that match the contents of the Receive Idle Cell Header Control Registers, RXIDL1–4 (0x20–23), are rejected. Individual bits in the Receive Idle Cell Mask Control Registers, IDLMSK1–4 (0x24–27), can be set to 1 or Don't Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their value. If idle cell rejection is disabled, cells pass directly to user traffic screening.

User traffic cell screening is similar to idle cell screening in that the incoming cells are compared to the Receive Cell Header Control Registers, RXHDR1–4 (0x18–1B). Individual bits in the Receive Cell Mask Control Registers, RXMSK1–4 (0x1C–1F), can be set to 1 or Don't Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their values. The RejHdr bit (bit 7) in the CVAL register (0x0C) determines whether matching cells are rejected or accepted. If it is set to 0, matching cells are accepted. If it is set to 1, matching cells are rejected. See Table 5-2 and Table 5-3.

Table 5-2. Cell Screening—Matching

Receive Cell Mask Bit	Receive Cell Header Bit	Incoming Bit	Result
0	0	0	Match
0	0	1	Fail
0	1	0	Fail
0	1	1	Match
1	x	x	Match

Table 5-3. Cell Screening—Accept/Reject Cell

Cell	Reject Header	Result
Match	0	Accept Cell
Match	1	Reject Cell
Fail	0	Reject Cell
Fail	1	Accept Cell

5.2.4 Cell Scrambler

The ATM standard requires cell scrambling to ensure that only valid headers are found in the cell delineation process. Scrambling randomizes any repeated patterns or other data strings that could be mistaken for valid headers. The CX2822x supports two types of scrambling as defined by ITU-T I.432:

1. Self Synchronizing Scrambler (SSS)
2. Distributed Sample Scrambler (DSS). Typically, SSS is used and is, therefore, the CX2822x's default method. However, xDSL in asynchronous format generally use DSS.

NOTE: If both SSS and DSS are enabled, SSS overrides DSS.

5.2.4.1 SSS Scrambling

SSS scrambling uses the polynomial $\times^{43} + 1$ to scramble the payload, leaving the five header bytes untouched. It can be enabled in EnTxCellScr, bit 5, of the CGEN register (0x08).

Descrambling uses the same polynomial to recover the 48-byte cell payload. It can be enabled in EnRxCellScr, bit 4, of the CVAL register (0x0C). SSS scrambling runs at up to 45 Mbps.

5.2.4.2 DSS Scrambling

DSS scrambling uses the $\times^{31} + \times^{28} + 1$ polynomial to scramble the entire cell, except the HEC byte. HEC is calculated after the first four bytes of the header have been scrambled. DSS scrambling is enabled in EnTxDSSScr, bit 1, of the CGEN register (0x08).

Descrambling uses the first six bits of the HEC for alignment. Once alignment is found, all eight bits of the HEC are sampled. Descrambling uses the same polynomial to recover the 48-byte cell payload. It is enabled in EnRxDSSScr, bit 0, of the CGEN register (0x08). If DSS descrambling fails, the CX2822x defaults to unscrambled mode.

5.2.5 Framing Modes (UTOPIA-to-Serial Configuration)

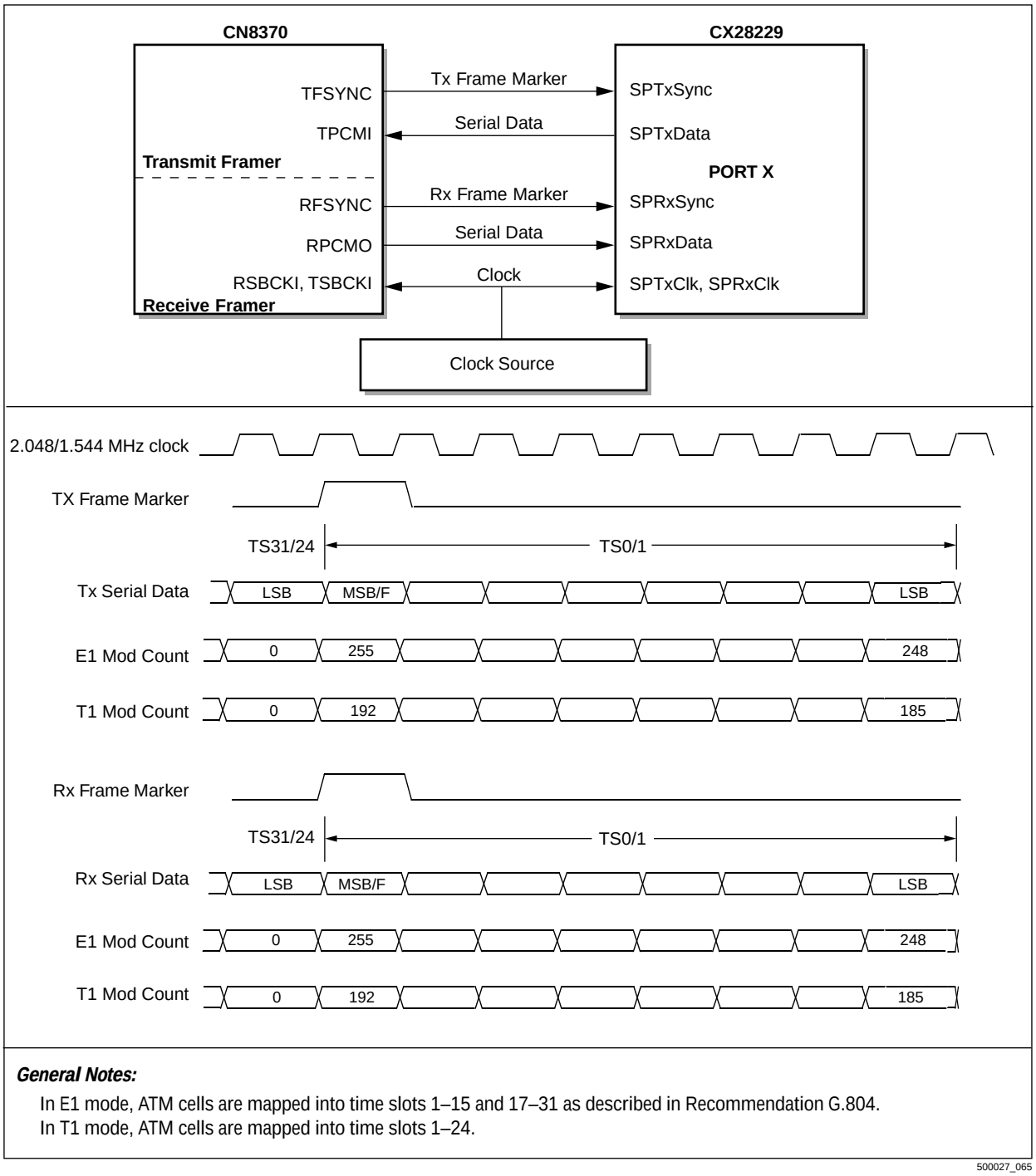
The CX2822x's eight serial ports can be individually configured for the major framing modes to a maximum of 10 Mbps: T1/E1 and DSL. A general purpose framing mode provides an interface to customized framers at a maximum of 10 Mbps. Each of the eight ports can be configured for a different mode.

5.2.5.1 T1/E1 Interface

This describes the timing requirements of the CX28229 when operating in T1 or E1 mode. Connection to a CN8370 T1/E1 framer is used as an example, as illustrated in Figure 5-4. The CX28229 receives a T1/E1 data stream from the external framer, ignores the T1/E1 overhead, extracts the ATM cells, and passes the ATM cells to the ATM layer device. In the transmit direction, the CX28229 inserts 0's in the overhead bit locations and fills the rest of the frame with ATM cells from the UTOPIA bus.

For the E1 mode, the ATM cells are mapped into time slots 1–15 and 17–31 as described in *Recommendation G.804*. For the T1 mode, the ATM cells are mapped into time slots 1–24.

Figure 5-4. CN8370 Interface Diagram

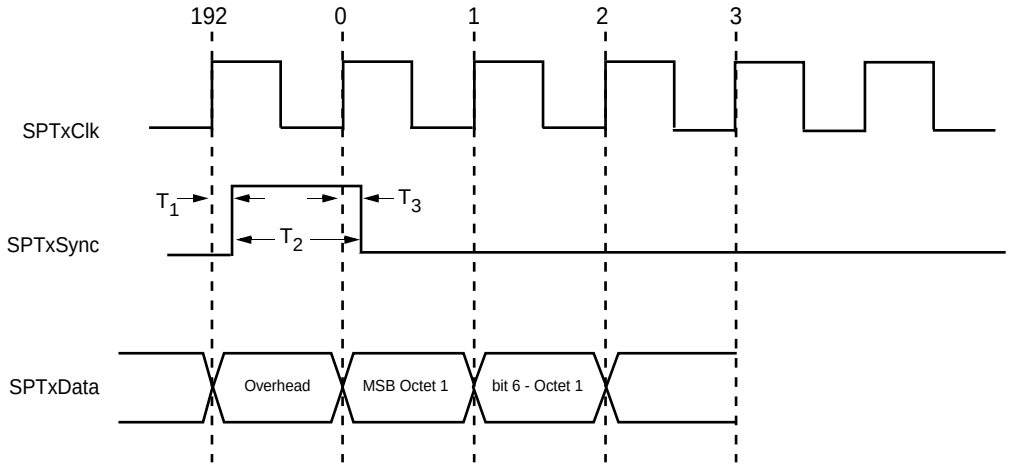


General Notes:

In E1 mode, ATM cells are mapped into time slots 1–15 and 17–31 as described in Recommendation G.804.
In T1 mode, ATM cells are mapped into time slots 1–24.

500027_065

Figure 5-5. Transmit Waveforms



General Notes:

The diagram shows the CX28229 programmed to sample on the rising edge of the clock.

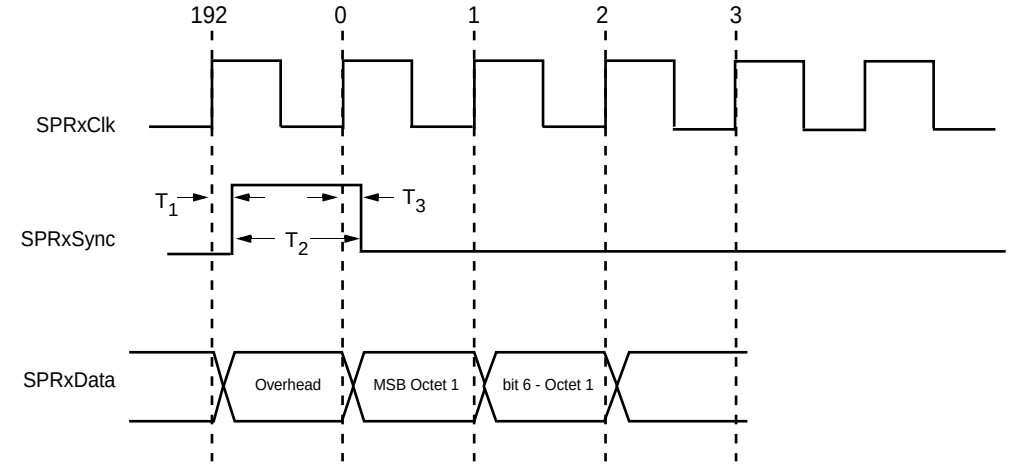
For T_1, SPTxSync must occur at least 10 ns *after* the rising edge of the 193rd clock.

T_2 must have a minimum of 1 clock period.

For T_3, the hold time is 10 ns after the rising edge of the clock.

500027_064

Figure 5-6. Receive Waveforms



General Notes:

The diagram shows the CX28229 programmed to sample on the rising edge of the clock.

The Overhead bit is sampled on the clock edge 0.

For T_1, SPRxSync must occur at least 10 ns *after* the rising edge of the 193rd clock.

T_2 must have a minimum of 1 clock period.

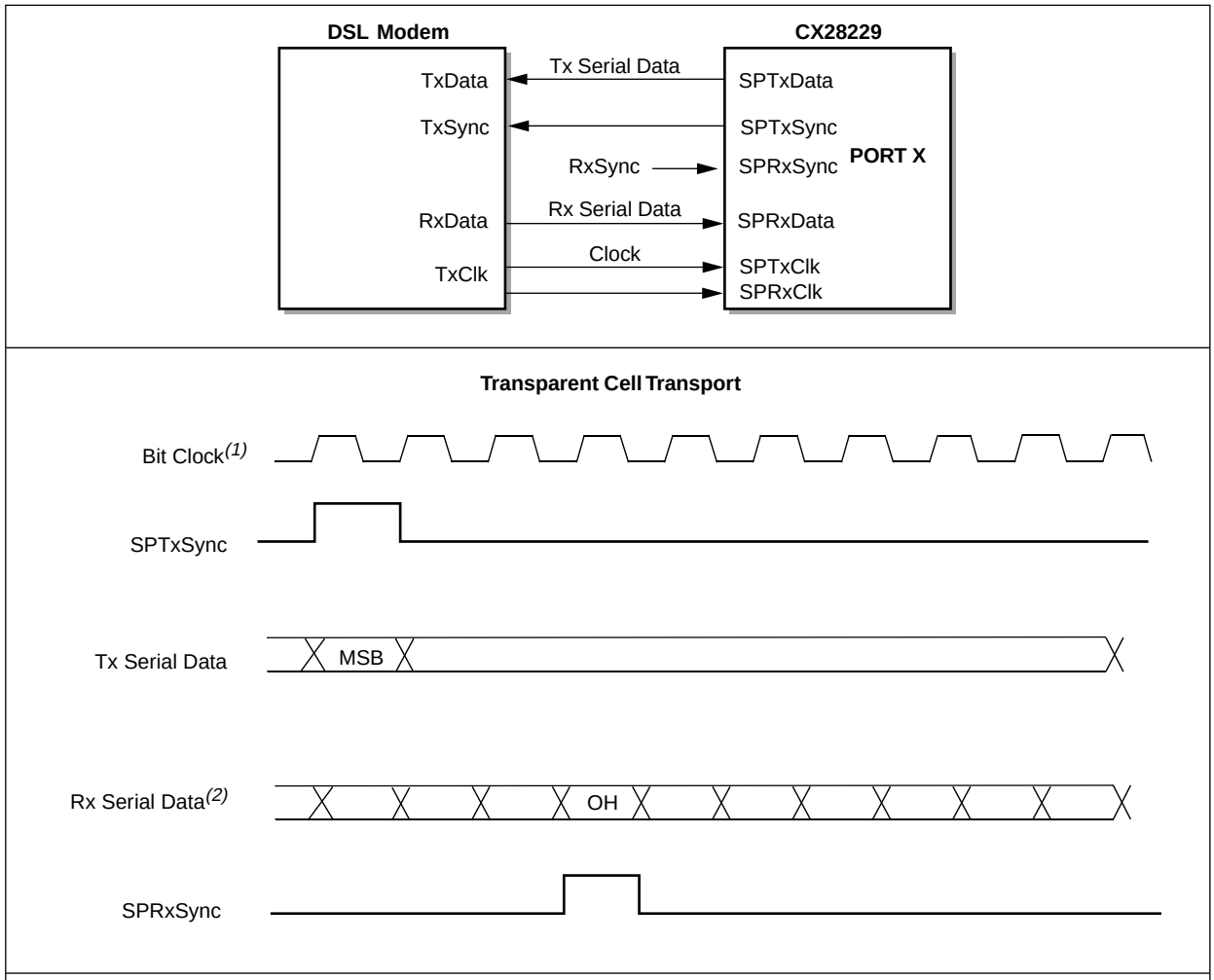
For T_3, the hold time is 10 ns after the rising edge of the clock.

500027_066

5.2.5.2 DSL Mode Interface

The CX2822x has a DSL mode interface as illustrated in Figure 5-7. This mode allows connection with framers that require frame synchronization. The CX2822x receives a data stream from the external framer, performs byte-alignment and cell delineation, and passes the ATM cells to the ATM layer device. The CX2822x performs the inverse process on transmitted data. In this mode, the framer must ensure that only ATM cells are present in the data stream.

Figure 5-7. DSL Mode



General Notes:

(1) The CX28229 operates at data rates up to 10 Mbps.

(2) RxData is ignored when SPRxSync is asserted based on it's programmable active level. This may be used to mask overhead bits in the receive data stream. Polarity is shown as active low in above figure.

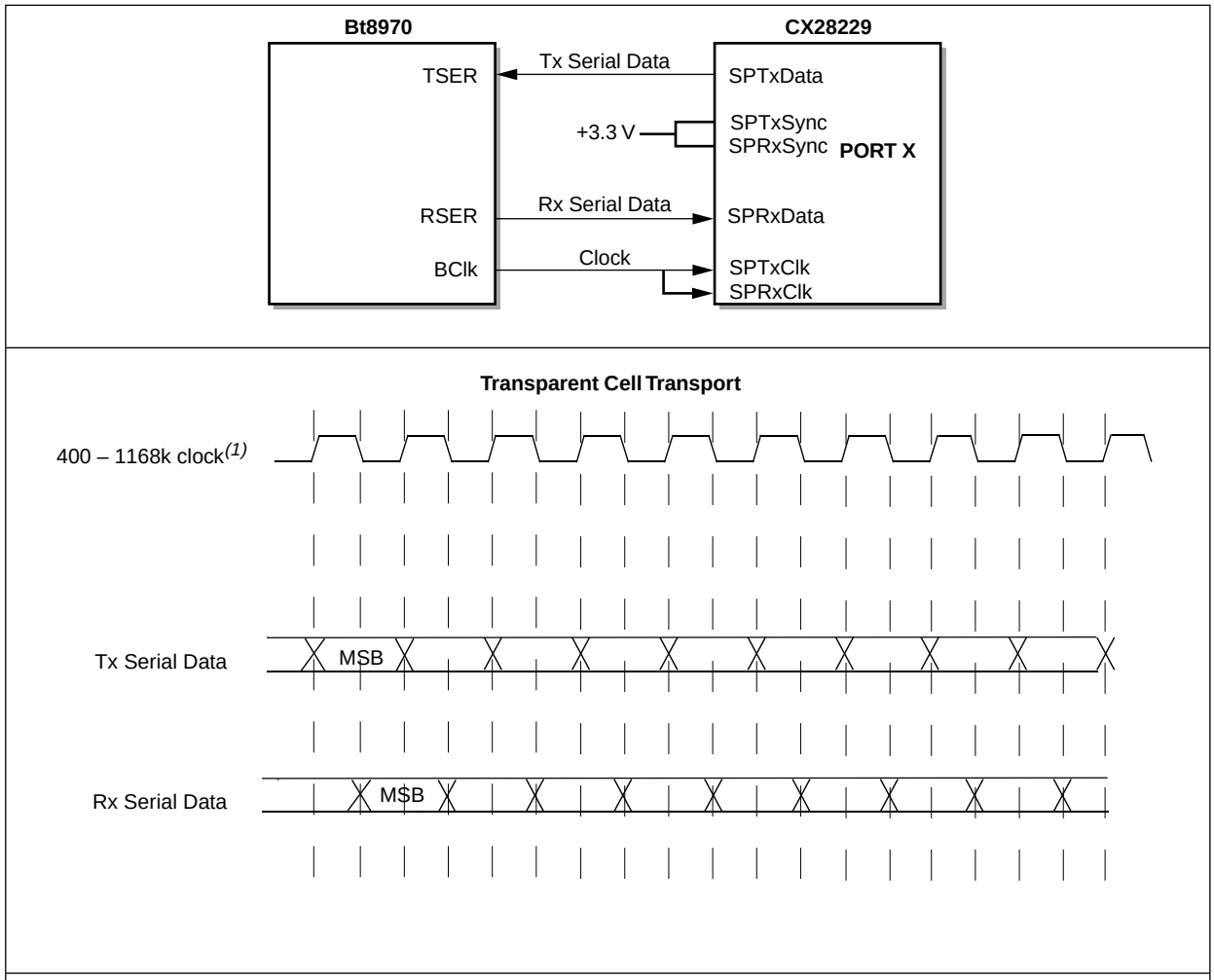
3. TxSync indicates the Start of Cell.
4. Tx and Rx are asynchronous.

500027_014

5.2.5.3 General Purpose Mode Interface

The CX2822x has a general purpose mode interface as illustrated in Figure 5-8. This mode allows connection with framers that do not provide frame synchronization. The CX2822x receives a data stream from the external framer, performs byte-alignment and cell delineation, and passes the ATM cells to the ATM layer device. The CX2822x performs the inverse process on transmitted data. In this mode, the framer must ensure that only ATM cells are present in the data stream.

Figure 5-8. General Purpose Mode



General Notes:

(1) The 1168 kbps limit is imposed by the Bt8970; the CX28229 operates at data rates up to 10 Mbps.

2. In general purpose mode, the SPTxSync and SPRxSync pins are ignored but should be tied high to prevent noise being introduced to the device.
3. Diagram shows default values for TxClkPol and RxClkPol (IOMODE register).

500027_014a

6 General Issues

6.1 Micro Interface

The microprocessor interface transfers control and status information in 8-bit data transfers between the external microprocessor and CX2822x by means of write and/or read access to internal registers. This interface allows the microprocessor to configure the CX2822x by writing various control registers. These control registers can also be read for configuration confirmation. This interface also provides the ability to read the device's current condition via its status registers and counters. Summary status is available for rapid interrupt identification.

The microprocessor interface can operate in either an asynchronous mode or a synchronous mode. The MSyncMode pin (N5) determines which mode is active.

In the synchronous mode, the timing of these signals is synchronized to MicroClk, which is intended to be directly driven by the external microprocessor. This interface is compatible with the RS8236 and CN8237 SAR devices, providing no-wait-state operation.

NOTE: The MicroClk is required for both modes. In asynchronous mode, a MicroClk frequency of up to 50MHz, must be present but can be asynchronous to the other microprocessor signals. In synchronous mode, MicroClk is limited to 25MHz.

6.1.1 Resets

There are four software controlled reset functions, two at the device level and two at the port level. The two levels allow a user to reset either the entire CX2822x with one command or only a port within the device. The two logic resets allow the user to keep the device or port in a reset state while the control registers are being programmed. When the reset bit is deasserted, all changes to the registers take place simultaneously.

At the device level, the software-controlled DevMstRst, bit 7, in the MODE register (0x0200), restarts all device functions and sets the control and status registers, including IMA, to their default values except this bit (DevMstRst). The DevLgcRst, bit 6, in the MODE register (0x0200) restarts all device functions in the TC block but leaves all control registers unaffected.

At the port level, the PrtMstRst, bit 7, in the PMODE register (0x04), restarts all port functions and sets the registers for the associated port to their default values except this bit (PrtMstRst). The PrtLgcRst, bit 6, in the PMODE register (0x04) restarts all functions but leaves the port control registers unaffected.

6.1.2 Counters (TC Block Only)

The CX2822x counters record events within the TC block. Two types of events are recorded: error events, such as Section BIP errors, and transmission events, such as transmitted ATM cells.

Counters comprised of more than one register must be accessed by reading the least significant byte (LSB) first. This guarantees that the value contained in each component register accurately reflects the composite counter value at the time the LSB was read, because the counter may be updated while the component registers are being read.

Each counter is large enough to accommodate the maximum number of events that may occur within a one-second interval. The counters are cleared after being read. Therefore, if the counters are read every second, the application will receive an accurate recording of all events.

6.1.2.1 One-second Latching

The CX2822x's implementation of one-second latching ensures the integrity of the statistics being gathered by the network management software. Internal statistics counters can be latched at one-second intervals, which are synchronized to the OneSecIO pin (pin R5). Therefore, the data read from the statistic counters represents the same one second of real-time data, independent of network management software timing.

The CX2822x implements one-second latching for both status signals and counter values. When the EnStatLat bit (bit 5) in the MODE register (0x0202) is written to a logical 1, a read from any of the status registers returns the state of the device at the time of the previous OneSecIO pin (pin R5) assertion. When the EnCntrLat bit (bit 4) in the MODE register (0x0202) is written to a logical 1, a read from any of the counters returns the state of the device at the time of the previous OneSecIO pin (pin R5) assertion. Every second, the counter is read, moved to the latch, and the counter is cleared. The latch is cleared when read.

Software can configure the OneSecIO pin as an output that equals the input from the 8kHzIn divided by 8000. When configured as an input, status registers and counters may be latched on the rising edge of this input. See Bit 0 of the Mode register (0x200).

NOTE: When latching is disabled and a counter is wider than one byte, the LSB should be read first to retain the values of the other bytes for a subsequent read.

6.1.2.2 Interrupts

The CX2822x's interrupt indications can be classified as either single- or dual-event; a single-event interrupt is triggered by a status assertion; a dual-event interrupt is triggered by either a status assertion or deassertion. Both types of interrupts are further described in the following examples.

Single-event interrupt: When a parity error occurs on the UTOPIA transmit data bus, an interrupt is generated on ParErrInt, bit 7, in the TXCELLINT register (0x2C). This bit is cleared when read.

Dual-event interrupt: When LOCD occurs, bit 7 of the corresponding RXCELLINT register (0x0D) is set to 1. This bit is cleared when the register is read. Once cell delineation is recovered, bit 7 is set to 1 again, generating another interrupt.

All interrupt bits have a corresponding enable bit. This allows software to disable or mask interrupts as required.

NOTE: The IMA block does not generate interrupts.

The CX2822x uses three levels of interrupt indications. The first level consists of receive or transmit interrupt indications, which correspond to specific events on a specific port. The second level summarizes first level interrupts and indicates framer and one-second interrupts for each port. The third level indicates which port generated an interrupt.

The first level interrupt indications are located in registers TXCELLINT and RXCELLINT for each port. Each interrupt bit in these registers can be disabled in the corresponding ENCELLR or ENCELLT register, respectively. The result is then ORed into the appropriate bit in the port's SUMINT register.

The second level consists of summary interrupt indications, located in the SUMINT register. It also includes the OneSecInt and the ExInt indications. Each interrupt bit in these registers can be disabled in the corresponding ENSUMINT register. The result is then ORed into the appropriate bit in the SUMPORT register.

The third level contains the overall interrupt indications for each port in the SUMPORT register. These bits can be disabled in the ENSUMPORT register. The result is ORed to the MicroInt* pin. The MicroInt* pin can be enabled or disabled by setting the EnIntPin (bit 3) in the MODE register (0x202).

Figure 6-1 illustrates the flow chart of the interrupt generation process and Figure 6-2 illustrates the registers involved in the interrupt generation process.

Figure 6-1. Interrupt Indication Flow Chart

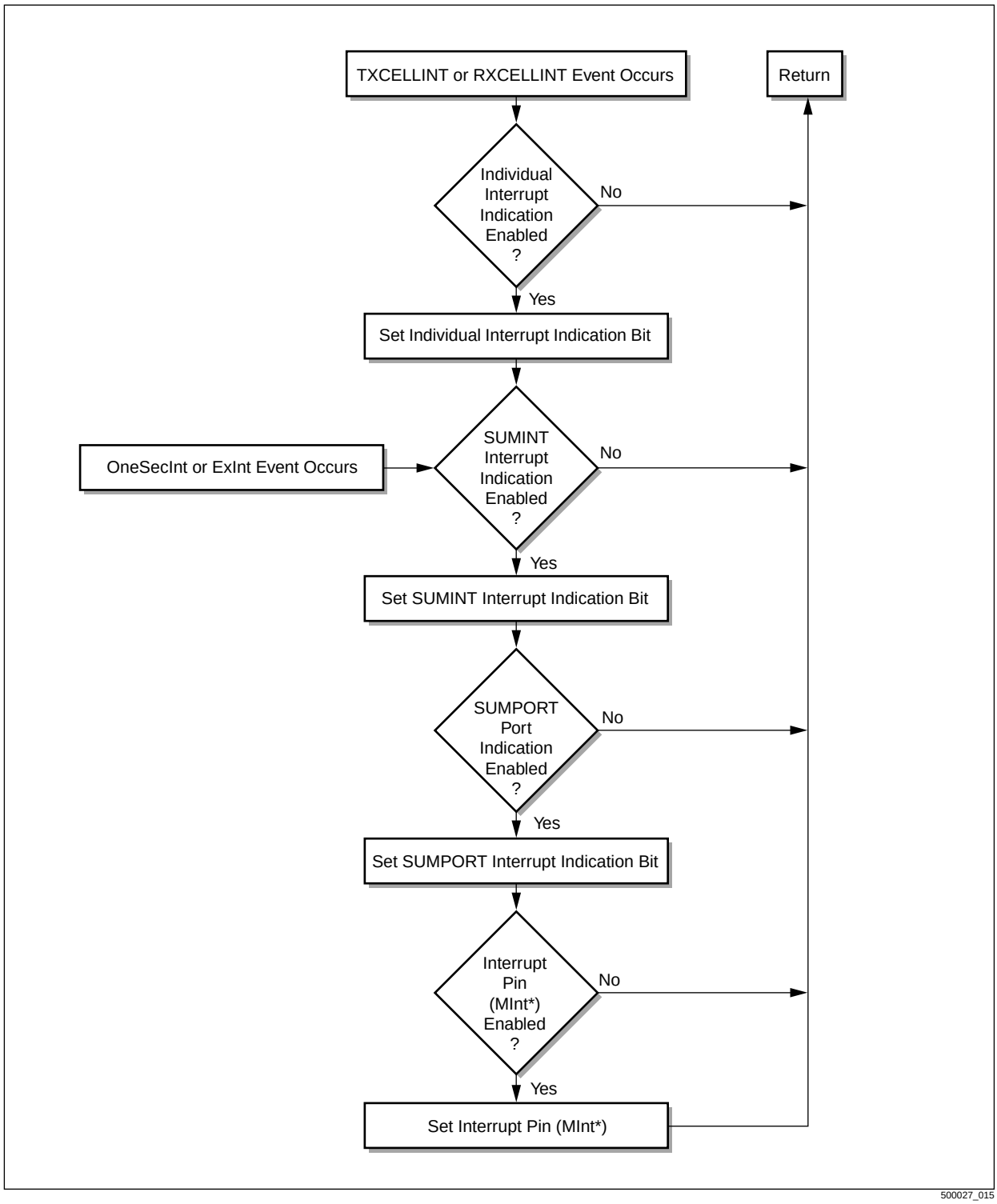
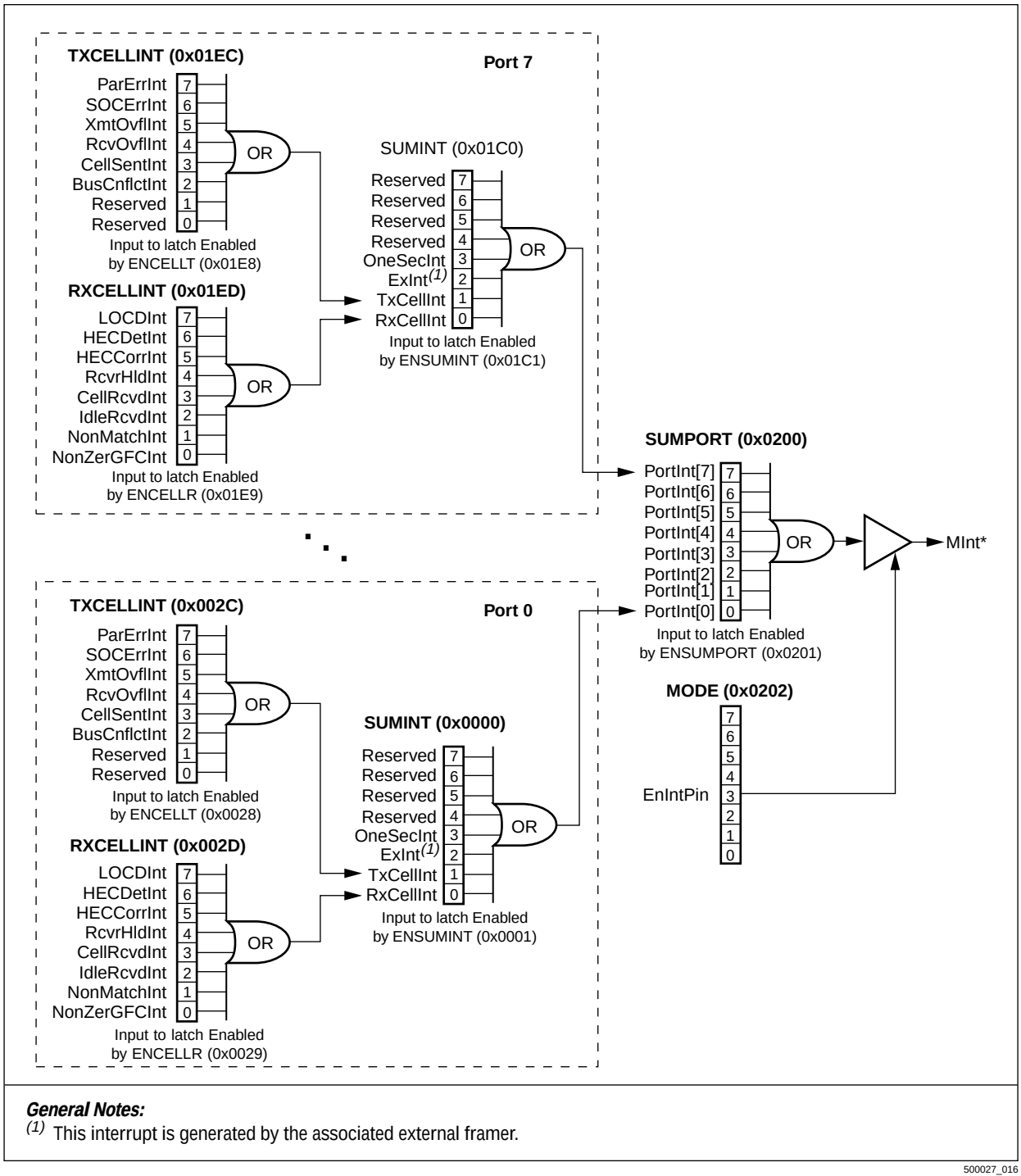


Figure 6-2. Interrupt Indication Diagram (TC Block)



General Notes:

(1) This interrupt is generated by the associated external framer.

500027_016

6.1.2.3 Interrupt Servicing

When an interrupt occurs on the MicroInt* pin (pin B19), it could have been generated by any of 128 events. The CX2822x's interrupt indication structure ensures that no more than a maximum of three register reads are needed to determine the source of an interrupt. The interrupt is traced back to its source using the following steps:

1. Read the SUMPORT register to see which port(s) shows an interrupt.
2. Read the appropriate SUMINT register to see which bit(s) shows an interrupt.
   - Bit 0, RxCellInt, reflects activity in the RXCELLINT register.
   - Bit 1, TxCellInt, reflects activity in the TXCELLINT register.
   - Bit 2, ExInt, indicates an interrupt from an external framer.
   - Bit 3, OneSecInt, indicates a one-second interrupt.
   - Bits 4–7 are reserved.
3. If necessary, read the appropriate TXCELLINT or RXCELLINT register.

All Level 1 bits are cleared when the register is read. Once the register is read, ALL bits in that register are reset to their default values. Therefore, interrupt service routines must be designed to handle multiple interrupts in the same registers. In Level 2, OneSecInt and ExInt are cleared when the register is read. However, the TxCellInt and RxCellInt bits are cleared only when the corresponding Level 1 register is read and cleared. Level 3 bits are cleared when the entire corresponding Level 2 register has been read and cleared.

7 Registers

The CX2822x registers control and observe the device's operations. Table 7-1 lists the address ranges that represent a device control and status range. The registers in each port range are replicated for the other ports. Table 7-2 lists the device-level control and status registers. Table 7-3 lists the port-level control and status registers. All registers are 8 bits wide. All control registers can be read to verify contents.

NOTE: Control bits that do not have a documented function are reserved and must be written to a logical 0.

Table 7-1. Address Ranges

Port Offset Address Range (Hex)	Description	Port Base Address (Hex)
0000–003F	Port 0 Control and Status Registers	0000
0040–007F	Port 1 Control and Status Registers	0040
0080–00BF	Port 2 Control and Status Registers	0080
00C0–00FF	Port 3 Control and Status Registers	00C0
0100–013F	Port 4 Control and Status Registers	0100
0140–017F	Port 5 Control and Status Registers	0140
0180–01BF	Port 6 Control and Status Registers	0180
01C0–01FF	Port 7 Control and Status Registers	01C0
0200–0208	Device Control and Status Registers	—
0209–300	Reserved, set to a logical 0.	—
300–30D	Reserved, set to a logical 0.	—
320–32D	Reserved, set to a logical 0.	—
340–34D	Reserved, set to a logical 0.	—
360–36D	Reserved, set to a logical 0.	—
380–38D	Reserved, set to a logical 0.	—
3A0–3AD	Reserved, set to a logical 0.	—
3C0–3CD	Reserved, set to a logical 0.	—
3E0–3ED	Reserved, set to a logical 0.	—
0400–07FF	IMA Control and Status Registers	—

The device level registers in Table 7-2 provide control for the device's major operating modes, as well as status and control for summary interrupts.

Table 7-2. Device Control and Status Registers

Address	Name	Type	OneSec Latching	Description	Page Number
0x0200	MODE	R/W	—	Device Mode Control Register	page 7-64
0x0201	PHYINTFC	R/W	—	PHY-side Interface Control Register	page 7-65
0x0202	ATMINTFC	R/W	—	ATM-side Interface Control Register	page 7-65
0x0203	OUTSTAT	R/W	—	Output Status Control Register	page 7-65
0x0204	SUMPORT	R	—	Summary Port Interrupt Status Register	page 7-66
0x0205	ENSUMPORT	R/W	—	Summary Port Interrupt Control Register	page 7-66
0x0208	PART/VER	R	—	Part Number/Version Register	page 7-67

The registers listed in Table 7-3 are replicated for each port. Two methods can be used to determine the exact address of a specific register in a specific port. All numbers are in hexadecimal.

1. Add the port offset address to the port base address as shown in Table 7-1. For example:
   For Port 3, IOMODE register
   00C0 (Port 3 base address) + 0x05 (port offset address) = 00C5
2. Use the following formula:
   0x40 (port register map size) × *n* (port number) + port offset address = exact register address

Table 7-3. Port Control and Status Registers *(1 of 3)*

Port Offset Address	Name	Type	One-second Latching	Description	Page Number
0x00	SUMINT	R	—	Summary Interrupt Status Register	page 7-33
0x01	ENSUMINT	R/W	—	Summary Interrupt Control Register	page 7-34
0x02	—	—	—	Reserved, set to a logical 0	—
0x03	—	—	—	Reserved, set to a logical 0	—
0x04	PMODE	R/W	—	Port Mode Control Register	page 7-35
0x05	IOMODE	R/W	—	Input/Output Mode Control Register	page 7-36
0x08	CGEN	R/W	—	Cell Generation Control Register	page 7-37
0x09	HDRFIELD	R/W	—	Header Field Control Register	page 7-38
0x0A	IDLPAY	R/W	—	Transmit Idle Cell Payload Control Register	page 7-38
0x0B	ERRPAT	R/W	—	Error Pattern Control Register	page 7-39
0x0C	CVAL	R/W	—	Cell Validation Control Register	page 7-39
0x0D	UTOP1	R/W	—	UTOPIA Control Register 1	page 7-40
0x0E	UTOP2	R/W	—	UTOPIA Control Register 2	page 7-40

Table 7-3. Port Control and Status Registers *(2 of 3)*

Port Offset Address	Name	Type	One-second Latching	Description (Continued)	Page Number
0x0F	UDF2	R/W	—	UDF2 Control Register	page 7-41
0x10	TXHDR1	R/W	—	Transmit Cell Header Control Register 1	page 7-41
0x11	TXHDR2	R/W	—	Transmit Cell Header Control Register 2	page 7-42
0x12	TXHDR3	R/W	—	Transmit Cell Header Control Register 3	page 7-42
0x13	TXHDR4	R/W	—	Transmit Cell Header Control Register 4	page 7-43
0x14	TXIDL1	R/W	—	Transmit Idle Cell Header Control Register 1	page 7-43
0x15	TXIDL2	R/W	—	Transmit Idle Cell Header Control Register 2	page 7-44
0x16	TXIDL3	R/W	—	Transmit Idle Cell Header Control Register 3	page 7-44
0x17	TXIDL4	R/W	—	Transmit Idle Cell Header Control Register 4	page 7-45
0x18	RXHDR1	R/W	—	Receive Cell Header Control Register 1	page 7-45
0x19	RXHDR2	R/W	—	Receive Cell Header Control Register 2	page 7-46
0x1A	RXHDR3	R/W	—	Receive Cell Header Control Register 3	page 7-46
0x1B	RXHDR4	R/W	—	Receive Cell Header Control Register 4	page 7-47
0x1C	RXMSK1	R/W	—	Receive Cell Mask Control Register 1	page 7-47
0x1D	RXMSK2	R/W	—	Receive Cell Mask Control Register 2	page 7-48
0x1E	RXMSK3	R/W	—	Receive Cell Mask Control Register 3	page 7-48
0x1F	RXMSK4	R/W	—	Receive Cell Mask Control Register 4	page 7-49
0x20	RXIDL1	R/W	—	Receive Idle Cell Header Control Register 1	page 7-49
0x21	RXIDL2	R/W	—	Receive Idle Cell Header Control Register 2	page 7-50
0x22	RXIDL3	R/W	—	Receive Idle Cell Header Control Register 3	page 7-50
0x23	RXIDL4	R/W	—	Receive Idle Cell Header Control Register 4	page 7-51
0x24	IDLMSK1	R/W	—	Receive Idle Cell Mask Control Register 1	page 7-51
0x25	IDLMSK2	R/W	—	Receive Idle Cell Mask Control Register 2	page 7-52
0x26	IDLMSK3	R/W	—	Receive Idle Cell Mask Control Register 3	page 7-52
0x27	IDLMSK4	R/W	—	Receive Idle Cell Mask Control Register 4	page 7-53
0x28	ENCELLT	R/W	—	Transmit Cell Interrupt Control Register	page 7-53
0x29	ENCELLR	R/W	—	Receive Cell Interrupt Control Register	page 7-54
0x2A	—	—	—	Reserved, set to a logical 0	—
0x2B	—	—	—	Reserved, set to a logical 0	—
0x2C	TXCELLINT	R	—	Transmit Cell Interrupt Indication Control Register	page 7-54
0x2D	RXCELLINT	R	—	Receive Cell Interrupt Indication Control Register	page 7-55
0x2E	TXCELL	R	(1)	Transmit Cell Status Control Register	page 7-56
0x2F	RXCELL	R	(1)	Receive Cell Status Control Register	page 7-56
0x30	IDLCNTL	R	(2)	Idle Cell Receive Counter (low byte)	page 7-57

Table 7-3. Port Control and Status Registers *(3 of 3)*

Port Offset Address	Name	Type	One-second Latching	Description (Continued)	Page Number
0x31	IDLCNTM	R	(2)	Idle Cell Receive Counter (middle byte)	page 7-57
0x32	IDLCNTH	R	(2)	Idle Cell Receive Counter (high byte)	page 7-58
0x33	LOCDCNT	R	(2)	LOCD Event Counter	page 7-58
0x34	TXCNTL	R	(2)	Transmitted Cell Counter (low byte)	page 7-59
0x35	TXCNTM	R	(2)	Transmitted Cell Counter (mid byte)	page 7-59
0x36	TXCNTH	R	(2)	Transmitted Cell Counter (high byte)	page 7-60
0x37	CORRCNT	R	(2)	Corrected HEC Error Counter	page 7-60
0x38	RXCNTL	R	(2)	Received Cell Counter (low byte)	page 7-61
0x39	RXCNTM	R	(2)	Received Cell Counter (mid byte)	page 7-61
0x3A	RXCNTH	R	(2)	Received Cell Counter (high byte)	page 7-62
0x3B	UNCCNT	R	(2)	Uncorrected HEC Error Counter	page 7-62
0x3C	NONCNTL	R	(2)	Non-Matching Cell Counter (low byte)	page 7-63
0x3D	NONCNTH	R	(2)	Non-Matching Cell Counter (high byte)	page 7-63
0x3E	—	—	—	Reserved, set to a logical 0	—
0x3F	—	—	—	Reserved, set to a logical 0	—

FOOTNOTE:
(1) One-second latching is enabled by setting EnStatLat (bit 5) in the MODE register (0x0202) to a logical 1.
(2) One-second latching is enabled by setting EnCntrLat (bit 4) in the MODE register (0x0202) to a logical 1.

Table 7-4 lists several registers used for CX2822x's basic functions, including device- and port-level operating modes.

Table 7-4. General Use Registers

Port Offset Address	Name	Description	Page Number
0x200	MODE	Device Mode Control Register	page 7-64
0x04	PMODE	Port Mode Control Register	page 7-35
0x05	IOMODE	Input/Output Mode Control Register	page 7-36
0x203	OUTSTAT	Output Pin Control Register	page 7-65

Table 7-5 lists the control registers used for transmission of traffic.

Table 7-5. Cell Transmit Registers

Port Offset Address	Name	Description	Page Number
0x08	CGEN	Cell Generation Control Register	page 7-37
0x09	HDRFIELD	Header Field Control Register	page 7-38
0x0A	IDLPAY	Transmit Idle Cell Payload Control Register	page 7-38
0x0B	ERRPAT	Error Pattern Control Register	page 7-39
0x10	TXHDR1	Transmit Cell Header Control Register 1	page 7-41
0x11	TXHDR2	Transmit Cell Header Control Register 2	page 7-42
0x12	TXHDR3	Transmit Cell Header Control Register 3	page 7-42
0x13	TXHDR4	Transmit Cell Header Control Register 4	page 7-43
0x14	TXIDL1	Transmit Idle Cell Header Control Register 1	page 7-43
0x15	TXIDL2	Transmit Idle Cell Header Control Register 2	page 7-44
0x16	TXIDL3	Transmit Idle Cell Header Control Register 3	page 7-44
0x17	TXIDL4	Transmit Idle Cell Header Control Register 4	page 7-45

Table 7-6 lists the control registers used for reception of traffic.

Table 7-6. Cell Receive Registers

Port Offset Address	Name	Description	Page Number
0x0C	CVAL	Cell Validation Control Register	page 7-39
0x18	RXHDR1	Receive Cell Header Control Register 1	page 7-45
0x19	RXHDR2	Receive Cell Header Control Register 2	page 7-46
0x1A	RXHDR3	Receive Cell Header Control Register 3	page 7-46
0x1B	RXHDR4	Receive Cell Header Control Register 4	page 7-47
0x1C	RXMSK1	Receive Cell Mask Control Register 1	page 7-47
0x1D	RXMSK2	Receive Cell Mask Control Register 2	page 7-48
0x1E	RXMSK3	Receive Cell Mask Control Register 3	page 7-48
0x1F	RXMSK4	Receive Cell Mask Control Register 4	page 7-49
0x20	RXIDL1	Receive Idle Cell Header Control Register 1	page 7-49
0x21	RXIDL2	Receive Idle Cell Header Control Register 2	page 7-50
0x22	RXIDL3	Receive Idle Cell Header Control Register 3	page 7-50
0x23	RXIDL4	Receive Idle Cell Header Control Register 4	page 7-51
0x24	IDLMSK1	Receive Idle Cell Mask Control Register 1	page 7-51
0x25	IDLMSK2	Receive Idle Cell Mask Control Register 2	page 7-52
0x26	IDLMSK3	Receive Idle Cell Mask Control Register 3	page 7-52
0x27	IDLMSK4	Receive Idle Cell Mask Control Register 4	page 7-53

Table 7-7 lists the control registers for the UTOPIA operations.

Table 7-7. UTOPIA Registers

Port Offset Address	Name	Description	Page Number
0x0D	UTOP1	UTOPIA Control Register 1	page 7-40
0x0E	UTOP2	UTOPIA Control Register 2	page 7-40

Table 7-8 lists interrupt enables, interrupt indications, and status information.

Table 7-8. Status and Interrupt Registers

Port Offset Address	Name	Description	Page Number
0x204	SUMPORT	Summary Port Interrupt Status Register	page 7-66
0x205	ENSUMPORT	Summary Port Interrupt Control Register	page 7-66
0x00	SUMINT	Summary Interrupt Indication Status Register	page 7-33
0x01	ENSUMINT	Summary Interrupt Control Register	page 7-34
0x28	ENCELLT	Transmit Cell Interrupt Control Register	page 7-53
0x29	ENCELLR	Receive Cell Interrupt Control Register)	page 7-54
0x2C	TXCELLINT	Transmit Cell Interrupt Indication Status Register	page 7-54
0x2D	RXCELLINT	Receive Cell Interrupt Indication Status Register	page 7-55
0x2E	TXCELL	Transmit Cell Status Register	page 7-56
0x2F	RXCELL	Receive Cell Status Register	page 7-56

Table 7-9 lists the CX2822x's counters. When the counters fill, they saturate and do not roll over. The counts have been sized to ensure against saturation within a one-second interval. Therefore, when one-second latching is enabled, the counters are read and cleared before they can saturate. All counters are cleared when read.

Table 7-9. Counters *(1 of 2)*

Port Offset Address	Name	Description	Page Number
0x30	LOCDCNT	LOCD Event Counter	page 7-58
0x31	CORRCNT	Corrected HEC Error Counter	page 7-60
0x32	UNCCNT	Uncorrected HEC Error Counter	page 7-62
0x34	TXCNTL	Transmitted Cell Counter [Low Byte])	page 7-59
0x35	TXCNTM	Transmitted Cell Counter [Mid Byte]	page 7-59
0x36	TXCNTH	Transmitted Cell Counter [High Byte]	page 7-60
0x38	RXCNTL	Received Cell Counter [Low Byte]	page 7-61

***Table 7-9. Counters** (2 of 2)*

Port Offset Address	Name	Description (Continued)	Page Number
0x39	RXCNTM	Received Cell Counter [Mid Byte]	page 7-61
0x3A	RXCNTH	Received Cell Counter [High Byte]	page 7-62
0x3C	NONCNTL	Non-matching Cell Counter [Low Byte]	page 7-63
0x3D	NONCNTH	Non-matching Cell Counter [High Byte]	page 7-63

Table 7-10 lists IMA control and status information.

***Table 7-10. IMA Control and Status Registers** (1 of 26)*

Address	Name	Description	Page Number
0x400	IMA_VER_1_CONFIG	Device Version I	page 7-68
0x401	IMA_VER_2_CONFIG	Device Version II	page 7-68
0x402	IMA_SUBSYS_CONFIG	Configuration Control	page 7-69
0x403	IMA_MISC_STATUS	Miscellaneous Status	page 7-69
0x404	IMA_MISC_CONFIG	Miscellaneous Control	page 7-70
0x405	IMA_MEM_LOW_TEST	Memory Test Address	page 7-70
0x406	IMA_MEM_HI_TEST	Memory Test Address	page 7-70
0x407	IMA_MEM_TEST_CTL	Memory Test Control	page 7-71
0x408	IMA_MEM_TEST_DATA	Memory Test Data	page 7-71
0x409	IMA_LNK_DIAG_CTL	Link Diagnostic Control	page 7-71
0x40a	IMA_LNK_DIFF_DEL	Link Differential Delay	page 7-72
0x40b	IMA_RCV_LNK_ANOMALIES	Receive Link Anomalies	page 7-73
0x40e	IMA_DIAG_XOR_BIT	Address Diagnostic	page 7-74
0x40f	IMA_DIAG	Diagnostic Register	page 7-74
0x410	IMA_TIM_REF_MUX_CTL_ADDR	TRL Control Address	page 7-75
0x411	IMA_TIM_REF_MUX_CTL_DATA	TRL Control Data	page 7-76
0x412	IMA_RX_PERSIST_CONFIG	Receive Persistence	page 7-77
0x413	IMA_ATM_UTOPIA_BUS_CTL	ATM Utopia Control	page 7-78
0x414	IMA_DIFF_DELAY_ADDR	Diff. Delay Control Address	page 7-78
0x415	IMA_DIFF_DELAY_DATA	Diff. Delay Control Data	page 7-79
0x416	IMA_DSL_CLOCK_GEN_ADDR	DSL Clock Generator Control Address	page 7-80
0x417	IMA_DSL_CLOCK_GEN_DATA	DSL Clock Generator Control Data	page 7-81
0x418	IMA_RX_TRANS_TABLE	Receive Translation Table Address	page 7-83
0x419	IMA_RX_ATM_TRANS_TABLE	Receive Translation Table Internal Channel	page 7-84
0x41b	IMA_TX_TRANS_TABLE	Transmit Translation Table Address	page 7-85

Table 7-10. IMA Control and Status Registers *(2 of 26)*

Address	Name	Description (Continued)	Page Number
0x41c	IMA_TX_ATM_TRANS_TABLE	Transmit Translation Table Internal Channel	page 7-86
0x41e	IMA_LNK_SEM	Link Table Control	page 7-108
0x41f	IMA_GRP_1TO4_SEM	Groups 1–4 Table Control	page 7-88
0x51f	IMA_GRP_5TO8_SEM	Groups 5–8 Table Control	page 7-89
0x61f	IMA_GRP_9TO12_SEM	Groups 9–12 Table Control	page 7-90
0x71f	IMA_GRP_13TO16_SEM	Groups 13–16 Table Control	page 7-91

Table 7-10. IMA Control and Status Registers *(3 of 26)*

Address	Name	Description (Continued)	Page Number
Transmit Groups 1–4 Configuration Tables			
0x420	IMA_TX_GRP1_RX_TEST_PATTERN	Tx GRP 1 Rx Test Pattern	page 7-92
0x421	IMA_TX_GRP1_CTL	Tx GRP 1 Control	page 7-93
0x422	IMA_TX_GRP1_FIRST_PHY_ADDR	Tx GRP 1 First Link Address	page 7-94
0x423	IMA_TX_GRP1_ID	Tx GRP 1 Tx Group ID	page 7-94
0x424	IMA_TX_GRP1_STAT_CTL	Tx GRP 1 Status / Control	page 7-95
0x425	IMA_TX_GRP1_TIMING_INFO	Tx GRP 1 Timing Control	page 7-96
0x426	IMA_TX_GRP1_TEST_CTL	Tx GRP 1 Test Control	page 7-97
0x427	IMA_TX_GRP1_TX_TEST_PATTERN	Tx GRP 1 Tx Test Pattern	page 7-97
0x428	IMA_TX_GRP2_RX_TEST_PATTERN	Tx GRP 2 Rx Test Pattern	page 7-92
0x429	IMA_TX_GRP2_CTL	Tx GRP 2 Control	page 7-93
0x42a	IMA_TX_GRP2_FIRST_PHY_ADDR	Tx GRP 2 First Link Address	page 7-94
0x42b	IMA_TX_GRP2_ID	Tx GRP 2 Tx Group ID	page 7-94
0x42c	IMA_TX_GRP2_STAT_CTL	Tx GRP 2 Status / Control	page 7-95
0x42d	IMA_TX_GRP2_TIMING_INFO	Tx GRP 2 Timing Control	page 7-96
0x42e	IMA_TX_GRP2_TEST_CTL	Tx GRP 2 Test Control	page 7-97
0x42f	IMA_TX_GRP2_TX_TEST_PATTERN	Tx GRP 2 Tx Test Pattern	page 7-97
0x430	IMA_TX_GRP3_RX_TEST_PATTERN	Tx GRP 3 Rx Test Pattern	page 7-92
0x431	IMA_TX_GRP3_CTL	Tx GRP 3 Control	page 7-93
0x432	IMA_TX_GRP3_FIRST_PHY_ADDR	Tx GRP 3 First Link Address	page 7-94
0x433	IMA_TX_GRP3_ID	Tx GRP 3 Tx Group ID	page 7-94
0x434	IMA_TX_GRP3_STAT_CTL	Tx GRP 3 Status / Control	page 7-95
0x435	IMA_TX_GRP3_TIMING_INFO	Tx GRP 3 Timing Control	page 7-96
0x436	IMA_TX_GRP3_TEST_CTL	Tx GRP 3 Test Control	page 7-97
0x437	IMA_TX_GRP3_TX_TEST_PATTERN	Tx GRP 3 Tx Test Pattern	page 7-97
0x438	IMA_TX_GRP4_RX_TEST_PATTERN	Tx GRP 4 Rx Test Pattern	page 7-92
0x439	IMA_TX_GRP4_CTL	Tx GRP 4 Control	page 7-93
0x43a	IMA_TX_GRP4_FIRST_PHY_ADDR	Tx GRP 4 First Link Address	page 7-94
0x43b	IMA_TX_GRP4_ID	Tx GRP 4 Tx Group ID	page 7-94
0x43c	IMA_TX_GRP4_STAT_CTL	Tx GRP 4 Status / Control	page 7-95
0x43d	IMA_TX_GRP4_TIMING_INFO	Tx GRP 4 Timing Control	page 7-96
0x43e	IMA_TX_GRP4_TEST_CTL	Tx GRP 4 Test Control	page 7-97
0x43f	IMA_TX_GRP4_TX_TEST_PATTERN	Tx GRP 4 Tx Test Pattern	page 7-97

Table 7-10. IMA Control and Status Registers *(4 of 26)*

Address	Name	Description (Continued)	Page Number
Group 1–4 TX Cell Counters			
0x440 0x441 0x442 0x443 0x444 0x445 0x446 0x447	IMA_TX_GRP1_CELL_COUNT_LSB IMA_TX_GRP1_CELL_COUNT_MSB IMA_TX_GRP2_CELL_COUNT_LSB IMA_TX_GRP2_CELL_COUNT_MSB IMA_TX_GRP3_CELL_COUNT_LSB IMA_TX_GRP3_CELL_COUNT_MSB IMA_TX_GRP4_CELL_COUNT_LSB IMA_TX_GRP4_CELL_COUNT_MSB	Group 1 Transmit Cell Count LSBs Group 1 Transmit Cell Count MSBs Group 2 Transmit Cell Count LSBs Group 2 Transmit Cell Count MSBs Group 3 Transmit Cell Count LSBs Group 3 Transmit Cell Count MSBs Group 4 Transmit Cell Count LSBs Group 4 Transmit Cell Count MSBs	page 7-98
Group 1–4 RX Cell Counters			
0x450 0x451 0x452 0x453 0x454 0x455 0x456 0x457	IMA_RX_GRP1_CELL_COUNT_LSB IMA_RX_GRP1_CELL_COUNT_MSB IMA_RX_GRP2_CELL_COUNT_LSB IMA_RX_GRP2_CELL_COUNT_MSB IMA_RX_GRP3_CELL_COUNT_LSB IMA_RX_GRP3_CELL_COUNT_MSB IMA_RX_GRP4_CELL_COUNT_LSB IMA_RX_GRP4_CELL_COUNT_MSB	Group 1 Receive Cell Count LSBs Group 1 Receive Cell Count MSBs Group 2 Receive Cell Count LSBs Group 2 Receive Cell Count MSBs Group 3 Receive Cell Count LSBs Group 3 Receive Cell Count MSBs Group 4 Receive Cell Count LSBs Group 4 Receive Cell Count MSBs	page 7-99
0x458	IMA_RX_SOC_DETECTOR	Loss of PhyURxSOC Detector	page 7-87

Table 7-10. IMA Control and Status Registers *(5 of 26)*

Address	Name	Description (Continued)	Page Number
Port 0–7 Control and Status			
0x460 0x461 0x462 0x463 0x464 0x465 0x466 0x467	IMA_TX_LNK0_CTL IMA_TX_LNK1_CTL IMA_TX_LNK2_CTL IMA_TX_LNK3_CTL IMA_TX_LNK4_CTL IMA_TX_LNK5_CTL IMA_TX_LNK6_CTL IMA_TX_LNK7_CTL	Tx Link 0 Control Tx Link 1 Control Tx Link 2 Control Tx Link 3 Control Tx Link 4 Control Tx Link 5 Control Tx Link 6 Control Tx Link 7 Control	page 7-109
0x468 0x469 0x46a 0x46b 0x46c 0x46d 0x46e 0x46f	IMA_TX_LNK0_STATE IMA_TX_LNK1_STATE IMA_TX_LNK2_STATE IMA_TX_LNK3_STATE IMA_TX_LNK4_STATE IMA_TX_LNK5_STATE IMA_TX_LNK6_STATE IMA_TX_LNK7_STATE	Tx Link 0 Status Tx Link 1 Status Tx Link 2 Status Tx Link 3 Status Tx Link 4 Status Tx Link 5 Status Tx Link 6 Status Tx Link 7 Status	page 7-110
0x470 0x471 0x472 0x473 0x474 0x475 0x476 0x477	IMA_TX_LNK0_ID IMA_TX_LNK1_ID IMA_TX_LNK2_ID IMA_TX_LNK3_ID IMA_TX_LNK4_ID IMA_TX_LNK5_ID IMA_TX_LNK6_ID IMA_TX_LNK7_ID	Tx Link 0 Assigned LID Tx Link 1 Assigned LID Tx Link 2 Assigned LID Tx Link 3 Assigned LID Tx Link 4 Assigned LID Tx Link 5 Assigned LID Tx Link 6 Assigned LID Tx Link 7 Assigned LID	page 7-111
0x480 0x481 0x482 0x483 0x484 0x485 0x486 0x487	IMA_RX_LNK0_CTL IMA_RX_LNK1_CTL IMA_RX_LNK2_CTL IMA_RX_LNK3_CTL IMA_RX_LNK4_CTL IMA_RX_LNK5_CTL IMA_RX_LNK6_CTL IMA_RX_LNK7_CTL	Rx Link 0 Control Rx Link 1 Control Rx Link 2 Control Rx Link 3 Control Rx Link 4 Control Rx Link 5 Control Rx Link 6 Control Rx Link 7 Control	page 7-112
0x488 0x489 0x48a 0x48b 0x48c 0x48d 0x48e 0x48f	IMA_RX_LNK0_STATE IMA_RX_LNK1_STATE IMA_RX_LNK2_STATE IMA_RX_LNK3_STATE IMA_RX_LNK4_STATE IMA_RX_LNK5_STATE IMA_RX_LNK6_STATE IMA_RX_LNK7_STATE	Rx Link 0 Status Rx Link 1 Status Rx Link 2 Status Rx Link 3 Status Rx Link 4 Status Rx Link 5 Status Rx Link 6 Status Rx Link 7 Status	page 7-113
0x490 0x491 0x492 0x493 0x494 0x495 0x496 0x497	IMA_RX_LNK0_DEFECT IMA_RX_LNK1_DEFECT IMA_RX_LNK2_DEFECT IMA_RX_LNK3_DEFECT IMA_RX_LNK4_DEFECT IMA_RX_LNK5_DEFECT IMA_RX_LNK6_DEFECT IMA_RX_LNK7_DEFECT	Rx Link 0 Defects Rx Link 1 Defects Rx Link 2 Defects Rx Link 3 Defects Rx Link 4 Defects Rx Link 5 Defects Rx Link 6 Defects Rx Link 7 Defects	page 7-114

Table 7-10. IMA Control and Status Registers *(6 of 26)*

Address	Name	Description (Continued)	Page Number
0x498 0x499 0x49a 0x49b 0x49c 0x49d 0x49e 0x49f	IMA_FE_TX_LNK0_CFG IMA_FE_TX_LNK1_CFG IMA_FE_TX_LNK2_CFG IMA_FE_TX_LNK3_CFG IMA_FE_TX_LNK4_CFG IMA_FE_TX_LNK5_CFG IMA_FE_TX_LNK6_CFG IMA_FE_TX_LNK7_CFG	FE Tx Link 0 Link Config FE Tx Link 1 Link Config FE Tx Link 2 Link Config FE Tx Link 3 Link Config FE Tx Link 4 Link Config FE Tx Link 5 Link Config FE Tx Link 6 Link Config FE Tx Link 7 Link Config	page 7-115
0x4a0 0x4a1 0x4a2 0x4a3 0x4a4 0x4a5 0x4a6 0x4a7	IMA_FE_LNK0_STATE IMA_FE_LNK1_STATE IMA_FE_LNK2_STATE IMA_FE_LNK3_STATE IMA_FE_LNK4_STATE IMA_FE_LNK5_STATE IMA_FE_LNK6_STATE IMA_FE_LNK7_STATE	Rx Link 0 FE Status Rx Link 1 FE Status Rx Link 2 FE Status Rx Link 3 FE Status Rx Link 4 FE Status Rx Link 5 FE Status Rx Link 6 FE Status Rx Link 7 FE Status	page 7-116
0x4a8 0x4a9 0x4aa 0x4ab 0x4ac 0x4ad 0x4ae 0x4af	IMA_RX_LNK0_ID IMA_RX_LNK0_ID IMA_RX_LNK0_ID IMA_RX_LNK0_ID IMA_RX_LNK0_ID IMA_RX_LNK0_ID IMA_RX_LNK0_ID IMA_RX_LNK0_ID	Rx Link 0 Assigned LID Rx Link 1 Assigned LID Rx Link 2 Assigned LID Rx Link 3 Assigned LID Rx Link 4 Assigned LID Rx Link 5 Assigned LID Rx Link 6 Assigned LID Rx Link 7 Assigned LID	page 7-117
0x4b0 0x4b1 0x4b2 0x4b3 0x4b4 0x4b5 0x4b6 0x4b7	IMA_RX_LNK0_IV_CNT IMA_RX_LNK1_IV_CNT IMA_RX_LNK2_IV_CNT IMA_RX_LNK3_IV_CNT IMA_RX_LNK4_IV_CNT IMA_RX_LNK5_IV_CNT IMA_RX_LNK6_IV_CNT IMA_RX_LNK7_IV_CNT	Rx Link 0 IV-IMA Counter Rx Link 1 IV-IMA Counter Rx Link 2 IV-IMA Counter Rx Link 3 IV-IMA Counter Rx Link 4 IV-IMA Counter Rx Link 5 IV-IMA Counter Rx Link 6 IV-IMA Counter Rx Link 7 IV-IMA Counter	page 7-118
0x4b8 0x4b9 0x4ba 0x4bb 0x4bc 0x4bd 0x4be 0x4bf	IMA_RX_LNK0_OIF_CNT IMA_RX_LNK1_OIF_CNT IMA_RX_LNK2_OIF_CNT IMA_RX_LNK3_OIF_CNT IMA_RX_LNK4_OIF_CNT IMA_RX_LNK5_OIF_CNT IMA_RX_LNK6_OIF_CNT IMA_RX_LNK7_OIF_CNT	Rx Link 0 OIF-IMA Counter Rx Link 1 OIF-IMA Counter Rx Link 2 OIF-IMA Counter Rx Link 3 OIF-IMA Counter Rx Link 4 OIF-IMA Counter Rx Link 5 OIF-IMA Counter Rx Link 6 OIF-IMA Counter Rx Link 7 OIF-IMA Counter	page 7-119
0x4c0 0x4c1 0x4c2 0x4c3 0x4c4 0x4c5 0x4c6 0x4c7	IMA_FE_TX_LNK0_GRP_ID IMA_FE_TX_LNK1_GRP_ID IMA_FE_TX_LNK2_GRP_ID IMA_FE_TX_LNK3_GRP_ID IMA_FE_TX_LNK4_GRP_ID IMA_FE_TX_LNK5_GRP_ID IMA_FE_TX_LNK6_GRP_ID IMA_FE_TX_LNK7_GRP_ID	Rx Link 0 Captured GRP ID Rx Link 1 Captured GRP ID Rx Link 2 Captured GRP ID Rx Link 3 Captured GRP ID Rx Link 4 Captured GRP ID Rx Link 5 Captured GRP ID Rx Link 6 Captured GRP ID Rx Link 7 Captured GRP ID	page 7-120

Table 7-10. IMA Control and Status Registers *(7 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 1–4 Configuration Tables			
0x4d0	IMA_RX_GRP1_CFG	Rx GRP 1 Configuration	page 7-100
0x4d1	IMA_RX_GRP1_CTL	Rx GRP 1 Control	page 7-101
0x4d2	IMA_RX_GRP1_FIRST_PHY_ADDR	Rx GRP 1 First Link Address	page 7-102
0x4d3	IMA_RX_GRP1_ID	Rx GRP 1 Rx Group ID	page 7-103
0x4d4	IMA_RX_GRP2_CFG	Rx GRP 2 Configuration	page 7-100
0x4d5	IMA_RX_GRP2_CTL	Rx GRP 2 Control	page 7-101
0x4d6	IMA_RX_GRP2_FIRST_PHY_ADDR	Rx GRP 2 First Link Address	page 7-102
0x4d7	IMA_RX_GRP2_ID	Rx GRP 2 Rx Group ID	page 7-103
0x4d8	IMA_RX_GRP3_CFG	Rx GRP 3 Configuration	page 7-100
0x4d9	IMA_RX_GRP3_CTL	Rx GRP 3 Control	page 7-101
0x4da	IMA_RX_GRP3_FIRST_PHY_ADDR	Rx GRP 3 First Link Address	page 7-102
0x4db	IMA_RX_GRP3_ID	Rx GRP 3 Rx Group ID	page 7-103
0x4dc	IMA_RX_GRP4_CFG	Rx GRP 4 Configuration	page 7-100
0x4dd	IMA_RX_GRP4_CTL	Rx GRP 4 Control	page 7-101
0x4de	IMA_RX_GRP4_FIRST_PHY_ADDR	Rx GRP 4 First Link Address	page 7-102
0x4df	IMA_RX_GRP4_ID	Rx GRP 4 Rx Group ID	page 7-103

Table 7-10. IMA Control and Status Registers *(8 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 1–4 Far-End Status			
0x4e0	IMA_RX_GRP1_RX_TEST_PATTERN	Rx GRP 1 Rx Test Pattern	page 7-103
0x4e2	IMA_RX_GRP1_STAT_CTL_CHANGE	Rx GRP 1 SCCI	page 7-104
0x4e3	IMA_RX_GRP1_ACTUAL_GRP_ID	Rx GRP 1 Rx Group ID	page 7-104
0x4e4	IMA_RX_GRP1_STAT_CTL	Rx GRP 1 Status / Control	page 7-105
0x4e5	IMA_RX_GRP1_TIMING_INFO	Rx GRP 1 Timing Control	page 7-106
0x4e6	IMA_RX_GRP1_TEST_CTL	Rx GRP 1 Test Control	page 7-106
0x4e7	IMA_RX_GRP1_TX_TEST_PATTERN	Rx GRP 1 Tx Test Pattern	page 7-107
0x4e8	IMA_RX_GRP2_RX_TEST_PATTERN	Rx GRP 2 Rx Test Pattern	page 7-103
0x4ea	IMA_RX_GRP2_STAT_CTL_CHANGE	Rx GRP 2 SCCI	page 7-104
0x4eb	IMA_RX_GRP2_ACTUAL_GRP_ID	Rx GRP 2 Rx Group ID	page 7-104
0x4ec	IMA_RX_GRP2_STAT_CTL	Rx GRP 2 Status / Control	page 7-105
0x4ed	IMA_RX_GRP2_TIMING_INFO	Rx GRP 2 Timing Control	page 7-106
0x4ee	IMA_RX_GRP2_TEST_CTL	Rx GRP 2 Test Control	page 7-106
0x4ef	IMA_RX_GRP2_TX_TEST_PATTERN	Rx GRP 2 Tx Test Pattern	page 7-107
0x4f0	IMA_RX_GRP3_RX_TEST_PATTERN	Rx GRP 3 Rx Test Pattern	page 7-103
0x4f2	IMA_RX_GRP3_STAT_CTL_CHANGE	Rx GRP 3 SCCI	page 7-104
0x4f3	IMA_RX_GRP3_ACTUAL_GRP_ID	Rx GRP 3 Rx Group ID	page 7-104
0x4f4	IMA_RX_GRP3_STAT_CTL	Rx GRP 3 Status / Control	page 7-105
0x4f5	IMA_RX_GRP3_TIMING_INFO	Rx GRP 3 Timing Control	page 7-106
0x4f6	IMA_RX_GRP3_TEST_CTL	Rx GRP 3 Test Control	page 7-106
0x4f7	IMA_RX_GRP3_TX_TEST_PATTERN	Rx GRP 3 Tx Test Pattern	page 7-107
0x4f8	IMA_RX_GRP4_RX_TEST_PATTERN	Rx GRP 4 Rx Test Pattern	page 7-103
0x4fa	IMA_RX_GRP4_STAT_CTL_CHANGE	Rx GRP 4 SCCI	page 7-104
0x4fb	IMA_RX_GRP4_ACTUAL_GRP_ID	Rx GRP 4 Rx Group ID	page 7-104
0x4fc	IMA_RX_GRP4_STAT_CTL	Rx GRP 4 Status / Control	page 7-105
0x4fd	IMA_RX_GRP4_TIMING_INFO	Rx GRP 4 Timing Control	page 7-106
0x4fe	IMA_RX_GRP4_TEST_CTL	Rx GRP 4 Test Control	page 7-106
0x4ff	IMA_RX_GRP4_TX_TEST_PATTERN	Rx GRP 4 Tx Test Pattern	page 7-107

Table 7-10. IMA Control and Status Registers *(9 of 26)*

Address	Name	Description (Continued)	Page Number
Transmit Groups 5–8 Configuration Tables			
0x520	IMA_TX_GRP5_RX_TEST_PATTERN	Tx GRP 5 Rx Test Pattern	page 7-92
0x521	IMA_TX_GRP5_CTL	Tx GRP 5 Control	page 7-93
0x522	IMA_TX_GRP5_FIRST_PHY_ADDR	Tx GRP 5 First Link Address	page 7-94
0x523	IMA_TX_GRP5_ID	Tx GRP 5 Tx Group ID	page 7-94
0x524	IMA_TX_GRP5_STAT_CTL	Tx GRP 5 Status / Control	page 7-95
0x525	IMA_TX_GRP5_TIMING_INFO	Tx GRP 5 Timing Control	page 7-96
0x526	IMA_TX_GRP5_TEST_CTL	Tx GRP 5 Test Control	page 7-97
0x527	IMA_TX_GRP5_TX_TEST_PATTERN	Tx GRP 5 Tx Test Pattern	page 7-97
0x528	IMA_TX_GRP6_RX_TEST_PATTERN	Tx GRP 6 Rx Test Pattern	page 7-92
0x529	IMA_TX_GRP6_CTL	Tx GRP 6 Control	page 7-93
0x52a	IMA_TX_GRP6_FIRST_PHY_ADDR	Tx GRP 6 First Link Address	page 7-94
0x52b	IMA_TX_GRP6_ID	Tx GRP 6 Tx Group ID	page 7-94
0x52c	IMA_TX_GRP6_STAT_CTL	Tx GRP 6 Status / Control	page 7-95
0x52d	IMA_TX_GRP6_TIMING_INFO	Tx GRP 6 Timing Control	page 7-96
0x52e	IMA_TX_GRP6_TEST_CTL	Tx GRP 6 Test Control	page 7-97
0x52f	IMA_TX_GRP6_TX_TEST_PATTERN	Tx GRP 6 Tx Test Pattern	page 7-97
0x530	IMA_TX_GRP7_RX_TEST_PATTERN	Tx GRP 7 Rx Test Pattern	page 7-92
0x531	IMA_TX_GRP7_CTL	Tx GRP 7 Control	page 7-93
0x532	IMA_TX_GRP7_FIRST_PHY_ADDR	Tx GRP 7 First Link Address	page 7-94
0x533	IMA_TX_GRP7_ID	Tx GRP 7 Tx Group ID	page 7-94
0x534	IMA_TX_GRP7_STAT_CTL	Tx GRP 7 Status / Control	page 7-95
0x535	IMA_TX_GRP7_TIMING_INFO	Tx GRP 7 Timing Control	page 7-96
0x536	IMA_TX_GRP7_TEST_CTL	Tx GRP 7 Test Control	page 7-97
0x537	IMA_TX_GRP7_TX_TEST_PATTERN	Tx GRP 7 Tx Test Pattern	page 7-97
0x538	IMA_TX_GRP8_RX_TEST_PATTERN	Tx GRP 8 Rx Test Pattern	page 7-92
0x539	IMA_TX_GRP8_CTL	Tx GRP 8 Control	page 7-93
0x53a	IMA_TX_GRP8_FIRST_PHY_ADDR	Tx GRP 8 First Link Address	page 7-94
0x53b	IMA_TX_GRP8_ID	Tx GRP 8 Tx Group ID	page 7-94
0x53c	IMA_TX_GRP8_STAT_CTL	Tx GRP 8 Status / Control	page 7-95
0x53d	IMA_TX_GRP8_TIMING_INFO	Tx GRP 8 Timing Control	page 7-96
0x53e	IMA_TX_GRP8_TEST_CTL	Tx GRP 8 Test Control	page 7-97
0x53f	IMA_TX_GRP8_TX_TEST_PATTERN	Tx GRP 8 Tx Test Pattern	page 7-97

Table 7-10. IMA Control and Status Registers *(10 of 26)*

Address	Name	Description (Continued)	Page Number
Group 5–8 TX Cell Counters			
0x540	IMA_TX_GRP5_CELL_COUNT_LSB	Group 5 Transmit Cell Count LSBs	page 7-98
0x541	IMA_TX_GRP5_CELL_COUNT_MSB	Group 5 Transmit Cell Count MSBs	
0x542	IMA_TX_GRP6_CELL_COUNT_LSB	Group 6Transmit Cell Count LSBs	
0x543	IMA_TX_GRP6_CELL_COUNT_MSB	Group 6 Transmit Cell Count MSBs	
0x544	IMA_TX_GRP7_CELL_COUNT_LSB	Group 7 Transmit Cell Count LSBs	
0x545	IMA_TX_GRP7_CELL_COUNT_MSB	Group 7Transmit Cell Count MSBs	
0x546	IMA_TX_GRP8_CELL_COUNT_LSB	Group 8 Transmit Cell Count LSBs	
0x547	IMA_TX_GRP8_CELL_COUNT_MSB	Group 8 Transmit Cell Count MSBs	
Group 5–8 RX Cell Counters			
0x550	IMA_RX_GRP5_CELL_COUNT_LSB	Group 5 Receive Cell Count LSBs	page 7-99
0x551	IMA_RX_GRP5_CELL_COUNT_MSB	Group 5 Receive Cell Count MSBs	
0x552	IMA_RX_GRP6_CELL_COUNT_LSB	Group 6 Receive Cell Count LSBs	
0x553	IMA_RX_GRP6_CELL_COUNT_MSB	Group 6 Receive Cell Count MSBs	
0x554	IMA_RX_GRP7_CELL_COUNT_LSB	Group 7 Receive Cell Count LSBs	
0x555	IMA_RX_GRP7_CELL_COUNT_MSB	Group 7 Receive Cell Count MSBs	
0x556	IMA_RX_GRP8_CELL_COUNT_LSB	Group 8 Receive Cell Count LSBs	
0x557	IMA_RX_GRP8_CELL_COUNT_MSB	Group 8 Receive Cell Count MSBs	

Table 7-10. IMA Control and Status Registers *(11 of 26)*

Address	Name	Description (Continued)	Page Number
Port 8–15 Control and Status			
0x560 0x561 0x562 0x563 0x564 0x565 0x566 0x567	IMA_TX_LNK8_CTL IMA_TX_LNK9_CTL IMA_TX_LNK10_CTL IMA_TX_LNK11_CTL IMA_TX_LNK12_CTL IMA_TX_LNK13_CTL IMA_TX_LNK14_CTL IMA_TX_LNK15_CTL	Tx Link 8 Control Tx Link 9 Control Tx Link 10 Control Tx Link 11 Control Tx Link 12 Control Tx Link 13 Control Tx Link 14 Control Tx Link 15 Control	page 7-109
0x568 0x569 0x56a 0x56b 0x56c 0x56d 0x56e 0x56f	IMA_TX_LNK8_STATE IMA_TX_LNK9_STATE IMA_TX_LNK10_STATE IMA_TX_LNK11_STATE IMA_TX_LNK12_STATE IMA_TX_LNK13_STATE IMA_TX_LNK14_STATE IMA_TX_LNK15_STATE	Tx Link 8 Status Tx Link 9 Status Tx Link 10 Status Tx Link 11 Status Tx Link 12 Status Tx Link 13 Status Tx Link 14 Status Tx Link 15 Status	page 7-110
0x570 0x571 0x572 0x573 0x574 0x575 0x576 0x577	IMA_TX_LNK8_ID IMA_TX_LNK9_ID IMA_TX_LNK10_ID IMA_TX_LNK11_ID IMA_TX_LNK12_ID IMA_TX_LNK13_ID IMA_TX_LNK14_ID IMA_TX_LNK15_ID	Tx Link 8 Assigned LID Tx Link 9 Assigned LID Tx Link 10 Assigned LID Tx Link 11 Assigned LID Tx Link 12 Assigned LID Tx Link 13 Assigned LID Tx Link 14 Assigned LID Tx Link 15 Assigned LID	page 7-111
0x580 0x581 0x582 0x583 0x584 0x585 0x586 0x587	IMA_RX_LNK8_CTL IMA_RX_LNK9_CTL IMA_RX_LNK10_CTL IMA_RX_LNK11_CTL IMA_RX_LNK12_CTL IMA_RX_LNK13_CTL IMA_RX_LNK14_CTL IMA_RX_LNK15_CTL	Rx Link 8 Control Rx Link 9 Control Rx Link 10Control Rx Link 11 Control Rx Link 12 Control Rx Link 13 Control Rx Link 14 Control Rx Link 15 Control	page 7-112
0x588 0x589 0x58a 0x58b 0x58c 0x58d 0x58e 0x58f	IMA_RX_LNK8_STATE IMA_RX_LNK9_STATE IMA_RX_LNK10_STATE IMA_RX_LNK11_STATE IMA_RX_LNK12_STATE IMA_RX_LNK13_STATE IMA_RX_LNK14_STATE IMA_RX_LNK15_STATE	Rx Link 8 Status Rx Link 9 Status Rx Link 10 Status Rx Link 11 Status Rx Link 12 Status Rx Link 13 Status Rx Link 14 Status Rx Link 15 Status	page 7-113
0x590 0x591 0x592 0x593 0x594 0x595 0x596 0x597	IMA_RX_LNK8_DEFECT IMA_RX_LNK9_DEFECT IMA_RX_LNK10_DEFECT IMA_RX_LNK11_DEFECT IMA_RX_LNK12_DEFECT IMA_RX_LNK13_DEFECT IMA_RX_LNK14_DEFECT IMA_RX_LNK15_DEFECT	Rx Link 8 Defects Rx Link 9 Defects Rx Link 10 Defects Rx Link 11 Defects Rx Link 12 Defects Rx Link 13 Defects Rx Link 14 Defects Rx Link 15 Defects	page 7-114

Table 7-10. IMA Control and Status Registers *(12 of 26)*

Address	Name	Description (Continued)	Page Number
0x598 0x599 0x59a 0x59b 0x59c 0x59d 0x59e 0x59f	IMA_FE_TX_LNK8_CFG IMA_FE_TX_LNK9_CFG IMA_FE_TX_LNK10_CFG IMA_FE_TX_LNK11_CFG IMA_FE_TX_LNK12_CFG IMA_FE_TX_LNK13_CFG IMA_FE_TX_LNK14_CFG IMA_FE_TX_LNK15_CFG	FE Tx Link 8 Link Config FE Tx Link 9 Link Config FE Tx Link 10 Link Config FE Tx Link 11 Link Config FE Tx Link 12 Link Config FE Tx Link 13 Link Config FE Tx Link 14 Link Config FE Tx Link 15 Link Config	page 7-115
0x5a0 0x5a1 0x5a2 0x5a3 0x5a4 0x5a5 0x5a6 0x5a7	IMA_FE_LNK8_STATE IMA_FE_LNK9_STATE IMA_FE_LNK10_STATE IMA_FE_LNK11_STATE IMA_FE_LNK12_STATE IMA_FE_LNK13_STATE IMA_FE_LNK14_STATE IMA_FE_LNK15_STATE	Rx Link 8 FE Status Rx Link 9 FE Status Rx Link 10 FE Status Rx Link 11 FE Status Rx Link 12 FE Status Rx Link 13 FE Status Rx Link 14 FE Status Rx Link 15 FE Status	page 7-116
0x5a8 0x5a9 0x5aa 0x5ab 0x5ac 0x5ad 0x5ae 0x5af	IMA_RX_LNK8_ID IMA_RX_LNK9_ID IMA_RX_LNK10_ID IMA_RX_LNK11_ID IMA_RX_LNK12_ID IMA_RX_LNK13_ID IMA_RX_LNK14_ID IMA_RX_LNK15_ID	Rx Link 8 Assigned LID Rx Link 9 Assigned LID Rx Link 10 Assigned LID Rx Link 11 Assigned LID Rx Link 12 Assigned LID Rx Link 13 Assigned LID Rx Link 14 Assigned LID Rx Link 15 Assigned LID	page 7-117
0x5b0 0x5b1 0x5b2 0x5b3 0x5b4 0x5b5 0x5b6 0x5b7	IMA_RX_LNK8_IV_CNT IMA_RX_LNK9_IV_CNT IMA_RX_LNK10_IV_CNT IMA_RX_LNK11_IV_CNT IMA_RX_LNK12_IV_CNT IMA_RX_LNK13_IV_CNT IMA_RX_LNK14_IV_CNT IMA_RX_LNK15_IV_CNT	Rx Link 8 IV-IMA Counter Rx Link 9 IV-IMA Counter Rx Link 10 IV-IMA Counter Rx Link 11 IV-IMA Counter Rx Link 12 IV-IMA Counter Rx Link 13 IV-IMA Counter Rx Link 14 IV-IMA Counter Rx Link 15 IV-IMA Counter	page 7-118
0x5b8 0x5b9 0x5ba 0x5bb 0x5bc 0x5bd 0x5be 0x5bf	IMA_RX_LNK8_OIF_CNT IMA_RX_LNK9_OIF_CNT IMA_RX_LNK10_OIF_CNT IMA_RX_LNK11_OIF_CNT IMA_RX_LNK12_OIF_CNT IMA_RX_LNK13_OIF_CNT IMA_RX_LNK14_OIF_CNT IMA_RX_LNK15_OIF_CNT	Rx Link 8 OIF-IMA Counter Rx Link 9 OIF-IMA Counter Rx Link 10 OIF-IMA Counter Rx Link 11 OIF-IMA Counter Rx Link 12 OIF-IMA Counter Rx Link 13 OIF-IMA Counter Rx Link 14 OIF-IMA Counter Rx Link 15 OIF-IMA Counter	page 7-119
0x5c0 0x5c1 0x5c2 0x5c3 0x5c4 0x5c5 0x5c6 0x5c7	IMA_FE_TX_LNK8_GRP_ID IMA_FE_TX_LNK9_GRP_ID IMA_FE_TX_LNK10_GRP_ID IMA_FE_TX_LNK11_GRP_ID IMA_FE_TX_LNK12_GRP_ID IMA_FE_TX_LNK13_GRP_ID IMA_FE_TX_LNK14_GRP_ID IMA_FE_TX_LNK15_GRP_ID	Rx Link 8 Captured GRP ID Rx Link 9 Captured GRP ID Rx Link 10 Captured GRP ID Rx Link 11 Captured GRP ID Rx Link 12 Captured GRP ID Rx Link 13 Captured GRP ID Rx Link 14 Captured GRP ID Rx Link 15 Captured GRP ID	page 7-120

Table 7-10. IMA Control and Status Registers *(13 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 5–8 Configuration Tables			
0x5d0	IMA_RX_GRP5_CFG	Rx GRP 5 Configuration	page 7-100
0x5d1	IMA_RX_GRP5_CTL	Rx GRP 5 Control	page 7-101
0x5d2	IMA_RX_GRP5_FIRST_PHY_ADDR	Rx GRP 5 First Link Address	page 7-102
0x5d3	IMA_RX_GRP5_ID	Rx GRP 5 Rx Group ID	page 7-103
0x5d4	IMA_RX_GRP6_CFG	Rx GRP 6 Configuration	page 7-100
0x5d5	IMA_RX_GRP6_CTL	Rx GRP 6 Control	page 7-101
0x5d6	IMA_RX_GRP6_FIRST_PHY_ADDR	Rx GRP 6 First Link Address	page 7-102
0x5d7	IMA_RX_GRP6_ID	Rx GRP 6 Rx Group ID	page 7-103
0x5d8	IMA_RX_GRP7_CFG	Rx GRP 7 Configuration	page 7-100
0x5d9	IMA_RX_GRP7_CTL	Rx GRP 7 Control	page 7-101
0x5da	IMA_RX_GRP7_FIRST_PHY_ADDR	Rx GRP 7 First Link Address	page 7-102
0x5db	IMA_RX_GRP7_ID	Rx GRP 7 Rx Group ID	page 7-103
0x5dc	IMA_RX_GRP8_CFG	Rx GRP 8 Configuration	page 7-100
0x5dd	IMA_RX_GRP8_CTL	Rx GRP 8 Control	page 7-101
0x5de	IMA_RX_GRP8_FIRST_PHY_ADDR	Rx GRP 8 First Link Address	page 7-102
0x5df	IMA_RX_GRP8_ID	Rx GRP 8 Rx Group ID	page 7-103

Table 7-10. IMA Control and Status Registers *(14 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 5–8 Far-End Status			
0x5e0	IMA_RX_GRP5_RX_TEST_PATTERN	Rx GRP 5 Rx Test Pattern	page 7-103
0x5e2	IMA_RX_GRP5_STAT_CTL_CHANGE	Rx GRP 5 SCCI	page 7-104
0x5e3	IMA_RX_GRP5_ACTUAL_GRP_ID	Rx GRP 5 Rx Group ID	page 7-104
0x5e4	IMA_RX_GRP5_STAT_CTL	Rx GRP 5 Status / Control	page 7-105
0x5e5	IMA_RX_GRP5_TIMING_INFO	Rx GRP 5 Timing Control	page 7-106
0x5e6	IMA_RX_GRP5_TEST_CTL	Rx GRP 5 Test Control	page 7-106
0x5e7	IMA_RX_GRP5_TX_TEST_PATTERN	Rx GRP 5 Tx Test Pattern	page 7-107
0x5e8	IMA_RX_GRP6_RX_TEST_PATTERN	Rx GRP 6 Rx Test Pattern	page 7-103
0x5ea	IMA_RX_GRP6_STAT_CTL_CHANGE	Rx GRP 6 SCCI	page 7-104
0x5eb	IMA_RX_GRP6_ACTUAL_GRP_ID	Rx GRP 6 Rx Group ID	page 7-104
0x5ec	IMA_RX_GRP6_STAT_CTL	Rx GRP 6 Status / Control	page 7-105
0x5ed	IMA_RX_GRP6_TIMING_INFO	Rx GRP 6 Timing Control	page 7-106
0x5ee	IMA_RX_GRP6_TEST_CTL	Rx GRP 6 Test Control	page 7-106
0x5ef	IMA_RX_GRP6_TX_TEST_PATTERN	Rx GRP 6 Tx Test Pattern	page 7-107
0x5f0	IMA_RX_GRP7_RX_TEST_PATTERN	Rx GRP 7 Rx Test Pattern	page 7-103
0x5f2	IMA_RX_GRP7_STAT_CTL_CHANGE	Rx GRP 7 SCCI	page 7-104
0x5f3	IMA_RX_GRP7_ACTUAL_GRP_ID	Rx GRP 7 Rx Group ID	page 7-104
0x5f4	IMA_RX_GRP7_STAT_CTL	Rx GRP 7 Status / Control	page 7-105
0x5f5	IMA_RX_GRP7_TIMING_INFO	Rx GRP 7 Timing Control	page 7-106
0x5f6	IMA_RX_GRP7_TEST_CTL	Rx GRP 7 Test Control	page 7-106
0x5f7	IMA_RX_GRP7_TX_TEST_PATTERN	Rx GRP 7 Tx Test Pattern	page 7-107
0x5f8	IMA_RX_GRP8_RX_TEST_PATTERN	Rx GRP 8 Rx Test Pattern	page 7-103
0x5fa	IMA_RX_GRP8_STAT_CTL_CHANGE	Rx GRP 8 SCCI	page 7-104
0x5fb	IMA_RX_GRP8_ACTUAL_GRP_ID	Rx GRP 8 Rx Group ID	page 7-104
0x5fc	IMA_RX_GRP8_STAT_CTL	Rx GRP 8 Status / Control	page 7-105
0x5fd	IMA_RX_GRP8_TIMING_INFO	Rx GRP 8 Timing Control	page 7-106
0x5fe	IMA_RX_GRP8_TEST_CTL	Rx GRP 8 Test Control	page 7-106
0x5ff	IMA_RX_GRP8_TX_TEST_PATTERN	Rx GRP 8 Tx Test Pattern	page 7-107

Table 7-10. IMA Control and Status Registers *(15 of 26)*

Address	Name	Description (Continued)	Page Number
Transmit Groups 9–12 Configuration Tables			
0x620	IMA_TX_GRP9_RX_TEST_PATTERN	Tx GRP 9 Rx Test Pattern	page 7-92
0x621	IMA_TX_GRP9_CTL	Tx GRP 9 Control	page 7-93
0x622	IMA_TX_GRP9_FIRST_PHY_ADDR	Tx GRP 9 First Link Address	page 7-94
0x623	IMA_TX_GRP9_ID	Tx GRP 9 Tx Group ID	page 7-94
0x624	IMA_TX_GRP9_STAT_CTL	Tx GRP 9 Status / Control	page 7-95
0x625	IMA_TX_GRP9_TIMING_INFO	Tx GRP 9 Timing Control	page 7-96
0x626	IMA_TX_GRP9_TEST_CTL	Tx GRP 9 Test Control	page 7-97
0x627	IMA_TX_GRP9_TX_TEST_PATTERN	Tx GRP 9 Tx Test Pattern	page 7-97
0x628	IMA_TX_GRP10_RX_TEST_PATTERN	Tx GRP 10 Rx Test Pattern	page 7-92
0x629	IMA_TX_GRP10_CTL	Tx GRP 10 Control	page 7-93
0x62a	IMA_TX_GRP10_FIRST_PHY_ADDR	Tx GRP 10 First Link Address	page 7-94
0x62b	IMA_TX_GRP10_ID	Tx GRP 10 Tx Group ID	page 7-94
0x62c	IMA_TX_GRP10_STAT_CTL	Tx GRP 10 Status / Control	page 7-95
0x62d	IMA_TX_GRP10_TIMING_INFO	Tx GRP 10 Timing Control	page 7-96
0x62e	IMA_TX_GRP10_TEST_CTL	Tx GRP 10 Test Control	page 7-97
0x62f	IMA_TX_GRP10_TX_TEST_PATTERN	Tx GRP 10 Tx Test Pattern	page 7-97
0x630	IMA_TX_GRP11_RX_TEST_PATTERN	Tx GRP 11 Rx Test Pattern	page 7-92
0x631	IMA_TX_GRP11_CTL	Tx GRP 11 Control	page 7-93
0x632	IMA_TX_GRP11_FIRST_PHY_ADDR	Tx GRP 11 First Link Address	page 7-94
0x633	IMA_TX_GRP11_ID	Tx GRP 11 Tx Group ID	page 7-94
0x634	IMA_TX_GRP11_STAT_CTL	Tx GRP 11 Status / Control	page 7-95
0x635	IMA_TX_GRP11_TIMING_INFO	Tx GRP 11 Timing Control	page 7-96
0x636	IMA_TX_GRP11_TEST_CTL	Tx GRP 11 Test Control	page 7-97
0x637	IMA_TX_GRP11_TX_TEST_PATTERN	Tx GRP 11 Tx Test Pattern	page 7-97
0x638	IMA_TX_GRP12_RX_TEST_PATTERN	Tx GRP 12 Rx Test Pattern	page 7-92
0x639	IMA_TX_GRP12_CTL	Tx GRP 12 Control	page 7-93
0x63a	IMA_TX_GRP12_FIRST_PHY_ADDR	Tx GRP 12 First Link Address	page 7-94
0x63b	IMA_TX_GRP12_ID	Tx GRP 12 Tx Group ID	page 7-94
0x63c	IMA_TX_GRP12_STAT_CTL	Tx GRP 12 Status / Control	page 7-95
0x63d	IMA_TX_GRP12_TIMING_INFO	Tx GRP 12 Timing Control	page 7-96
0x63e	IMA_TX_GRP12_TEST_CTL	Tx GRP 12 Test Control	page 7-97
0x63f	IMA_TX_GRP12_TX_TEST_PATTERN	Tx GRP 12 Tx Test Pattern	page 7-97

Table 7-10. IMA Control and Status Registers *(16 of 26)*

Address	Name	Description (Continued)	Page Number
Group 9-12 TX Cell Counters			
0x640	IMA_TX_GRP9_CELL_COUNT_LSB	Group 9 Transmit Cell Count LSBs	page 7-98
0x641	IMA_TX_GRP9_CELL_COUNT_MSB	Group 9 Transmit Cell Count MSBs	
0x642	IMA_TX_GRP10_CELL_COUNT_LSB	Group 10Transmit Cell Count LSBs	
0x643	IMA_TX_GRP10_CELL_COUNT_MSB	Group 10 Transmit Cell Count MSBs	
0x644	IMA_TX_GRP11_CELL_COUNT_LSB	Group 11 Transmit Cell Count LSBs	
0x645	IMA_TX_GRP11_CELL_COUNT_MSB	Group 11Transmit Cell Count MSBs	
0x646	IMA_TX_GRP12_CELL_COUNT_LSB	Group 12 Transmit Cell Count LSBs	
0x647	IMA_TX_GRP12_CELL_COUNT_MSB	Group 12 Transmit Cell Count MSBs	
Group 9-12 RX Cell Counters			
0x650	IMA_RX_GRP9_CELL_COUNT_LSB	Group 9 Receive Cell Count LSBs	page 7-99
0x651	IMA_RX_GRP9_CELL_COUNT_MSB	Group 9 Receive Cell Count MSBs	
0x652	IMA_RX_GRP10_CELL_COUNT_LSB	Group 10 Receive Cell Count LSBs	
0x653	IMA_RX_GRP10_CELL_COUNT_MSB	Group 10 Receive Cell Count MSBs	
0x654	IMA_RX_GRP11_CELL_COUNT_LSB	Group 11 Receive Cell Count LSBs	
0x655	IMA_RX_GRP11_CELL_COUNT_MSB	Group 11 Receive Cell Count MSBs	
0x656	IMA_RX_GRP12_CELL_COUNT_LSB	Group 12 Receive Cell Count LSBs	
0x657	IMA_RX_GRP12_CELL_COUNT_MSB	Group 12 Receive Cell Count MSBs	

Table 7-10. IMA Control and Status Registers *(17 of 26)*

Address	Name	Description (Continued)	Page Number
Port 16–23 Control and Status			
0x660 0x661 0x662 0x663 0x664 0x665 0x666 0x667	IMA_TX_LNK16_CTL IMA_TX_LNK17_CTL IMA_TX_LNK18_CTL IMA_TX_LNK19_CTL IMA_TX_LNK20_CTL IMA_TX_LNK21_CTL IMA_TX_LNK22_CTL IMA_TX_LNK23_CTL	Tx Link 16 Control Tx Link 17 Control Tx Link 18 Control Tx Link 19 Control Tx Link 20 Control Tx Link 21 Control Tx Link 22 Control Tx Link 23 Control	page 7-109
0x668 0x669 0x66a 0x66b 0x66c 0x66d 0x66e 0x66f	IMA_TX_LNK16_STATE IMA_TX_LNK17_STATE IMA_TX_LNK18_STATE IMA_TX_LNK19_STATE IMA_TX_LNK20_STATE IMA_TX_LNK21_STATE IMA_TX_LNK22_STATE IMA_TX_LNK23_STATE	Tx Link 16 Status Tx Link 17 Status Tx Link 18 Status Tx Link 19 Status Tx Link 20 Status Tx Link 21 Status Tx Link 22 Status Tx Link 23 Status	page 7-110
0x670 0x671 0x672 0x673 0x674 0x675 0x676 0x677	IMA_TX_LNK16_ID IMA_TX_LNK17_ID IMA_TX_LNK18_ID IMA_TX_LNK19_ID IMA_TX_LNK20_ID IMA_TX_LNK21_ID IMA_TX_LNK22_ID IMA_TX_LNK23_ID	Tx Link 16 Assigned LID Tx Link 17 Assigned LID Tx Link 18 Assigned LID Tx Link 19 Assigned LID Tx Link 20 Assigned LID Tx Link 21 Assigned LID Tx Link 22 Assigned LID Tx Link 23 Assigned LID	page 7-111
0x680 0x681 0x682 0x683 0x684 0x685 0x686 0x687	IMA_RX_LNK16_CTL IMA_RX_LNK17_CTL IMA_RX_LNK18_CTL IMA_RX_LNK19_CTL IMA_RX_LNK20_CTL IMA_RX_LNK21_CTL IMA_RX_LNK22_CTL IMA_RX_LNK23_CTL	Rx Link 16 Control Rx Link 17 Control Rx Link 18 Control Rx Link 19 Control Rx Link 20 Control Rx Link 21 Control Rx Link 22 Control Rx Link 23 Control	page 7-112
0x688 0x689 0x68a 0x68b 0x68c 0x68d 0x68e 0x68f	IMA_RX_LNK16_STATE IMA_RX_LNK17_STATE IMA_RX_LNK18_STATE IMA_RX_LNK19_STATE IMA_RX_LNK20_STATE IMA_RX_LNK21_STATE IMA_RX_LNK22_STATE IMA_RX_LNK23_STATE	Rx Link 16 Status Rx Link 17 Status Rx Link 18 Status Rx Link 19 Status Rx Link 20 Status Rx Link 21 Status Rx Link 22 Status Rx Link 23 Status	page 7-113
0x690 0x691 0x692 0x693 0x694 0x695 0x696 0x697	IMA_RX_LNK16_DEFECT IMA_RX_LNK17_DEFECT IMA_RX_LNK18_DEFECT IMA_RX_LNK19_DEFECT IMA_RX_LNK20_DEFECT IMA_RX_LNK21_DEFECT IMA_RX_LNK22_DEFECT IMA_RX_LNK23_DEFECT	Rx Link 16 Defects Rx Link 17 Defects Rx Link 18 Defects Rx Link 19 Defects Rx Link 20 Defects Rx Link 21 Defects Rx Link 22 Defects Rx Link 23 Defects	page 7-114

Table 7-10. IMA Control and Status Registers *(18 of 26)*

Address	Name	Description (Continued)	Page Number
0x698 0x699 0x69a 0x69b 0x69c 0x69d 0x69e 0x69f	IMA_FE_TX_LNK16_CFG IMA_FE_TX_LNK17_CFG IMA_FE_TX_LNK18_CFG IMA_FE_TX_LNK19_CFG IMA_FE_TX_LNK20_CFG IMA_FE_TX_LNK21_CFG IMA_FE_TX_LNK22_CFG IMA_FE_TX_LNK23_CFG	FE Tx Link 16 Link Config FE Tx Link 17 Link Config FE Tx Link 18 Link Config FE Tx Link 19 Link Config FE Tx Link 20 Link Config FE Tx Link 21 Link Config FE Tx Link 22 Link Config FE Tx Link 23 Link Config	page 7-115
0x6a0 0x6a1 0x6a2 0x6a3 0x6a4 0x6a5 0x6a6 0x6a7	IMA_FE_LNK16_STATE IMA_FE_LNK17_STATE IMA_FE_LNK18_STATE IMA_FE_LNK19_STATE IMA_FE_LNK20_STATE IMA_FE_LNK21_STATE IMA_FE_LNK22_STATE IMA_FE_LNK23_STATE	Rx Link 16 FE Status Rx Link 17 FE Status Rx Link 18 FE Status Rx Link 19 FE Status Rx Link 20 FE Status Rx Link 21 FE Status Rx Link 22 FE Status Rx Link 23 FE Status	page 7-116
0x6a8 0x6a9 0x6aa 0x6ab 0x6ac 0x6ad 0x6ae 0x6af	IMA_RX_LNK16_ID IMA_RX_LNK17_ID IMA_RX_LNK18_ID IMA_RX_LNK19_ID IMA_RX_LNK20_ID IMA_RX_LNK21_ID IMA_RX_LNK22_ID IMA_RX_LNK23_ID	Rx Link 16 Assigned LID Rx Link 17 Assigned LID Rx Link 18 Assigned LID Rx Link 19 Assigned LID Rx Link 20 Assigned LID Rx Link 21 Assigned LID Rx Link 22 Assigned LID Rx Link 23 Assigned LID	page 7-117
0x6b0 0x6b1 0x6b2 0x6b3 0x6b4 0x6b5 0x6b6 0x6b7	IMA_RX_LNK16_IV_CNT IMA_RX_LNK17_IV_CNT IMA_RX_LNK18_IV_CNT IMA_RX_LNK19_IV_CNT IMA_RX_LNK20_IV_CNT IMA_RX_LNK21_IV_CNT IMA_RX_LNK22_IV_CNT IMA_RX_LNK23_IV_CNT	Rx Link 16 IV-IMA Counter Rx Link 17 IV-IMA Counter Rx Link 18 IV-IMA Counter Rx Link 19 IV-IMA Counter Rx Link 20 IV-IMA Counter Rx Link 21 IV-IMA Counter Rx Link 22 IV-IMA Counter Rx Link 23 IV-IMA Counter	page 7-118
0x6b8 0x6b9 0x6ba 0x6bb 0x6bc 0x6bd 0x6be 0x6bf	IMA_RX_LNK16_OIF_CNT IMA_RX_LNK17_OIF_CNT IMA_RX_LNK18_OIF_CNT IMA_RX_LNK19_OIF_CNT IMA_RX_LNK20_OIF_CNT IMA_RX_LNK21_OIF_CNT IMA_RX_LNK22_OIF_CNT IMA_RX_LNK23_OIF_CNT	Rx Link 16 OIF-IMA Counter Rx Link 17 OIF-IMA Counter Rx Link 18 OIF-IMA Counter Rx Link 19 OIF-IMA Counter Rx Link 20 OIF-IMA Counter Rx Link 21 OIF-IMA Counter Rx Link 22 OIF-IMA Counter Rx Link 23 OIF-IMA Counter	page 7-119
0x6c0 0x6c1 0x6c2 0x6c3 0x6c4 0x6c5 0x6c6 0x6c7	IMA_FE_TX_LNK16_GRP_ID IMA_FE_TX_LNK17_GRP_ID IMA_FE_TX_LNK18_GRP_ID IMA_FE_TX_LNK19_GRP_ID IMA_FE_TX_LNK20_GRP_ID IMA_FE_TX_LNK21_GRP_ID IMA_FE_TX_LNK22_GRP_ID IMA_FE_TX_LNK23_GRP_ID	Rx Link 16 Captured GRP ID Rx Link 17 Captured GRP ID Rx Link 18 Captured GRP ID Rx Link 19 Captured GRP ID Rx Link 20 Captured GRP ID Rx Link 21 Captured GRP ID Rx Link 22 Captured GRP ID Rx Link 23 Captured GRP ID	page 7-120

Table 7-10. IMA Control and Status Registers *(19 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 9–12 Configuration Tables			
0x6d0	IMA_RX_GRP9_CFG	Rx GRP 9 Configuration	page 7-100
0x6d1	IMA_RX_GRP9_CTL	Rx GRP 9 Control	page 7-101
0x6d2	IMA_RX_GRP9_FIRST_PHY_ADDR	Rx GRP 9 First Link Address	page 7-102
0x6d3	IMA_RX_GRP9_ID	Rx GRP 9 Rx Group ID	page 7-103
0x6d4	IMA_RX_GRP10_CFG	Rx GRP 10 Configuration	page 7-100
0x6d5	IMA_RX_GRP10_CTL	Rx GRP 10 Control	page 7-101
0x6d6	IMA_RX_GRP10_FIRST_PHY_ADDR	Rx GRP 10 First Link Address	page 7-102
0x6d7	IMA_RX_GRP10_ID	Rx GRP 10 Rx Group ID	page 7-103
0x6d8	IMA_RX_GRP11_CFG	Rx GRP 11 Configuration	page 7-100
0x6d9	IMA_RX_GRP11_CTL	Rx GRP 11 Control	page 7-101
0x6da	IMA_RX_GRP11_FIRST_PHY_ADDR	Rx GRP 11 First Link Address	page 7-102
0x6db	IMA_RX_GRP11_ID	Rx GRP 11 Rx Group ID	page 7-103
0x6dc	IMA_RX_GRP12_CFG	Rx GRP 12 Configuration	page 7-100
0x6dd	IMA_RX_GRP12_CTL	Rx GRP 12 Control	page 7-101
0x6de	IMA_RX_GRP12_FIRST_PHY_ADDR	Rx GRP 12 First Link Address	page 7-102
0x6df	IMA_RX_GRP12_ID	Rx GRP 12 Rx Group ID	page 7-103

Table 7-10. IMA Control and Status Registers *(20 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 9–12 Far-End Status			
0x6e0	IMA_RX_GRP9_RX_TEST_PATTERN	Rx GRP 9 Rx Test Pattern	page 7-103
0x6e2	IMA_RX_GRP9_STAT_CTL_CHANGE	Rx GRP 9 SCCI	page 7-104
0x6e3	IMA_RX_GRP9_ACTUAL_GRP_ID	Rx GRP 9 Rx Group ID	page 7-104
0x6e4	IMA_RX_GRP9_STAT_CTL	Rx GRP 9 Status / Control	page 7-105
0x6e5	IMA_RX_GRP9_TIMING_INFO	Rx GRP 9 Timing Control	page 7-106
0x6e6	IMA_RX_GRP9_TEST_CTL	Rx GRP 9 Test Control	page 7-106
0x6e7	IMA_RX_GRP9_TX_TEST_PATTERN	Rx GRP 9 Tx Test Pattern	page 7-107
0x6e8	IMA_RX_GRP10_RX_TEST_PATTERN	Rx GRP 10 Rx Test Pattern	page 7-103
0x6ea	IMA_RX_GRP10_STAT_CTL_CHANGE	Rx GRP 10 SCCI	page 7-104
0x6eb	IMA_RX_GRP10_ACTUAL_GRP_ID	Rx GRP 10 Rx Group ID	page 7-104
0x6ec	IMA_RX_GRP10_STAT_CTL	Rx GRP 10 Status / Control	page 7-105
0x6ed	IMA_RX_GRP10_TIMING_INFO	Rx GRP 10 Timing Control	page 7-106
0x6ee	IMA_RX_GRP10_TEST_CTL	Rx GRP 10 Test Control	page 7-106
0x6ef	IMA_RX_GRP10_TX_TEST_PATTERN	Rx GRP 10 Tx Test Pattern	page 7-107
0x6f0	IMA_RX_GRP11_RX_TEST_PATTERN	Rx GRP 11 Rx Test Pattern	page 7-103
0x6f2	IMA_RX_GRP11_STAT_CTL_CHANGE	Rx GRP 11 SCCI	page 7-104
0x6f3	IMA_RX_GRP11_ACTUAL_GRP_ID	Rx GRP 11 Rx Group ID	page 7-104
0x6f4	IMA_RX_GRP11_STAT_CTL	Rx GRP 11 Status / Control	page 7-105
0x6f5	IMA_RX_GRP11_TIMING_INFO	Rx GRP 11 Timing Control	page 7-106
0x6f6	IMA_RX_GRP11_TEST_CTL	Rx GRP 11 Test Control	page 7-106
0x6f7	IMA_RX_GRP11_TX_TEST_PATTERN	Rx GRP 11 Tx Test Pattern	page 7-107
0x6f8	IMA_RX_GRP12_RX_TEST_PATTERN	Rx GRP 12 Rx Test Pattern	page 7-103
0x6fa	IMA_RX_GRP12_STAT_CTL_CHANGE	Rx GRP 12 SCCI	page 7-104
0x6fb	IMA_RX_GRP12_ACTUAL_GRP_ID	Rx GRP 12 Rx Group ID	page 7-104
0x6fc	IMA_RX_GRP12_STAT_CTL	Rx GRP 12 Status / Control	page 7-105
0x6fd	IMA_RX_GRP12_TIMING_INFO	Rx GRP 12 Timing Control	page 7-106
0x6fe	IMA_RX_GRP12_TEST_CTL	Rx GRP 12 Test Control	page 7-106
0x6ff	IMA_RX_GRP12_TX_TEST_PATTERN	Rx GRP 12 Tx Test Pattern	page 7-107

Table 7-10. IMA Control and Status Registers *(21 of 26)*

Address	Name	Description (Continued)	Page Number
Transmit Groups 13–16 Configuration Tables			
0x720	IMA_TX_GRP13_RX_TEST_PATTERN	Tx GRP 13 Rx Test Pattern	page 7-92
0x721	IMA_TX_GRP13_CTL	Tx GRP 13 Control	page 7-93
0x722	IMA_TX_GRP13_FIRST_PHY_ADDR	Tx GRP 13 First Link Address	page 7-94
0x723	IMA_TX_GRP13_ID	Tx GRP 13 Tx Group ID	page 7-94
0x724	IMA_TX_GRP13_STAT_CTL	Tx GRP 13 Status / Control	page 7-95
0x725	IMA_TX_GRP13_TIMING_INFO	Tx GRP 13 Timing Control	page 7-96
0x726	IMA_TX_GRP13_TEST_CTL	Tx GRP 13 Test Control	page 7-97
0x727	IMA_TX_GRP13_TX_TEST_PATTERN	Tx GRP 13 Tx Test Pattern	page 7-97
0x728	IMA_TX_GRP14_RX_TEST_PATTERN	Tx GRP 14 Rx Test Pattern	page 7-92
0x729	IMA_TX_GRP14_CTL	Tx GRP 14 Control	page 7-93
0x72a	IMA_TX_GRP14_FIRST_PHY_ADDR	Tx GRP 14 First Link Address	page 7-94
0x72b	IMA_TX_GRP14_ID	Tx GRP 14 Tx Group ID	page 7-94
0x72c	IMA_TX_GRP14_STAT_CTL	Tx GRP 14 Status / Control	page 7-95
0x72d	IMA_TX_GRP14_TIMING_INFO	Tx GRP 14 Timing Control	page 7-96
0x72e	IMA_TX_GRP14_TEST_CTL	Tx GRP 14 Test Control	page 7-97
0x72f	IMA_TX_GRP14_TX_TEST_PATTERN	Tx GRP 14 Tx Test Pattern	page 7-97
0x730	IMA_TX_GRP15_RX_TEST_PATTERN	Tx GRP 15 Rx Test Pattern	page 7-92
0x731	IMA_TX_GRP15_CTL	Tx GRP 15 Control	page 7-93
0x732	IMA_TX_GRP15_FIRST_PHY_ADDR	Tx GRP 15 First Link Address	page 7-94
0x733	IMA_TX_GRP15_ID	Tx GRP 15 Tx Group ID	page 7-94
0x734	IMA_TX_GRP15_STAT_CTL	Tx GRP 15 Status / Control	page 7-95
0x735	IMA_TX_GRP15_TIMING_INFO	Tx GRP 15 Timing Control	page 7-96
0x736	IMA_TX_GRP15_TEST_CTL	Tx GRP 15 Test Control	page 7-97
0x737	IMA_TX_GRP15_TX_TEST_PATTERN	Tx GRP 15 Tx Test Pattern	page 7-97
0x738	IMA_TX_GRP16_RX_TEST_PATTERN	Tx GRP 16 Rx Test Pattern	page 7-92
0x739	IMA_TX_GRP16_CTL	Tx GRP 16 Control	page 7-93
0x73a	IMA_TX_GRP16_FIRST_PHY_ADDR	Tx GRP 16 First Link Address	page 7-94
0x73b	IMA_TX_GRP16_ID	Tx GRP 16 Tx Group ID	page 7-94
0x73c	IMA_TX_GRP16_STAT_CTL	Tx GRP 16 Status / Control	page 7-95
0x73d	IMA_TX_GRP16_TIMING_INFO	Tx GRP 16 Timing Control	page 7-96
0x73e	IMA_TX_GRP16_TEST_CTL	Tx GRP 16 Test Control	page 7-97
0x73f	IMA_TX_GRP16_TX_TEST_PATTERN	Tx GRP 16 Tx Test Pattern	page 7-97

Table 7-10. IMA Control and Status Registers *(22 of 26)*

Address	Name	Description (Continued)	Page Number
Group 13-16 TX Cell Counters			
0x740	IMA_TX_GRP13_CELL_COUNT_LSB	Group 13 Transmit Cell Count LSBs	page 7-98
0x741	IMA_TX_GRP13_CELL_COUNT_MSB	Group 13 Transmit Cell Count MSBs	
0x742	IMA_TX_GRP14_CELL_COUNT_LSB	Group 14Transmit Cell Count LSBs	
0x743	IMA_TX_GRP14_CELL_COUNT_MSB	Group 14 Transmit Cell Count MSBs	
0x744	IMA_TX_GRP15_CELL_COUNT_LSB	Group 15 Transmit Cell Count LSBs	
0x745	IMA_TX_GRP15_CELL_COUNT_MSB	Group 15Transmit Cell Count MSBs	
0x746	IMA_TX_GRP16_CELL_COUNT_LSB	Group 16 Transmit Cell Count LSBs	
0x747	IMA_TX_GRP16_CELL_COUNT_MSB	Group 16 Transmit Cell Count MSBs	
Group 13-16 RX Cell Counters			
0x750	IMA_RX_GRP13_CELL_COUNT_LSB	Group 13 Receive Cell Count LSBs	page 7-99
0x751	IMA_RX_GRP13_CELL_COUNT_MSB	Group 13 Receive Cell Count MSBs	
0x752	IMA_RX_GRP14_CELL_COUNT_LSB	Group 14 Receive Cell Count LSBs	
0x753	IMA_RX_GRP14_CELL_COUNT_MSB	Group 14 Receive Cell Count MSBs	
0x754	IMA_RX_GRP15_CELL_COUNT_LSB	Group 15 Receive Cell Count LSBs	
0x755	IMA_RX_GRP15_CELL_COUNT_MSB	Group 15 Receive Cell Count MSBs	
0x756	IMA_RX_GRP16_CELL_COUNT_LSB	Group 16 Receive Cell Count LSBs	
0x757	IMA_RX_GRP16_CELL_COUNT_MSB	Group 16 Receive Cell Count MSBs	

Table 7-10. IMA Control and Status Registers *(23 of 26)*

Address	Name	Description (Continued)	Page Number
Port 24–31 Control and Status			
0x760 0x761 0x762 0x763 0x764 0x765 0x766 0x767	IMA_TX_LNK24_CTL IMA_TX_LNK25_CTL IMA_TX_LNK26_CTL IMA_TX_LNK27_CTL IMA_TX_LNK28_CTL IMA_TX_LNK29_CTL IMA_TX_LNK30_CTL IMA_TX_LNK31_CTL	Tx Link 24 Control Tx Link 25 Control Tx Link 26 Control Tx Link 27 Control Tx Link 28 Control Tx Link 29 Control Tx Link 30 Control Tx Link 31 Control	page 7-109
0x768 0x769 0x76a 0x76b 0x76c 0x76d 0x76e 0x76f	IMA_TX_LNK24_STATE IMA_TX_LNK25_STATE IMA_TX_LNK26_STATE IMA_TX_LNK27_STATE IMA_TX_LNK28_STATE IMA_TX_LNK29_STATE IMA_TX_LNK30_STATE IMA_TX_LNK31_STATE	Tx Link 24 Status Tx Link 25 Status Tx Link 26 Status Tx Link 27 Status Tx Link 28 Status Tx Link 29 Status Tx Link 30 Status Tx Link 31 Status	page 7-110
0x770 0x771 0x772 0x773 0x774 0x775 0x776 0x777	IMA_TX_LNK24_ID IMA_TX_LNK25_ID IMA_TX_LNK26_ID IMA_TX_LNK27_ID IMA_TX_LNK28_ID IMA_TX_LNK29_ID IMA_TX_LNK30_ID IMA_TX_LNK31_ID	Tx Link 24 Assigned LID Tx Link 25 Assigned LID Tx Link 26 Assigned LID Tx Link 27 Assigned LID Tx Link 28 Assigned LID Tx Link 29 Assigned LID Tx Link 30 Assigned LID Tx Link 31 Assigned LID	page 7-111
0x780 0x781 0x782 0x783 0x784 0x785 0x786 0x787	IMA_RX_LNK24_CTL IMA_RX_LNK25_CTL IMA_RX_LNK26_CTL IMA_RX_LNK27_CTL IMA_RX_LNK28_CTL IMA_RX_LNK29_CTL IMA_RX_LNK30_CTL IMA_RX_LNK31_CTL	Rx Link 24 Control Rx Link 25 Control Rx Link 26 Control Rx Link 27 Control Rx Link 28 Control Rx Link 29 Control Rx Link 30 Control Rx Link 31 Control	page 7-112
0x788 0x789 0x78a 0x78b 0x78c 0x78d 0x78e 0x78f	IMA_RX_LNK24_STATE IMA_RX_LNK25_STATE IMA_RX_LNK26_STATE IMA_RX_LNK27_STATE IMA_RX_LNK28_STATE IMA_RX_LNK29_STATE IMA_RX_LNK30_STATE IMA_RX_LNK31_STATE	Rx Link 24 Status Rx Link 25 Status Rx Link 26 Status Rx Link 27 Status Rx Link 28 Status Rx Link 29 Status Rx Link 30 Status Rx Link 31 Status	page 7-113
0x790 0x791 0x792 0x793 0x794 0x795 0x796 0x797	IMA_RX_LNK24_DEFECT IMA_RX_LNK25_DEFECT IMA_RX_LNK26_DEFECT IMA_RX_LNK27_DEFECT IMA_RX_LNK28_DEFECT IMA_RX_LNK29_DEFECT IMA_RX_LNK30_DEFECT IMA_RX_LNK31_DEFECT	Rx Link 24 Defects Rx Link 25 Defects Rx Link 26 Defects Rx Link 27 Defects Rx Link 28 Defects Rx Link 29 Defects Rx Link 30 Defects Rx Link 31 Defects	page 7-114

Table 7-10. IMA Control and Status Registers *(24 of 26)*

Address	Name	Description (Continued)	Page Number
0x798 0x799 0x79a 0x79b 0x79c 0x79d 0x79e 0x79f	IMA_FE_TX_LNK24_CFG IMA_FE_TX_LNK25_CFG IMA_FE_TX_LNK26_CFG IMA_FE_TX_LNK27_CFG IMA_FE_TX_LNK28_CFG IMA_FE_TX_LNK29_CFG IMA_FE_TX_LNK30_CFG IMA_FE_TX_LNK31_CFG	FE Tx Link 24 Link Config FE Tx Link 25 Link Config FE Tx Link 26 Link Config FE Tx Link 27 Link Config FE Tx Link 28 Link Config FE Tx Link 29 Link Config FE Tx Link 30 Link Config FE Tx Link 31 Link Config	page 7-115
0x7a0 0x7a1 0x7a2 0x7a3 0x7a4 0x7a5 0x7a6 0x7a7	IMA_FE_LNK24_STATE IMA_FE_LNK25_STATE IMA_FE_LNK26_STATE IMA_FE_LNK27_STATE IMA_FE_LNK28_STATE IMA_FE_LNK29_STATE IMA_FE_LNK30_STATE IMA_FE_LNK31_STATE	Rx Link 24 FE Status Rx Link 25 FE Status Rx Link 26 FE Status Rx Link 27 FE Status Rx Link 28 FE Status Rx Link 29 FE Status Rx Link 30 FE Status Rx Link 31 FE Status	page 7-116
0x7a8 0x7a9 0x7aa 0x7ab 0x7ac 0x7ad 0x7ae 0x7af	IMA_RX_LNK24_ID IMA_RX_LNK25_ID IMA_RX_LNK26_ID IMA_RX_LNK27_ID IMA_RX_LNK28_ID IMA_RX_LNK29_ID IMA_RX_LNK30_ID IMA_RX_LNK31_ID	Rx Link 24 Assigned LID Rx Link 25 Assigned LID Rx Link 26 Assigned LID Rx Link 27 Assigned LID Rx Link 28 Assigned LID Rx Link 29 Assigned LID Rx Link 30 Assigned LID Rx Link 31 Assigned LID	page 7-117
0x7b0 0x7b1 0x7b2 0x7b3 0x7b4 0x7b5 0x7b6 0x7b7	IMA_RX_LNK24_IV_CNT IMA_RX_LNK25_IV_CNT IMA_RX_LNK26_IV_CNT IMA_RX_LNK27_IV_CNT IMA_RX_LNK28_IV_CNT IMA_RX_LNK29_IV_CNT IMA_RX_LNK30_IV_CNT IMA_RX_LNK31_IV_CNT	Rx Link 24 IV-IMA Counter Rx Link 25 IV-IMA Counter Rx Link 26 IV-IMA Counter Rx Link 27 IV-IMA Counter Rx Link 28 IV-IMA Counter Rx Link 29 IV-IMA Counter Rx Link 30 IV-IMA Counter Rx Link 31 IV-IMA Counter	page 7-118
0x7b8 0x7b9 0x7ba 0x7bb 0x7bc 0x7bd 0x7be 0x7bf	IMA_RX_LNK24_OIF_CNT IMA_RX_LNK25_OIF_CNT IMA_RX_LNK26_OIF_CNT IMA_RX_LNK27_OIF_CNT IMA_RX_LNK28_OIF_CNT IMA_RX_LNK29_OIF_CNT IMA_RX_LNK30_OIF_CNT IMA_RX_LNK31_OIF_CNT	Rx Link 24 OIF-IMA Counter Rx Link 25 OIF-IMA Counter Rx Link 26 OIF-IMA Counter Rx Link 27 OIF-IMA Counter Rx Link 28 OIF-IMA Counter Rx Link 29 OIF-IMA Counter Rx Link 30 OIF-IMA Counter Rx Link 31 OIF-IMA Counter	page 7-119
0x7c0 0x7c1 0x7c2 0x7c3 0x7c4 0x7c5 0x7c6 0x7c7	IMA_FE_TX_LNK24_GRP_ID IMA_FE_TX_LNK25_GRP_ID IMA_FE_TX_LNK26_GRP_ID IMA_FE_TX_LNK27_GRP_ID IMA_FE_TX_LNK28_GRP_ID IMA_FE_TX_LNK29_GRP_ID IMA_FE_TX_LNK30_GRP_ID IMA_FE_TX_LNK31_GRP_ID	Rx Link 24 Captured GRP ID Rx Link 25 Captured GRP ID Rx Link 26 Captured GRP ID Rx Link 27 Captured GRP ID Rx Link 28 Captured GRP ID Rx Link 29 Captured GRP ID Rx Link 30 Captured GRP ID Rx Link 31 Captured GRP ID	page 7-120

Table 7-10. IMA Control and Status Registers *(25 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 13–16 Configuration Tables			
0x7d0	IMA_RX_GRP13_CFG	Rx GRP 13 Configuration	page 7-100
0x7d1	IMA_RX_GRP13_CTL	Rx GRP 13 Control	page 7-101
0x7d2	IMA_RX_GRP13_FIRST_PHY_ADDR	Rx GRP 13 First Link Address	page 7-102
0x7d3	IMA_RX_GRP13_ID	Rx GRP 13 Rx Group ID	page 7-103
0x7d4	IMA_RX_GRP14_CFG	Rx GRP 14 Configuration	page 7-100
0x7d5	IMA_RX_GRP14_CTL	Rx GRP 14 Control	page 7-101
0x7d6	IMA_RX_GRP14_FIRST_PHY_ADDR	Rx GRP 14 First Link Address	page 7-102
0x7d7	IMA_RX_GRP14_ID	Rx GRP 14 Rx Group ID	page 7-103
0x7d8	IMA_RX_GRP15_CFG	Rx GRP 15 Configuration	page 7-100
0x7d9	IMA_RX_GRP15_CTL	Rx GRP 15 Control	page 7-101
0x7da	IMA_RX_GRP15_FIRST_PHY_ADDR	Rx GRP 15 First Link Address	page 7-102
0x7db	IMA_RX_GRP15_ID	Rx GRP 15 Rx Group ID	page 7-103
0x7dc	IMA_RX_GRP16_CFG	Rx GRP 16 Configuration	page 7-100
0x7dd	IMA_RX_GRP16_CTL	Rx GRP 16 Control	page 7-101
0x7de	IMA_RX_GRP16_FIRST_PHY_ADDR	Rx GRP 16 First Link Address	page 7-102
0x7df	IMA_RX_GRP16_ID	Rx GRP 16 Rx Group ID	page 7-103

Table 7-10. IMA Control and Status Registers *(26 of 26)*

Address	Name	Description (Continued)	Page Number
Receive Groups 13–16 Far-End Status			
0x7e0	IMA_RX_GRP13_RX_TEST_PATTERN	Rx GRP 13 Rx Test Pattern	page 7-103
0x7e2	IMA_RX_GRP13_STAT_CTL_CHANGE	Rx GRP 13 SCCI	page 7-104
0x7e3	IMA_RX_GRP13_ACTUAL_GRP_ID	Rx GRP 13 Rx Group ID	page 7-104
0x7e4	IMA_RX_GRP13_STAT_CTL	Rx GRP 13 Status / Control	page 7-105
0x7e5	IMA_RX_GRP13_TIMING_INFO	Rx GRP 13 Timing Control	page 7-106
0x7e6	IMA_RX_GRP13_TEST_CTL	Rx GRP 13 Test Control	page 7-106
0x7e7	IMA_RX_GRP13_TX_TEST_PATTERN	Rx GRP 13 Tx Test Pattern	page 7-107
0x7e8	IMA_RX_GRP14_RX_TEST_PATTERN	Rx GRP 14 Rx Test Pattern	page 7-103
0x7ea	IMA_RX_GRP14_STAT_CTL_CHANGE	Rx GRP 14 SCCI	page 7-104
0x7eb	IMA_RX_GRP14_ACTUAL_GRP_ID	Rx GRP 14 Rx Group ID	page 7-104
0x7ec	IMA_RX_GRP14_STAT_CTL	Rx GRP 14 Status / Control	page 7-105
0x7ed	IMA_RX_GRP14_TIMING_INFO	Rx GRP 14 Timing Control	page 7-106
0x7ee	IMA_RX_GRP14_TEST_CTL	Rx GRP 14 Test Control	page 7-106
0x7ef	IMA_RX_GRP14_TX_TEST_PATTERN	Rx GRP 14 Tx Test Pattern	page 7-107
0x7f0	IMA_RX_GRP15_RX_TEST_PATTERN	Rx GRP 15 Rx Test Pattern	page 7-103
0x7f2	IMA_RX_GRP15_STAT_CTL_CHANGE	Rx GRP 15 SCCI	page 7-104
0x7f3	IMA_RX_GRP15_ACTUAL_GRP_ID	Rx GRP 15 Rx Group ID	page 7-104
0x7f4	IMA_RX_GRP15_STAT_CTL	Rx GRP 15 Status / Control	page 7-105
0x7f5	IMA_RX_GRP15_TIMING_INFO	Rx GRP 15 Timing Control	page 7-106
0x7f6	IMA_RX_GRP15_TEST_CTL	Rx GRP 15 Test Control	page 7-106
0x7f7	IMA_RX_GRP15_TX_TEST_PATTERN	Rx GRP 15 Tx Test Pattern	page 7-107
0x7f8	IMA_RX_GRP16_RX_TEST_PATTERN	Rx GRP 16 Rx Test Pattern	page 7-103
0x7fa	IMA_RX_GRP16_STAT_CTL_CHANGE	Rx GRP 16 SCCI	page 7-104
0x7fb	IMA_RX_GRP16_ACTUAL_GRP_ID	Rx GRP 16 Rx Group ID	page 7-104
0x7fc	IMA_RX_GRP12_STAT_CTL	Rx GRP 16 Status / Control	page 7-105
0x7fd	IMA_RX_GRP16_TIMING_INFO	Rx GRP 16 Timing Control	page 7-106
0x7fe	IMA_RX_GRP16_TEST_CTL	Rx GRP 16 Test Control	page 7-106
0x7ff	IMA_RX_GRP16_TX_TEST_PATTERN	Rx GRP 16 Tx Test Pattern	page 7-107

0x00—SUMINT (Summary Interrupt Indication Status Register)

The SUMINT register indicates the one-second interrupts, external framer interrupts, and port summary interrupts.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	—	—	Reserved, set to a logical 0.
3	—	OneSecInt(1)	When a logical 1 is read, this bit indicates a One Second Interrupt. This interrupt signifies that a rising edge occurred on the OneSecIO pin (pin R5). This interrupt is generated for each rising edge on the OneSecIO pin.
2	0	—	Reserved, set to a logical 0.
1	—	TxCellInt(3)	When a logical 1 is read, this bit indicates a Transmit Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the TxCellInt register (0x2C).
0	—	RxCellInt(3)	When a logical 1 is read, this bit indicates a Receive Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the RxCellInt register (0x2D).

FOOTNOTE:

(1) This bit is cleared when this register is read in any of the eight ports.

(2) Single event—A 1 to 0 transition on the corresponding pin causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

(3) This bit is a summary indication of any interrupt events that occurred in the indicated registers. This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bits in the corresponding interrupt indication registers are read and automatically cleared.

0x01—ENSUMINT (Summary Interrupt Control Register)

The ENSUMINT register controls which of the interrupts listed in the SUMINT register (0x00) appear in the SUMPORT register and on the MicroInt* (pin T1), provided the corresponding ENSUMPORT bit is enabled and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	0	EnOneSecInt	When written to a logical 1, this bit enables the one-second interrupt generated by the OneSecIO pin (pin R5) to appear on the MicroInt* output pin (pin T1).
2	0	—	Reserved, set to a logical 0.
1	0	EnTxCellInt	When written to a logical 1, this bit enables the transmit cell interrupts located in the TxCellInt register (0x2C). These interrupts appear can on the MicroInt* pin (pin T1), provided that EnPortInt in the ENSUMPORT register (0x0201) is enabled for this port and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.
0	0	EnRxCellInt	When written to a logical 1, this bit enables the receive cell interrupts located in the RxCellInt register (0x2D). These interrupts can appear on the MicroInt* pin (pin T1), provided that EnPortInt in the ENSUMPORT register (0x0201) is enabled for this port and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

0x04—PMODE (Port Mode Control Register)

The PMODE register controls the port-level software resets, source loopback, and physical layer interface mode.

Bit	Default	Name	Description
7	0	PrtMstRst	When written to a logical 1, this bit initiates a Port Master Reset. All internal state machines associated with this port are reset and all control registers for this port, except this one, assume their default values. Only bits 0–6 in this register are overwritten with their default values.
6	0	PrtLgcRst	When written to a logical 1, this bit initiates a Port Logic Reset. All internal state machines associated with this port are reset but all registers (0x00–0x3F) listed as "Type: W/R" in Table 7-3 are unaltered. Output signals for this port are three-state during Port Logic Reset.
5	0	SrcLoop(1)	When written to a logical 1, this bit enables a source loopback. The line transmit clock and data outputs are connected to the line receive clock and data inputs. Refer to Figure 2-8. During Source loopback, the device is automatically configured for General Purpose mode (ignoring the contents of the PhyType[2:0] bits).
4	0	FeLnLoop(1)	Enables Far-end line loopback. In this mode, the receive data is processed by the TC block and looped back at the UTOPIA interface to the transmit side. Refer to Figure 2-9.
3	0	—	Reserved, set to a logical 0.
2	0	PhyType[2](1)	These bits determine the Physical Layer Interface Mode: 000—T1 mode 001—E1 mode 010—Reserved 011—Reserved 100—Reserved 101—General Purpose 110—DSL Mode 111—Power Down In General Purpose Mode, the SPRxSync and SPTxSync pins are ignored. (However, good design practice would have them tied high.)
1	0	PhyType[1](1)	
0	0	PhyType[0](1)	

FOOTNOTE:
(1) These bits should only be changed when the device or port logic reset is asserted.

0x05—IOMODE (Input/Output Mode Control Register)

The IOMODE register controls the line interface signal polarities and status outputs.

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	0	RxSyncPol(1)	This bit determines the Receiver Synchronization input Polarity. When written to a logical 1, the active level on the SPRxSync input is high. When written to a logical 0, the active level is low.
5	0	RxClkPol(1)	This bit determines the Receiver Clock Input Polarity. When written to a logical 1, the active edge on the SPRxClk input is the falling edge. When written to a logical 0, the active edge is the rising edge.
4	0	TxSyncPol(1)	This bit determines the Transmitter Synchronization input Polarity. When written to a logical 1, the active level on the SPTxSync input is high. When written to a logical 0, the active level is low.
3	0	TxClkPol(1)	This bit determines the Transmitter Clock Input Polarity. When written to a logical 1, the active edge on the SPTxClk input is the falling edge. When written to a logical 0, the active edge is the rising edge.
2	0	—	Reserved, set to 0.
1	0	—	Reserved, set to 0.
0	0	—	Reserved, set to 0.

FOOTNOTE:

(1) These bits should only be changed when the device or port logic reset is asserted.

0x08—CGEN (Cell Generation Control Register)

The CGEN register controls the device's cell generation functions.

Bit	Default	Name	Description
7	0	DisHEC	When written to a logical 1, this bit disables internal generation of the HEC field. When disabled, the HEC field from the UTOPIA interface remains unchanged in the transmitted cell. When written to a logical 0, HEC is internally calculated and inserted in the transmitted cell.
6	1	EnTxCos	When written to a logical 1, this bit enables the Transmit HEC Coset. When written to a logical 0, the HEC Coset is disabled.
5	1	EnTxCellScr	When written to a logical 1, this bit enables the Transmit Cell Scrambler. When written to a logical 0, the Transmit Cell Scrambler is disabled.
4	0	ErrHEC	When written to a logical 1, this bit causes the ERRPAT register to be XORed with the calculated HEC byte for one transmit cell. These bits are cleared automatically by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register.
3	0	DSLSyncPol	This bit controls the polarity of the sync pulse in DSL mode. Set to 1 for active high and to 0 for active low.
2	0	—	Reserved, write to a logical 0.
1	0	EnTxDSSScr	When written to a logical 1, this bit enables the Transmit DSS Scrambler. When written to a logical 0, the Transmit DSS Scrambler is disabled.
0	0	EnRxDSSScr	When written to a logical 1, this bit enables the Receive DSS Scrambler. When written to a logical 0, the Receive DSS Scrambler is disabled.

0x09—HDRFIELD (Header Field Control Register)

The HDRFIELD register controls the header insertion elements.

Bit	Default	Name	Description
7	0	—	Reserved, write to a logical 0.
6	0	—	Reserved, write to a logical 0.
5	0	—	Reserved, write to a logical 0.
4	0	InsGFC	When written to a logical 1, this bit inserts a Generic Flow Control (GFC) field in the outgoing header from the TXHDR registers. When written to a logical 0, the GFC field is not changed prior to transmission.
3	0	InsVPI	When written to a logical 1, this bit inserts a Virtual Path Identifier (VPI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VPI field is not changed prior to transmission.
2	0	InsVCI	When written to a logical 1, this bit inserts a Virtual Channel Identifier (VCI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VCI field is not changed prior to transmission.
1	0	InsPT	When written to a logical 1, this bit inserts a Payload Type (PT) field in the outgoing header from the TXHDR registers. When written to a logical 0, the PT field is not changed prior to transmission.
0	0	InsCLP	When written to a logical 1, this bit inserts a Cell Loss Priority (CLP) bit in the outgoing header from the TXHDR registers. When written to a logical 0, the CLP field is not changed prior to transmission.

0x0A—IDLPAY (Transmit Idle Cell Payload Control Register)

The IDLPAY register contains the transmit idle cell payload.

Bit	Default	Name	Description
7	0	IdlPay[7]	These bits hold the Transmit Idle Cell Payload values for outgoing idle cells.
6	1	IdlPay[6]	
5	1	IdlPay[5]	
4	0	IdlPay[4]	
3	1	IdlPay[3]	
2	0	IdlPay[2]	
1	1	IdlPay[1]	
0	0	IdlPay[0]	

0x0B—ERRPAT (Error Pattern Control Register)

The ERRPAT register provides the error pattern for the HEC error insertion function. ErrHEC (bit 4) in the CGEN register (0x08) enables this function. Each bit in the error pattern register is XORed with the corresponding bit of the calculated HEC byte to be errored.

Bit	Default	Name	Description
7	0	ErrPat[7]	Error pattern bit 7.
6	0	ErrPat[6]	Error pattern bit 6.
5	0	ErrPat[5]	Error pattern bit 5.
4	0	ErrPat[4]	Error pattern bit 4.
3	0	ErrPat[3]	Error pattern bit 3.
2	0	ErrPat[2]	Error pattern bit 2.
1	0	ErrPat[1]	Error pattern bit 1.
0	0	ErrPat[0]	Error pattern bit 0.

0x0C—CVAL (Cell Validation Control Register)

The CVAL register controls the validation of incoming cells.

Bit	Default	Name	Description
7	0	RejHdr	When written to a logical 1, this bit enables the Rejection of certain Header cells. When enabled, cells with headers matching the RXHDRx/RXMSKx definition are rejected and all others are accepted. When written to a logical 0, cells with matching headers are accepted and cells with non-matching headers are rejected.
6	1	DelIdle	When written to a logical 1, this bit enables the Deletion of Idle Cells. When enabled, cells matching the RXIDL/IDLMSK definition are deleted from the received cell stream. When written to a logical 0, idle cells are included in the received stream.
5	1	EnRxCos	When written to a logical 1, this bit enables the Receive HEC Coset. When written to a logical 0, the HEC Coset is disabled.
4	1	EnRxCellScr	When written to a logical 1, this bit enables the Receive Cell Scrambler. When written to a logical 0, the Receive Cell Scrambler is disabled.
3	0	EnHECCorr	When written to a logical 1, this bit enables HEC Correction. When written to a logical 0, HEC Correction is disabled.
2	0	DisHECChk	When written to a logical 1, this bit disables HEC Checking. When written to a logical 0, HEC checking is performed as a cell validation criterion. See Table 5-1.
1	0	DisCellRcvr	When written to a logical 1, this bit disables the Cell Receiver. When disabled, all cell reception is disabled on the next cell boundary. When written to a logical 0, cell reception begins or resumes on the next cell boundary.
0	0	DisLOCD	When written to a logical 1, this bit disables Loss of Cell Delineation. When disabled, cells are passed even if cell delineation has not been found. When written to a logical 0, cells are passed only while cell alignment has been achieved. See Table 5-1.

0x0D—UTOP1 (UTOPIA Control Register 1)

The UTOP1 register controls the UTOPIA resets, parity orientation, and the transmit FIFO fill-level threshold.

Bit	Default	Name	Description
7	0	TxReset	When written to a logical 1, this bit resets the transmit FIFO pointers. This reset should only be used as a test function because it can create short cells.
6	0	RxReset	When written to a logical 1, this bit resets the receive FIFO pointers. This reset should only be used as a test function because it can create short cells.
5	0	—	Reserved, write to a logical 0.
4	0	—	Reserved, write to a logical 0.
3	0	—	Reserved, write to a logical 0.
2	0	—	Reserved, write to a logical 0.
1	0	—	Reserved, write to a logical 0.
0	0	—	Reserved, write to a logical 0.

FOOTNOTE:
(1) These bits should only be changed when the device or port logic reset is asserted.

0x0E—UTOP2 (UTOPIA Control Register 2) (TC Block)

The UTOP2 register contains the multi-PHY address value for the port.

Bit	Default	Name	Description
7	0	—	Reserved, write to a logical 0.
6	0	—	Reserved, write to a logical 0.
5	x	UtopDis(1)	When written to a logical 1, this bit disables UTOPIA outputs for this port. **Version** / **Default** CX28229-11 / 0 CX28229-12 and later / 1
4	0	MphyAddr[4]—MSB(1)	These bits are the Multi-PHY Device Address. Each CX2822x port should have a unique address. These bits correspond to the URxAddr and UTxAddr pins. When the pin matches the bit values, the port is accessed. This port ignores any transactions meant for another port or PHY device.
3	0	MphyAddr[3](1)	
2	(2)	MphyAddr[2](1)	
1	(2)	MphyAddr[1](1)	
0	(2)	MphyAddr[0]—LSB(1)	

FOOTNOTE:
(1) These bits should only be changed when the device or port logic reset is asserted.
(2) The default for these bits is the port number for each port. (000—Port 0, 001—Port 1, 010—Port 2, 011—Port 3, 100—Port 4, 101—Port 5, 110—Port 6, 111—Port 7)

0x0F—UDF2 (UDF2 Control Register)

The contents of the UDF2 register are inserted into the UDF2 byte on the UTOPIA receive bus when operating in 16-bit UTOPIA mode.

Bit	Default	Name	Description
7	0	UDF2[7]	The contents of this register are output over the UTOPIA receive bus when operating in UTOPIA 16-bit mode. The default matches the port address.
6	0	UDF2[6]	
5	0	UDF2[5]	
4	0	UDF2[4]	
3	0	UDF2[3]	
2	(1)	UDF2[2]	
1	(1)	UDF2[1]	
0	(1)	UDF2[0]	

FOOTNOTE:

(1) The default for these bits is the port number for each port. (000—Port 0, 001—Port 1, 010—Port 2, 011—Port 3, 100—Port 4, 101—Port 5, 110—Port 6, 111—Port 7)

0x10—TXHDR1 (Transmit Cell Header Control Register 1)

The TXHDR1 register contains the first byte of the Transmit Cell Header. It controls the header value that is inserted in the transmitted cell. This header consists of 32 bits divided among four registers (TXHDR1–4).

Bit	Default	Name	Description
7	0	TxHdr1[7]	These bits hold the Transmit Header values for Octet 1 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). GFC/VPI bits (for UNI they are GFC bits, for NNI they are VPI bits)
6	0	TxHdr1[6]	
5	0	TxHdr1[5]	
4	0	TxHdr1[4]	
3	0	TxHdr1[3]	VPI bits
2	0	TxHdr1[2]	
1	0	TxHdr1[1]	
0	0	TxHdr1[0]	

0x11—TXHDR2 (Transmit Cell Header Control Register 2)

The TXHDR2 register contains the second byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

Bit	Default	Name	Description
7	0	TxHdr2[7]	These bits hold the Transmit Header values for Octet 2 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). VPI bits
6	0	TxHdr2[6]	
5	0	TxHdr2[5]	
4	0	TxHdr2[4]	
3	0	TxHdr2[3]	VCI bits
2	0	TxHdr2[2]	
1	0	TxHdr2[1]	
0	0	TxHdr2[0]	

0x12—TXHDR3 (Transmit Cell Header Control Register 3)

The TXHDR3 register contains the third byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

Bit	Default	Name	Description
7	0	TxHdr3[7]	These bits hold the Transmit Header values for Octet 3 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09). VCI bits
6	0	TxHdr3[6]	
5	0	TxHdr3[5]	
4	0	TxHdr3[4]	
3	0	TxHdr3[3]	
2	0	TxHdr3[2]	
1	0	TxHdr3[1]	
0	0	TxHdr3[0]	

0x13—TXHDR4 (Transmit Cell Header Control Register 4)

The TXHDR4 register contains the fourth byte of the Transmit Cell Header. (See 0x10—TXHDR1.)

Bit	Default	Name	Description
7	0	TxHdr4[7]	These bits hold the Transmit Header values for Octet 4 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09).
6	0	TxHdr4[6]	
5	0	TxHdr4[5]	VCI bits
4	0	TxHdr4[4]	
3	0	TxHdr4[3]	Payload-type bits
2	0	TxHdr4[2]	
1	0	TxHdr4[1]	
0	0	TxHdr4[0]	Cell Loss Priority bit

0x14—TXIDL1 (Transmit Idle Cell Header Control Register 1)

The TXIDL1 register contains the first byte of the Transmit Idle Cell Header. It controls the header value that is inserted in the transmitted idle cells. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	TxIdl1[7]	These bits hold the Transmit Idle Cell Header values for Octet 1 of the outgoing cell.
6	0	TxIdl1[6]	
5	0	TxIdl1[5]	GFC/VPI bits (for UNI they are GFC bits, for NNI the are VPI bits)
4	0	TxIdl1[4]	
3	0	TxIdl1[3]	VPI bits
2	0	TxIdl1[2]	
1	0	TxIdl1[1]	
0	0	TxIdl1[0]	

0x15—TXIDL2 (Transmit Idle Cell Header Control Register 2)

The TXIDL2 register contains the second byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

Bit	Default	Name	Description
7	0	TxIdl2[7]	These bits hold the Transmit Idle Cell Header values for Octet 2 of the outgoing cell.
6	0	TxIdl2[6]	
5	0	TxIdl2[5]	VPI bits
4	0	TxIdl2[4]	
3	0	TxIdl2[3]	
2	0	TxIdl2[2]	VCI bits
1	0	TxIdl2[1]	
0	0	TxIdl2[0]	

0x16—TXIDL3 (Transmit Idle Cell Header Control Register 3)

The TXIDL3 register contains the third byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

Bit	Default	Name	Description
7	0	TxIdl3[7]	These bits hold the Transmit Idle Cell Header values for Octet 3 of the outgoing cell.
6	0	TxIdl3[6]	
5	0	TxIdl3[5]	
4	0	TxIdl3[4]	
3	0	TxIdl3[3]	
2	0	TxIdl3[2]	VCI bits
1	0	TxIdl3[1]	
0	0	TxIdl3[0]	

0x17—TXIDL4 (Transmit Idle Cell Header Control Register 4)

The TXIDL4 register contains the fourth byte of the Transmit Idle Cell Header. (See 0x14—TXIDL1.)

Bit	Default	Name	Description
7	0	TxIdl4[7]	These bits hold the Transmit Idle Cell Header values for Octet 4 of the outgoing cell.
6	0	TxIdl4[6]	
5	0	TxIdl4[5]	VCI bits
4	0	TxIdl4[4]	
3	0	TxIdl4[3]	
2	0	TxIdl4[2]	Payload-type bits
1	0	TxIdl4[1]	
0	1	TxIdl4[0]	Cell Loss Priority bit

0x18—RXHDR1 (Receive Cell Header Control Register 1)

The RXHDR1 register contains the first byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port if an incoming ATM cell header matches the value in the header register. Receive Header Mask Registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxHdr1[7]	These bits hold the Receive Header values for Octet 1 of the incoming cell.
6	0	RxHdr1[6]	
5	0	RxHdr1[5]	
4	0	RxHdr1[4]	
3	0	RxHdr1[3]	
2	0	RxHdr1[2]	
1	0	RxHdr1[1]	
0	0	RxHdr1[0]	

0x19—RXHDR2 (Receive Cell Header Control Register 2)

The RXHDR2 register contains the second byte of the Receive Cell Header. (See 0x18—RXHDR1.)

Bit	Default	Name	Description
7	0	RxHdr2[7]	These bits hold the Receive Header values for Octet 2 of the incoming cell.
6	0	RxHdr2[6]	
5	0	RxHdr2[5]	
4	0	RxHdr2[4]	
3	0	RxHdr2[3]	
2	0	RxHdr2[2]	
1	0	RxHdr2[1]	
0	0	RxHdr2[0]	

0x1A—RXHDR3 (Receive Cell Header Control Register 3)

The RXHDR3 register contains the third byte of the Receive Cell Header. (See 0x18—RXHDR1.)

Bit	Default	Name	Description
7	0	RxHdr3[7]	These bits hold the Receive Header values for Octet 3 of the incoming cell.
6	0	RxHdr3[6]	
5	0	RxHdr3[5]	
4	0	RxHdr3[4]	
3	0	RxHdr3[3]	
2	0	RxHdr3[2]	
1	0	RxHdr3[1]	
0	0	RxHdr3[0]	

0x1B—RXHDR4 (Receive Cell Header Control Register 4)

The RXHDR4 register contains the fourth byte of the Receive Cell Header. (See 0x18—RXHDR1.)

Bit	Default	Name	Description
7	0	RxHdr4[7]	These bits hold the Receive Header values for Octet 4 of the incoming cell.
6	0	RxHdr4[6]	
5	0	RxHdr4[5]	
4	0	RxHdr4[4]	
3	0	RxHdr4[3]	
2	0	RxHdr4[2]	
1	0	RxHdr4[1]	
0	0	RxHdr4[0]	

0x1C—RXMSK1 (Receive Cell Mask Control Register 1)

The RXMSK1 register contains the first byte of the Receive Cell Mask. It modifies ATM cell screening, which compares the Receive Cell Header Registers to the incoming cells. Setting a bit in the Mask Register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1 bit 0 to 1 causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	1	RxMsk1[7]	These bits hold the Receive Header Mask for Octet 1 of the incoming cell.
6	1	RxMsk1[6]	
5	1	RxMsk1[5]	
4	1	RxMsk1[4]	
3	1	RxMsk1[3]	
2	1	RxMsk1[2]	
1	1	RxMsk1[1]	
0	1	RxMsk1[0]	

0x1D—RXMSK2 (Receive Cell Mask Control Register 2)

The RXMSK2 register contains the second byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

Bit	Default	Name	Description
7	1	RxMsk2[7]	These bits hold the Receive Header Mask for Octet 2 of the incoming cell.
6	1	RxMsk2[6]	
5	1	RxMsk2[5]	
4	1	RxMsk2[4]	
3	1	RxMsk2[3]	
2	1	RxMsk2[2]	
1	1	RxMsk2[1]	
0	1	RxMsk2[0]	

0x1E—RXMSK3 (Receive Cell Mask Control Register 3)

The RXMSK3 register contains the third byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

Bit	Default	Name	Description
7	1	RxMsk3[7]	These bits hold the Receive Header Mask for Octet 3 of the incoming cell.
6	1	RxMsk3[6]	
5	1	RxMsk3[5]	
4	1	RxMsk3[4]	
3	1	RxMsk3[3]	
2	1	RxMsk3[2]	
1	1	RxMsk3[1]	
0	1	RxMsk3[0]	

0x1F—RXMSK4 (Receive Cell Mask Control Register 4)

The RXMSK4 register contains the fourth byte of the Receive Cell Mask. (See 0x1D—RXMSK1.)

Bit	Default	Name	Description
7	1	RxMsk4[7]	These bits hold the Receive Header Mask for Octet 4 of the incoming cell.
6	1	RxMsk4[6]	
5	1	RxMsk4[5]	
4	1	RxMsk4[4]	
3	1	RxMsk4[3]	
2	1	RxMsk4[2]	
1	1	RxMsk4[1]	
0	1	RxMsk4[0]	

0x20—RXIDL1 (Receive Idle Cell Header Control Register 1)

The RXIDL1 register contains the first byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are discarded from the received stream if register CVAL (0x0C) bit 6 is set to 1. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	RxIdl1[7]	These bits hold the Receive Idle cell header for Octet 1 of the incoming cell.
6	0	RxIdl1[6]	
5	0	RxIdl1[5]	
4	0	RxIdl1[4]	
3	0	RxIdl1[3]	
2	0	RxIdl1[2]	
1	0	RxIdl1[1]	
0	0	RxIdl1[0]	

0x21—RXIDL2 (Receive Idle Cell Header Control Register 2)

The RXIDL2 register contains the second byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

Bit	Default	Name	Description
7	0	RxIdl2[7]	These bits hold the Receive Idle cell header for Octet 2 of the incoming cell.
6	0	RxIdl2[6]	
5	0	RxIdl2[5]	
4	0	RxIdl2[4]	
3	0	RxIdl2[3]	
2	0	RxIdl2[2]	
1	0	RxIdl2[1]	
0	0	RxIdl2[0]	

0x22—RXIDL3 (Receive Idle Cell Header Control Register 3)

The RXIDL3 register contains the third byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

Bit	Default	Name	Description
7	0	RxIdl3[7]	These bits hold the Receive Idle cell header for Octet 3 of the incoming cell.
6	0	RxIdl3[6]	
5	0	RxIdl3[5]	
4	0	RxIdl3[4]	
3	0	RxIdl3[3]	
2	0	RxIdl3[2]	
1	0	RxIdl3[1]	
0	0	RxIdl3[0]	

0x23—RXIDL4 (Receive Idle Cell Header Control Register 4)

The RXIDL4 register contains the fourth byte of the Receive Idle Cell Header. (See 0x20—RXIDL1.)

Bit	Default	Name	Description
7	0	RxIdl4[7]	These bits hold the Receive Idle cell header for Octet 4 of the incoming cell.
6	0	RxIdl4[6]	
5	0	RxIdl4[5]	
4	0	RxIdl4[4]	
3	0	RxIdl4[3]	
2	0	RxIdl4[2]	
1	0	RxIdl4[1]	
0	1	RxIdl4[0]	

0x24—IDLMSK1 (Receive Idle Cell Mask Control Register 1)

The IDLMSK1 register contains the first byte of the Receive Idle Cell Mask. It modifies ATM cell screening, which compares the Receive Idle Cell Header Registers to the incoming cells. Setting a bit in the Mask Register causes the corresponding bit in the received ATM idle cell header to be disregarded for screening. For example, setting IDLMSK1 bit 0 to 1 causes cells to be accepted as ATM idle cells with either 1 or 0 in the octet 1, bit 0 position. This header consists of 32 bits divided among four registers.

Bit	Default	Name	Description
7	0	IdlMsk1[7]	These bits hold the Receive Idle cell header mask for Octet 1 of the incoming cell.
6	0	IdlMsk1[6]	
5	0	IdlMsk1[5]	
4	0	IdlMsk1[4]	
3	0	IdlMsk1[3]	
2	0	IdlMsk1[2]	
1	0	IdlMsk1[1]	
0	0	IdlMsk1[0]	

0x25—IDLMSK2 (Receive Idle Cell Mask Control Register 2)

The IDLMSK2 register contains the second byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

Bit	Default	Name	Description
7	0	IdlMsk2[7]	These bits hold the Receive Idle cell header mask for Octet 2 of the incoming cell.
6	0	IdlMsk2[6]	
5	0	IdlMsk2[5]	
4	0	IdlMsk2[4]	
3	0	IdlMsk2[3]	
2	0	IdlMsk2[2]	
1	0	IdlMsk2[1]	
0	0	IdlMsk2[0]	

0x26—IDLMSK3 (Receive Idle Cell Mask Control Register 3)

The IDLMSK3 register contains the third byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

Bit	Default	Name	Description
7	0	IdlMsk3[7]	These bits hold the Receive Idle cell header mask for Octet 3 of the incoming cell.
6	0	IdlMsk3[6]	
5	0	IdlMsk3[5]	
4	0	IdlMsk3[4]	
3	0	IdlMsk3[3]	
2	0	IdlMsk3[2]	
1	0	IdlMsk3[1]	
0	0	IdlMsk3[0]	

0x27—IDLMSK4 (Receive Idle Cell Mask Control Register 4)

The IDLMSK4 register contains the fourth byte of the Receive Idle Cell Mask. (See 0x24—RXMSKL1.)

Bit	Default	Name	Description
7	0	IdlMsk4[7]	These bits hold the Receive Idle cell header mask for Octet 4 of the incoming cell.
6	0	IdlMsk4[6]	
5	0	IdlMsk4[5]	
4	0	IdlMsk4[4]	
3	0	IdlMsk4[3]	
2	0	IdlMsk4[2]	
1	0	IdlMsk4[1]	
0	0	IdlMsk4[0]	

0x28—ENCELLT (Transmit Cell Interrupt Control Register)

The ENCELLT register controls which of the interrupts listed in the TxCellInt register (0x2C) appear on the MicroInt* pin (pin T1), provided that both EnTxCellInt (bit 1) in the ENSUMINT register (0x01) and EnPortInt in the ENSUMPORT register (0x0201) for this port are enabled, and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

Bit	Default	Name	Description
7	1	EnParErrInt	When written to a logical 1, this bit enables the Parity Error Interrupt.
6	1	EnSOCErrInt	When written to a logical 1, this bit enables the Start of Cell Error Interrupt.
5	1	EnTxOvflInt	When written to a logical 1, this bit enables the Transmit FIFO Overflow Interrupt.
4	1	EnRxOvflInt	When written to a logical 1, this bit enables the Receive FIFO Overflow Interrupt.
3	1	EnCellSentInt	When written to a logical 1, this bit enables the Cell Sent Interrupt.
2	1	—	Reserved for factory test, ignore.
1	0	—	Reserved, set to a logical 0.
0	0	—	Reserved, set to a logical 0.

0x29—ENCELLR (Receive Cell Interrupt Control Register)

The ENCELLR register controls which of the interrupts listed in the RxCellInt register (0x2D) appear on the MicroInt* pin (pin T1), provided that both EnRxCellInt (bit 0) in the ENSUMINT register (0x01) and EnPortInt in the ENSUMPORT register (0x0201) for this port are enabled, and EnIntPin (bit 3) in the MODE register (0x0202) is enabled.

Bit	Default	Name	Description
7	1	EnLOCDInt	When written to a logical 1, this bit enables a Loss of Cell Delineation Interrupt.
6	1	EnHECDetInt	When written to a logical 1, this bit enables a HEC Error Detected Interrupt.
5	1	EnHECCorrInt	When written to a logical 1, this bit enables a HEC Error Corrected Interrupt.
4	0	—	Reserved, write to a logical 0.
3	1	EnCellRcvdInt	When written to a logical 1, this bit enables a Cell Received Interrupt.
2	1	EnIdleRcvdInt	When written to a logical 1, this bit enables an Idle Cell Received Interrupt.
1	1	EnNonMatchInt	When written to a logical 1, this bit enables a Non-matching Cell Received Interrupt.
0	1	EnNonZerGFCInt	When written to a logical 1, this bit enables a Non-zero GFC Received Interrupt.

0x2C—TXCELLINT (Transmit Cell Interrupt Indication Status Register)

The TXCELLINT register indicates that a change of status has occurred within the transmit status signals.

Bit	Default	Name	Description
7	—	ParErrInt(1)	When a logical 1 is read, this bit indicates that a Parity Error occurred.
6	—	SOCErrInt(1)	When a logical 1 is read, this bit indicates that a Start of Cell Error occurred.
5	—	TxOvflInt(1)	When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow occurred.
4	—	RxOvflInt(1)	When a logical 1 is read, this bit indicates that a Receive FIFO Overflow occurred.
3	—	CellSentInt(1)	When a logical 1 is read, this bit indicates that a cell has been sent.
2	—	—	Reserved for factory test, ignore.
1	0	—	Reserved, set to a logical 0.
0	0	—	Reserved, write to a logical 0.

FOOTNOTE:

(1) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

0x2D—RXCELLINT (Receive Cell Interrupt Indication Status Register)

The RXCELLINT register indicates that a change of status has occurred within the receive status signals.

Bit	Default	Name	Description
7	—	LOCDInt(1)	When a logical 1 is read, this bit indicates that a Loss of Cell Delineation has occurred.
6	—	HECDetInt(2)	When a logical 1 is read, this bit indicates that a HEC Error was detected.
5	—	HECCorrInt(2)	When a logical 1 is read, this bit indicates that a HEC Error was corrected.
4	—	—	Reserved, write to a logical 0.
3	—	CellRcvdInt(2)	When a logical 1 is read, this bit indicates that a cell has been received.
2	—	IdleRcvdInt(2)	When a logical 1 is read, this bit indicates that an Idle Cell has been received.
1	—	NonMatchInt(2)	When a logical 1 is read, this bit indicates that a Non-matching Cell has been received.
0	—	NonZerGFCInt(2)	When a logic 1 is read, this bit indicates that a Non-zero GFC has been received.

FOOTNOTE:

(1) Dual event—Either a 0 to 1 or a 1 to 0 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

(2) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

0x2E—TXCELL (Transmit Cell Status Register)

The TXCELL register contains status for the cell transmitter. This register is cleared on read.

Bit	Default	Name	Description
7	—	ParErr(1)	When a logical 1 is read, this bit indicates that a parity error was received on the transmit UTOPIA input data octet.
6	—	SOCErr(1)	When a logical 1 is read, this bit indicates that a Start of Cell Error was received on the UTxSOC pin (pin W12).
5	—	TxOvfl(1)	When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow condition occurred in the transmit UTOPIA FIFO.
4	—	RxOvfl(1)	When a logical 1 is read, this bit indicates that a Receive FIFO Overflow condition occurred in the receive UTOPIA FIFO.
3	—	CellSent(1)	When a logical 1 is read, this bit indicates that a non-idle cell was formatted and transmitted.
2	—	—	Reserved for factory test, ignore.
1	0	—	Reserved, set to a logical 0.
0	0	—	Reserved, set to a logical 0.

FOOTNOTE:
(1) This status indicates an event that occurred since the register was last read.

0x2F—RXCELL (Receive Cell Status Register)

The RXCELL register contains status for the cell receiver. This register is cleared on read.

Bit	Default	Name	Description
7	—	LOCD(1)	When a logical 1 is read, this bit indicates a Loss of Cell Delineation.
6	—	HECDet(2)	When a logical 1 is read, this bit indicates that an uncorrected HEC Error was detected.
5	—	HECCorr(2)	When a logical 1 is read, this bit indicates that a HEC Error was corrected.
4	—	—	Reserved, ignore this bit.
3	—	CellRcvd	When logical 1 is read, this bit indicates that a valid cell was received.
2	—	IdleRcvd(2)	When a logical 1 is read, this bit indicates that a cell with a header matching the receive idle cell header value and mask criteria was received.
1	—	NonMatch(2)	When a logical 1 is read, this bit indicates that a cell has been rejected by the cell screening function.
0	—	NonZerGFC(2)	When a logical 1 is read, this bit indicates that a cell with a Non-zero GFC field in the header was received.

FOOTNOTE:
(1) This status reflects the current state of the circuit.
(2) This status indicates an event that occurred since the register was last read.

0x30—IDLCNTL (Idle Cell Receive Counter [Low Byte])

The IDLCNTL counter tracks the number of received idle cells. This byte of the counter should be read first. The counter is cleared on read.

Bit	Default	Name	Description
7	—	IdleCnt[7]	Received cell counter bit 7.
6	—	IdleCnt[6]	Received cell counter bit 6.
5	—	IdleCnt[5]	Received cell counter bit 5.
4	—	IdleCnt[4]	Received cell counter bit 4.
3	—	IdleCnt[3]	Received cell counter bit 3.
2	—	IdleCnt[2]	Received cell counter bit 2.
1	—	IdleCnt[1]	Received cell counter bit 1.
0	—	IdleCnt[0]	Received cell counter bit 0 (LSB).

0x31—IDLCNTM (Idle Cell Receive Counter [Mid Byte])

The IDLCNTM counter tracks the number of received cells. The counter is cleared on read.

Bit	Default	Name	Description
7	—	IdleCnt[15]	Received cell counter bit 15.
6	—	IdleCnt[14]	Received cell counter bit 14.
5	—	IdleCnt[13]	Received cell counter bit 13.
4	—	IdleCnt[12]	Received cell counter bit 12.
3	—	IdleCnt[11]	Received cell counter bit 11.
2	—	IdleCnt[10]	Received cell counter bit 10.
1	—	IdleCnt[9]	Received cell counter bit 9.
0	—	IdleCnt[8]	Received cell counter bit 8.

0x32—IDLCNTH (Idle Cell Receive Counter [High Byte])

The IDLCNTH counter tracks the number of received cells. The counter is cleared on read.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	0	—	Reserved, set to a logical 0.
2	—	IdleCnt[18]	Received cell counter bit 18 (MSB).
1	—	IdleCnt[17]	Received cell counter bit 17.
0	—	IdleCnt[16]	Received cell counter bit 16.

0x33—LOCDCNT (LOCD Event Counter)

This counter tracks the number of times that cell delineation was lost. Note that the LOCD interrupt is a dual event interrupt and is set when cell delineation is lost or regained. Thus the number of LOCD events will not match the number of LOCD interrupts.

Bit	Default	Name	Description
7	—	LOCDCnt[7]	LOCD Event counter bit 7 (MSB).
6	—	LOCDCnt[6]	LOCD Event counter bit 6.
5	—	LOCDCnt[5]	LOCD Event counter bit 5.
4	—	LOCDCnt[4]	LOCD Event counter bit 4.
3	—	LOCDCnt[3]	LOCD Event counter bit 3.
2	—	LOCDCnt[2]	LOCD Event counter bit 2.
1	—	LOCDCnt[1]	LOCD Event counter bit 1.
0	—	LOCDCnt[0]	LOCD Event counter bit 0 (LSB).

0x34—TXCNTL (Transmitted Cell Counter [Low Byte])

The TXCNTL counter tracks the number of transmitted cells. This byte of the counter should be read first. The counter is cleared on read.

Bit	Default	Name	Description
7	—	TxCnt[7]	Transmitted cell counter bit 7.
6	—	TxCnt[6]	Transmitted cell counter bit 6.
5	—	TxCnt[5]	Transmitted cell counter bit 5.
4	—	TxCnt[4]	Transmitted cell counter bit 4.
3	—	TxCnt[3]	Transmitted cell counter bit 3.
2	—	TxCnt[2]	Transmitted cell counter bit 2.
1	—	TxCnt[1]	Transmitted cell counter bit 1.
0	—	TxCnt[0]	Transmitted cell counter bit 0 (LSB).

0x35—TXCNTM (Transmitted Cell Counter [Mid Byte])

The TXCNTM counter tracks the number of transmitted cells. The counter is cleared on read.

Bit	Default	Name	Description
7	—	TxCnt[15]	Transmitted cell counter bit 15.
6	—	TxCnt[14]	Transmitted cell counter bit 14.
5	—	TxCnt[13]	Transmitted cell counter bit 13.
4	—	TxCnt[12]	Transmitted cell counter bit 12.
3	—	TxCnt[11]	Transmitted cell counter bit 11.
2	—	TxCnt[10]	Transmitted cell counter bit 10.
1	—	TxCnt[9]	Transmitted cell counter bit 9.
0	—	TxCnt[8]	Transmitted cell counter bit 8.

0x36—TXCNTH (Transmitted Cell Counter [High Byte])

The TXCNTH counter tracks the number of transmitted cells. The counter is cleared on read.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	0	—	Reserved, set to a logical 0.
2	—	TxCnt[18]	Transmitted cell counter bit 18 (MSB).
1	—	TxCnt[17]	Transmitted cell counter bit 17.
0	—	TxCnt[16]	Transmitted cell counter bit 16.

0x37—CORRCNT (Corrected HEC Error Counter)

The CORRCNT counter tracks the number of corrected HEC errors. The counter is cleared on read.

Bit	Default	Name	Description
7	—	CorrCnt[7]	Corrected HEC Error counter bit 7 (MSB).
6	—	CorrCnt[6]	Corrected HEC Error counter bit 6.
5	—	CorrCnt[5]	Corrected HEC Error counter bit 5.
4	—	CorrCnt[4]	Corrected HEC Error counter bit 4.
3	—	CorrCnt[3]	Corrected HEC Error counter bit 3.
2	—	CorrCnt[2]	Corrected HEC Error counter bit 2.
1	—	CorrCnt[1]	Corrected HEC Error counter bit 1.
0	—	CorrCnt[0]	Corrected HEC Error counter bit 0 (LSB).

0x38—RXCNTL (Received Cell Counter [Low Byte])

The RXCNTL counter tracks the number of received cells. This byte of the counter should be read first. The counter is cleared on read.

Bit	Default	Name	Description
7	—	RxCnt[7]	Received cell counter bit 7.
6	—	RxCnt[6]	Received cell counter bit 6.
5	—	RxCnt[5]	Received cell counter bit 5.
4	—	RxCnt[4]	Received cell counter bit 4.
3	—	RxCnt[3]	Received cell counter bit 3.
2	—	RxCnt[2]	Received cell counter bit 2.
1	—	RxCnt[1]	Received cell counter bit 1.
0	—	RxCnt[0]	Received cell counter bit 0 (LSB).

0x39—RXCNTM (Received Cell Counter [Mid Byte])

The RXCNTM register tracks the number of received cells. The counter is cleared on read.

Bit	Default	Name	Description
7	—	RxCnt[15]	Received cell counter bit 15.
6	—	RxCnt[14]	Received cell counter bit 14.
5	—	RxCnt[13]	Received cell counter bit 13.
4	—	RxCnt[12]	Received cell counter bit 12.
3	—	RxCnt[11]	Received cell counter bit 11.
2	—	RxCnt[10]	Received cell counter bit 10.
1	—	RxCnt[9]	Received cell counter bit 9.
0	—	RxCnt[8]	Received cell counter bit 8.

0x3A—RXCNTH (Received Cell Counter [High Byte])

The RXCNTH counter tracks the number of received cells. The counter is cleared on read.

Bit	Default	Name	Description
7	0	—	Reserved, set to a logical 0.
6	0	—	Reserved, set to a logical 0.
5	0	—	Reserved, set to a logical 0.
4	0	—	Reserved, set to a logical 0.
3	0	—	Reserved, set to a logical 0.
2	—	RxCnt[18]	Received cell counter bit 18 (MSB).
1	—	RxCnt[17]	Received cell counter bit 17.
0	—	RxCnt[16]	Received cell counter bit 16.

0x3B—UNCCNT (Uncorrected HEC Error Counter)

The UNCCNT counter tracks the number of uncorrected HEC errors. The counter is cleared on read.

Bit	Default	Name	Description
7	—	UncCnt[7]	Uncorrected HEC Error counter bit 7 (MSB).
6	—	UncCnt[6]	Uncorrected HEC Error counter bit 6.
5	—	UncCnt[5]	Uncorrected HEC Error counter bit 5.
4	—	UncCnt[4]	Uncorrected HEC Error counter bit 4.
3	—	UncCnt[3]	Uncorrected HEC Error counter bit 3.
2	—	UncCnt[2]	Uncorrected HEC Error counter bit 2.
1	—	UncCnt[1]	Uncorrected HEC Error counter bit 1.
0	—	UncCnt[0]	Uncorrected HEC Error counter bit 0 (LSB).

0x3C—NONCNTL (Non-matching Cell Counter [Low Byte])

The NONCNTL counter tracks the number of non-matching cells. This byte of the counter should be read first. The counter is cleared on read.

Bit	Default	Name	Description
7	—	NonCnt[7]	Non-matching cell counter bit 7.
6	—	NonCnt[6]	Non-matching cell counter bit 6.
5	—	NonCnt[5]	Non-matching cell counter bit 5.
4	—	NonCnt[4]	Non-matching cell counter bit 4.
3	—	NonCnt[3]	Non-matching cell counter bit 3.
2	—	NonCnt[2]	Non-matching cell counter bit 2.
1	—	NonCnt[1]	Non-matching cell counter bit 1.
0	—	NonCnt[0]	Non-matching cell counter bit 0 (LSB).

0x3D—NONCNTH (Non-matching Cell Counter [High Byte])

The NONCNTH counter tracks the number of non-matching cells. The counter is cleared on read.

Bit	Default	Name	Description
7	—	NonCnt[15]	Non-matching cell counter bit 15 (MSB).
6	—	NonCnt[14]	Non-matching cell counter bit 14.
5	—	NonCnt[13]	Non-matching cell counter bit 13.
4	—	NonCnt[12]	Non-matching cell counter bit 12.
3	—	NonCnt[11]	Non-matching cell counter bit 11.
2	—	NonCnt[10]	Non-matching cell counter bit 10.
1	—	NonCnt[9]	Non-matching cell counter bit 9.
0	—	NonCnt[8]	Non-matching cell counter bit 8.

0x200—MODE (Device Mode Control Register)

Bit	Default	Name	Description
7	0	DevMstRst	Device master reset. When set high, all internal state machines in the TC block are held in reset and all registers (except this bit) assume their default values.
6	0	DevLgcRst	Device logic reset. When set high, all internal state machines in the TC block are held in reset but register values are unaffected.
5	0	EnStatLat	When set to 1, the one-second status latching is enabled. The value of the status bits are the events which occurred between the last two one-second events. Any events occurring after the last one-second event is not reflected when the status register is read. Those events are reflected in the status register upon the next one-second event. When a status register is read, the status is cleared and is not updated until the next one-second event. When set to 0, the one-second status latching is disabled. The value of a status register is the events occurred since the last read of the status register.
4	0	EnCntrLat	When set to 1, the one-second counter latching is enabled. The value of the counter is the number of events counted between the last two one-second events. Any events occurring after the last one-second event is not reflected when the counter is read. Those events are reflected in the counter upon the next one-second event. When a counter is read, the count is cleared and is not updated until the next one-second event. When set to 0, the one-second counter latching is disabled. The value of a counter is the number of events counted since the last read of the counter.
3	0	EnIntPin	Enables the MicroInt* output pin.
2–1	00	—	Reserved, set to zero.
0	0	OneSecOut	When set to 1, the OneSecIO pin is configured as an output. The pin provides a one-second event pulse. The one-second event is generated internally of the device. The event occurs after the device has counted 8000 periods of a 8 KHz clock. When set to 0, the OneSecIO pin is configured as an input. The one-second event must be genetared externally, by pulsing the OneSecIO pin for low-high-low.

0x201—PHYINTFC (PHY-side Interface Control Register)

Bit	Default	Name	Description
7	0	—	Reserved, set to 0.
6	1	DisTCUtopia	When set to 1, the internal IMA/TC UTOPIA interface is disabled.
5–0	000000	—	Reserved, set to zero.

0x202—ATMINTFC (ATM-side Interface Control Register)

Bit	Default	Name	Description
7–6	11	ATMmux[1:0]	Controls the ATM-side UTOPIA interface mux. 00 – External interface is placed in Tristate mode. 01 – Utopia level 2 interface to IMA32 block is enabled. 10 – Utopia level 2 interface to TC block is enabled. 11 – External interface is placed in Tristate mode.
5	0	BusWidth	When set to 0, the 16-bit UTOPIA bus is enabled. When set to 1, the 8-bit UTOPIA bus is enabled. When the ATM UTOPIA interface to IMA32 block is enabled (ATMmux[1:0] = "01"), this bit controls the bus width of the IMA32 core ATM-side UTOPIA interface. In this case, the TC ATM-side UTOPIA interface is always 8-bit. When the ATM UTOPIA interface to TC block is enabled, (ATMmux[1:0] = "10"), this bit controls the bus width of the TC ATM-side UTOPIA interface.
4	0	—	Reserved, set to zero.
3	0	—	Reserved, set to zero.
2–0	000	—	Reserved, set to zero.

0x203—OUTSTAT (Output Status Control Register)

Bit	Default	Name	Description
7–2	000000	—	Reserved, set to zero.
1–0	00	StatOut[1:0]	The value written into these bits will be asserted on the StatOut[1:0] output pins.

0x204—SUMPORT (Summary Port Interrupt Status Register)

Bit	Default	Name	Description
7	0	PortInt[7][1]	This bit is a summary indicator of the interrupts from the Port 7 SUMINT register (0x1C0).
6	0	PortInt[6][1]	This bit is a summary indicator of the interrupts from the Port 6 SUMINT register (0x180).
5	0	PortInt[5][1]	This bit is a summary indicator of the interrupts from the Port 5 SUMINT register (0x140).
4	0	PortInt[4][1]	This bit is a summary indicator of the interrupts from the Port 4 SUMINT register (0x100).
3	0	PortInt[3][1]	This bit is a summary indicator of the interrupts from the Port 3 SUMINT register (0x0C0).
2	0	PortInt[2][1]	This bit is a summary indicator of the interrupts from the Port 2 SUMINT register (0x080).
1	0	PortInt[1][1]	This bit is a summary indicator of the interrupts from the Port 1 SUMINT register (0x040).
0	0	PortInt[0][1]	This bit is a summary indicator of the interrupts from the Port 0 SUMINT register (0x000).

FOOTNOTE:

(1) This bit is a pointer to the next interrupt indication register to be read. This bit will be cleared when the interrupt bit in the corresponding interrupt indication register is read and automatically cleared.

0x205—ENSUMPORT (Summary Port Interrupt Control Register)

Bit	Default	Name	Description
7	1	EnPortInt[7]	When set, this bit enables PortInt[7] to appear on the MicroInt* output.
6	1	EnPortInt[6]	When set, this bit enables PortInt[6] to appear on the MicroInt* output.
5	1	EnPortInt[5]	When set, this bit enables PortInt[5] to appear on the MicroInt* output.
4	1	EnPortInt[4]	When set, this bit enables PortInt[4] to appear on the MicroInt* output.
3	1	EnPortInt[3]	When set, this bit enables PortInt[3] to appear on the MicroInt* output.
2	1	EnPortInt[2]	When set, this bit enables PortInt[2] to appear on the MicroInt* output.
1	1	EnPortInt[1]	When set, this bit enables PortInt[1] to appear on the MicroInt* output.
0	1	EnPortInt[0]	When set, this bit enables PortInt[0] to appear on the MicroInt* output.

0x208—PART/VER (Part Number/Version Register)

Bit	Default	Name	Description
7–4	pppp	PartNum[3:0]	Part number controlled by bondout: IMA2 – 0100 IMA4 – 0101 IMA8/32 – 1001
3–0	0001	Version[3:0]	Version number of the device. 0001—Version -11 0010—Version -12 0011—Version -13 0100—Version -14

7.1 IMA Subsystem Registers

The IMA Subsystem layer contains configuration and status information that is common to all IMA groups.

0x400—IMA_VER_1_CONFIG (IMA Type and Version Code I)

The IMA_Version I and II registers contain the type and revision level of the IMA core. **Read-only**.

Bit	Default	Name	Description
7–4		IMA Core Type I	0x0 = CX28224, 2 ports 2 IMA groups 0x2 = CX28225, 4 ports 4 IMA groups 0x8 = CX28229, 32 ports 16 IMA groups
3	1	IMA Core Type II	1 = Internal memory present
2–0		Version Code I	0x4 = CX2822x family major revision level

0x401—IMA_VER_2_CONFIG (IMA Version Codes II and III)

This register is **read-only**.

Bit	Default	Name	Description
7–4		Version Code II	4 bit code: 0x2 = CX2822x-13 and earlier 0x3 = CX2822x-14
3–0		Version Code III	4 bit code: CX2822x-11 = 0 CX2822x-12 = 3 CX2822x-13 = 4 CX2822x-14 = 0

0x402—IMA_SUBSYS_CONFIG (IMA Configuration Control)

This register contains some of the basic IMA Subsystem configuration.

Bit	Default	Name	Description
7–6	0	Link Type	Sets default link type for all IMA groups. Not used with variable rate facilities 0 = T1 1 = E1 2 = Alternate T1 (1.544 Mbps payload) 3 = Alternate E1 (1.984 Mbps payload)
5–4	0	SRAM size	0 = 25 ms (E1 mode) 1 = 50 ms 2 = 100 ms 3 = 200 ms
3	0	Number of SRAMs	0 = 1 SRAM, Set to 0 for all CX2822X devices
2–0	0	Number of Ports	This field indicates the range of valid PHY addresses. 0: addresses 0x00–0x03 are valid 1: addresses 0x00–0x07 are valid 2: addresses 0x00–0x0B are valid 3: addresses 0x00–0x0F are valid 4: addresses 0x00–0x13 are valid 5: addresses 0x00–0x17 are valid 6: addresses 0x00–0x1B are valid 7: addresses 0x00–0x1F are valid This field has different ranges depending on Product type: CX28224: Unused, Set to 0 CX28225: Unused, Set to 0 CX28229: Range: 0–7

0x403—IMA_MISC_STATUS (IMA Miscellaneous Status)

This register contains miscellaneous status information for the IMA Subsystem. **Read-only**.

Bit	Default	Name	Description
7	—	State of TxAddr[4]	This bit is the current state of the signal ATMUTxAddr[4].
6	—	State of RxAddr[4]	This bit is the current state of the signal ATMURxAddr[4].
5	—	—	Reserved
4	—	ATM Data Width	This bit indicates whether the ATM Utopia bus is operating in 16 bit (high) or 8 bit (low) data mode.
3	—	IMA_RefClk Error	This bit is set high if a transition detector for IMA_RefClk detects a bad signal. This bit is active high and is reset upon reading this address.
2	—	Tx ATM Parity Error	This bit indicates that a parity error has been detected on the Transmit ATM side Utopia bus. This bit is active high and is reset upon reading this address.
1	—	—	Reserved.
0	—	Rx PHY Parity Error	This bit indicates that a parity error has been detected on the Receive PHY side cell bus. This bit is active high and is reset upon reading this address.

0x404—IMA_MISC_CONFIG (IMA Miscellaneous Control)

This register contains some of the basic IMA Subsystem configuration.

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0
6	0	Alternate GTSM Mode	1 = When the GTSM is down, ATMUTxClAv for that group is controlled as if all configured links in the group are Active. 0 = When the GTSM is down, ATMUTxClAv for that group is inactive.
5–4	0	PHY Size	This two bit field determines the use of the PHY side ClAv and En* signals 0 = ClAv and En* for every 4 PHY addresses (support 8 ports total) 1 = ClAv and En* for every 16 PHY addresses (support 32 ports total) 2 = ClAv and En* for all PHY addresses (support 32 ports total) 3 = ClAv and En* for every 8 PHY addresses (support 16 ports total)
3	0	Enable External HEC Checker	1 = Bit 7 of the HEC Byte is a HEC error flag 0 = Use the HEC Error checker within the IMA block
2	0	Check ATMUTxAddr[4] and ATMURxAddr[4]	0 = mask bits (don't care) 1 = Check ATMUTxAddr[4] and TMURxAddr[4] for correct value
1	0	Check ATMUTxAddr[3] and ATMURxAddr[3]	0 = mask bits (don't care) 1 = Check ATMUTxAddr[3] and ATMURxAddr[3] for correct value
0	0	Check ATMUTxAddr[2] and ATMURxAddr[2]	0 = mask bits (don't care) 1 = Check ATMUTxAddr[2] and ATMURxAddr[2] for correct value

0x405—IMA_MEM_LOW_TEST (IMA Memory Test Address (Bits 0–7))

Registers 0x405—0x408 are used to perform memory diagnostic tests on the internal or external differential delay SRAM.

Bit	Default	Name	Description
7–0	0x00	Memory Test Address	This field contains the least significant bits of the memory test address for the selected memory component. Range: 0x00–0xFF

0x406—IMA_MEM_HI_TEST (IMA Memory Test Address (Bits 8–15))

Bit	Default	Name	Description
7–0	0x00	Memory Test Address	This field contains the middle significant bits of the memory test address for the selected memory component. Range: 0x00–0xFF

0x407—IMA_MEM_TEST_CTL (IMA Memory Test Control / Address MSBs)

Bit	Default	Name	Description
7	0	Memory Test Address Bit 20	This field contains the most significant bit of the memory test address for the selected memory component.
6–4	0	RAM Test Access	0 = no test selected, normal operation 1 = SRAM Test 2–7 = Reserved
3–0	0	Memory Test Address Bits 19–16	This field contains the most significant bits of the memory test address for the selected memory component. Range: 0x00–0x0F

0x408—IMA_MEM_TEST_DATA (IMA Memory Test Data)

Bit	Default	Name	Description
7–0	0x00	Memory Test Data	This field contains the data to be written or read from the memory test address for the selected memory component. Range: 0x00–0xFF

0x409—IMA_LNK_DIAG_CTL (IMA Link Diagnostic Control Register)

This register is used to specify a port number for observation of link differential delay and anomalies. The contents of this register are used to report the link information via registers 0x409–0x40B. Bit 5 of this register is **read-only**.

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0
6	—	—	Reserved. Set to 0
5	—	Link Delay Write Counter	This field contains the most significant bit of the SRAM write counter for the diagnostic link (selected using the field below).
4–0	0x00	Link Diagnostic PHY Address	This field contains the PHY Cell Bus Address of the port for which a diagnostic measurement is to be performed. Range: 0x00–0x1F

0x40A—IMA_LNK_DIFF_DEL (IMA Link Differential Delay Write Counter)

This register, along with bit 5 of address 0x409, reports the value of the SRAM write phase at the time when the read phase is 0. This phase information is used to calculate the link differential delay.

Bit	Default	Name	Description
7–0	—	Link Delay Write Counter	This field contains a snapshot of 8 of the least significant bits of the SRAM write counter for the diagnostic link (selected using address 0x409). All others (Range: 0x00–0xFF) Delay Window = 0 (see register 0x415): Value = Cell_count >> 1 Delay Window = 1–3 (see register 0x415): Value = Cell_count Delay Window = 4 (see register 0x415): Value = Cell_count >> 2

0x40B—IMA_RCV_LNK_ANOMALIES (IMA Receive Link Anomalies)

These anomalies are for the diagnostic link selected using address 0x409. The bits in this register are **read-only** and are cleared upon read.

Bit	Default	Name	Description
7	—	ICP-ERR Anomaly	1 = ICP-ERR anomaly was active sometime since the last time this register was read 0 = ICP-ERR defect was inactive
6	—	ICP-INV Anomaly—Unexpected IMA Label	1 = Unexpected IMA Label condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA Label condition was inactive
5	—	ICP-INV Anomaly—Unexpected LID	1 = Unexpected LID condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected LID condition was inactive
4	—	ICP-INV Anomaly—Unexpected IMA ID	1 = Unexpected IMA ID condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA ID condition was inactive
3	—	ICP-INV Anomaly—Unexpected M	1 = Unexpected M condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected M condition was inactive
2	—	ICP-INV Anomaly—Unexpected IMA Frame Number	1 = Unexpected IMA Frame Number condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA Frame Number condition was inactive
1	—	ICP-INV Anomaly—Unexpected IMA Cell Offset	1 = Unexpected IMA Cell Offset condition of the ICP-INV anomaly was active sometime since the last time this register was read 0 = Unexpected IMA Cell Offset condition was inactive
0	—	ICP-MIS Anomaly	1 = ICP-MIS anomaly was active sometime since the last time this register was read 0 = ICP-MIS defect was inactive

0x40E—IMA_DIAG_XOR_BIT (IMA Diagnostic Bit)

This register provides a single bit that can be used by a diagnostic test routine to verify the connectivity of the microprocessor address lines to the IMA device. This bit is **read-only**.

Bit	Default	Name	Description
7	—	—	Reserved.
6	—	—	Reserved.
5	—	—	Reserved.
4	—	—	Reserved.
3	—	—	Reserved.
2	—	—	Reserved.
1	—	—	Reserved.
0	—	Address Diagnostic Bit	Exclusive OR of address bits from previous IMA core access. The number of bits in the exclusive OR operation is 10.

0x40F—IMA_DIAG (IMA Diagnostic Register)

This register provides an isolated 8 bit storage register that can be used by a diagnostic test routine to verify the connectivity of the microprocessor data lines to the IMA device.

Bit	Default	Name	Description
7–0	0x00	Data Diagnostic Register	An 8 bit register that can be written and read by the processor. The register is not used within the IMA Block.

0x410—IMA_TIM_REF_MUX_CTL_ADDR (IMA Timing Reference Multiplexer Control Address)

This register is used in conjunction with 0x411 to configure various timing elements within the IMA core. Register 0x410 and 0x411 are an indirect register pair in that a particular timing element is selected using register 0x410 and the configuration for that timing element is programmed using register 0x411.

Bit	Default	Name	Description
7–6	0	Multiplexer Type	0 = Set timing reference for a Rx IMA Group 1 = Set timing reference for a Tx IMA Group 2 = Set timing source for Tx_TRL Outputs 3 = Set the Clock Divisor for an IMA group
5	—	—	Reserved. Set to 0.
4	—	—	Reserved. Set to 0.
3–0	0	Multiplexer ID	For Multiplexer Type = 0, Multiplexer Type = 1, and Multiplexer Type = 3: CX28224: 0–1: IMA Group 1–2 CX28225: 0–3: IMA Group 1–4 CX28229: 0–0xF: IMA Group 1–16 For Multiplexer Type = 2: 0–1: Tx_TRL[0]–Tx_TRL[1] output

0x411—IMA_TIM_REF_MUX_CTL_DATA (IMA Timing Reference Multiplexer Control Data)

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0.
6	—	—	Reserved. Set to 0.
			For Multiplexer Type 0 and 1
5–0	0x00	Timing Source	0x00–0x1F: Select timing from a Receive Port (see register 0x416) CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31 0x20: Use IMA_SysClk/24 or DSL generator output as source (see register 0x416) 0x21: Use IMA_RefClk as source
			For Multiplexer Type 2
5–0	0x00	Timing Source	0x00–0x1F: Select timing from a Receive Port (see register 0x416) CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31 0x20: Use IMA_SysClk/24 0x21: Use IMA_RefClk as source 0x22: Use 8 kHz as source
			For Multiplexer Type 3
5	—	—	Reserved. Set to 0.
4	—	—	Reserved. Set to 0.
3–0	0x0	Clock Divisor	This field contains the clock divider multiplier for the group. The IMA group number is set by writing to the Multiplexer ID field in address 0x410. 0 = Based on Link Type field in address 0x002 1 = 1/1 2 = 192/193 3 = 15/16

0x412—IMA_RX_PERSIST_CONFIG (IMA Receive Persistence Configuration)

Bit	Default	Name	Description
7	0	—	Reserved. Set to 0.
6	0	Alpha Value(1)	0: $\alpha = 1$ 1: $\alpha = 2$
5–3	0	Beta Value(2)	0: $\beta = 1$ 1: $\beta = 2$ 2: $\beta = 3$ 3: $\beta = 4$ 4: $\beta = 5$
2–0	0	Gamma Value(3)	0: $\gamma = 1$ 1: $\gamma = 2$ 2: $\gamma = 3$ 3: $\gamma = 4$ 4: $\gamma = 5$

FOOTNOTE:
(1) The Alpha Value is the number of consecutive invalid ICP cells needed for the link to leave the IMA Sync state.
(2) The Beta Value is the number of consecutive errored ICP cells needed for the link to leave the IMA Sync state.
(3) The Gamma Value is the number of consecutive valid ICP cells needed for the link to enter the IMA Sync state.

0x413—IMA_ATM_UTOPIA_BUS_CTL (IMA ATM Utopia Bus Control)

This register configures the operation of the ATM side UTOPIA bus and the sample time of PhyUTxClAv for an IMA group.

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0.
6	0	ATM Address Mode	0 = Utopia Level 2 (multiple addresses) 1 = Utopia Level 1 (single fixed address, no address latching)
5	0	ATMURxSOC Three-state Disable	0 = ATMURxSOC, ATMURxData[], and ATMURxPrty three-state when not selected 1 = ATMURxSOC, ATMURxData[], and ATMURxPrty do not three-state
4	0	ATMURxClAv Mode	0 = ATMURxClAv is set active for selected channel during cell transfer 1 = ATMURxClAv is set inactive for selected channel during cell transfer
3	0	ATMUTxClAv Last 4 Bytes/Words Mode	0 = ATMUTxClAv is forced inactive/active (based on the state of bit 2) during last 4 bytes/words for selected channel during cell transfer 1 = ATMUTxClAv reflects true cell available status during last 4 bytes/words for selected channel during cell transfer
2	0	ATMUTxClAv Mode	0 = ATMUTxClAv is set inactive for selected channel during cell transfer 1 = ATMUTxClAv is set active for selected channel during cell transfer
1	0	ClAv Three-state Disable	0 = ATMURxClAv and ATMUTxClAv threestate when not selected 1 = ATMURxClAv and ATMUTxClAv do not threestate
0	0	PHYUTxClAv Sample Time	0 = For an IMA group, sample PhyUTxClAv during an ICP cell to determine SICP rate 1 = For an IMA group, delay sampling PhyUTxClAv until >5 payload byte periods after an ICP transfer

0x414—IMA_DIFF_DELAY_ADDR (IMA Differential Delay Control Address)

This register is used in conjunction with 0x415 to configure the differential delay operation of the IMA core. Register 0x414 and 0x415 are an indirect register pair in that a particular IMA group is selected using register 0x414 and the configuration for that IMA group is programmed using register 0x415.

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0.
6	0	Control Type	0 = Set Delay Threshold for an IMA group 1 = Set Delay Window for an IMA group
5	—	—	Reserved. Set to 0.
4	—	—	Reserved. Set to 0.
3–0	0x0	Group Number	CX28224: 0–1: IMA Group 1–2 CX28225: 0–3: IMA Group 1–4 CX28229: 0–0xF: IMA Group 1–16

0x415—IMA_DIFF_DELAY_DATA (IMA Differential Delay Control Data)

Bit	Default	Name	Description
For Control Type = 0			
7–0	0x00	Differential Delay Threshold	This field contains the cell offset that corresponds to differential delay threshold setting for the group. Delay Window = 0, 5: Value = 255–(Cell_count >> 1) Delay Window = 1–3, 6–7: Value = 255–Cell_count Delay Window = 4: Value = 255–(Cell_count >> 2)
For Control Type = 1			
7	—	—	Reserved. Set to 0.
6	—	—	Reserved. Set to 0.
5	—	—	Reserved. Set to 0.
4	—	—	Reserved. Set to 0.
3	—	—	Reserved. Set to 0.
2–0		Delay Window	This field contains the number of IMA frames (assuming M=128) that are examined when setting the differential delay buffer. This field is set based on the facility payload rate. 0 = 8 frames (1024 cells), for payload rates ≥ 1024 kbps 1 = 4 frames (512 cells), for 1024 kbps > payload rates ≥ 512 kbps 2 = 2 frames (256 cells), for 512 kbps > payload rates ≥ 256 kbps 3 = 1 frame (128 cells), for payload rates < 256 kbps 4 = 16 frames (2048 cells), for payload rates ≥ 1024 kbps 5 = 8 frames (1024 cells), for 1024 kbps > payload rates ≥ 512 kbps 6 = 4 frames (512 cells), for 512 kbps > payload rates ≥ 256 kbps 7 = 2 frame (256 cells), for payload rates < 256 kbps

0x416—IMA_DSL_CLOCK_GEN_ADDR (IMA DSL Clock Generator Control)

This register is used in conjunction with 0x417 to configure the operation of the DSL Clock Generator in the IMA core. Register 0x416 and 0x417 are an indirect register pair in that a particular clock generator element is selected using register 0x416 and the configuration for that element is programmed using register 0x417.

The overall operation of the clock generators are governed by the following equations:

- Prescaler Factor = Prescaler Numerator / (Prescaler Terminal Count + 1)
- Intermediate Frequency = Reference Clock Frequency * Prescaler Factor
- Reference Denominator = 257 + Reference Clock Divisor
- 8 kHz = Intermediate Frequency / (Reference Denominator)

Link Payload Rate = 8 kbps * (Multiplier Factor)

A further constraint is:

- Maximum Link Payload Rate ≤ Intermediate Frequency ≤ IMA_SysClk/16

In a typical G.shdsl application, Intermediate Frequency is set to 2.56 MHz and the Reference Denominator is set to 320. Other settings are possible as long as the above equations and constraints are met.

Bit	Default	Name	Description
7–5	0	Control Type	0 = Basic Setup 1 = Pre-scaler Terminal Count 2 = Pre-scaler Numerator 3 = Reference Divisor 4 = IMA Group Factor LSBs 5 = IMA Group Factor MSB 6 = Rx Timing Synthesizer Factor LSBs 7 = Rx Timing Synthesizer Factor MSB
For Control Type = 0, 1, 2, 3			
4–0	—	—	Reserved. Set to 0.
For Control Type = 4, 5			
4	0	Transmit / Receive	0 = Receive IMA Group 1 = Transmit IMA Group
3–0	0x0	Group Number	CX28224: 0–1: IMA Group 1–2 CX28225: 0–3: IMA Group 1–4 CX28229: 0–0xF: IMA Group 1–16
For Control Type = 6, 7			
4–0	0x00	Port Number	CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31

0x417—IMA_DSL_CLOCK_GEN_DATA (IMA_DSL Clock Generator Data)

This register is used in conjunction with 0x416 to configure the operation of the DSL Clock Generator in the IMA core. Register 0x416 and 0x417 are an indirect register pair in that a particular clock generator element is selected using register 0x416 and the configuration for that element is programmed using register 0x417.

Bit	Default	Name	Description
For Control Type = 0			
7	—	—	Reserved. Set to 0.
6	0	EnRxSyn	Enable Rx Timing Synthesizers 0 = Use SPRxClk inputs 1 = Use synthesizers instead of SPRxClk inputs
5	0	DSLClkGen	Substitute DSL clock generator 0 = Use IMA_SysClk/24 in IMA group clock and Tx_TRL selectors 1 = Use DSL Clock generator outputs when Timing Source is set to 0x20 in register 0x411.
4	0	IMA_ClkSel	0 = Use IMA_SysClk as input to DSL Clock Generators 1 = Use IMA_RefClk as input to DSL Clock Generators
3–0	—	—	Reserved. Set to 0.
For Control Type = 1			
7–0	0x00	Pre-scaler Terminal Count	This field contains the terminal count of the pre-scaler clock divider. The pre-scaler denominator is the value of this field plus 1.
For Control Type = 2			
7–0	0x00	Pre-scaler Numerator	This field contains the numerator for the pre-scaler.
For Control Type = 3			
7–0	0x00	Reference Clock Divisor	This field contains 8 of the 9 bits of the terminal count for the reference clock divisor. The reference clock divisor counts from 0 to the terminal count which is given by the value of this field plus 257. As an example if the value of this register is 63 decimal, then the reference clock divisor will be 320.
For Control Type = 4			
7–0	0x00	Group Clock Multiplier Factor (lsbs)	This register contains the 8 lsbs of the payload bandwidth for the ports used in the IMA group. The contents of this register are multiplied by 8kbps in order to obtain the bandwidth.
For Control Type = 5			
7–1	—	—	Reserved. Set to 0.
0	0	Group Clock Multiplier Factor (msb)	This register contains the msb of the payload bandwidth for the ports used in the IMA group. The contents of this register are multiplied by 2048kbps in order to obtain the bandwidth.
For Control Type = 6			
7–0	0x00	Port Clock Multiplier Factor (lsbs)	This register contains the 8 lsbs of the payload bandwidth for the specific port of the Rx Timing clock synthesizer. The contents of this register are multiplied by 8kbps in order to obtain the bandwidth.

Bit	Default	Name	Description (Continued)
For Control Type = 7			
7–1	—	—	Reserved. Set to 0.
0	0	Port Clock Multiplier Factor (msb)	This register contains the msb of the payload bandwidth for the specific port of the Rx Timing clock synthesizer. The contents of this register are multiplied by 2048kbps in order to obtain the bandwidth.

0x418—IMA_RX_TRANS_TABLE (IMA Receive Translation Table Address)

This register is used in conjunction with 0x419 for configure the translation between the ATM side Utopia addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x418 and 0x419 are an indirect register pair in that a address is selected using register 0x418 and the configuration for that address is programmed using register 0x419.

Bit	Default	Name	Description
7		Translation Type	0 = the value in bits 5–0 enables ATM address –> IMA internal channel translations 1 = the value in bits 5–0 enables IMA internal channel –> ATM address translations
6	—	—	Don't care. Ignore.
For Translation Type = 0			
5	—	—	Don't care. Ignore.
4–0		ATM Utopia Address	For Type 0, this field contains the ATM Side Utopia address. Range: 0x00–0x1F
For Translation Type = 1			
5–0		Internal IMA Channel	For Type 1, this field contains the IMA internal channel address. Range 0x00–0x1F: Bypass Receive Port CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31 Range 0x20–0x2F: IMA Group CX28224: 0x20–0x21: IMA Group 1–2 CX28225: 0x20–0x23: IMA Group 1–4 CX28229: 0x20–0x2F: IMA Group 1–16

0x419—IMA_RX_ATM_TRANS_TABLE (IMA Receive ATM Translation Table Internal Channel)

This register is used in conjunction with 0x418 for configure the translation between the ATM side Utopia addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x418 and 0x419 are an indirect register pair in that an address is selected using register 0x418 and the configuration for that address is programmed using register 0x419.

Bit	Default	Name	Description
For Translation Type = 0			
7	—	—	Don't care. Ignore.
6	—	—	Don't care. Ignore.
5–0		Internal IMA Channel	This field contains the mapping for the ATM Utopia address set in register 0x418. Range 0x00–0x1F: Bypass Receive Port CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31 Range 0x20–0x2F: IMA Group CX28224: 0x20–0x21: IMA Group 1–2 CX28225: 0x20–0x23: IMA Group 1–4 CX28229: 0x20–0x2F: IMA Group 1–16 0x30 All devices: ATM address is not assigned to this device
For Translation Type = 1			
7		Channel Active	1 = Internal Channel Active 0 = Internal Channel Inactive
6	—	—	Don't care. Ignore.
5	—	—	Don't care. Ignore.
4–0		ATM Utopia Address	This field contains the mapping for the Internal IMA channel set in register 0x418. Range: 0x00–0x1F

0x41B—IMA_TX_TRANS_TABLE (IMA Transmit Translation Table Address)

This register is used in conjunction with 0x41C for configure the translation between the ATM side Utopia addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x41B and 0x41C are an indirect register pair in that a address is selected using register 0x41B and the configuration for that address is programmed using register 0x41C.

Bit	Default	Name	Description
7		Translation Type	0 = the value in bits 5–0 enables ATM address –> IMA internal channel translations 1 = the value in bits 5–0 enables IMA internal channel –> ATM address translations
6	—	—	Don't care. Ignore.
For Translation Type = 0			
5	—	—	Don't care. Ignore.
4–0		ATM Utopia Address	For Type 0, this field contains the ATM Side Utopia address. Range: 0x00–0x1F
For Translation Type = 1			
5–0		Internal IMA Channel	For Type 1, this field contains the IMA internal channel address. Range 0x00–0x1F: Bypass Transmit Port CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31 Range 0x20–0x2F: IMA Group CX28224: 0x20–0x21: IMA Group 1–2 CX28225: 0x20–0x23: IMA Group 1–4 CX28229: 0x20–0x2F: IMA Group 1–16

0x41C—IMA_TX_ATM_TRANS_TABLE (Transmit ATM Translation Table Internal Channel)

This register is used in conjunction with 0x41B for configure the translation between the ATM side Utopia addresses and the internal channels (bypass ports and IMA groups) associated with the IMA core. Register 0x41B and 0x41C are an indirect register pair in that a address is selected using register 0x41B and the configuration for that address is programmed using register 0x41C.

Bit	Default	Name	Description
For Translation Type = 0			
7	—	—	Don't care. Ignore.
6	—	—	Don't care. Ignore.
5–0		Internal IMA Channel	This field contains the mapping for the ATM Utopia address set in register 0x41B. Range 0x00–0x1F: Bypass Transmit Port CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31 Range 0x20–0x2F: IMA Group CX28224: 0x20–0x21: IMA Group 1–2 CX28225: 0x20–0x23: IMA Group 1–4 CX28229: 0x20–0x2F: IMA Group 1–16 0x30 All devices: ATM address is not assigned to this device
For Translation Type = 1			
7		Channel Active	1 = Internal Channel Active 0 = Internal Channel Inactive
6	—	—	Don't care. Ignore.
5	—	—	Don't care. Ignore.
4–0		ATM Utopia Address	This field contains the mapping for the Internal IMA channel set in register 0x41B. Range: 0x00–0x1F

0x458—IMA_RX_SOC_DETECTOR (PHY Utopia RX_SOC Detector)

This register is used to monitor phyURxSOC for conditions where a cell transfer occurs without an assertion of the Start-of-cell signal. Use of this register requires first setting the port address in bits 4–0 and then reading the state of the Loss-of-start-of-cell in bit 7.

Bit	Default	Name	Description
7	—	Loss of Start of Cell	This bit indicates that a cell transfer occurred for the selected port and phyURxSOC was not asserted. This occurrence is saved internally until the state is read using this register. The read operation will clear the internal state.
6	—	—	Reserved. Set to 0.
5	—	—	Reserved. Set to 0.
4–0	0x00	Port Number	This field contains the PHY Cell Bus Address of the SOC being examined CX28224: 0–1: Port 0–1 CX28225: 0–3: Port 0–3 CX28229: 0–0x1F: Port 0–31

7.2 IMA Group

The IMA Group layer contains configuration and status information that is associated with IMA groups.

0x41F—IMA_GRP_1TO4_SEM (Group Table Control I)

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

Bit	Default	Name	Description
7	0	Update Enable for Receive group 4	addresses 0x4DC–0x4DF (Not defined for CX28224)
6	0	Update Enable for Receive group 3	addresses 0x4D8–0x4DB (Not defined for CX28224)
5	0	Update Enable for Receive group 2	addresses 0x4D4–0x4D7
4	0	Update Enable for Receive group 1	addresses 0x4D0–0x4D3
3	0	Update Enable for Transmit group 4	addresses 0x438–0x43F (Not defined for CX28224)
2	0	Update Enable for Transmit group 3	addresses 0x430–0x437 (Not defined for CX28224)
1	0	Update Enable for Transmit group 2	addresses 0x428–0x42F
0	0	Update Enable for Transmit group 1	addresses 0x420–0x427

0x51F—IMA_GRP_5TO8_SEM (Group Table Control II (CX28229 Only))

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

Bit	Default	Name	Description
7	0	Update Enable for Receive group 8	addresses 0x5DC–0x5DF (Not defined for CX28224 and CX28225)
6	0	Update Enable for Receive group 7	addresses 0x5D8–0x5DB (Not defined for CX28224 and CX28225)
5	0	Update Enable for Receive group 6	addresses 0x5D4–0x5D7 (Not defined for CX28224 and CX28225)
4	0	Update Enable for Receive group 5	addresses 0x5D0–0x5D3 (Not defined for CX28224 and CX28225)
3	0	Update Enable for Transmit group 8	addresses 0x538–0x53F (Not defined for CX28224 and CX28225)
2	0	Update Enable for Transmit group 7	addresses 0x530–0x537 (Not defined for CX28224 and CX28225)
1	0	Update Enable for Transmit group 6	addresses 0x528–0x52F (Not defined for CX28224 and CX28225)
0	0	Update Enable for Transmit group 5	addresses 0x520–0x527 (Not defined for CX28224 and CX28225)

0x61F—IMA_GRP_9TO12_SEM (Group Table Control III (CX28229 Only))

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

Bit	Default	Name	Description
7	0	Update Enable for Receive group 12	addresses 0x6DC–0x6DF (Not defined for CX28224 and CX28225)
6	0	Update Enable for Receive group 11	addresses 0x6D8–0x6DB (Not defined for CX28224 and CX28225)
5	0	Update Enable for Receive group 10	addresses 0x6D4–0x6D7 (Not defined for CX28224 and CX28225)
4	0	Update Enable for Receive group 9	addresses 0x6D0–0x6D3 (Not defined for CX28224 and CX28225)
3	0	Update Enable for Transmit group 12	addresses 0x638–0x63F (Not defined for CX28224 and CX28225)
2	0	Update Enable for Transmit group 11	addresses 0x630–0x637 (Not defined for CX28224 and CX28225)
1	0	Update Enable for Transmit group 10	addresses 0x628–0x62F (Not defined for CX28224 and CX28225)
0	0	Update Enable for Transmit group 9	addresses 0x620–0x627 (Not defined for CX28224 and CX28225)

0x71F—IMA_GRP_13TO16_SEM (Group Table Control IV (CX28229 Only))

For the following bits, 1 = the group table is being updated, 0 = the group table is not being updated. The update enable must be set to 1 prior to writing the group table. All elements of the group table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The group tables are described below.

NOTE: This register cannot be read back.

Bit	Default	Name	Description
7	0	Update Enable for Receive group 16	addresses 0x7DC–0x7DF (Not defined for CX28224 and CX28225)
6	0	Update Enable for Receive group 15	addresses 0x7D8–0x7DB (Not defined for CX28224 and CX28225)
5	0	Update Enable for Receive group 14	addresses 0x7D4–0x7D7 (Not defined for CX28224 and CX28225)
4	0	Update Enable for Receive group 13	addresses 0x7D0–0x7D3 (Not defined for CX28224 and CX28225)
3	0	Update Enable for Transmit group 16	addresses 0x738–0x73F (Not defined for CX28224 and CX28225)
2	0	Update Enable for Transmit group 15	addresses 0x730–0x737 (Not defined for CX28224 and CX28225)
1	0	Update Enable for Transmit group 14	addresses 0x728–0x72F (Not defined for CX28224 and CX28225)
0	0	Update Enable for Transmit group 13	addresses 0x720–0x727 (Not defined for CX28224 and CX28225)

IMA_TX_GRP*n*_RX_TEST_PATTERN (Transmit Group Rx Test Pattern)

This register contains the value of the Rx Test Pattern field for the transmitted ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x420	0x428	0x430	0x438	0x520	0x528	0x530	0x538	0x620	0x628	0x630	0x638	0x720	0x728	0x730	0x738
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	0x00	Rx Test Pattern	In support of the Test Pattern Procedure, this field is set equal to the value acquired from the Receive side test link. See address 0x4E7. When the Test Pattern Procedure is inactive, the Rx Test Pattern field should be set to 0xFF. Range: 0x00–0xFF

IMA_TX_GRP*n*_CTL (Transmit Group Control Register)

This register, in conjunction with the IMA_TX_GRP*n*_FIRST_PHY_ADDR register, controls the operation of the Transmit IMA group.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x421	0x429	0x431	0x439	0x521	0x529	0x531	0x539	0x621	0x629	0x631	0x639	0x721	0x729	0x731	0x739
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7	0	Group Enable	1 = Group is established and a round-robin is created 0 = Group is not established
6	0	SW Timeout Expired	1 = certain LSM transitions (Unusable → Usable, Usable → Active) are allowed 0 = certain LSM transitions (Unusable → Usable, Usable → Active) are blocked
5	—	—	Reserved. Set to 0.
4	0	Group Inhibit	1 = Group is inhibited from carrying traffic 0 = Group is not inhibited
3	—	—	Reserved. Set to 0.
2–0	0x0	Group Size	Sets the number of configured links within group. Range: 0x0–0x7 (1–8 links in group)

IMA_TX_GRP*n*_FIRST_PHY_ADDR (Transmit First PHY Address)

This register, in conjunction with the IMA_TX_GRP*n*_CTL register, controls the operation of the Transmit IMA group.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x422	0x42A	0x432	0x43A	0x522	0x52A	0x532	0x53A	0x622	0x62A	0x632	0x63A	0x722	0x72A	0x732	0x73A
CX28224	Not Applicable														
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0.
6	—	—	Reserved. Set to 0.
5	0x0	Tx IMA Version	IMA OAM Label value 1 = IMA v1.1 0 = IMA v1.0
4–0	0x00	Link PHY Address	This field contains the PHY port address of the Transmit link with the lowest LID in the group. CX28224: Range: 0–1 CX28225: Range: 0–3 CX28229: Range: 0–0x1F

IMA_TX_GRP*n*_ID (Transmit Group ID)

This register contains the value of the IMA Group ID field for the transmitted ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x423	0x42B	0x433	0x43B	0x523	0x52B	0x533	0x53B	0x623	0x62B	0x633	0x63B	0x723	0x72B	0x733	0x73B
CX28224	Not Applicable														
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	0x00	Tx Group ID	This field contains the Transmit Group ID sent in the Transmit ICP cells of all links within the group. Range: 0x00–0xFF

IMA_TX_GRP*n*_STAT_CTL (Transmit Group Status and Control)

This register contains the value of the Group Status and Control field for the transmitted ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x424	0x42C	0x434	0x43C	0x524	0x52C	0x534	0x53C	0x624	0x62C	0x634	0x63C	0x724	0x72C	0x734	0x73C
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–4	0x00	Group State	0 = Start-up 1 = Start-up-Ack 2 = Config-Abort–Unsupported M 3 = Config-Abort–Incompatible Symmetry 4 = Config-Abort–Unsupported IMA Version 5–7 = Reserved for other Config-Abort states 8 = Insufficient Links 9 = Blocked 0xA = Operational 0xB–F = reserved
3–2	0	Group Symmetry	0 = Symmetrical configuration and operation 1 = Symmetrical configuration and asymmetrical operation 2 = Asymmetrical configuration and operation 3 = Alternate symmetrical configuration and operation
1–0	0	Frame Length (M)	0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256

IMA_TX_GRP*n*_TIMING_INFO (Transmit Timing Information)

This register contains the value of the Transmit Timing Information field for the transmitted ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x425	0x42D	0x435	0x43D	0x525	0x52D	0x535	0x53D	0x625	0x62D	0x635	0x63D	0x725	0x72D	0x735	0x73D
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7	0		Unused: Set to 0.
6	0		Unused: Set to 0.
5	0	Tx Clock Mode	0 = Independent Transmit Clock (ITC) 1 = Common Transmit Clock (CTC)
4	0		Unused: Set to 0.
3	0		Unused: Set to 0.
2–0	0	Timing Reference Link ID	This field contains the LID of the Transmit TRL. Range: 0x0–0x7

IMA_TX_GRP*n*_TEST_CTL (Transmit Test Control)

This register contains the value of the Tx Test Control field for the transmitted ICP cells.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x426	0x42E	0x436	0x43E	0x526	0x52E	0x536	0x53E	0x626	0x62E	0x636	0x63E	0x726	0x72E	0x736	0x73E
CX28224	Not Applicable														
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7	0		Unused: Set to 0.
6	0		Unused: Set to 0.
5	0	Test Link Command	0 = Inactive 1 = Active
4	0		Unused: Set to 0.
3	0		Unused: Set to 0.
2–0	0	Test Link ID	This field contains the LID of the Transmit Test Link. Range: 0x0–0x7

IMA_TX_GRP*n*_TX_TEST_PATTERN (Transmit Group Tx Test Pattern)

This register contains the value of the Tx Test Pattern field for the transmitted ICP cells.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x427	0x42F	0x437	0x43F	0x527	0x52F	0x537	0x53F	0x627	0x62F	0x637	0x63F	0x727	0x72F	0x737	0x73F
CX28224	Not Applicable														
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	0x0	Tx Test Pattern	If the Test Link Command is set to Active, the Tx Test Pattern is sent in the ICP cell of the Transmit Test Link. For other links and when the Test Link Command is Inactive, the Tx Test Pattern in the Transmit ICP cells will automatically be set to 0x00. Range: 0x00–0xFF

IMA_TX_GRP*n*_CELL_COUNT_LSB (Transmit Cell Count LSBs)

This register contains the least significant bits of a 16 bit count of the number of ATM layer cells transmitted over the Transmit links within the group. The register is read only. Status clears upon read.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x440	0x442	0x444	0x446	0x540	0x542	0x544	0x546	0x640	0x642	0x644	0x646	0x740	0x742	0x744	0x746
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7-0	0	Transmit Cell Count LSBs	Transmit Group Cell Count: This field contains the least significant bits of a 16-bit count of the number of ATM layer cells transmitted over the Transmit links within the group. A write operation with data = 0x01 to the first address (0x440 for Group #1, 0x442 for Group #2, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the state of the counter, The first address should be read first. The second address (0x441 for Group #1, 0x443 for Group #2, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters.

IMA_TX_GRP*n*_CELL_COUNT_MSB (Transmit Cell Count MSBs)

This register contains the most significant bits of a 16 bit count of the number of ATM layer cells transmitted over the Transmit links within the group. The register is read only. Status clears upon read.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x441	0x443	0x445	0x447	0x541	0x543	0x545	0x547	0x641	0x643	0x645	0x647	0x741	0x743	0x745	0x747
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7-0	0	Transmit Cell Count MSBs	Transmit Group Cell Count: This field contains the most significant bits of a 16 bit count of the number of ATM layer cells transmitted over the Transmit links within the group. A write operation with data = 0x01 to the first address (0x440 for Group #1, 0x442 for Group #2, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the counter. A read operation should then be performed to read the previous state of the counter. The first address should be read first. The second address (0x441 for Group #1, 0x443 for Group #2, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters.

IMA_RX_GRP*n*_CELL_COUNT_LSB (Receive Cell Count LSBs)

This register contains the least significant bits of a 16 bit count of the number of ATM layer cells received over the Receive links within the group. The register is read only. Status clears upon read.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x450	0x452	0x454	0x456	0x550	0x552	0x554	0x556	0x650	0x652	0x654	0x656	0x750	0x752	0x754	0x756
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7-0	0	Receive Cell Count LSBs	Receive Group Cell Count: This field contains the least significant bits of a 16 bit count of the number of ATM layer cells received over the Receive links within the group. A write operation with data = 0x01 to the first address (0x450 for Group #1, 0x452 for Group #2, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the counter. A read operation should then be performed to read the previous state of the counter. The first address should be read first. The second address (0x451 for Group #1, 0x453 for Group #2, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters.

IMA_RX_GRP*n*_CELL_COUNT_MSB (Receive Cell Count MSBs)

This register contains the most significant bits of a 16 bit count of the number of ATM layer cells received over the Receive links within the group. The register is read only. Status clears upon read.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x451	0x453	0x455	0x457	0x551	0x553	0x555	0x557	0x651	0x653	0x655	0x657	0x751	0x753	0x755	0x757
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7-0	0	Receive Cell Count MSBs	Receive Group Cell Count: This field contains the most significant bits of a 16 bit count of the number of ATM layer cells received over the Receive links within the group. A write operation with data = 0x01 to the first address (0x450 for Group #1, 0x452 for Group #2, etc.) transfers the state of all 16 bits of the counter to registers that are accessible to the microprocessor bus and clears the counter. A read operation should then be performed to read the previous state of the counter. The first address should be read first. The second address (0x451 for Group #1, 0x453 for Group #2, etc.) is read next. A write operation with data = 0x00 to the first address of each group returns back to the raw counters.

IMA_RX_GRP*n*_CFG (Receive Group Status and Control)

This register, in conjunction with the IMA_RX_GRP*n*_CTL and IMA_RX_GRP*n*_FIRST_PHY_ADDR registers, controls the operation of the Receive IMA group.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x4D0	0x4D4	0x4D8	0x4DC	0x5D0	0x5D4	0x5D8	0x5DC	0x6D0	0x6D4	0x6D8	0x6DC	0x7D0	0x7D4	0x7D8	0x7DC
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7	0	Check Group ID	1 = The receive group ID is compared with the expected Group ID as part of link framing 0 = the receive group ID is ignored
6	0	Acquire Frame Length	1 = The frame length and IMA version acquired from the received link is used as part of link framing 0 = The frame length and IMA version from the received link is compared against the expected frame length and IMA version as part of link framing
5–4	0	Maximum Differential Delay	Reserved. Set to 0.
3–2	0	Group Symmetry	0 = Symmetrical configuration and operation 1 = Symmetrical configuration and asymmetrical operation 2 = Asymmetrical configuration and operation 3 = Alternate symmetrical configuration and operation
1–0	0	Frame Length (M)	0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256

IMA_RX_GRP*n*_CTL (Receive Group Control Register)

This register, in conjunction with the IMA_RX_GRP*n*_CFG and IMA_RX_GRP*n*_FIRST_PHY_ADDR registers, controls the operation of the Receive IMA group.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x4D1	0x4D5	0x4D9	0x4DD	0x5D1	0x5D5	0x5D9	0x5DD	0x6D1	0x6D5	0x6D9	0x6DD	0x7D1	0x7D5	0x7D9	0x7DD
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7	0	Group Enable	1 = Group is established and a round-robin is created 0 = Group is not established
6	0	SW Timeout Expired	1 = certain LSM transitions (Usable → Active) are allowed 0 = certain LSM transitions (Usable → Active) are blocked
5	0	Resync Group	1 = Enables the link differential delay synchronization process 0 = disables the link differential delay synchronization process
4	—	Drain Buffer	This bit is used by the software driver to reset the differential delay in T1/E1 mode: 1 = Allows the differential delay buffer to drain excess cell buffering. 0 = Normal delay buffering.
3	—	—	Reserved. Set to 0.
2–0	0x0	Group Size	Sets the number of configured links within group. Range: 0x0–0x7 (1–8 links in group)

IMA_RX_GRP*n*_FIRST_PHY_ADDR (Receive First PHY Address)

This register, in conjunction with the IMA_RX_GRP*n*_CTL and IMA_RX_GRP*n*_CFG registers, controls the operation of the Receive IMA group.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x4D2	0x4D6	0x4DA	0x4DE	0x5D2	0x5D6	0x5DA	0x5DE	0x6D2	0x6D6	0x6DA	0x6DE	0x7D2	0x7D6	0x7DA	0x7DE
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0.
6	—	—	Reserved. Set to 0.
5	0	Rx IMA Version	(IMA OAM Label value) 1 = IMA v1.1 0 = IMA v1.0
4–0	0x00	Link PHY Address	This field contains the PHY port address of the Receive link with the lowest LID in the group. CX28224: Range: 0–1 CX28225: Range: 0–3 CX28229: Range: 0–0x1F

IMA_RX_GRP*n*_ID (Expected Receive Group ID)

This register contains the value of the Expected IMA Group ID field for the received ICP cells.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x4D3	0x4D7	0x4DB	0x4DF	0x5D3	0x5D7	0x5DB	0x5DF	0x6D3	0x6D7	0x6DB	0x6DF	0x7D3	0x7D7	0x7DB	0x7DF
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	0x00	Expected Rx Group ID	This field contains the Group ID expected in the Receive ICP cells of all links in this group. Range: 0x00–0xFF

IMA_RX_GRP*n*_RX_TEST_PATTERN (Receive Group Rx Test Pattern)

This **read-only** register contains the value of the Rx Test Pattern field acquired from the received ICP cells.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x4E0	0x4E8	0x4F0	0x4F8	0x5E0	0x5E8	0x5F0	0x5F8	0x6E0	0x6E8	0x6F0	0x6F8	0x7E0	0x7E8	0x7F0	0x7F8
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	—	Rx Test Pattern	This field reflects the value of the Rx Test Pattern byte acquired from the Receive side test link. Range: 0x00–0xFF

IMA_RX_GRP*n*_STAT_CTL_CHANGE (Receive Group Status & Control Change Indication)

This **read-only** register contains the value of the Status and Control Indication field acquired from the received ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x4E2	0x4EA	0x4F2	0x4FA	0x5E2	0x5EA	0x5F2	0x5FA	0x6E2	0x6EA	0x6F2	0x6FA	0x7E2	0x7EA	0x7F2	0x7FA
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	—	Rx SCCI	This field reflects the value of the Status & Change Control Indication byte acquired from the Receive ICP cells of the monitored link. Range: 0x00–0xFF

IMA_RX_GRP*n*_ACTUAL_GRP_ID (Actual Receive Group ID)

This **read-only** register contains the value of the IMA ID field acquired from the received ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x4E3	0x4EB	0x4F3	0x4FB	0x5E3	0x5EB	0x5F3	0x5FB	0x6E3	0x6EB	0x6F3	0x6FB	0x7E3	0x7EB	0x7F3	0x7FB
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	—	Actual Rx Group ID	This field contains the Group ID acquired from the Receive ICP cells of the monitored link. Range: 0x00–0xFF

IMA_RX_GRP*n*_STAT_CTL (Receive Group Status and Control)

This **read-only** register contains the value of the Group Status and Control field acquired from the received ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x4E4	0x4EC	0x4F4	0x4FC	0x5E4	0x5EC	0x5F4	0x5FC	0x6E4	0x6EC	0x6F4	0x6FC	0x7E4	0x7EC	0x7F4	0x7FC
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–4	—	Group State	0 = Start-up 1 = Start-up-Ack 2 = Config-Abort–Unsupported M 3 = Config-Abort–Incompatible Symmetry 4 = Config-Abort–Unsupported IMA Version 5–7 = Reserved for other Config-Abort states 8 = Insufficient Links 9 = Blocked 0xA = Operational 0xB–F = reserved
3–2	—	Group Symmetry	0 = Symmetrical configuration and operation 1 = Symmetrical configuration and asymmetrical operation 2 = Asymmetrical configuration and operation
1–0	—	Frame Length (M)	0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256

IMA_RX_GRP*n*_TIMING_INFO (Receive Timing Information)

This **read-only** register contains the value of the Transmit Timing Information field acquired from the received ICP cells.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x4E5	0x4ED	0x4F5	0x4FD	0x5E5	0x5ED	0x5F5	0x5FD	0x6E5	0x6ED	0x6F5	0x6FD	0x7E5	0x7ED	0x7F5	0x7FD
CX28224	Not Applicable														
CX28225	Not Applicable														
CX28229															

Bit	Default	Name	Description
7	—	—	Unused
6	—	—	Unused
5	—	Rx Clock Mode	0 = Independent Transmit Clock (ITC) 1 = Common Transmit Clock (CTC)
4–0	—	Timing Reference Link ID	This field contains the LID of the Receive TRL. Range: 0x0–0x1F

IMA_RX_GRP*n*_TEST_CTL (Receive Test Control)

This **read-only** register contains the value of the Tx Test Control field acquired from the received ICP cells.

Group 1–16 Address

n=1	*n*=2	*n*=3	*n*=4	*n*=5	*n*=6	*n*=7	*n*=8	*n*=9	*n*=10	*n*=11	*n*=12	*n*=13	*n*=14	*n*=15	*n*=16
0x4E6	0x4EE	0x4F6	0x4FE	0x5E6	0x5EE	0x5F6	0x5FE	0x6E6	0x6EE	0x6F6	0x6FE	0x7E6	0x7EE	0x7F6	0x7FE
CX28224	Not Applicable														
CX28225	Not Applicable														
CX28229															

Bit	Default	Name	Description
7	—	—	Unused
6	—	—	Unused
5	—	Test Link Command	0 = Inactive 1 = Active
4–0	—	Test Link ID	This field contains the LID of the Receive Test Link. Range: 0x0–0x1F

IMA_RX_GRP*n*_TX_TEST_PATTERN (Receive Group Tx Test Pattern)

This **read-only** register contains the value of the Tx Test Pattern field acquired from the received ICP cells.

Group 1–16 Address

***n*=1**	***n*=2**	***n*=3**	***n*=4**	***n*=5**	***n*=6**	***n*=7**	***n*=8**	***n*=9**	***n*=10**	***n*=11**	***n*=12**	***n*=13**	***n*=14**	***n*=15**	***n*=16**
0x4E7	0x4EF	0x4F7	0x4FF	0x5E7	0x5EF	0x5F7	0x5FF	0x6E7	0x6EF	0x6F7	0x6FF	0x7E7	0x7EF	0x7F7	0x7FF
CX28224		Not Applicable													
CX28225				Not Applicable											
CX28229															

Bit	Default	Name	Description
7–0	—	Tx Test Pattern	If the Test Link Command is set to Active, the Tx Test Pattern is accessed from the ICP cell of the Transmit Test Link. This register should be read multiple times (debounced) to ensure receipt of a valid test pattern. Range: 0x00–0xFF

7.3 IMA Link Registers

The IMA Link layer contains configuration and status information that is associated with IMA groups or pass-through facilities.

0x41E—IMA_LNK_SEM (Link Table Control Register)

For the following bits, 1 = the link table is being updated, 0 = the link table is not being updated. The update enable must be set to 1 prior to writing the link table. All elements of the link table must be re-written. After writing to all 8 elements, the update enable is reset to 0. The link tables are described below.

NOTE:This register cannot be read back.

Bit	Default	Name	Description
7	0	Update Enable for Receive facilities 24–31	addresses 0x780–0x787, 0x7A8–0x7AF (Not defined for CX28224 and CX28225)
6	0	Update Enable for Receive facilities 16–23	addresses 0x680–0x687, 0x6A8–0x6AF (Not defined for CX28224 and CX28225)
5	0	Update Enable for Receive facilities 8–15	addresses 0x580–0x587, 0x5A8–0x5AF (Not defined for CX28224 and CX28225)
4	0	Update Enable for Receive facilities 0–7	addresses 0x480–0x487, 0x4A8–0x4AF
3	0	Update Enable for Transmit facilities 24–31	addresses 0x760–0x767, 0x770–0x777 (Not defined for CX28224 and CX28225)
2	0	Update Enable for Transmit facilities 16–23	addresses 0x660–0x667, 0x670–0x677 (Not defined for CX28224 and CX28225)
1	0	Update Enable for Transmit facilities 8–15	addresses 0x560–0x567, 0x570–0x577 (Not defined for CX28224 and CX28225)
0	0	Update Enable for Transmit facilities 0–7	addresses 0x460–0x467, 0x470–0x477

IMA_TX_LNK*n*_CTL (Transmit Link Control Register)

This register, in conjunction with IMA_TX_LNK*n*_ID register, configures the IMA link attributes for the Transmit port.

hex address:

n	Address
0	0x460
1	0x461
2	0x462
3	0x463
4	0x464
5	0x465
6	0x466
7	0x467
8	0x560
9	0x561
10	0x562
11	0x563
12	0x564
13	0x565
14	0x566
15	0x567

n	Address
16	0x660
17	0x661
18	0x662
19	0x663
20	0x664
21	0x665
22	0x666
23	0x667
24	0x760
25	0x761
26	0x762
27	0x763
28	0x764
29	0x765
30	0x766
31	0x767

Bit	Default	Name	Description
7	0	Link Assigned	1 = Facility is part of IMA Group 0 = Facility is a bypass channel (pass-through or unassigned)
6	0	Link Inhibit	1 = Link is blocked from use 0 = Link is not inhibited
5	0	Link Fault	1 = Link Fault Failure is active 0 = Link Fault Failure is inactive
4–0	0	Next Link PHY Address	This field contains the PHY address of the next link in the IMA Group. If the link is a pass-through facility, this field is ignored but is recommended to be set to the PHY address of the pass-through facility (i.e., set to 0 for PHY address 0, set to 1 for PHY address 1, etc.). CX28224: Range: 0–1 CX28225: Range: 0–3 CX28229: Range: 0–0x1F

IMA_TX_LNK*n*_STATE (Transmit Link Status Register)

This **read-only** register provides state and status information for the Transmit link.

hex address:

n	Address
0	0x468
1	0x469
2	0x46A
3	0x46B
4	0x46C
5	0x46D
6	0x46E
7	0x46F
8	0x568
9	0x569
10	0x56A
11	0x56B
12	0x56C
13	0x56D
14	0x56E
15	0x56F

n	Address
16	0x668
17	0x669
18	0x66A
19	0x66B
20	0x66C
21	0x66D
22	0x66E
23	0x66F
24	0x768
25	0x769
26	0x76A
27	0x76B
28	0x76C
29	0x76D
30	0x76E
31	0x76F

Bit	Default	Name	Description
7–6	—	Tx-Stuff-IMA Counter	This field contains a count of the number of Near-End Transmit cell stuffing events. Upon a read of this address, the contents of the counter is transferred to a register that is accessible to the microprocessor bus and the counter is cleared.
5	—	—	Reserved.
4	—	—	Reserved.
3	0	Waiting for SW Timer	1 = a transition of the Transmit LSM is waiting for an enable from software 0 = no transition of the LSM is waiting for software
2–0	0x0	NE Tx LSM State	0 = Not In Group 1 = Unusable—no reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active

IMA_TX_LNK*n*_ID (Transmit Link ID Register)

This register, in conjunction with IMA_TX_LNK*n*_CTL register, configures the IMA link attributes for the Transmit port.

hex address:

n	Address
0	0x470
1	0x471
2	0x472
3	0x473
4	0x474
5	0x475
6	0x476
7	0x477
8	0x570
9	0x571
10	0x572
11	0x573
12	0x574
13	0x575
14	0x576
15	0x577

n	Address
16	0x670
17	0x671
18	0x672
19	0x673
20	0x674
21	0x675
22	0x676
23	0x677
24	0x770
25	0x771
26	0x772
27	0x773
28	0x774
29	0x775
30	0x776
31	0x777

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0
6	—	—	Reserved. Set to 0
5	—	—	Reserved. Set to 0
4	—	—	Reserved. Set to 0
3	—	—	Reserved. Set to 0
2–0	—	Link ID	This field contains the Transmit Link ID assigned to this facility. Range: 0x00–0x07

IMA_RX_LNK*n*_CTL (Receive Link Control Register)

This register, in conjunction with IMA_RX_LNK*n*_ID register, configures the IMA link attributes for the Receive port.

hex address:

n	Address
0	0x480
1	0x481
2	0x482
3	0x483
4	0x484
5	0x485
6	0x486
7	0x487
8	0x580
9	0x581
10	0x582
11	0x583
12	0x584
13	0x585
14	0x586
15	0x587

n	Address
16	0x680
17	0x681
18	0x682
19	0x683
20	0x684
21	0x685
22	0x686
23	0x687
24	0x780
25	0x781
26	0x782
27	0x783
28	0x784
29	0x785
30	0x786
31	0x787

Bit	Default	Name	Description
7	0	Link Assigned	1 = Facility is part of IMA Group 0 = Facility is a bypass channel (pass-through or unassigned)
6–5	0	Link State	0 = Link is not inhibited 1 = Link Fault Failure is active 2 = Link is blocked from use 3 = Rx Failed condition
4–0	0	Next Link PHY Address	This field contains the PHY address of the next link in the IMA Group. If the link is a pass-through facility, this field is ignored but is recommended to be set to the PHY address of the pass-through facility (i.e., set to 0 for PHY address 0, set to 1 for PHY address 1, etc.). CX28224: Range: 0–1 CX28225: Range: 0–3 CX28229: Range: 0–0x1F

IMA_RX_LNK*n*_STATE (Receive Link Status Register)

This **read-only** register provides state and status information for the Receive link.

hex address:

n	Address
0	0x488
1	0x489
2	0x48A
3	0x48B
4	0x48C
5	0x48D
6	0x48E
7	0x48F
8	0x588
9	0x589
10	0x58A
11	0x58B
12	0x58C
13	0x58D
14	0x58E
15	0x58F

n	Address
16	0x688
17	0x689
18	0x68A
19	0x68B
20	0x68C
21	0x68D
22	0x68E
23	0x68F
24	0x788
25	0x789
26	0x78A
27	0x78B
28	0x78C
29	0x78D
30	0x78E
31	0x78F

Bit	Default	Name	Description
7–6	—	Rx-Stuff-IMA Counter	This field contains a count of the number of Near-End Receive cell stuffing events. Upon a read of this address, the contents of the counter is transferred to a register that is accessible to the microprocessor bus and the counter is cleared.
5	—	—	Reserved.
4	—	—	Reserved.
3	0	Waiting for SW Timer	1 = a transition of the Receive LSM is waiting for an enable from software 0 = no transition of the LSM is waiting for software
2–0	0	NE Rx LSM State	0 = Not In Group 1 = Unusable—no reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active

IMA_RX_LNK*n*_DEFECT (Receive Link Defects Register)

This register provides state and status information for the Receive link. This register is primarily **read-only** except for bit 1 which is read/write.

hex address:

n	Address
0	0x490
1	0x491
2	0x492
3	0x493
4	0x494
5	0x495
6	0x496
7	0x497
8	0x590
9	0x591
10	0x592
11	0x593
12	0x594
13	0x595
14	0x596
15	0x597

n	Address
16	0x690
17	0x691
18	0x692
19	0x693
20	0x694
21	0x695
22	0x696
23	0x697
24	0x790
25	0x791
26	0x792
27	0x793
28	0x794
29	0x795
30	0x796
31	0x797

Bit	Default	Name	Description
7	—	Δ (LIF Defect)	1 = The LIF defect has changed state since the last time this register was read 0 = the LIF defect has not changed state
6	—	LIF Defect	1 = The LIF defect is currently active 0 = the LIF defect is inactive
5	—	Δ (LODS Defect)	1 = The LODS defect has changed state since the last time this register was read 0 = the LODS defect has not changed state
4	—	LODS Defect	1 = The LODS defect is currently active 0 = the LODS defect is inactive
3	—	Δ (RDI Defect)	1 = The RDI defect has changed state since the last time this register was read 0 = the RDI defect has not changed state
2	—	RDI Defect	1 = The RDI defect is currently active 0 = the RDI defect is inactive
1	—	PHY Defect	1 = A PHY defect is active 0 = all PHY defects are inactive
0	—	Rx_TRL Error	This bit is set high if the transition detector for the Rx_TRL input detects a bad signal. This bit is active high and is reset upon reading this address.

IMA_FE_TX_LNK*n*_CFG (FE Transmit Configuration Register)

This **read-only** register provides Far-End Transmit configuration information for the Receive link.

hex address:

n	Address
0	0x498
1	0x499
2	0x49A
3	0x49B
4	0x49C
5	0x49D
6	0x49E
7	0x49F
8	0x598
9	0x599
10	0x59A
11	0x59B
12	0x59C
13	0x59D
14	0x59E
15	0x59F

n	Address
16	0x698
17	0x699
18	0x69A
19	0x69B
20	0x69C
21	0x69D
22	0x69E
23	0x69F
24	0x798
25	0x799
26	0x79A
27	0x79B
28	0x79C
29	0x79D
30	0x79E
31	0x79F

Bit	Default	Name	Description
7–6	—	Frame Length (M)	This field contains the contents of the frame length field for the ICP cell arriving on this facility. 0 = M is 32 1 = M is 64 2 = M is 128 3 = M is 256
5	—	IMA Version	(IMA OAM Label value) 1 = IMA v1.1 0 = IMA v1.0
4–0	—	Link ID	This field contains the contents of the Link ID field for the ICP cell arriving on this facility. Range: 0x0–0xF.

IMA_FE_LNK*n*_STATE (FE Link Status Register)

This **read-only** register provides Far-End link status information for the facility.

hex address:

n	Address
0	0x4A0
1	0x4A1
2	0x4A2
3	0x4A3
4	0x4A4
5	0x4A5
6	0x4A6
7	0x4A7
8	0x5A0
9	0x5A1
10	0x5A2
11	0x5A3
12	0x5A4
13	0x5A5
14	0x5A6
15	0x5A7

n	Address
16	0x6A0
17	0x6A1
18	0x6A2
19	0x6A3
20	0x6A4
21	0x6A5
22	0x6A6
23	0x6A7
24	0x7A0
25	0x7A1
26	0x7A2
27	0x7A3
28	0x7A4
29	0x7A5
30	0x7A6
31	0x7A7

Bit	Default	Name	Description
7–5	—	FE Tx LSM State	0 = Not In Group 1 = Unusable—no reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active
4–2	—	FE Rx LSM State	0 = Not In Group 1 = Unusable—no reason given 2 = Unusable—Fault 3 = Unusable—Mis-connected 4 = Unusable—Blocked 5 = Unusable—Failed 6 = Usable 7 = Active

Bit	Default	Name	Description (Continued)
1–0	—	FE Rx Defect Indicator	0 = No Defects 1 = Physical link defect 2 = LIF defect 3 = LODS defect

IMA_RX_LNK*n*_ID (Receive Link ID Register)

This register, in conjunction with IMA_RX_LNK*n*_CTL register, configures the IMA link attributes for the Receive port.

hex address:

n	Address
0	0x4A8
1	0x4A9
2	0x4AA
3	0x4AB
4	0x4AC
5	0x4AD
6	0x4AE
7	0x4AF
8	0x5A8
9	0x5A9
10	0x5AA
11	0x5AB
12	0x5AC
13	0x5AD
14	0x5AE
15	0x5AF

n	Address
16	0x6A8
17	0x6A9
18	0x6AA
19	0x6AB
20	0x6AC
21	0x6AD
22	0x6AE
23	0x6AF
24	0x7A8
25	0x7A9
26	0x7AA
27	0x7AB
28	0x7AC
29	0x7AD
30	0x7AE
31	0x7AF

Bit	Default	Name	Description
7	—	—	Reserved. Set to 0
6	—	—	Reserved. Set to 0
5	—	—	Reserved. Set to 0
4–0	—	Link ID	This field contains the Receive Link ID assigned to this facility. Range: 0x00–0x1F

IMA_RX_LNK*n*_IV_CNT (IMA Violation Counter Register)

This **read-only** register contains a count of the IV-IMA Anomalies for the Receive link.

hex address:

n	Address
0	0x4B0
1	0x4B1
2	0x4B2
3	0x4B3
4	0x4B4
5	0x4B5
6	0x4B6
7	0x4B7
8	0x5B0
9	0x5B1
10	0x5B2
11	0x5B3
12	0x5B4
13	0x5B5
14	0x5B6
15	0x5B7

n	Address
16	0x6B0
17	0x6B1
18	0x6B2
19	0x6B3
20	0x6B4
21	0x6B5
22	0x6B6
23	0x6B7
24	0x7B0
25	0x7B1
26	0x7B2
27	0x7B3
28	0x7B4
29	0x7B5
30	0x7B6
31	0x7B7

Bit	Default	Name	Description
7–0	—	IV-IMA Counter	This field contains a count of the ICP-ERR, ICP-INV, and ICP-MIS anomalies. Writing a 0x01 to address 0x4B0 will freeze the value of all the IV-IMA and OIF-IMA counters in the defined registers. The internal counters are cleared by this action. After all the registers have been read, writing a 0x00 to address 0x4B0 will release the “freeze” and the defined registers will reflect the current anomaly count.

IMA_RX_LNK*n*_OIF_CNT (Out-of-IMA Frame Counter Register)

This **read-only** register contains a count of the OIF-IMA Anomalies for the Receive link.

hex address:

n	Address
0	0x4B8
1	0x4B9
2	0x4BA
3	0x4BB
4	0x4BC
5	0x4BD
6	0x4BE
7	0x4BF
8	0x5B8
9	0x5B9
10	0x5BA
11	0x5BB
12	0x5BC
13	0x5BD
14	0x5BE
15	0x5BF

n	Address
16	0x6B8
17	0x6B9
18	0x6BA
19	0x6BB
20	0x6BC
21	0x6BD
22	0x6BE
23	0x6BF
24	0x7B8
25	0x7B9
26	0x7BA
27	0x7BB
28	0x7BC
29	0x7BD
30	0x7BE
31	0x7BF

Bit	Default	Name	Description
7	—	—	Reserved.
6	—	—	Reserved.
5	—	—	Reserved.
4	—	—	Reserved.
3–0	—	OIF-IMA Counter	This field contains a count of the OIF anomalies. Writing a 0x01 to address 0x4B0 will freeze the value of all the IV-IMA and OIF-IMA counters in the defined registers. The internal counters are cleared by this action. After all the registers have been read, writing a 0x00 to address 0x4B0 will release the “freeze” and the defined registers will reflect the current anomaly count.

IMA_FE_TX_LNK*n*_GRP_ID (FE Transmit Group ID Register)

This **read-only** register contains the value of the IMA ID field acquired from the received ICP for the Receive link.

hex address:

n	Address
0	0x4C0
1	0x4C1
2	0x4C2
3	0x4C3
4	0x4C4
5	0x4C5
6	0x4C6
7	0x4C7
8	0x5C0
9	0x5C1
10	0x5C2
11	0x5C3
12	0x5C4
13	0x5C5
14	0x5C6
15	0x5C7

n	Address
16	0x6C0
17	0x6C1
18	0x6C2
19	0x6C3
20	0x6C4
21	0x6C5
22	0x6C6
23	0x6C7
24	0x7C0
25	0x7C1
26	0x7C2
27	0x7C3
28	0x7C4
29	0x7C5
30	0x7C6
31	0x7C7

Bit	Default	Name	Description
7–0	—	Actual Rx Group ID	This field contains the value of the Group ID field from the ICP cells for this facility. Range: 0x00–0xFF

8 Electrical and Mechanical Specifications

This chapter describes the electrical and mechanical aspects of the CX2822x. It includes timing diagrams, absolute maximum ratings, DC characteristics, and mechanical drawings.

8.1 Timing Specifications

This section provides timing diagrams and descriptions for the various interfaces of the CX2822x. The timing relationship labels are numbered when they occur more than once in a diagram, so each label is unique. This numbering aids in identifying the appropriate label in the timing table. Signals are measured at the 50% point of the changing edge, except for those involving high impedance transitions, which are measured at 10% and 90%.

Figure 8-1 and Figure 8-2 illustrate how input and output waveforms are defined.

Figure 8-1. Input Waveform

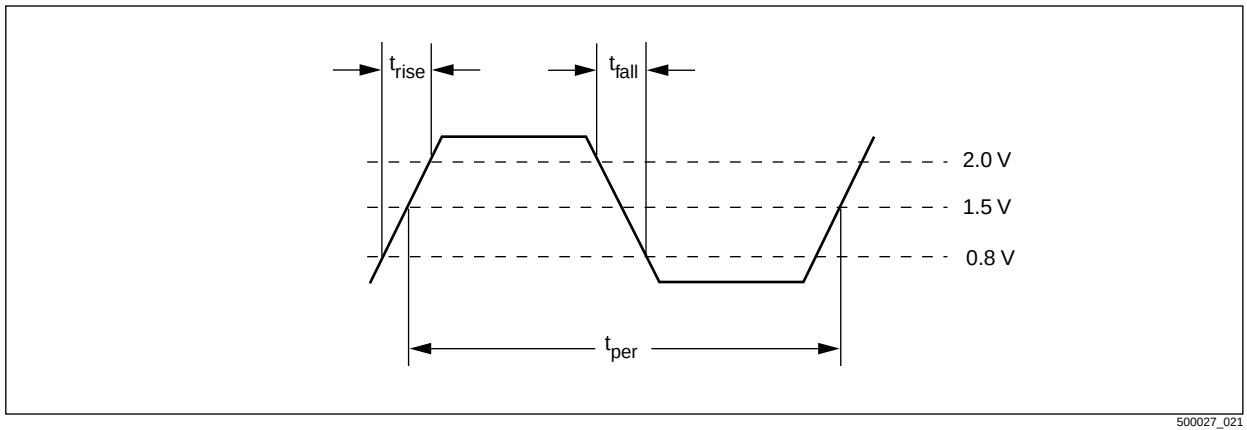
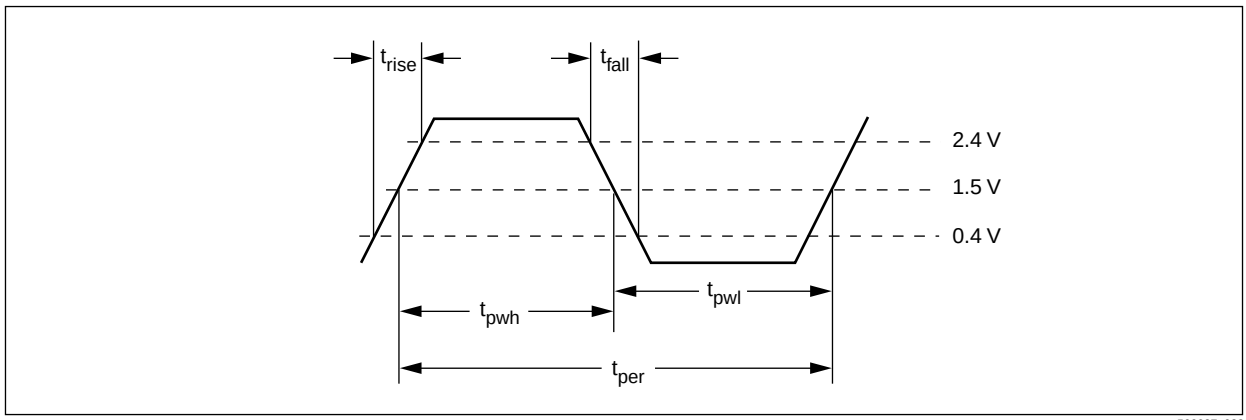


Figure 8-2. Output Waveform



8.1.1 Microprocessor Timing

Figures 8-3 through 8-6 and Tables 8-1 through 8-4 show the timing requirements and characteristics of the microprocessor interface. Capacitive load on all signals is 50pF.

Figure 8-3. Microprocessor Timing Diagram—Asynchronous Read

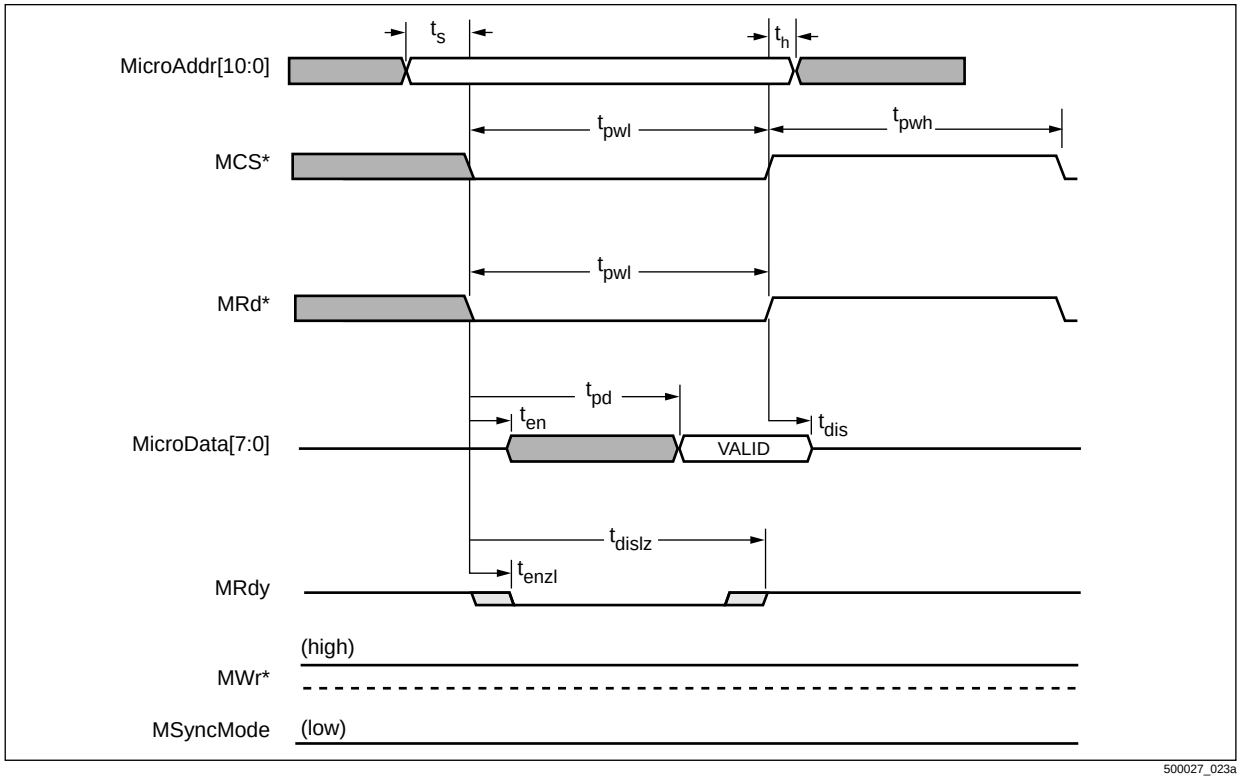


Table 8-1. Microprocessor Timing Table—Asynchronous Read

Label	Description	Min	Max	Unit
MicroClk	Microprocessor Clock	—	50	MHz
t_{pwh}	Pulse Width High	3 * MicroClk + 15	—	ns
t_{pwl}	Pulse Width Low	3 * MicroClk + 15	—	ns
t_s	Setup, MicroAddr[10:0] to the falling edge of (MCS* + MRd*)(1)	2	—	ns
t_h	Hold, MicroAddr[10:0] from the rising edge of (MCS* + MRd*)(2)	7	—	ns
t_{en}	Enable, MicroData[7:0] from the falling edge of (MCS* + MRd*)(1)	2	20	ns
t_{pd}	Propagation Delay, MicroData[7:0] from the falling edge of (MCS* + MRd*)(1)	2 * MicroClk	3 * MicroClk +14	ns
t_{dis}	Disable, MicroData[7:0] from the rising edge of (MCS* + MRd*)(2)	2	20	ns
t_{enzl}	Enable, MRdy from the falling edge of (MCS* + MRd*)(1)	1	20	ns
t_{dislz}	Disable, MRdy from the falling edge of (MCS* + MRd*)(1)	2.5 * MicroClk	3.5 * MicroClk +15	ns

FOOTNOTE:
(1) Timing starts from whichever is asserted last.
(2) Timing relative to whichever goes inactive first.

Figure 8-4. MIcroprocessor Timing Diagram—Asynchronous Write

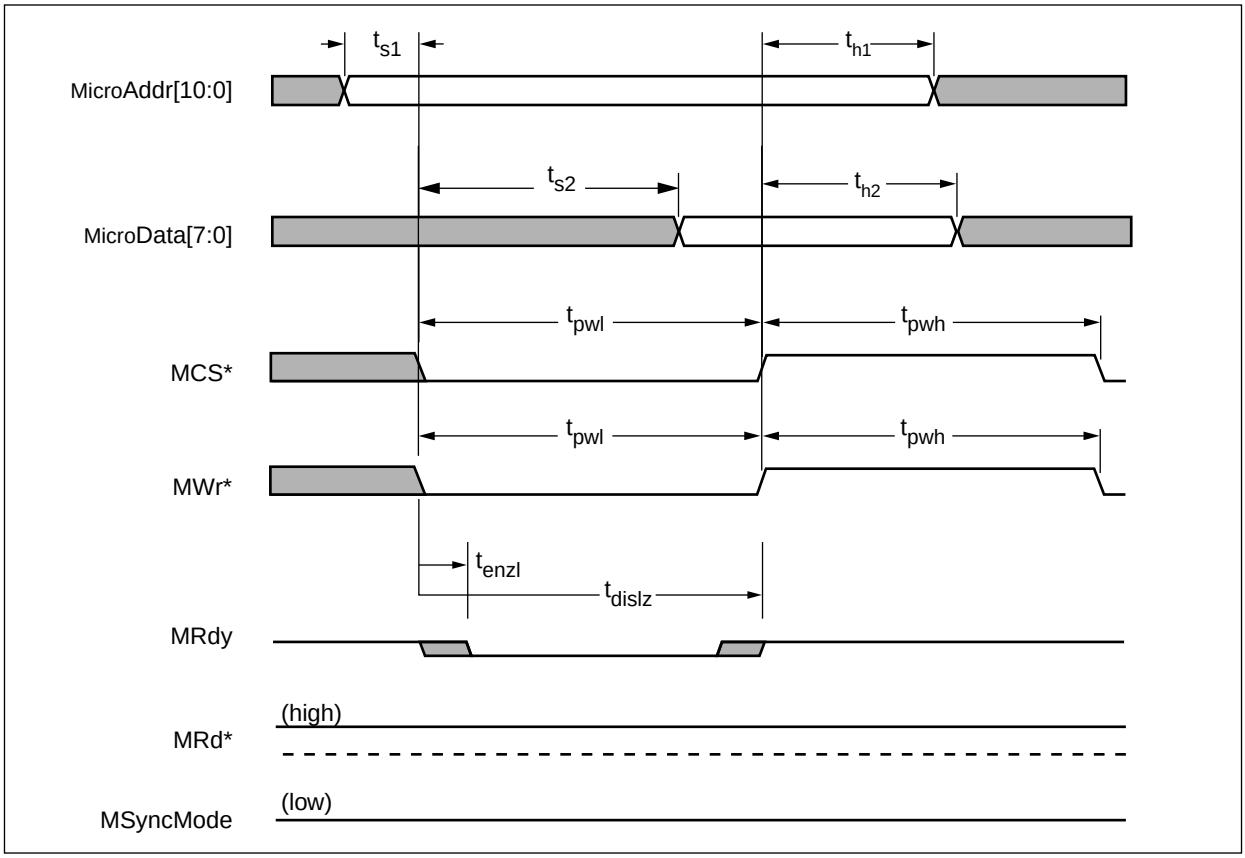
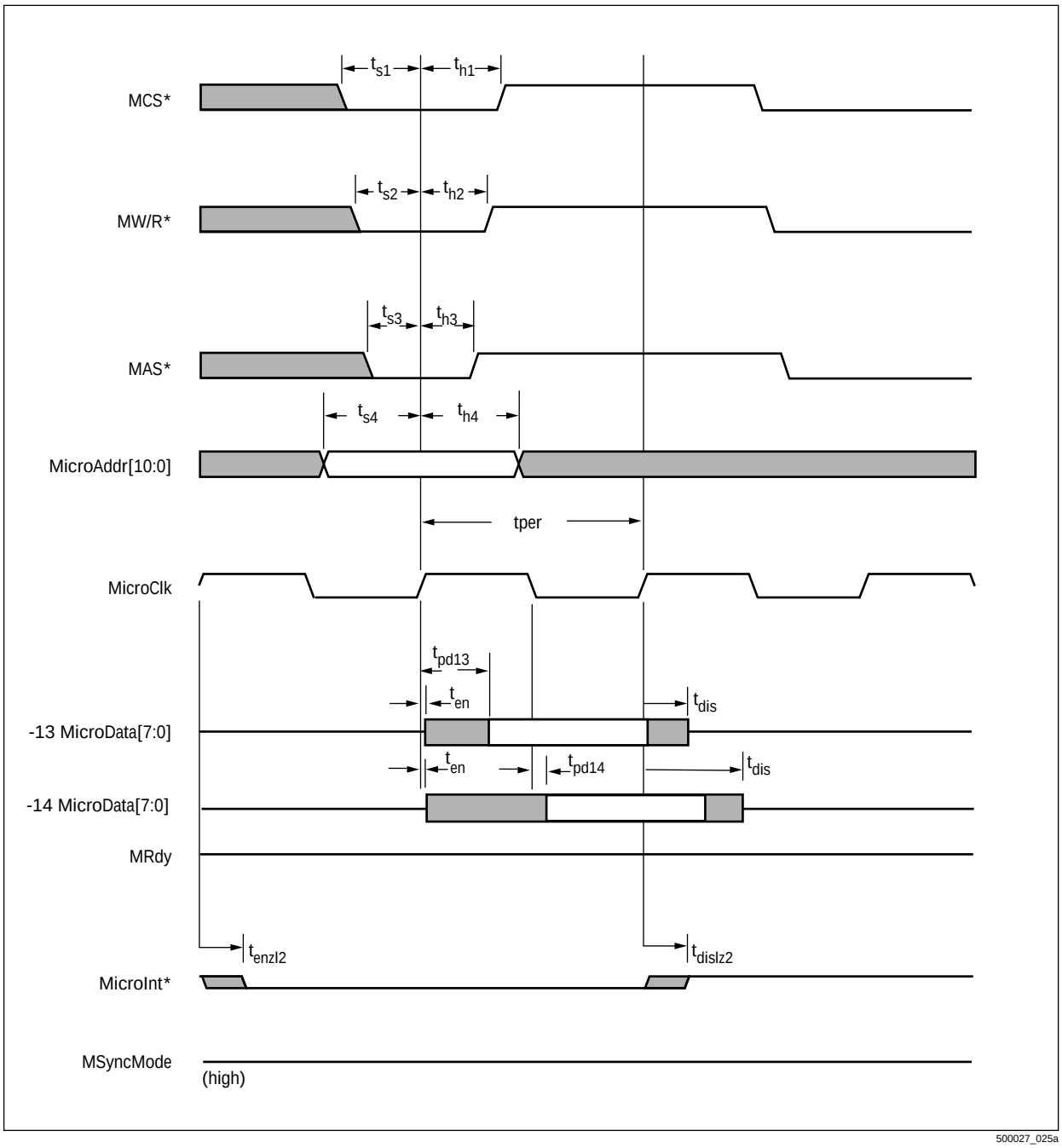


Table 8-2. Microprocessor Timing Table—Asynchronous Write

Label	Description	Min	Max	Unit
MicroClk	Microprocessor Clock	—	50	MHz
t_{pwl}	Pulse Width Low (MCS* + MWr*)	3 * MicroClk + 15	—	ns
t_{pwh}	Pulse Width High (MCS* + MWr*)	3 * MicroClk + 15	—	ns
t_{s1}	Setup, MicroAddr[10:0] to the falling edge of (MCS* + MWr*)(1)	2	—	ns
t_{h1}	Hold, MicroAddr[10:0] from the rising edge of (MCS* + MWr*)(2)	7	—	ns
t_{s2}	Setup, MicroData[7:0] from the falling edge of (MCS* + MWr*)(1)	—	1 MicroClk	ns
t_{h2}	Hold, MicroData[6:0] from the rising edge of (MCS* + MWr*)(2)	7	—	ns
t_{enzl}	Enable, MRdy from the falling edge of (MCS* + MWr*)(1)	2	20	ns
t_{dislz}	Disable, MRdy from the falling edge of (MCS* + MWr*)(1)	2.5 * MicroClk	3.5 * MicroClk +15	ns

FOOTNOTE:
(1) Timing starts from whichever is asserted last.
(2) Timing relative to whichever goes inactive first.

Figure 8-5. Microprocessor Timing Diagram—Synchronous Read



500027_025a

Table 8-3. Microprocessor Timing Table—Synchronous Read

Label	Description	Min	Max	Unit
MicroClk	Microprocessor Clock	—	25	MHz
t_{per}	Microprocessor Clock Period Duty Cycle	40	60	%
t_{s1}	Setup, MCS* to the rising edge of MicroClk	5	—	ns
t_{h1}	Hold, MCS* from the rising edge of MicroClk	2	—	ns
t_{s2}	Setup, MW/R, MRd* to the rising edge of MicroClk	5	—	ns
t_{h2}	Hold, MW/R, MRd* from the rising edge of MicroClk	2	—	ns
t_{s3}	Setup, MAS* to the rising edge of MicroClk	5	—	ns
t_{h3}	Hold, MAS* from the rising edge of MicroClk	2	—	ns
t_{s4}	Setup, MicroAddr[10:0] to the rising edge of MicroClk	5	—	ns
t_{h4}	Hold, MicroAddr[10:0] from the rising edge of MicroClk	2	—	ns
t_{en}	Enable, MicroData[7:0] from the rising edge of MicroClk	2	15	ns
t_{pd13}	Propagation Delay, MicroData[7:0] from the rising edge of MicroClk	2	26	ns
t_{pd14}	Propagation Delay, MicroData[7:0] from the falling edge of MicroClk	2	10	ns
t_{dis}	Disable, MicroData[7:0] from the rising edge of MicroClk	2	15	ns
t_{enzl2}	Enable, MicroInt* from the rising edge of MicroClk	2	15	ns
t_{dislz2}	Disable, MicroInt* from the rising edge of MicroClk	2	15	ns

Figure 8-6. Microprocessor Timing Diagram—Synchronous Write

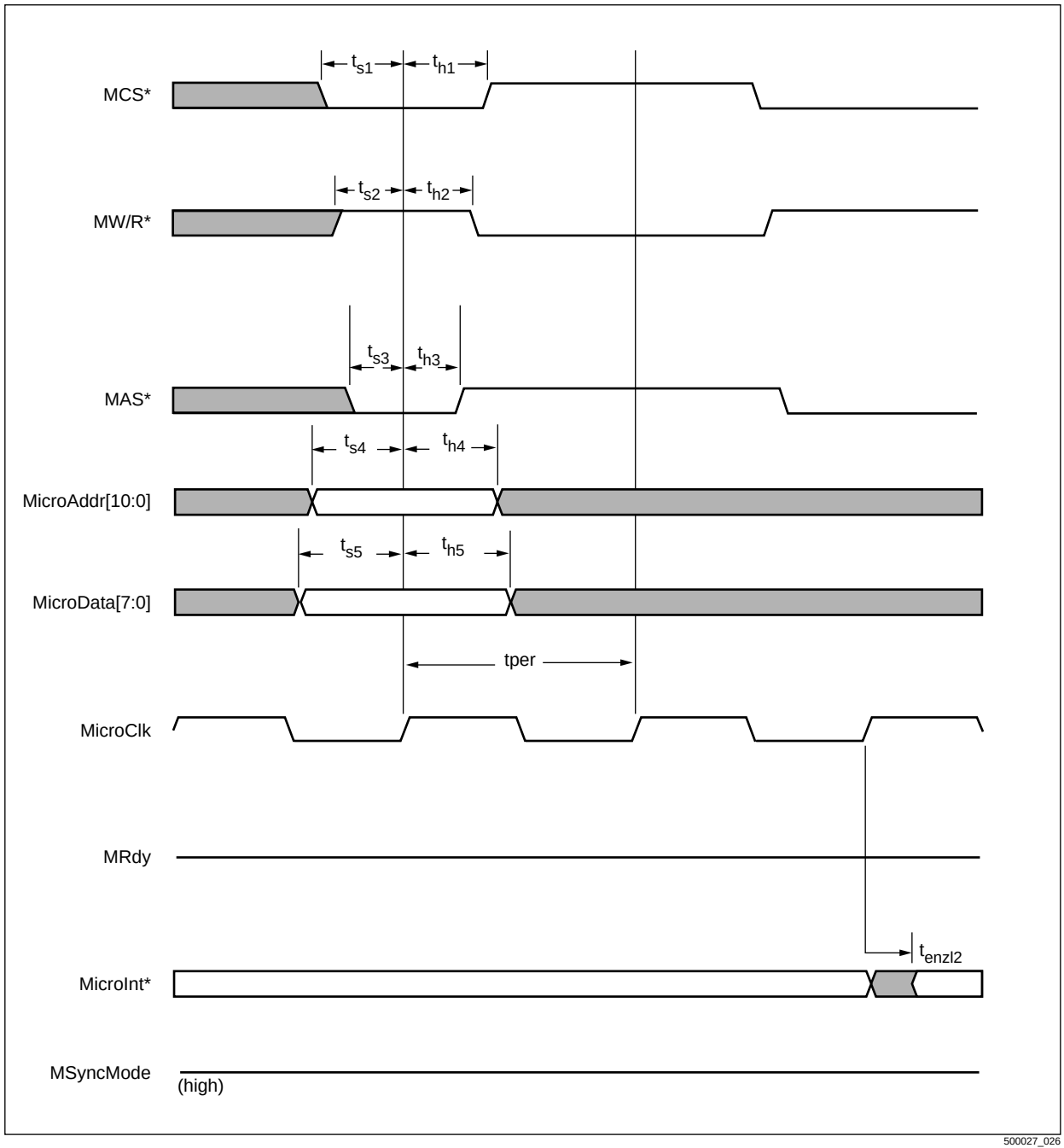


Table 8-4. Microprocessor Timing Table—Synchronous Write

Label	Description	Min	Max	Unit
MicroClk	Microprocessor Clock	—	25	MHz
t_{per}	Microprocessor Clock Period Duty Cycle	40	60	%
t_{s1}	Setup, MCS* to the rising edge of MicroClk	5	—	ns
t_{h1}	Hold, MCS* from the rising edge of MicroClk	2	—	ns
t_{s2}	Setup, MW/R, MRd* to the rising edge of MicroClk	5	—	ns
t_{h2}	Hold, MW/R, MRd* from the rising edge of MicroClk	2	—	ns
t_{s3}	Setup, MAS* to the rising edge of MicroClk	5	—	ns
t_{h3}	Hold, MAS* from the rising edge of MicroClk	2	—	ns
t_{s4}	Setup, MicroAddr[10:0] to the rising edge of MicroClk	5	—	ns
t_{h4}	Hold, MicroAddr[10:0] from the rising edge of MicroClk	2	—	ns
t_{s5}	Setup, MicroData[7:0] to the rising edge of MicroClk	5	—	ns
t_{h5}	Hold, MicroData[7:0] from the rising edge of MicroClk	2	—	ns
t_{enzI2}	Enable, MicroInt* from the rising edge of MicroClk	2	15	ns

8.1.2 Framer (Line) Interface Timing

Figures 8-7 through 8-8 and Tables 8-5 through 8-6 show the timing requirements and characteristics of the Framer (Line) interface. Diagrams are shown with the rising edge as the active edge. See "0x05—IOMODE (Input/Output Mode Control Register)" on page 7-32.

Figure 8-7. Framer (Line) Transmit Timing Diagram

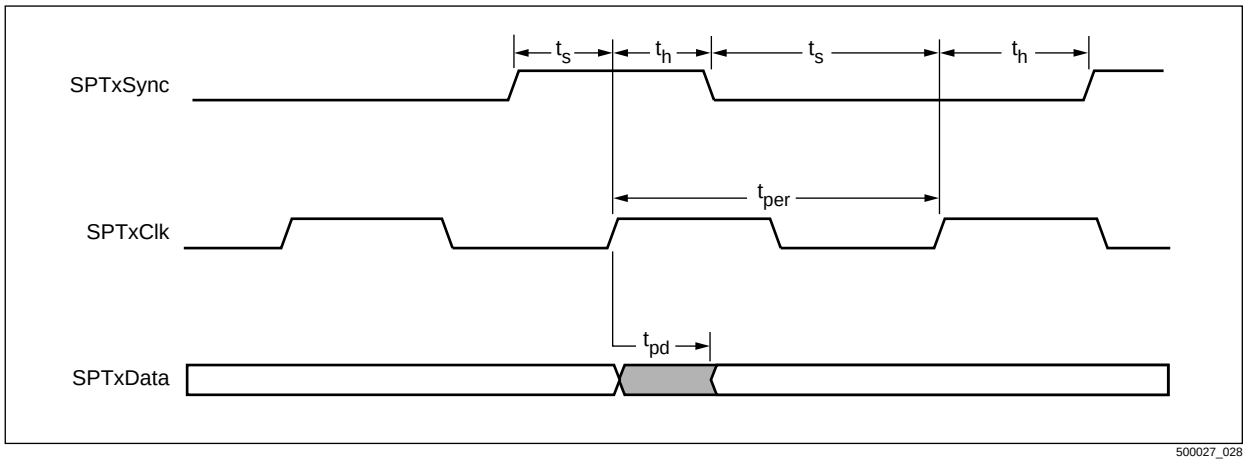


Table 8-5. Framer (Line) Transmit Timing Table

Label	Description	Min	Max	Unit
	Frequency	—	10	MHz
	SPTxClk duty cycle	40	60	%
t_s	Setup, SPTxSync to the active edge of SPTxClk	10	—	ns
t_h	Hold, SPTxSync from the active edge of SPTxClk	10	—	ns
t_{pd}	Propagation Delay, SPTxData from the active edge of SPTxClk	1	17	ns

Figure 8-8. Framer (Line) Receive Timing Diagram

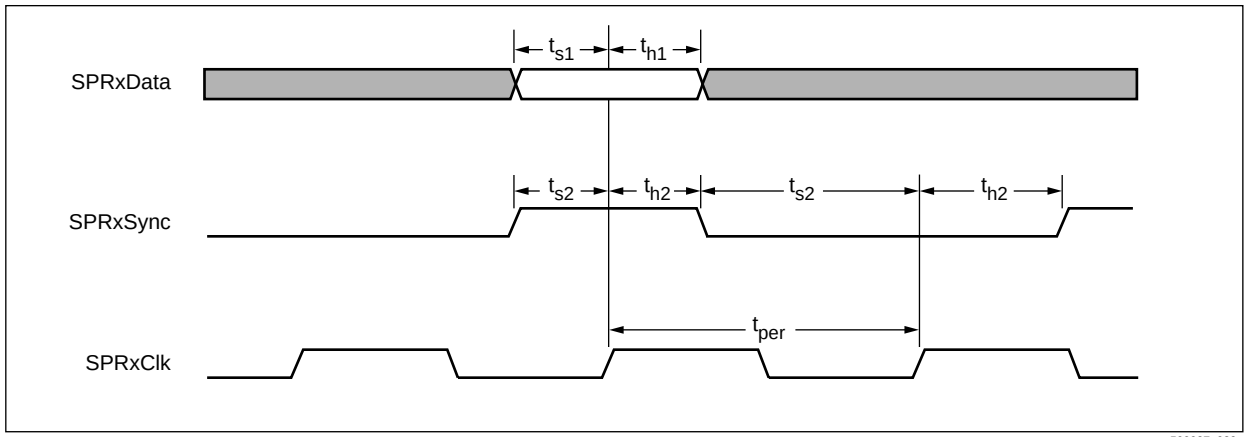


Table 8-6. Framer (Line) Receive Timing Table

Label	Description	Min	Max	Unit
	Frequency	—	10	MHz
	SPRxClk duty cycle	40	60	%
t_{s1}	Setup, SPRxData to the active edge of SPRxClk	6	—	ns
t_{h1}	Hold, SPRxData from the active edge of SPRxClk	3	—	ns
t_{s2}	Setup, SPRxSync to the active edge of SPRxClk	10	—	ns
t_{h2}	Hold, SPRxSync from the active edge of SPRxClk	10	—	ns

8.1.3 UTOPIA Interface Timing (ATM Layer)

Figures 8-9 through 8-10 and Tables 8-7 through 8-8 show the timing requirements and characteristics of the UTOPIA interface.

Figure 8-9. UTOPIA Transmit Timing Diagram

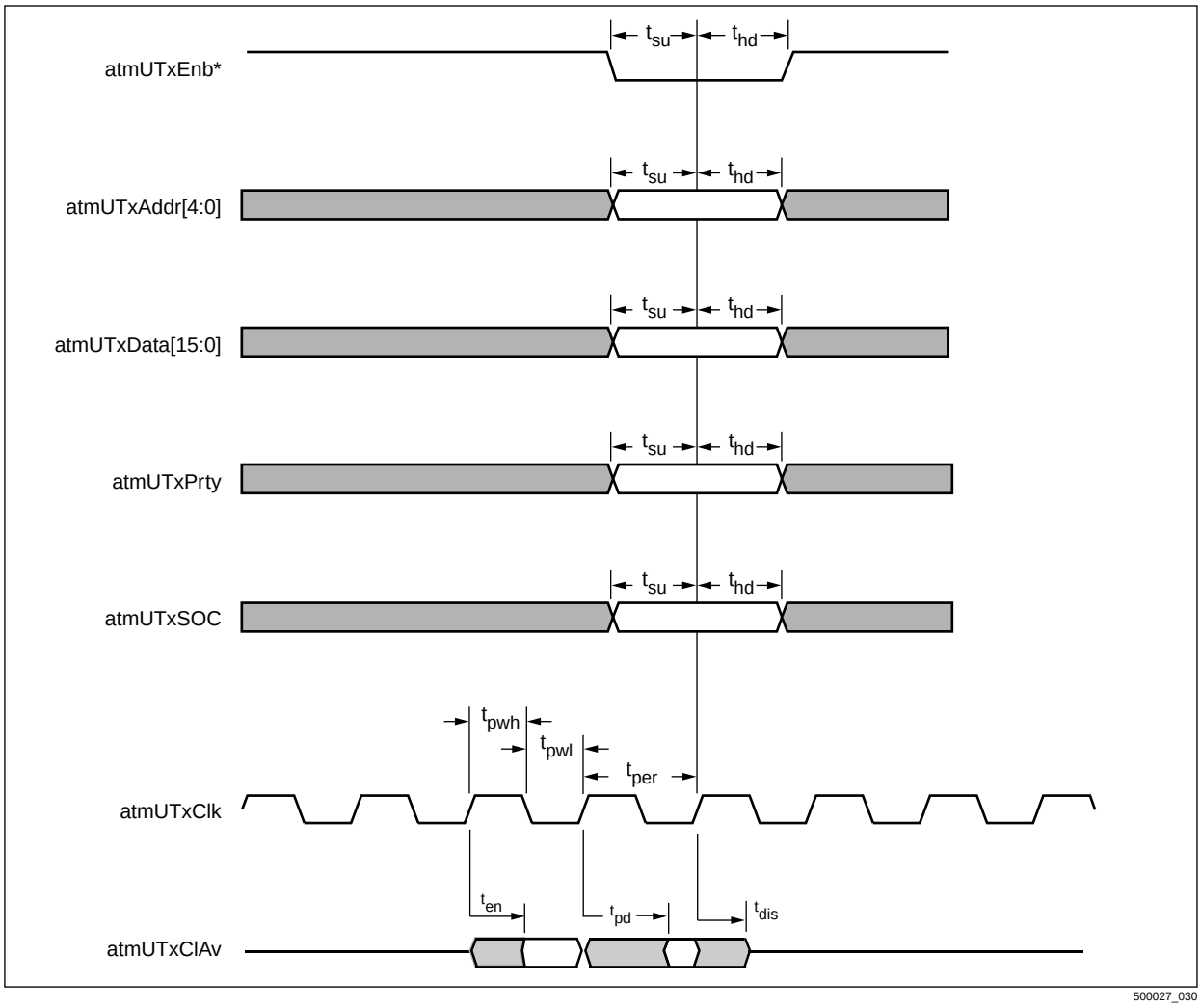


Table 8-7. UTOPIA Transmit Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, atmUTxClk	8	—	ns
t_{pwh}	Pulse Width High, atmUTxClk	8	—	ns
t_{per}	Period, atmUTxClk	20(1)	—	ns
t_{su}	Setup, to the rising edge of atmUTxClk	4	—	ns
t_{hd}	Hold, from the rising edge of atmUTxClk	1	—	ns
t_{pd}	Propagation Delay, UTxClAv from the rising edge of atmUTxClk	1	16	ns
t_{en}	Enable, atmUTxClAv from the rising edge of atmUTxClk	1	16	ns
t_{dis}	Disable, atmUTxClAv from the rising edge of atmUTxClk	0	16	ns

FOOTNOTE:
(1) When configured for TC Only Mode or UL2 8-bit, the UTOPIA interface is limited to 33 MHz or t_{per} = 30 ns minimum.

Figure 8-10. UTOPIA Receive Timing Diagram

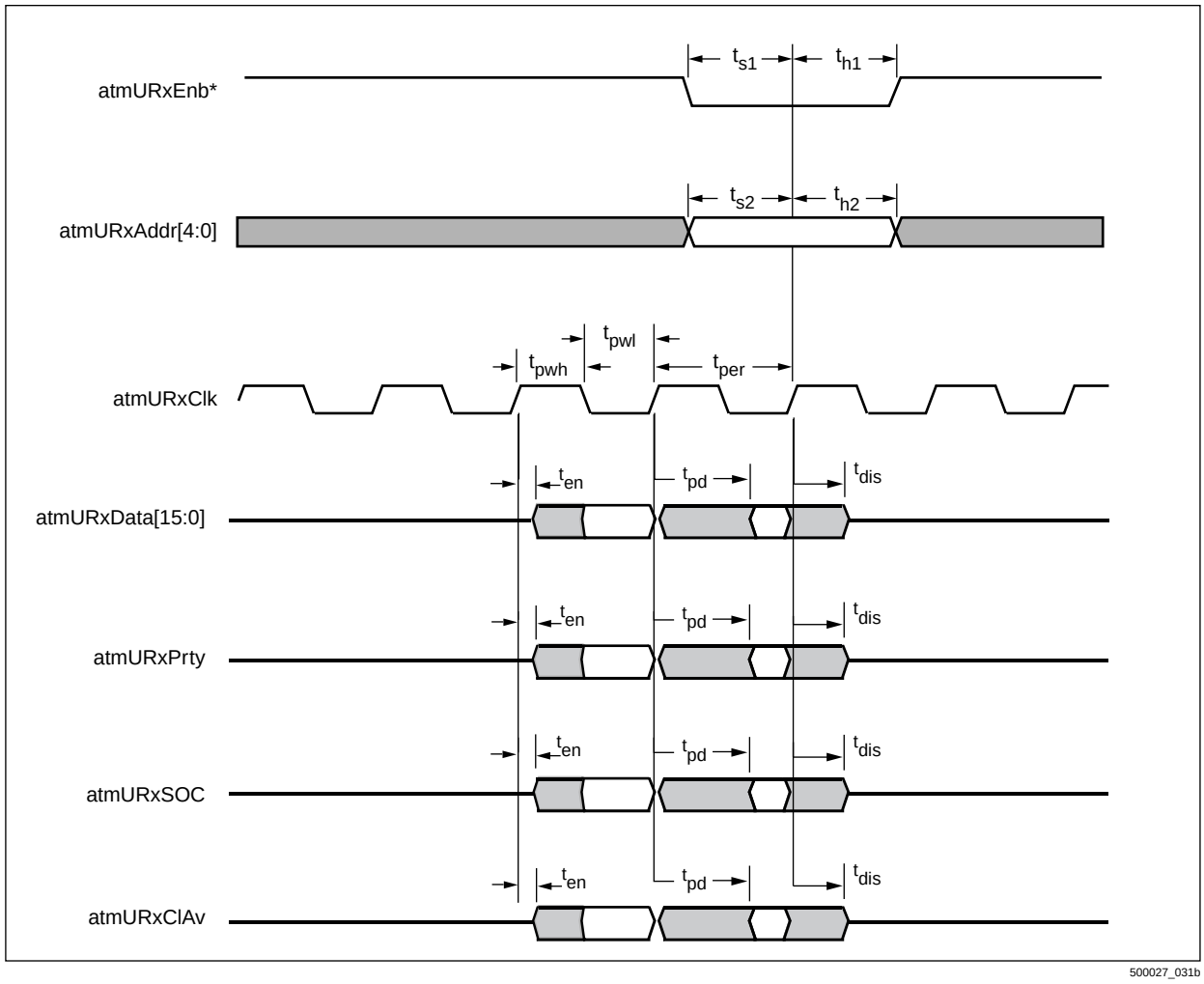


Table 8-8. UTOPIA Receive Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, atmURxClk	8	—	ns
t_{pwh}	Pulse Width High, atmURxClk	8	—	ns
t_{per}	Period, atmURxClk	20(1)	—	ns
t_{s1}	Setup, atmURxEnb* to the rising edge of atmURxClk	4	—	ns
t_{h1}	Hold, atmURxEnb* from the rising edge of atmURxClk	1	—	ns
t_{s2}	Setup, atmURxAddr to the rising edge of atmURxClk	4	—	ns
t_{h2}	Hold, atmURxAddr from the rising edge of atmURxClk	1	—	ns
t_{pd}	Propagation Delay, URxClAv from the rising edge of atmURxClk	1	16	ns
t_{en}	Enable, from the rising edge of atmURxClk	1	16	ns
t_{dis}	Disable, from the rising edge of atmURxClk	0	16	ns

FOOTNOTE:
(1) When configured for TC Only Mode or UL2 8-bit, the UTOPIA interface is limited to 33 MHz or t_{per} = 30 ns minimum.

8.1.4 UTOPIA Interface Timing (PHY Layer)

Figures 8-11 through 8-12 and Tables 8-10 through 8-9 show the timing requirements and characteristics of the UTOPIA interface.

The timing requirements and characteristics were calculated based on 35 pF loading.

Figure 8-11. UTOPIA Transmit Timing Diagram

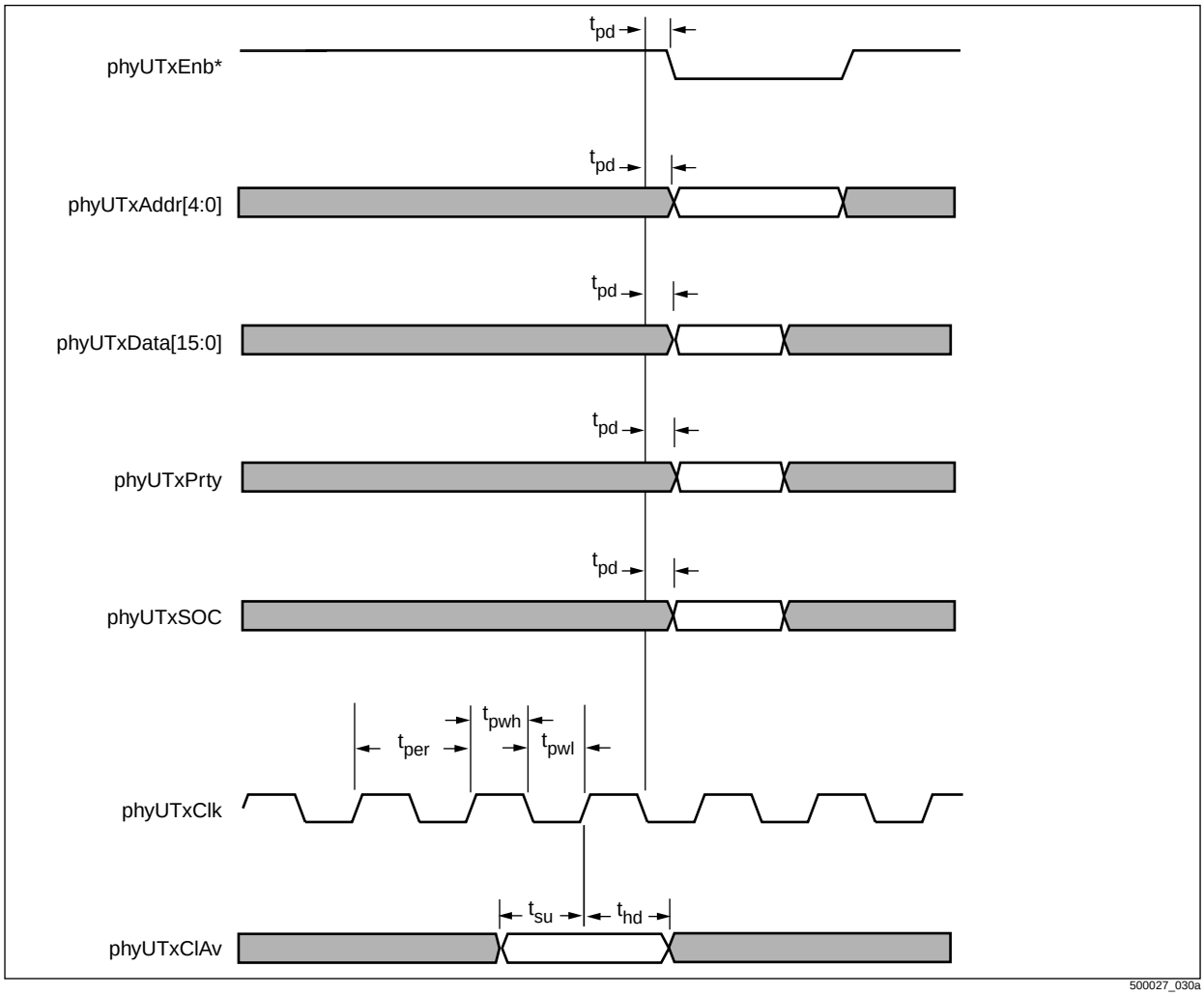


Table 8-9. UTOPIA Transmit Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, phyUTxClk	16	—	ns
t_{pwh}	Pulse Width High, phyUTxClk	16	—	ns
t_{per}	Period, phyUTxClk	40	—	ns
t_{su}	Setup, to the rising edge of phyUTxClk	10	—	ns
t_{hd}	Hold, from the rising edge of phyUTxClk	1	—	ns
t_{pd}	Propagation delay, from the falling edge of phyUTxClk	1	8	ns

Figure 8-12. UTOPIA Receive Timing Diagram

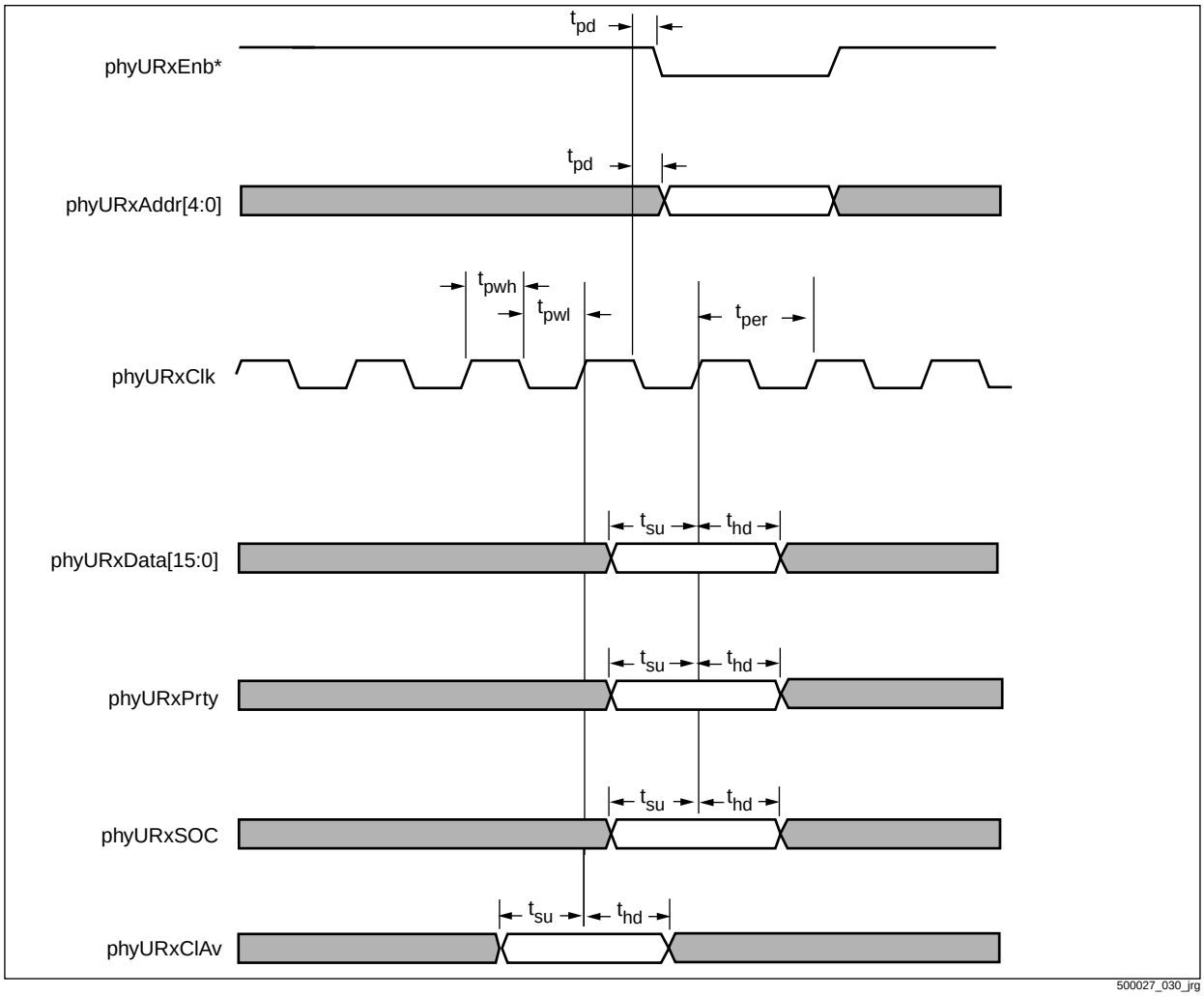


Table 8-10. UTOPIA Receive Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, phyURxClk	16	—	ns
t_{pwh}	Pulse Width High, phyURxClk	16	—	ns
t_{per}	Period, phyURxClk	40	—	ns
t_{su}	Setup, to the rising edge of phyURxClk	10	—	ns
t_{hd}	Hold, from the rising edge of phyURxClk	1	—	ns
t_{pd}	Propagation delay, phyURxClAv from the falling edge of phyURxClk	1	8	ns

8.1.5 JTAG Interface Timing

Figure 8-13 and Table 8-11 show the timing requirements and characteristics of the JTAG interface.

Figure 8-13. JTAG Timing Diagram

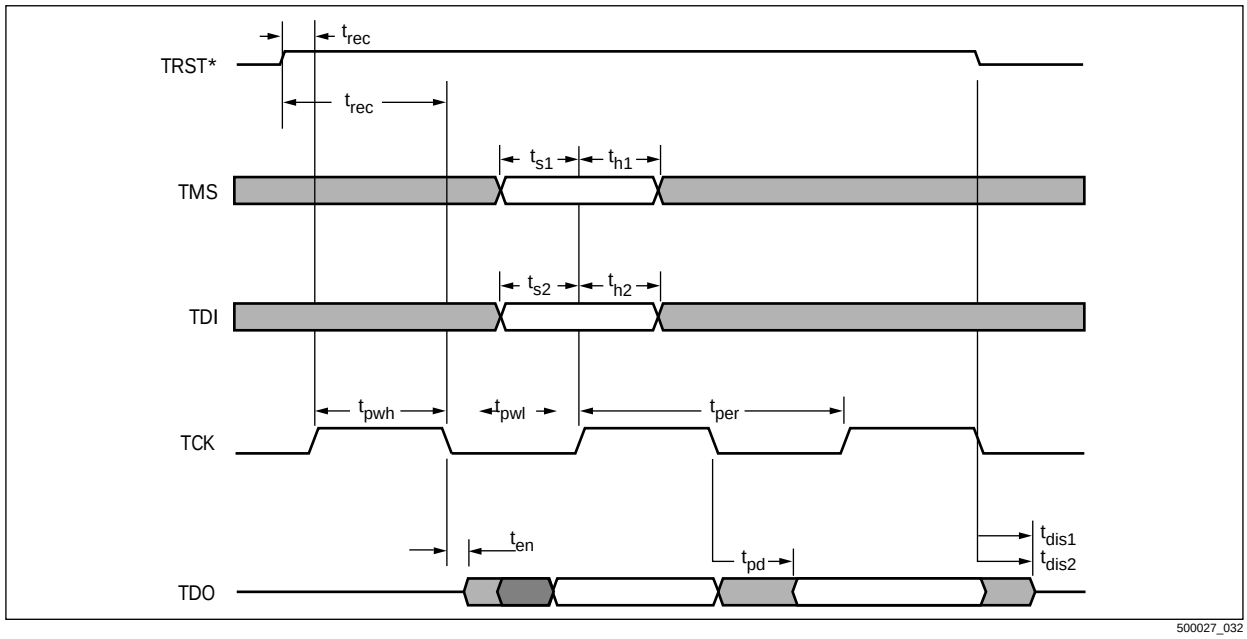


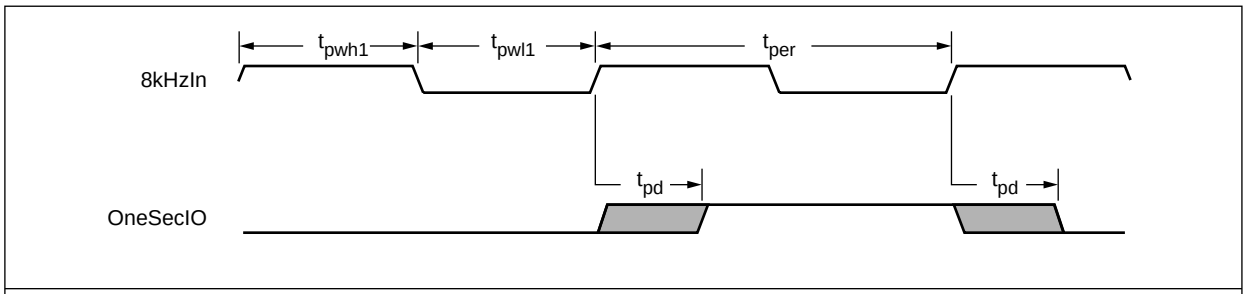
Table 8-11. JTAG Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, TCK	16	—	ns
t_{pwh}	Pulse Width High, TCK	16	—	ns
t_{per}	Period, TCK	40	—	ns
t_{rec}	Recovery, the rising edge of TCK from the rising edge of TRST*	2.5	—	ns
t_{s1}	Setup, TMS to the rising edge of TCK	2	—	ns
t_{h1}	Hold, TMS from the rising edge of TCK	2	—	ns
t_{s2}	Setup, TDI to the rising edge of TCK	2	—	ns
t_{h2}	Hold, TDI from the rising edge of TCK	20	—	ns
t_{en}	Enable, TDO from the falling edge of TCK	0.8	7	ns
t_{pd}	Propagation Delay, TDO from the falling edge of TCK	0.8	7	ns
t_{dis1}	Disable, TDO from the falling edge of TCK	0.8	7	ns
t_{dis2}	Disable, TDO from the falling edge of TRST*	0.8	7	ns
	Inputs with respect to TCK rise	2.0	20.0	ns
	Outputs with respect to TCK rise	0.5	15.0	ns
GENERAL NOTE: All loads equal 80 pF.				

8.1.6 One-second Interface Timing

Figure 8-14 and Table 8-12 show the timing requirements and characteristics of the one-second interface.

Figure 8-14. One-second Timing Diagram



General Notes:

When OneSecIO is configured as an output, it is equal to 8kHzIn/8000.

500027_033

Table 8-12. One-second Timing Table

Label	Description	Min	Max	Unit
	8KHzIn Clock Frequency	0.01	100	KHz
t_{per}	8KHzIn Duty Cycle	40%	60%	
t_{pd}	Propagation Delay, OneSecOut from the rising edge of OneSecClk	1	15	ns

8.2 Expansion Memory Port Timing

Figure 8-15. Read/Write Timing

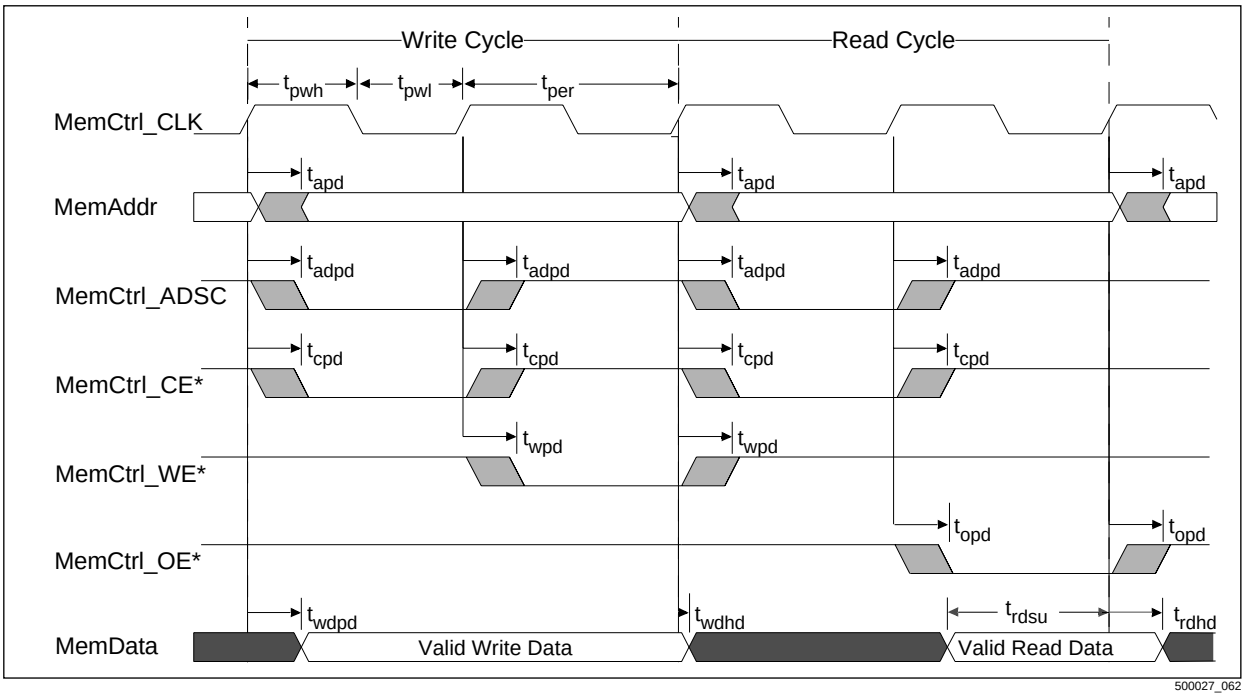


Table 8-13. Expansion Memory Port Read/Write Timing Table

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low	8	—	ns
t_{pwh}	Pulse Width High	8	—	ns
t_{per}	Period	20	—	ns
t_{apd}	Propagation Delay, MemAddr from rising edge of MemCtrl_CLK	1.0	10.0	ns
t_{adpd}	Propagation Delay, MemCtrl_ADSC from rising edge of MemCtrl_CLK	1.0	10.0	ns
t_{cpd}	Propagation Delay, MemCtrl_CE* from rising edge of MemCtrl_CLK	1.0	10.0	ns
t_{wpd}	Propagation Delay, MemCtrl_WE* from rising edge of MemCtrl_CLK	1.0	10.0	ns
t_{opd}	Propagation Delay, MemCtrl_OE* from rising edge of MemCtrl_CLK	1.0	10.0	ns
t_{wdpd}	Propagation Delay, valid write data from rising edge of MemCtrl_CLK	—	10.0	ns
t_{wdhd}	Hold, valid write data from rising edge of MemCtrl_CLK	1.0	—	ns
t_{rdsu}	Setup, read data to rising edge of MemCtrl_CLK	5.0	—	ns
t_{rdhd}	Hold, read data from rising edge of MemCtrl_CLK	1.0	—	ns
The timing requirements and characterization were calculated based on 20 pF capacitive loading.				

8.3 Absolute Maximum Ratings

The absolute maximum ratings in Table 8-14 indicate the maximum stresses that the CX2822x can tolerate without risking permanent damage. These ratings are not typical of normal operation of the device. Exposure to absolute maximum rating conditions for extended periods of time may affect the device's reliability. This device should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

Table 8-14. Absolute Maximum Ratings (General)

Parameter	Value
Supply Voltage	–0.5 to +3.3 V
Input Voltage	–0.5 to Vdd + 0.5 V
Storage Temperature	–40 °C to 125 °C
Operating Temperature Range	–40 °C to 85 °C
Lead Temperature	+240 °C for 10 seconds
Junction Temperature	+150 °C
Maximum Current at Maximum Clock Frequencies	125 mA (1.8 V) 120 mA (3.3 V)
Static Discharge Voltage (Human Body Model)	±2000 V
Latch-up Current	±150 mA
DC Input Current	±20 mA

Table 8-15. Absolute Maximum Ratings (CX28229/CX28225/CX28224)

Parameter	Value
θ_{JC}	4 °C/W
θ_{JA} No Airflow	33 °C/W
θ_{JA} 1.5 m/s Airflow	29 °C/W

8.4 DC Characteristics

Table 8-16 lists the DC characteristics of the CX2822x.

Table 8-16. DC Characteristics

Parameter	Min	Typical	Max	Comments
Power Supply V_{DD} 3.3 V	3.0	3.3	3.6	VDC ±10%
Power Supply V_{DD} 1.8 V	1.71	1.8	1.89	VDC ±5%
Input Low Voltage (VIL)—TTL	0	—	0.8	VDC
Input High Voltage (VIH)—TTL	2.0	—	5.25	VDC
Output Voltage Low (TTL)	—	—	0.4	Volts; I_{OH} = 4.0 mA
Output Voltage High (TTL)	2.4	—	—	Volts; I_{OH} = 1500 µA
Input Leakage Current	–10	—	10	µA; Vin = PWR or GND
Three-state Output Leakage Current	–10	—	10	µA; Vout = PWR or GND
Input Capacitance	—	—	7	pF
Output Capacitance	—	—	7	pF
Bidirectional Capacitance	—	—	7	pF
Power				
V_{DD} 3.3 V	—	250	—	mW
V_{DD} 1.8 V	—	150	—	mW

8.5 Mechanical Drawing

The CX28224/5/9 is a 256-ball BGA package. A mechanical drawing of the device is provided in Figure 8-16 and Figure 8-17.

Figure 8-16. CX28224/5/9 Mechanical Drawing (Bottom View)

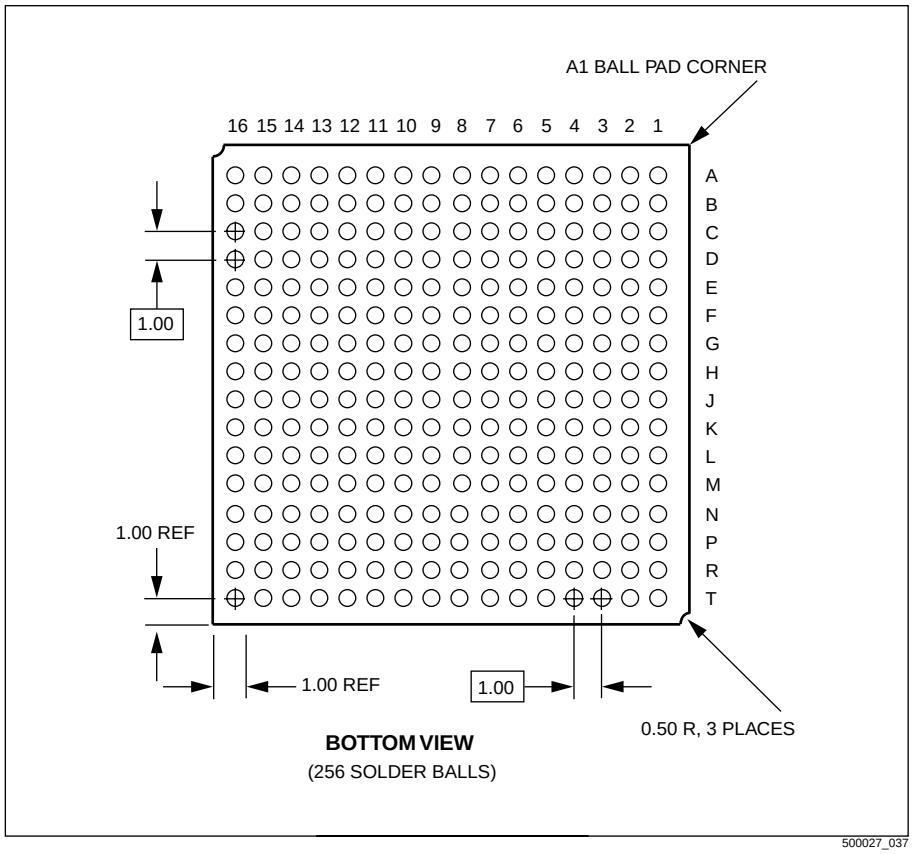
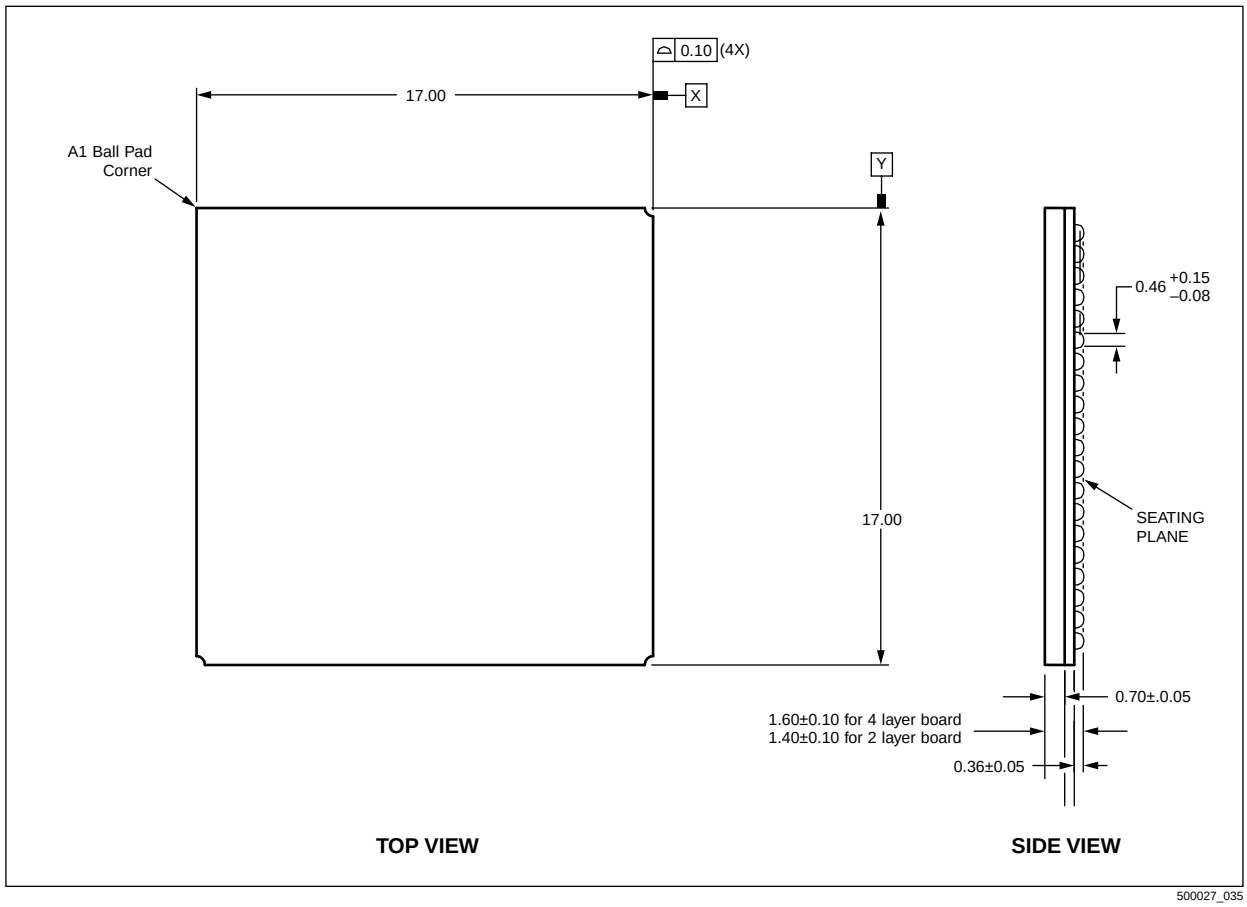


Figure 8-17. CX28224/5/9 Mechanical Drawing (Top and Side Views)



A IMA Version 1.1 PICS Proforma

To evaluate conformance of a particular implementation, it is necessary to have a statement of which capabilities and options have been implemented for a given protocol. Such a statement is called a Protocol Implementation Conformance Statement (PICS).

A.1 Scope

This annex provides the PICS proforma for the Inverse Multiplexing for ATM (IMA) Version 1.1 Specification as described in AF-PHY-0086.001[A-1] in compliance with the relevant requirements, and in accordance with the relevant guidelines, given in ISO/IEC 9646-2[A-3].

A.2 Definitions

This document uses the following terms defined in ISO/IEC 9646-1[A-2]:

- a Protocol Implementation Conformance Statement (PICS) is a statement made by the supplier of an implementation or a system, stating which capabilities have been implemented for a given protocol,
- a PICS Proforma is a document in the form of a questionnaire, designed by the protocol specifier or the conformance test suite specifier, which when completed for an implementation or a system, becomes the PICS, and
- a static conformance review is a review of the extent to which the static conformance requirements are met by the implementation, accomplished by comparing the PICS with the static conformance requirements expressed in the relevant protocol specification.

A.3 Symbols and Conventions

M—Mandatory

O—Option (may be selected to suit the implementation, provided that any requirements applicable to the options are observed)

A.4 Conformance

The supplier of a protocol implementation, which is claimed to conform to AF-PHY-0086.001[A-1], is required to complete a copy of the PICS proforma provided in the following sections of this annex and is required to provide the information necessary to identify both the supplier and the implementation.

A.5 IMA PICS Proforma

A.5.1 Global Statement of Conformance

The implementation described in this PICS Proforma meets all of the mandatory requirements of the protocol specification.

Yes__XX

No__

Note: Answering “No” indicates non-conformance to the protocol specification. Non-supported mandatory capabilities are to be identified in the following tables, with an explanation in the “Comments” section of each table as to why the implementation is “non conforming”.

A.5.2 Instructions for Completing the PICS Proforma

Each question in this section refers to a major function of the protocol. Answering “Yes” to a particular question states that the implementation supports all of the mandatory procedures for that function, as defined in the referenced section of AF-PHY-0086.001[A-1]. Answering “No” to a particular question in this section states that the implementation does not support that function of the protocol.

A supplier may also provide additional information, categorized as exceptional (X) or supplementary information. This additional information should be provided in the Support column as items labeled X<I> for exceptional or S<I> for supplementary information, respectively for cross-reference purposes, where <I> is any unambiguous number.

A.5.3 IMA Protocol Functions

Table A-1. Basic IMA Protocol (BIP) Definition Functions *(1 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
BIP.1	Does the implementation support a number N ($1 \leq N \leq 32$) of transmission links within an IMA group operating at the same nominal link cell rate (LCR)?		M	(R-1)	Yes X No__ $1 \leq N \leq 8$
BIP.2	Does the implementation support the IMA interface connected to another interface over clear channel facilities (implies cells generated by transmit IMA shall only be terminated at the receive IMA)?		M	(R-2)	Yes X No__
BIP.3	Does the interface specific TC sublayer of the implementation pass all cells to the IMA sublayer or provide an indication that a cell was received (this includes HEC errored cells)?		M	(R-3)	Yes X No__
BIP.4	Does the implementation prohibit cell rate decoupling at the interface specific TC sublayer?		M	(R-4)	Yes X No__
BIP.5	Does the implementation assign a LID unique within the IMA group to each Tx IMA link on each physical link?		M	(R-5)	Yes X No__
BIP.6	Does the implementation ensure that the LID does not change while the link is a member of the IMA group?		M	(R-6)	Yes X No__
BIP.7	Does the implementation distribute ATM cells arriving from the ATM layer over the N links in a cyclic round-robin fashion, and on a cell-by-cell basis?		M	(R-7)	Yes X No__
BIP.8	Does the implementation distribute ATM cells over the links using an ascending order based on the LID assigned to each link within the IMA group?		M	(R-8)	Yes X No__
BIP.9	Does the implementation support the ICP cell format defined in Table 2 on page 31 to convey IMA configuration, synchronization, status, and defect information to the far-end?		M	(R-9)	Yes X No__
BIP.10	Does the implementation perform cell rate decoupling by inserting IMA Filler cells in place of ATM cells when there is no cell available at the ATM layer?		M	(R-10)	Yes X No__
BIP.11	Does the implementation accept, on receive, ATM cells from the N links according to ascending order based on the LID received in the ICP cells on the incoming link?		M	(R-11)	Yes X No__
BIP.12	Does the implementation, on receive, compensate for link differential delays and rebuild the original ATM cell stream?		M	(R-11)	Yes X No__
BIP.13	Does the implementation discard received Filler cells and cells with bad HEC?		M	(R-11)	Yes X No__
BIP.14	Does the implementation process and discard incoming ICP cells?		M	(R-11)	Yes X No__
BIP.15	Does the implementation aggregate, on receive, the ATM cell stream to the ATM layer?		M	(R-11)	Yes X No__
BIP.16	Does the implementation preserve the order of incoming cells?		M	(R-11)	Yes X No__
BIP.17	Does the implementation use the ICP cell to maintain IMA protocol synchronization?		M	(R-12)	Yes X No__

Table A-1. Basic IMA Protocol (BIP) Definition Functions *(2 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
BIP.18	Does the implementation use the ICP cell to maintain link delay synchronization?		M	(R-12)	Yes_X_ No__
BIP.19	Does the implementation transmit first the most significant bit of each octet of the IMA OAM cell?		M	(R-13)	Yes_X_ No__
BIP.20	Does the implementation support the same cell header for both the Filler and ICP cell formats as defined in Table 1 on page 28 and Table 2 on page 31?		M	(R-14)	Yes_X_ No__
BIP.21	Does the implementation use bit 7 of octet 7 (CID field) of the Filler and ICP cells to identify the IMA OAM cell as an ICP or Filler cell?		M	(R-15)	Yes_X_ No__
BIP.22	Does the implementation use octets 52-53 as specified in ITU-T Recommendation I.610 [A-5] for octets 52-53 of the OAM cells of the F1/F3 flows?		M	(R-16)	Yes_X_ No__
BIP.23	Does the implementation support the Filler cell format defined in Table 1 on page 28?		M	(R-17)	Yes_X_ No__
BIP.24	Does the implementation support the ICP cell format defined in Table 2 on page 31?		M	(R-18)	Yes_X_ No__
BIP.25	Does the implementation transmit the content of the link specific fields appearing in class A over the link for which these fields apply?		M	(R-19)	Yes_X_ No__
BIP.26	Does the implementation transmit the same content of fields appearing in classes B and C of the ICP cell over all links within an IMA group?		M	(R-20)	Yes_X_ No__
BIP.27	Does the implementation use the LID bits (bits 4-0 of octet 7) in the ICP cell to identify the Link ID (range being 0 to 31)?		M	(R-21)	Yes_X_ No__
BIP.28	Does the implementation use the “Tx State” field, located in the Link “x” Information field in an ICP cell, to report the transmit state of the IMA link on which the NE IMA is transmitting ICP cells carrying LID = “x” (“x” being a value between 0 and 31)?		M	(R-22)	Yes_X_ No__
BIP.29	Does the implementation use the “Rx State”, located in the Link “x” Information field in an ICP cell, to report the receive state of the incoming IMA link on which the FE IMA is transmitting ICP cells carrying LID = “x” (“x” being a value between 0 and 31)?		M	(R-23)	Yes_X_ No__
BIP.30	Does the implementation use the “Rx Defect Indicators” field, located in the Link “x” Information field in an ICP cell, to report the Rx defect indicators corresponding to the incoming IMA link on which the FE IMA is transmitting ICP cells carrying LID = “x” (“x” being a value between 0 and 31)?		M	(R-24)	Yes_X_ No__
BIP.31	Does the implementation always transmit ICP cells with Octet 50 unused and set to “0x6A” as defined in ITU-T Recommendation I.432 [A-4]?		M	(R-25)	Yes_X_ No__
BIP.32	Does the implementation reserve the End-to-End Channel field (Octet 51) as a proprietary channel?		M	(R-26)	Yes_X_ No__
BIP.33	Does the implementation set the End-to-End Channel field (Octet 51) to “0” when not using this field?		M	(R-27)	Yes_X_ No__

Table A-1. Basic IMA Protocol (BIP) Definition Functions *(3 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
BIP.34	Does the implementation not rely on the processing of the End-to-End Channel field for any IMA functionality?		M	(R-28)	Yes X No__
BIP.35	Does the implementation only consider the information within ICP cells exhibiting neither a HEC nor a CRC-10 error?		M	(R-29)	Yes X No__
BIP.36	Does the implementation always transmit "0x03" over the OAM Label in the Filler and ICP cells?		M	(R-30)	Yes X No__
BIP.37	If the implementation does not support the IMA version proposed by the OAM Label received from the far-end IMA unit, does the implementation report the "Config-Aborted - Unsupported IMA Version" state over the "Group Status and Control" field?		M	(R-31)	Yes X No__
BIP.38	Does the implementation transmit IMA frames, composed of M consecutive cells, on each link within the IMA group?		M	(R-32)	Yes X No__
BIP.39	Does the implementation send ICP cells on each link once per IMA frame, hence every M cells?		M	(R-33)	Yes X No__
BIP.40	Does the implementation use the IFSN field in the ICP cell to indicate the sequence number of the IMA frame?		M	(R-34)	Yes X No__
BIP.41	Does the implementation increment the IFSN field in the ICP cell from 0 to 255 and repeat the sequence?		M	(R-35)	Yes X No__
BIP.42	Does the implementation increment the IFSN field in the ICP cell with each IMA frame on a per-link basis?		M	(R-36)	Yes X No__
BIP.43	Within an IMA frame, does the implementation place identical IFSN values in the ICP cells sent on each link?		M	(R-36)	Yes X No__
BIP.44	Does the implementation align the transmission of the IMA frame on all links within an IMA group?		M	(R-37)	Yes X No__
BIP.45	Does the implementation use the ICP Cell Offset field (octet 9) to indicate the location of the ICP cell within the IMA frame of length M cells?		M	(R-38)	Yes X No__
BIP.46	Does the implementation always set the value of the ICP cell offset between 0 and M-1 where M is the IMA frame length in cells?		M	(R-39)	Yes X No__
BIP.47	Does the implementation distribute the ICP cells, from link to link within the IMA group, in an uniform fashion across the IMA frame?		O	(O-1)	Yes X No__
BIP.48	Does the implementation select the offset of the ICP cell sent of any link when the link is assigned a LID?		M	(R-40)	Yes X No__
BIP.49	Does the implementation retain the offset of the ICP cell sent on a given link until the link is no longer part of the group?		M	(R-40)	Yes X No__
BIP.50	Does the implementation always use the Frame Length field in the ICP cell to indicate the value of M?		M	(R-41)	Yes X No__
BIP.51	Does the implementation support M = 128?		M	(R-42)	Yes X No__
BIP.52	Does the implementation support M = 32?		O	(O-2)	Yes X No__
BIP.53	Does the implementation support M = 64?		O	(O-2)	Yes X No__
BIP.54	Does the implementation support M = 256?		O	(O-2)	Yes X No__

Table A-1. Basic IMA Protocol (BIP) Definition Functions *(4 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
BIP.55	Does the implementation only change the value M at group start-up time?		M	(R-43)	Yes X No__
BIP.56	Does the implementation use on transmit the value configured by the UM?	(O-2)	M	(CR-1)	Yes X No__
BIP.57	Does the implementation allow different values of M in both Tx and Rx directions?	(O-2)	M	(CR-2)	Yes X No__
BIP.58	Does the implementation synchronize its incoming links using the received M value for IMA frame synchronization?	(O-2)	M	(CR-3)	Yes X No__
BIP.59	Does the implementation abort the start-up procedure using the corresponding code in the Group Status and Control field of the ICP cell when it does not support the received M?		M	(R-44)	Yes X No__
BIP.60	Does the implementation allow to configure the value M?		O	(O-3)	Yes X No__
BIP.61	Does the implementation set the SCCI field to the previously transmitted SCCI field value, incremented modulo 256, to indicate a change on at least one of the fields appearing in octets 12 through 49 in the transmitted ICP cell?		M	(R-45)	Yes X No__
BIP.62	Does the implementation use the SCCI field to identify received ICP cells for processing when ICP cells are monitored on more than one link, or when the monitored link has changed?		M	(R-46)	Yes X No__
BIP.63	Does the implementation process the fields in octets 12 through 49 if the SCCI field has advanced beyond the SCCI value of the last processed ICP cell?		M	(R-46)	Yes X No__
BIP.64	Does the implementation select the IMA ID at group start-up time?		M	(R-47)	Yes X No__
BIP.65	Does the implementation transmit the IMA ID in the IMA ID field?		M	(R-48)	Yes X No__
BIP.66	Does the implementation allow to configure the value of IMA ID?		O	(O-4)	Yes X No__
BIP.67	Does the implementation use the "Group Symmetry Mode" field, specified in Table 2 on page 31, to indicate the symmetry of the IMA group?		M	(R-49)	Yes X No__
BIP.68	Does the implementation ensure that the symmetry of the group is only established or changed at group start-up time?		M	(R-50)	Yes X No__
BIP.69	Does the implementation support the Symmetrical Configuration and Operation mode?		M	(R-51)	Yes X No__
BIP.70	Does the implementation support the Symmetrical Configuration and Asymmetrical Operation mode?		O	(O-5)	Yes X No__
BIP.71	Does the implementation support the Asymmetrical Configuration and Operation mode?		O	(O-6)	Yes X No__
BIP.72	Does the implementation abort the start-up procedure using the appropriate code defined in the “Group Status and Control” field of the ICP cell (as specified in Table 2 on page 31) if the NE does not support the symmetry mode proposed by the FE?		M	(R-52)	Yes X No__

Table A-1. Basic IMA Protocol (BIP) Definition Functions *(5 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
BIP.73	Does the implementation abort the start-up procedure using the appropriate code defined in the “Group Status and Control” field of the ICP cell (as specified in Table 2 on page 31) if the symmetry mode proposed by the FE and the configured symmetry mode of the NE do not match?		M	(R-52)	Yes X No__
BIP.74	In order to allow a fast recovery when (O-5) or (O-6) is used at the NE and when the FE IMA unit can only be configured to the "Symmetrical Configuration and Operation" mode, does the implementation adjust to “Symmetrical Configuration and Operation”.		O	(O-7)	Yes X No__
BIP.75	Does the implementation support only the valid combinations of group symmetry modes at each end of the IMA virtual link as specified in Table 4 on page 36?		M	(R-53)	Yes X No__
BIP.76	Does the implementation allow configuration of the group mode?		O	(O-8)	Yes X No__
Comments: Maximum group size is 8 links.					

Table A-2. QoS Requirements Functions

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
QOS.1	Does the implementation support all ATM traffic/QoS classes supported by the ATM layer?		M	(R-54)	Yes X No__
Comments:					

Table A-3. CTC and ITC Operation Functions *(1 of 2)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
CIT.1	Does the implementation indicate to the FE in which transmit clock mode it is running in the “Transmit Clock Mode” field in the ICP cell?		M	(R-55)	Yes X No__
CIT.2	Does the implementation support the CTC mode in the transmit direction?		M	(R-56)	Yes X No__
CIT.3	Does the implementation only indicate to the FE that it is in the CTC mode when all the “transmit” clocks of the links in the group are derived from the same source?		M	(R-57)	Yes X No__
CIT.4	Does the implementation support the ITC mode in the transmit direction?		O	(O-9)	Yes X No__
CIT.5	Does the implementation indicate that it is in the ITC mode even if all the transmit clocks of the links in the group are derived from the same source?		O	(O-10)	Yes X No__
CIT.6	Does the implementation use the cell stuffing procedure to prevent link transmit buffer under-run or over-run?	(O-9)	M	(CR-4)	Yes X No__

Table A-3. CTC and ITC Operation Functions *(2 of 2)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
CIT.7	Does the implementation indicate a stuff event in the ICP cell preceding a stuff event using the mandatory LSI codes specified in Table 2 on page 30?		M	(R-58)	Yes X No__
CIT.8	Does the implementation perform stuffing by repeating the ICP cell containing the LSI code indicating that “this cell is 1 out of 2 ICP cells comprising the stuff event”?		M	(R-59)	Yes X No__
CIT.9	Does the implementation also indicate an incoming stuff event in the fourth, third, and second ICP preceding the stuff event using the optional LSI codes?		O	(O-11)	Yes X No__
CIT.10	At any given link, does the implementation ensure it does not introduce a stuff event more than once every 5*M ICP, Filler and ATM layer cells?		M	(R-60)	Yes X No__
CIT.11	Does the implementation remove one of any two consecutive ICP cells with LSI code indicating “this cell is 1 out of the 2 ICP cells comprising the stuff event”?		M	(R-61)	Yes X No__
CIT.12	Does the implementation ensure that the SICP cell is not counted as a cell for the purposes of determining the IMA round-robin sequence?		M	(R-61)	Yes X No__
CIT.13	Does the implementation support CTC and ITC modes on receive?		M	(R-62)	Yes X No__
CIT.14	Does the implementation inform the UM of a mismatch between the FE and NE IMA transmit clock modes?		M	(R-63)	Yes X No__
CIT.15	Does the implementation ensure that a restart is not caused if the implementation detects a mismatch between the FE and NE Transmit clock modes?		M	(R-63)	Yes X No__
CIT.16	Does the implementation rely on at least one ICP cell with a correct CRC-10 in order to process the incoming stuff cell indication code (this is recommended)?		O	(O-12)	Yes X No__
Comments:					

Table A-4. IMA Data Cell (IDC) Rate Implementation Functions

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
IDC.1	Does the implementation ensure on transmit that a Filler cell is not injected if an ATM layer cell is available for scheduling?		M	(R-64)	Yes X No__
IDC.2	Does the implementation only check on transmit that an ATM layer cell is available and accept that cell only when the Tx IDCC ticks?		M	(R-64)	Yes X No__
IDC.3	Does the implementation only select the TRL from the set of links whose transmit state is Active?		M	(R-65)	Yes X No__
IDC.4	If there is no link in the Active state, does the implementation select one of the links in the Usable state, if any, or one of the links in the Unusable state otherwise?		M	(R-66)	Yes X No__
IDC.5	Does the implementation only select or change the TRL during the following situations: during group start-up, when the previously selected TRL's transmit state changes from Active to any other state (e.g., Usable, Unusable, or Not In Group) while another link's transmit state is Active, or when the previously selected TRL's transmit state changes from Usable to Unusable or Not In Group while another link's transmit state is Active or Usable?		M	(R-67)	Yes X No__
IDC.6	Does the implementation indicate the selected or changed TRL to the FE over the "Transmit Timing Information" field in the ICP cell?		M	(R-68)	Yes X No__
IDC.7	Does the implementation derive the Tx IDCC from the selected TRL according to Equation 1 on page 40?		M	(R-69)	Yes X No__
IDC.8	When running in the CTC mode, does the implementation introduce a stuff event every 2048 ICP, Filler and ATM layer cells on all links?		M	(R-70)	Yes X No__
IDC.9	Does the implementation introduce a stuff event every 2048 ICP, Filler and ATM layer cells on the TRL?	(O-9)	M	(CR-5)	Yes X No__
IDC.10	Does the implementation introduce stuff events on links other than the TRL in order to compensate for the timing difference between the TRL and the other links?	(O-9)	M	(CR-6)	Yes X No__
IDC.11	Does the implementation remove CDV attributed to the presence of ICP cells by a mechanism equivalent to providing a small smoothing buffer into which cells are placed after reordering and after removing ICP cells?		M	(R-71)	Yes X No__
IDC.12	If the TRL is in the Working state and the FE has, for at least 100 milliseconds, identified a given link as the TRL, does the implementation derive the Rx IDCR using the incoming link indicated by the FE as the TRL?		M	(R-72)	Yes X No__
IDC.13	Does the implementation have an equivalent behavior to the following: when the IMA data cell clock at the receiver ticks, one cell is removed from the smoothing buffer; if the cell is a Filler cell, then the Filler cell is discarded and nothing passed to the ATM layer; if the cell is not a Filler cell, then it is passed to the ATM layer?		M	(R-73)	Yes X No__
Comments:					

Table A-5. Link Differential Delay (LDD) Functions

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
LDD.1	Does the implementation introduce a differential delay among the constituent links of a maximum of 2.5 cell times at the physical link rate?		M	(R-74)	Yes X No__
LDD.2	Does the implementation tolerate up to at least 25 milliseconds of link differential delay on receive?		M	(R-75)	Yes X No__
LDD.3	Does the implementation allow configuring the link differential delay tolerance?		O	(O-13)	Yes X No__
Comments:					

Table A-6. IMA Interface Operation (IIO) Functions *(1 of 4)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
IIO.1	Does the implementation support the Tx LSM defined in Table 8 on page 52?		M	(R-76)	Yes X No__
IIO.2	Does the implementation support the Rx LSM defined in Table 9 on page 53?		M	(R-77)	Yes X No__
IIO.3	Does the implementation signal the current state of the Tx LSM to the FE IMA unit via the ICP cells?		M	(R-78)	Yes X No__
IIO.4	Does the implementation perform the actions corresponding to the Tx LSM sub-states?		M	(R-78)	Yes X No__
IIO.5	Does the implementation update the Tx LSM according the occurrence of the events listed in Table 8 on page 52?		M	(R-78)	Yes X No__
IIO.6	Does the implementation treat sequentially the incoming events that trigger the Tx LSM, although the order of treatment is implementation specific if these events appear simultaneously?		M	(R-78)	Yes X No__
IIO.7	Does the implementation signal the current state of the Rx LSM to the FE IMA unit via the ICP cells?		M	(R-78)	Yes X No__
IIO.8	Does the implementation perform the actions corresponding to the Rx LSM sub-states?		M	(R-78)	Yes X No__
IIO.9	Does the implementation update the Rx LSM according the occurrence of the events listed in Table 9 on page 53?		M	(R-78)	Yes X No__
IIO.10	Does the implementation treat sequentially the incoming events that trigger the Rx LSM, although the order of treatment is implementation specific if these events appear simultaneously?		M	(R-78)	Yes X No__
IIO.11	Does the implementation report any change of the Tx and Rx LSMs within the next 2*M (where M is the M used by the IMA transmitter) cells on that link over the “Tx State" and "Rx State" fields of the Link Information field (refer to Table 3 on page 32)?		M	(R-79)	Yes X No__
IIO.12	Does the implementation use one of the Unusable encodings when reporting the Unusable state?		M	(R-80)	Yes X No__

Table A-6. IMA Interface Operation (IIO) Functions *(2 of 4)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
IIO.13	Does the implementation use "Inhibited", "Failed", "Fault" or "Mis-connected" as a reason when reporting the Unusable state?		O	(O-14)	Yes X No X Partial Usage
IIO.14	Does the implementation re-evaluate the TX and Rx LSMs state upon each incoming ICP cell with new state indication?		M	(R-81)	Yes X No__
IIO.15	Does the implementation allow the valid combinations of Tx and Rx LSM states and disallow the invalid combinations when running in the Symmetrical Configuration and Operation mode?		M	(R-82)	Yes X No__
IIO.16	Does the implementation allow the valid combinations of Tx and Rx LSM states and disallow the invalid combinations when running in the Symmetrical Configuration and Asymmetrical Operation mode?		M	(R-82)	Yes X No__
IIO.17	Does the implementation allow all combinations of Tx and Rx LSM states when running in the Asymmetrical Configuration and Operation mode?		M	(R-82)	Yes X No__
IIO.18	Does the implementation report any GSM states, with the exception of the Not Configured state, to the FE group using the corresponding value defined in the "Group Status and Control" field?		M	(R-83)	Yes X No__
IIO.19	Does the implementation always send over each link the same value in the "Group Status and Control" field for at least 2 consecutive IMA frames?		M	(R-84)	Yes X No__
IIO.20	Does the implementation validate the Rx OAM Label, Rx M, and Rx IMA ID over at least one link before moving into the Start-up-Ack state?		M	(R-85)	Yes X No__
IIO.21	Does the implementation use the validated Rx OAM Label, Rx M, and Rx IMA ID to achieve IMA frame synchronization as defined in Section 11 on page 68?		M	(R-86)	Yes X No__
IIO.22	Does the implementation ensure that at least P_{Tx} links in the transmit direction and P_{Rx} links in the received direction can be moved into the Active state before moving the GSM into the Operational state?		M	(R-87)	Yes X No__
IIO.23	Does the implementation ensure that P_{Tx} is greater than zero?		M	(R-88)	Yes X No__
IIO.24	Does the implementation ensure that P_{Rx} is greater than zero?		M	(R-88)	Yes X No__
IIO.25	Does the implementation ensure that P_{Tx} and P_{Rx} are equal when the configured in the Symmetrical Configuration and Operation mode?		M	(R-89)	Yes X No__
IIO.26	Does the implementation allow configuration of the value of P_{Tx}?		O	(O-15)	Yes X No__
IIO.27	Does the implementation allow configuration of the value of P_{Rx}?		O	(O-15)	Yes X No__
IIO.28	Does the implementation report the Config-Aborted state for at least one second when the configuration requested by the FE is unacceptable?		M	(R-90)	Yes X No__
IIO.29	Does the implementation support the GSM state transitions as defined in 13 on page 60?		M	(R-91)	Yes X No__

Table A-6. IMA Interface Operation (IIO) Functions *(3 of 4)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
IIO.30	Does the implementation determine and report that the group is up when both the local and remote GSMs are Operational?		M	(R-92)	Yes X No__
IIO.31	Does the implementation determine and report that the group is down when either the local or the remote GSM is not operational?		M	(R-92)	Yes X No__
IIO.32	Does the implementation report the proper reasons why the GSM is not operational?		M	(R-92)	Yes X No__
IIO.33	Does the implementation report the highest priority reason according to Table 14 on page 61?		M	(R-92)	Yes X No__
IIO.34	Does the implementation report the entrance of the GTSM into the Down state to the UM and ATM Layer Management?		M	(R-93)	Yes X No__
IIO.35	Is the report of the entrance of the GTSM into the Down state the only notification to the ATM Layer Management about Physical Layer defects or failures?		M	(R-93)	Yes X No__
IIO.36	Does the implementation report the return of the GTSM to the Up state to the UM and ATM Layer Management?		M	(R-94)	Yes X No__
IIO.37	Does the implementation ensure it does not drop any ATM layer cells when adding or recovering links while the GSM is maintained in the Operational state?		M	(R-95)	Yes X No__
IIO.38	Does the implementation ensure that it does not drop any ATM layer cells when deleting or inhibiting links while the GSM is maintained in the Operational state?		M	(R-96)	Yes X No__
IIO.39	When running the group start-up procedure, does the implementation ensure that all accepted links have their states changed to Tx=Usable in the same update of the ICP cell?		M	(R-97)	Yes X No__
IIO.40	When running the group start-up procedure and after the Tx state of all accepted links has been reported in a previous update of the ICP cell, does the implementation ensure that all accepted links have their states changed to Rx=Active in the same update of the ICP cell?		M	(R-98)	Yes X No__
IIO.41	When running the group start-up procedure and after the Rx state of all accepted links has been reported in a previous update of the ICP cell, does the implementation ensure that all accepted links have their states changed to Tx=Active in the same update of the ICP cell?		M	(R-99)	Yes X No__
IIO.42	When running the group start-up procedure, does the implementation wait a minimum of one second, unless all the configured links are being reported Tx=Usable by FE, before reporting links Rx=Active?		M	(R-100)	Yes X No__
IIO.43	When running the group start-up procedure, does the implementation wait a minimum of one second, unless all the configured links are being reported Rx=Active by FE, before reporting links Tx=Active?		M	(R-101)	Yes X No__
IIO.44	Does the implementation synchronize the insertion of new links or recovered links added using the slow recovery mechanism, defined in Section 12.1.3.1 on page 74, within the IMA RR?		M	(R-102)	Yes X No__

Table A-6. IMA Interface Operation (IIO) Functions *(4 of 4)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
IIO.45	Does the implementation execute only one LASR procedure per IMA group at any time (even if more than one link is inserted at the same time)?		M	(R-103)	Yes X No__
IIO.46	Does the implementation delay the insertion of one or more new links or a possible slow link recovery when the LASR is in progress until the link addition procedure is completed or aborted?		M	(R-104)	Yes X No__
IIO.47	When running the LASR procedure, does the implementation ensure that all the inserted links have their states changed to Tx=Usable in the same update of the ICP?		M	(R-105)	Yes X No__
IIO.48	When running the LASR procedure and after the Tx state of all accepted links has been reported Usable in a previous update of the ICP cell, does the implementation ensure that all the inserted links have their states changed to Rx=Active in the same update of the ICP cell?		M	(R-106)	Yes X No__
IIO.49	When running the LASR procedure and after the Rx state of all accepted links has been reported Active in a previous update of the ICP cell, does the implementation ensure that all the inserted links have their states changed to Tx=Active in the same update of the ICP cell?		M	(R-107)	Yes X No__
IIO.50	When running the LASR procedure, does the implementation wait a minimum of one second, unless all the inserted links are being reported Tx=Usable by FE, before reporting links Rx=Active?		M	(R-108)	Yes X No__
IIO.51	When running the LASR procedure, does the implementation wait a minimum of one second, unless the inserted links are being reported Rx=Active by FE, before reporting links Tx=Active?		M	(R-109)	Yes X No__
Comments: All FE Tx and Rx Unusable Sub-states supported. NE Rx Unusable sub-states supported: No reason, Failed, Inhibited. NE Tx Unusable sub-states supported: No reason.					

Table A-7. IMA Frame Synchronization (IFS) Mechanism Functions

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
IFS.1	Does the implementation perform IMA frame synchronization on each link, based on the IFSM defined in Figure 19 on page 69 and Table 16 on page 69?		M	(R-110)	Yes X No__
IFS.2	Does the implementation operate the IFSM for each link independently of any link defects and link delay compensation?		M	(R-111)	Yes X No__
IFS.3	Does the implementation support the default value 2 for Alpha(α)?		M	(R-112)	Yes X No__
IFS.4	Does the implementation support the default value 2 for Beta(β)?		M	(R-112)	Yes X No__
IFS.5	Does the implementation support the default value 1 for Gamma(γ)?		M	(R-112)	Yes X No__
IFS.6	Does the implementation support the value 1 for Alpha(α)?		O	(O-16)	Yes X No__
IFS.7	Does the implementation support the value 1 for Beta(β)?		O	(O-16)	Yes X No__
IFS.8	Does the implementation support the value 3 for Beta(β)?		O	(O-16)	Yes X No__
IFS.9	Does the implementation support the value 4 for Beta(β)?		O	(O-16)	Yes X No__
IFS.10	Does the implementation support the value 5 for Beta(β)?		O	(O-16)	Yes X No__
IFS.11	Does the implementation support the value 2 for Gamma(γ)?		O	(O-16)	Yes X No__
IFS.12	Does the implementation support the value 3 for Gamma(γ)?		O	(O-16)	Yes X No__
IFS.13	Does the implementation support the value 4 for Gamma(γ)?		O	(O-16)	Yes X No__
IFS.14	Does the implementation support the value 5 for Gamma(γ)?		O	(O-16)	Yes X No__
IFS.15	Does the implementation assume that any occurrence of HEC/CRC errored cell in the ICP cell position was an ICP cell?		M	(R-113)	Yes X No__
IFS.16	Does the implementation ignore the cell content of a HEC/CRC errored cell in the ICP cell position?		M	(R-113)	Yes X No__
IFS.17	Does the implementation go into the Hunt state from any other state when no longer getting cells from the physical layer?		O	(O-17)	Yes X No__
IFS.18	Does the implementation maintain IMA frame synchronization for cases 1, 2, 3, and 6 identified in Figure 20 on page 71?		M	(R-114)	Yes X No__
IFS.19	Does the implementation maintain IMA frame synchronization for case 4 identified in Figure 20 on page 71?		O	(O-18)	Yes X No__ Need (O-11)
IFS.20	Does the implementation maintain IMA frame synchronization for case 5 identified in Figure 20 on page 71?		O	(O-18)	Yes X No__
IFS.21	Does the implementation maintain IMA frame synchronization for case 7 identified in Figure 20 on page 71 when passing stuff indication over more than one of the previous ICP cells and when Beta(β) is greater than 2?		O	(O-19)	Yes X No__ Need (O-11)
Comments: (O-11) required to support (O-18) and (O-19).					

Table A-8. IMA Interface OAM Operation Functions *(1 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
OAM.1	Does the implementation report the following link remote defect indicators: link defects, LIF, and LODS?		M	(R-115)	Yes X No__
OAM.2	If several defects are detected at the same time, does the implementation report the defect with the highest priority, as listed in Table 17 on page 72?		M	(R-116)	Yes X No__
OAM.3	Does the implementation report any Rx defect to the far-end IMA within the next 2*M cells to be transmitted after the defect state has been entered as specified in Section 12.1.3 on page 72 (where M is the M used by the IMA transmitter)?		M	(R-117)	Yes X No__
OAM.4	Does the implementation perform error handling as specified in Figure 21 on page 73 and Figure 22 on page 74?		M	(R-118)	Yes X No__
OAM.5	On a given link, does the implementation pass to the ATM layer from the IMA sublayer any cells accumulated before the occurrence of an OCD or OIF anomaly on that link?		M	(R-119)	Yes X No__
OAM.6	Does the implementation inhibit the passing from the IMA sublayer to the ATM layer of any cells received on a link during an OCD or OIF anomaly condition reported on that link?		M	(R-120)	Yes X No__
OAM.7	Does the implementation replace with Filler cells all ATM layer cells received on a link after an OCD or OIF anomaly condition has been detected on that link?		M	(R-121)	Yes X No__
OAM.8	Does the implementation only report an Rx defect in the backward direction after LIF or LODS defect state is entered?		M	(R-122)	Yes X No__
OAM.9	Does the implementation report the LIF or LODS defect as specified in Section 12.1.2 on page 72?		M	(R-123)	Yes X No__
OAM.10	Does the implementation detect errored ICP cells as indicated in Table 18 on page 77?		M	(R-124)	Yes X No__
OAM.11	Does the implementation detect invalid ICP cells as indicated in Table 18 on page 77?		M	(R-124)	Yes X No__
OAM.12	Does the implementation detect missing ICP cells as indicated in Table 18 on page 77?		M	(R-124)	Yes X No__
OAM.13	Does the implementation report OIF events as indicated in Table 18 on page 77?		M	(R-124)	Yes X No__
OAM.14	Does the implementation report LIF defects as indicated in Table 18 on page 77?		M	(R-124)	Yes X No__
OAM.15	Does the implementation report LODS defects as indicated in Table 18 on page 77?		M	(R-124)	Yes X No__
OAM.16	Does the implementation report RDI-IMA defects as indicated in Table 18 on page 77?		M	(R-124)	Yes X No__
OAM.17	Does the implementation increment IV-IMA for every detected errored, invalid or missing ICP cell, except during seconds when a SES-IMA or UAS-IMA condition is reported, as indicated in Table 19 on page 77?		M	(R-125)	Yes X No__

Table A-8. IMA Interface OAM Operation Functions *(2 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
OAM.18	Does the implementation increment OIF-IMA for each reported OIF anomaly, except during seconds when a SES-IMA or UAS-IMA condition is reported, as indicated in Table 19 on page 77?		O	(O-20)	Yes X No__
OAM.19	Does the implementation increment SES-IMA for every one second interval containing ≥ 30 % of the ICP cells counted as IV-IMA, as indicated in Table 19 on page 77?		M	(R-126)	Yes X No__
OAM.20	Does the implementation increment SES-IMA for every one interval of one second containing one or more link defects (e.g., LOS, OOF/LOF, AIS, and LCD), except during seconds when an UAS-IMA condition is reported, as indicated in Table 19 on page 77?		M	(R-126)	Yes X No__
OAM.21	Does the implementation increment SES-IMA for every one second interval containing one or more LIF link defects, except during seconds when an UAS-IMA condition is reported, as indicated in Table 19 on page 77?		M	(R-126)	Yes X No__
OAM.22	Does the implementation increment SES-IMA for every one second interval containing one or more LODS link defects, except during seconds when a UAS-IMA condition is reported, as indicated in Table 19 on page 77?		M	(R-126)	Yes X No__
OAM.23	Does the implementation increment SES-IMA-FE for every one second interval containing one or more RDI-IMA defect, except during seconds when a UAS-IMA-FE condition is reported, as indicated in Table 19 on page 77?		M	(R-127)	Yes X No__
OAM.24	Does the period of NE unavailability begin at the onset of 10 contiguous SES-IMA (including the first 10 seconds to enter the UAS-IMA condition), as indicated in Table 19 on page 77?		M	(R-128)	Yes X No__
OAM.25	Does the period of NE unavailability end at the onset of 10 contiguous seconds with no SES-IMA (excluding the last 10 seconds to exit the UAS-IMA condition), as indicated in Table 19 on page 77?		M	(R-128)	Yes X No__
OAM.26	Does the implementation increment UAS-IMA for each one second interval when the UAS-IMA condition is reported, as indicated in Table 19 on page 77?		M	(R-128)	Yes X No__
OAM.27	Does the period of FE unavailability begin at the onset of 10 contiguous SES-IMA (including the first 10 seconds to enter the UAS-IMA condition), as indicated in Table 19 on page 77?		M	(R-129)	Yes X No__
OAM.28	Does the period of FE unavailability end at the onset of 10 contiguous seconds with no SES-IMA-FE (excluding the last 10 seconds to exit the UAS-IMA-FE condition), as indicated in Table 19 on page 77?		M	(R-129)	Yes X No__
OAM.29	Does the implementation increment UAS-IMA-FE for each one second interval when the UAS-IMA-FE condition is reported, as indicated in Table 19 on page 77?		M	(R-129)	Yes X No__
OAM.30	Does the implementation increment Tx-UUS-IMA for each second when the NE Tx LSM is Unusable, as indicated in Table 19 on page 77?		M	(R-130)	Yes X No__

Table A-8. IMA Interface OAM Operation Functions *(3 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
OAM.31	Does the implementation increment Rx-UUS-IMA for each second when the NE Rx LSM is Unusable, as indicated in Table 19 on page 77?		M	(R-131)	Yes X No__
OAM.32	Does the implementation increment Tx-UUS-IMA-FE for each second when the FE Tx LSM is reported Unusable, as indicated in Table 19 on page 77?		M	(R-132)	Yes X No__
OAM.33	Does the implementation increment Rx-UUS-IMA-FE for each second when the FE Rx LSM is reported Unusable, as indicated in Table 19 on page 77?		M	(R-133)	Yes X No__
OAM.34	Does the implementation increment Tx-FC each time the Tx-Mis-Connected link failure condition is entered, as indicated in Table 19 on page 77?		M	(R-134)	Yes X No__
OAM.35	Does the implementation increment Tx-FC each time the Tx-Fault link failure condition is entered, as indicated in Table 19 on page 77?		M	(R-134)	Yes X No__
OAM.36	Does the implementation increment Rx-FC each time the LIF link failure condition is entered, as indicated in Table 19 on page 77?		M	(R-135)	Yes X No__
OAM.37	Does the implementation increment Rx-FC each time the LODS link failure condition is entered, as indicated in Table 19 on page 77?		M	(R-135)	Yes X No__
OAM.38	Does the implementation increment Rx-FC each time the Rx-Mis-Connected link failure condition is entered, as indicated in Table 19 on page 77?		M	(R-135)	Yes X No__
OAM.39	Does the implementation increment Rx-FC each time the Rx-Fault link failure condition is entered, as indicated in Table 19 on page 77?		M	(R-135)	Yes X No__
OAM.40	Does the implementation increment Tx-FC-FE each time the Tx-Unusable-FE link failure condition is entered, as indicated in Table 19 on page 77?		O	(O-21)	Yes X No__
OAM.41	Does the implementation increment Rx-FC-FE each time the RFI-IMA link failure condition is entered, as indicated in Table 19 on page 77?		O	(O-22)	Yes X No__
OAM.42	Does the implementation increment Rx-FC-FE each time the Rx-Unusable-FE link failure condition is entered, as indicated in Table 19 on page 77?		O	(O-22)	Yes X No__
OAM.43	Does the implementation increment Tx-Stuff-IMA for each stuff event inserted in the transmit direction, as indicated in Table 19 on page 77?		O	(O-23)	Yes X No__
OAM.44	Does the implementation increment Rx-Stuff-IMA for each stuff event detected in the receive direction, except during seconds when a SES-IMA or UAS-IMA condition is reported, as indicated in Table 19 on page 77?		O	(O-24)	Yes X No__
OAM.45	Does the implementation increment GR-UAS-IMA for each second when the GTSM is down, as indicated in Table 19 on page 77?		M	(R-136)	Yes X No__

Table A-8. IMA Interface OAM Operation Functions *(4 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
OAM.46	Does the implementation increment GR-FC each time the Config-Aborted group failure condition is entered, as indicated in Table 19 on page 77?		M	(R-137)	Yes X No__
OAM.47	Does the implementation increment GR-FC each time the Insufficient-Links group failure condition is entered, as indicated in Table 19 on page 77?		M	(R-137)	Yes X No__
OAM.48	Does the implementation increment GR-FC-FE each time the Start-up-FE group failure condition is entered, as indicated in Table 19 on page 77?		O	(O-25)	Yes X No__
OAM.49	Does the implementation increment GR-FC-FE each time the Config-Aborted-FE group failure condition is entered, as indicated in Table 19 on page 77?		O	(O-25)	Yes X No__
OAM.50	Does the implementation increment GR-FC-FE each time the Insufficient-Links-FE group failure condition is entered, as indicated in Table 19 on page 77?		O	(O-25)	Yes X No__
OAM.51	Does the implementation increment GR-FC-FE each the Blocked-FE group failure condition is entered, as indicated in Table 19 on page 77?		O	(O-25)	Yes X No__
OAM.52	Does the implementation accumulate IMA performance parameters over 15 minute intervals?		O	(O-26)	Yes X No__
OAM.53	Does the implementation accumulate IMA performance parameters over 24 hour intervals?		O	(O-27)	Yes__ No X
OAM.54	Does the implementation keep the current/previous and recent data?	(O-26)	M	(CR-7)	Yes X No__
OAM.55	Does the implementation use the current data for threshold crossing?	(O-26)	M	(CR-8)	Yes__ No X
OAM.56	Does the implementation keep the current/previous and recent data?	(O-27)	M	(CR-9)	Yes__ No X
OAM.57	Does the implementation use the current data for threshold crossing?	(O-27)	M	(CR-10)	Yes__ No X
OAM.58	Does the implementation report a LIF failure alarm for the persistence of a LIF defect at the NE?		M	(R-138)	Yes X No__
OAM.59	Does the implementation report a LODS failure alarm for the persistence of a LODS defect at the NE?		M	(R-139)	Yes X No__
OAM.60	Does the implementation report a RFI-IMA failure alarm for the persistence of a RDI-IMA defect at the NE?		M	(R-140)	Yes X No__
OAM.61	Does the implementation report Tx-Mis-Connected failure alarm when the Tx link is detected as mis-connected?		M	(R-141)	Yes X No__
OAM.62	Does the implementation report Rx-Mis-Connected failure alarm when the Rx link is detected as mis-connected?		M	(R-142)	Yes X No__
OAM.63	Does the implementation report a Tx Fault failure alarm for any implementation specific Tx fault declared at the NE?		O	(O-28)	Yes__ No X

Table A-8. IMA Interface OAM Operation Functions *(5 of 5)*

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
OAM.64	Does the implementation report a Rx Fault failure alarm for any implementation specific Rx fault declared at the NE?		O	(O-29)	Yes__ No X
OAM.65	Does the implementation report a Tx-Unusable-FE failure alarm when it receives Tx-Unusable from FE?		M	(R-143)	Yes X No__
OAM.66	Does the implementation report a Rx-Unusable-FE failure alarm when it receives Rx-Unusable from FE?		M	(R-144)	Yes X No__
OAM.67	Does the implementation report a Start-up-FE failure alarm when it receives this signal from FE (the declaration of this failure alarm may be delayed to ensure the FE remains in Start-up)?		M	(R-145)	Yes X No__
OAM.68	Does the implementation report a Config-Aborted failure alarm when the FE tries to use unacceptable configuration parameters?		M	(R-146)	Yes X No__
OAM.69	Does the implementation report a Config-Aborted-FE failure alarm when the FE reports unacceptable configuration parameters?		M	(R-147)	Yes X No__
OAM.70	Does the implementation report an Insufficient-Links failure alarm when less than P_{Tx} transmit links or P_{Rx} receive links are active?		M	(R-148)	Yes X No__
OAM.71	Does the implementation report an Insufficient-Links-FE failure alarm when the FE reports that less than P_{Tx} transmit links or P_{Rx} receive links are active?		M	(R-149)	Yes X No__
OAM.72	Does the implementation report a Blocked-FE failure alarm when the FE reports that it is blocked?		M	(R-150)	Yes X No__
OAM.73	Does the implementation report GR-Timing-Mismatch when the FE transmit clock mode is different than the NE transmit clock mode?		M	(R-151)	Yes X No__
OAM.74	In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the implementation support 2.5 ± 0.5 seconds as a default persistence checking time to enter a failure alarm condition?		M	(R-152)	Yes X No__
OAM.75	In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the implementation support 10 ± 0.5 seconds as a default persistence clearing time to exit the failure alarm condition?		M	(R-152)	Yes X No__
OAM.76	In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the IMA allow configuration of other values for default persistence checking time to enter a failure alarm condition?		O	(O-30)	Yes X No__
OAM.77	In the case of the LIF, LODS, RFI-IMA and Fault failure alarms, does the IMA allow configuration of other values for default persistence checking time to exit the same failure alarm condition?		O	(O-30)	Yes X No__
OAM.78	Does the implementation ensure that the Tx-Fault failure alarm, as defined in (O-28) on page 79, is not cleared until the fault that led to the declaration of the alarm is no longer present for the duration specified to clear the alarm in (R-152) on page 80?	(O-28)	M	(CR-11)	Yes__ No X
OAM.79	Does the implementation ensure that the Rx-Fault failure alarm, as defined in (O-29) on page 79, is not cleared until the fault that led to the declaration of the alarm is no longer present for the duration specified to clear the alarm in (R-152) on page 80?	(O-29)	M	(CR-12)	Yes__ No X
Comments: 24 hour PM intervals require external software. No threshold crossing feature in driver. Link Fault failures are not defined in standard.					

Table A-9. Test Pattern Procedure (TPP) Functions

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
TPP.1	Does the implementation activate the Test Pattern procedure in the transmit direction?		O	(O-31)	Yes X No__
TPP.2	Does the implementation use the Test Link Command field in the ICP cell (as defined in the Tx Test Control field in Table 2 on page 31) to request the FE to activate the loop back of the test pattern contained in the Tx Test Pattern field?	(O-31)	M	(CR-12)	Yes X No__
TPP.3	Does the implementation use the Tx LID field defined in the Tx Test Control field in Table 2 on page 31 to identify to the FE which transmit link the FE should extract the Tx Test Pattern from in the received ICP cells?	(O-31)	M	(CR-12)	Yes X No__
TPP.4	Does the implementation send any changed values of the Test Link Command, Tx LID and Tx Test Pattern fields in ICP cells for at least 2 consecutive IMA frames over each link within the IMA group?	(O-31)	M	(CR-12)	Yes X No__
TPP.5	Does the implementation continue to send the same values of the Test Link Command, Tx LID and Tx Test Pattern fields as long as the IMA transmitter wants the FE IMA unit to loop back the test pattern?	(O-31)	M	(CR-12)	Yes X No__
TPP.6	Does the implementation monitor the incoming ICP cells on the links already recognized in the group to detect a change of the Test Link Command?		M	(R-153)	Yes X No__
TPP.7	If the Test Link Command field is detected as active over the links already recognized in the group and over the test link, does the implementation copy the value of the Tx Test Pattern field received from the test link, indicated over the Tx LID field, into the Rx Test Pattern field on every subsequent ICP cell sent over all outgoing links in the group?		M	(R-154)	Yes X No__
TPP.8	Does the implementation continue sending the same value over the Rx Test Pattern field until the IMA transmitter has received an indication to stop looping the pattern, to loop a new pattern received from the same link over the Tx Test Pattern, or to loop the test pattern received from another link (indicated over the Tx LID field)?		M	(R-155)	Yes X No__
TPP.9	Does the implementation return the “0xFF” pattern over the Rx Test Pattern field when the incoming test command is inactive or the test link is not detected?		M	(R-156)	Yes X No__
TPP.10	Does the implementation only handle one test pattern per IMA group at any given time?		M	(R-157)	Yes X No__
Comments:					

Table A-10. IMA Interaction with Plane Management Functions

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
IPM.1	Does the implementation process IMA group configuration indications received from the Plane Management?		M	(R-158)	Yes X No__
IPM.2	Does the implementation process IMA link addition/deletion indications received from the Plane Management?		M	(R-158)	Yes X No__
IPM.3	Does the implementation send IMA service operational status change indications to the Plane Management?		M	(R-158)	Yes X No__
IPM.4	Does the implementation send Tx/Rx cell rate change indications to the Plane Management?		M	(R-158)	Yes X No__
Comments: Plane Management software required to interface with driver API.					

Table A-11. Management Information Base (MIB) Functions

Item	Protocol feature	Cond. for Status	Status Pred.	Ref.	Support
MIB.1	Does the implementation support a UM based on SNMP?		O	(O-32)	Yes X No__
MIB.2	Does the implementation implement the mandatory objects in the IMA-MIBs defined in Appendix A on page 106?	(O-32)	M	(CR-17)	Yes__ No X
MIB.3	Does the implementation implement the optional objects in the IMA MIBs defined in Appendix A on page 106?	(O-32)	O	(O-33)	Yes__ No X
Comments: Support for MIB objects implemented. Requires SNMP agent software to create MIB using driver API.					

A.6 PICS Proforma References

[A-1] The ATM Forum, AF-PHY-0086.001, Inverse Multiplexing for ATM (IMA) Specification Version 1.1.

[A-2] ISO/IEC 9646-1: 1990, Information technology - Open systems interconnection - Conformance testing methodology and framework - Part 1: General concepts (See also ITU-T Recommendation X.290 (1991)).

[A-3] ISO/IEC 9646-2: 1990, Information technology - Open systems interconnection - Conformance testing methodology and framework - Part 2: Abstract test suite specification (See also ITU-T Recommendation X.291 (1991)).

[A-4] ITU-T Recommendation I.432 Series, “B-ISDN User-Network Interface - Physical Layer Specification”, April 1996.

[A-5] ITU-T Recommendation I.610, “B-ISDN Operation and Maintenance Principles and Functions”, 1995.

B

Boundary Scan

Please contact Mindspeed for information and files for Boundary Scan.

MINDSPEED™

www.mindspeed.com

General Information:
U.S. and Canada: (800) 854-8099
International: (949) 483-6996
Headquarters - Newport Beach
4311 Jamboree Rd. P.O. Box C
Newport Beach, CA. 92658-8902