Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

CX28365/6/4

x12, x6, x4 T3/E3 Framer and ATM Cell Transmission Convergence Sublayer Processor

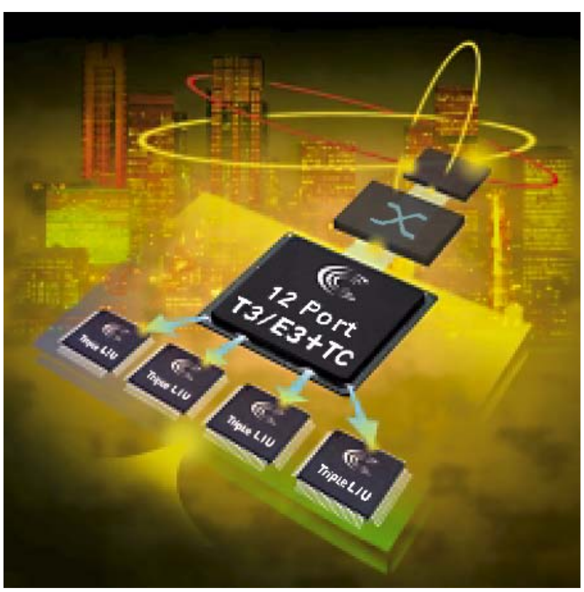
The CX2836x is a family of devices that provides up to twelve T3/E3 framers that support DS3-M13, DS3-C-bit parity, E3-G.751, and E3-G.832 transmission formats integrated with ATM physical layer processing functions. These functions are found in the *ATM Forum Cell-Based Transmission Convergence Sublayer Specification* (af-phy-0043.000), *DS3 Physical Layer Interface Specification* (af-phy-0054.000), and *E3 Public UNI Specification* (af-phy-0034.000).

The CX2836x provides framing recovery for M13, M23, C-bit parity, G.751, and G.832 formatted signals. Access is provided to the FEAC and TDL channels.

The CX2836x device allows for ease of configuration, while providing maximum flexibility to support the transmission and recovery of industry standard formats. It provides a flexible opportunity bit generation method to source opportunity bits on an individual framer.

The CX2836x provides a high-density and low-cost solution for T3 and E3 UNI and NNI ATM interfaces. A complete design for interfacing cells from a standard UTOPIA Level 2 system interface to the physical line connections requires only the addition of four triple Line Interface Units (LIUs) or a single twelve port LIU, and a microprocessor for configuration and control.

The CX28365 is an x12 T3/E3 framer with transmission convergence. The CX28366 is an x6 T3/E3 framer with transmission convergence, and the CX28364 is a quad T3/E3 framer with transmission convergence. Both the CX28366 and CX28364 perform identically to the CX28365.



Distinguishing Features

- Twelve, six, or four independent DS3/E3 framers in one package
- Line coding supported:
  - DS3: B3ZS, NRZ, AMI
  - E3: HDB3, NRZ, AMI
- Framing supported:
  - DS3: M13, M23, C-bit parity
  - E3: G.751, G.832
- Inserts and extracts opportunity bits
- Full FEAC and TDL channel support
- Full performance monitoring support per T1.231 standard
- Glueless interfaces to the following devices:
  - LIU Interfaces:
    - Mindspeed's DS3/E3/STS-1 LIU CX28333–1x, –3x, M28335
  - SAR interfaces: Bt8233/RS8234
  - Network processors: CX27440/CX27460
  - HDLC controllers: CX23500
- S-RAM-type processor interface
- PLCP or direct framing selectable per port
- Power supplies and power consumption
  - I/O 3.3 V, input 5 V tolerant, core 1.8 V
  - Low power operation (<190 mW per port)
- UTOPIA Interface
  - Level 2
  - 8- and 16-bit modes
  - Multi-PHY capability
  - Redundant channel
- Cell Delineator
  - Passes or rejects idle cells or selected cells based on header register configuration
  - Recovers cell alignment from HEC
  - Performs single-bit HEC error correction and multiple-bit detection
  - Generates cell status bits, cell counts, and error counts
  - Reads cell data from the UTOPIA FIFO
  - Inserts idle cells when no traffic is available
  - ITU I.432-compliant

Testing

- JTAG boundary scan support

Applications

- Digital Cross-Connect Systems
- Optical Transport Equipment
- Access Concentrators
- ATM Switches
- Concentrators
- Routers

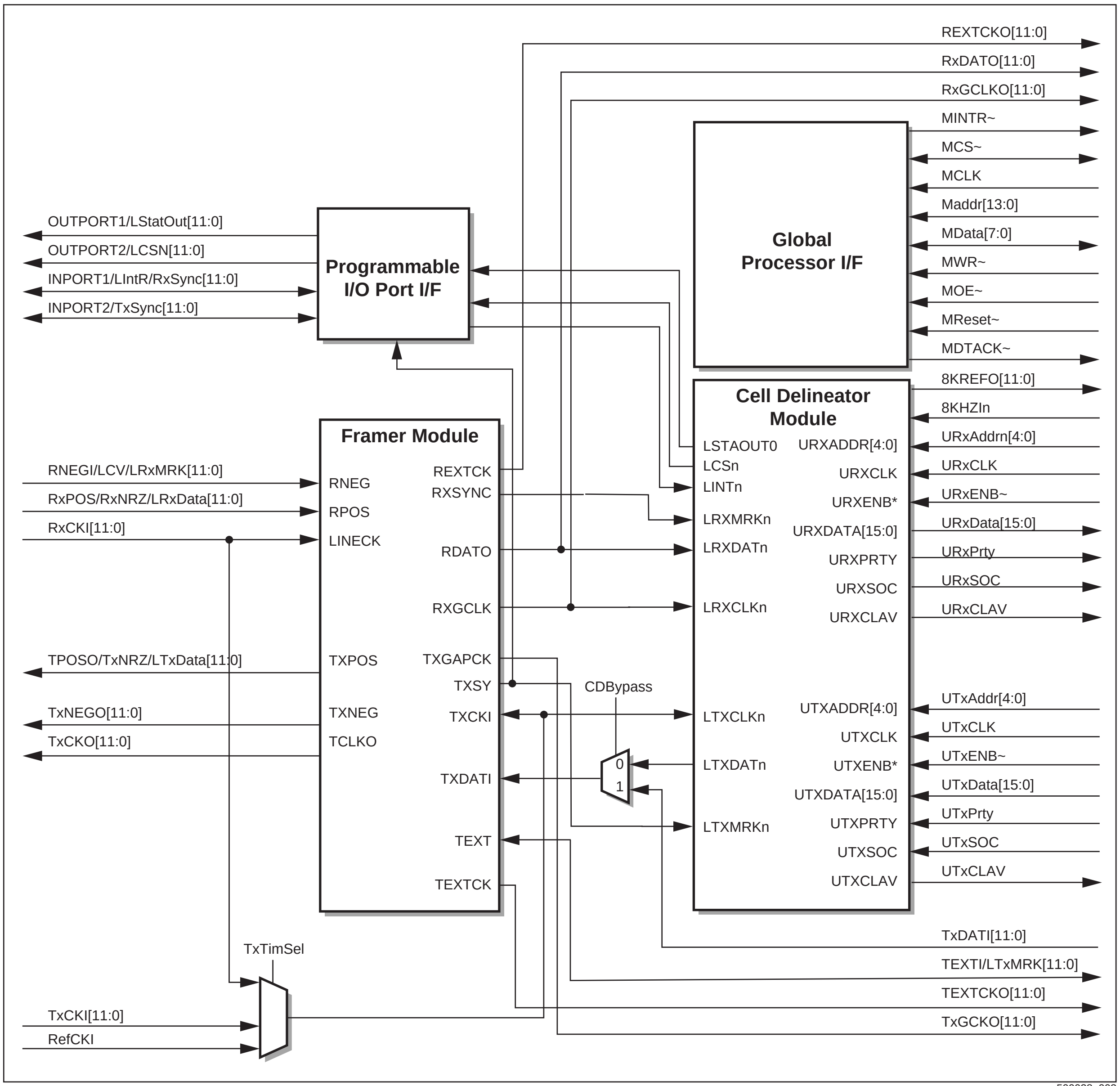
Ordering Information

Model Number	Number of Framers	Package	Ambient Temperature Range
CX28365	12	456-ball, 35 mm PBGA	–40 °C to 85 °C
CX28366	6	456-ball, 35 mm PBGA	–40 °C to 85 °C
CX28364	4	456-ball, 35 mm PBGA	–40 °C to 85 °C

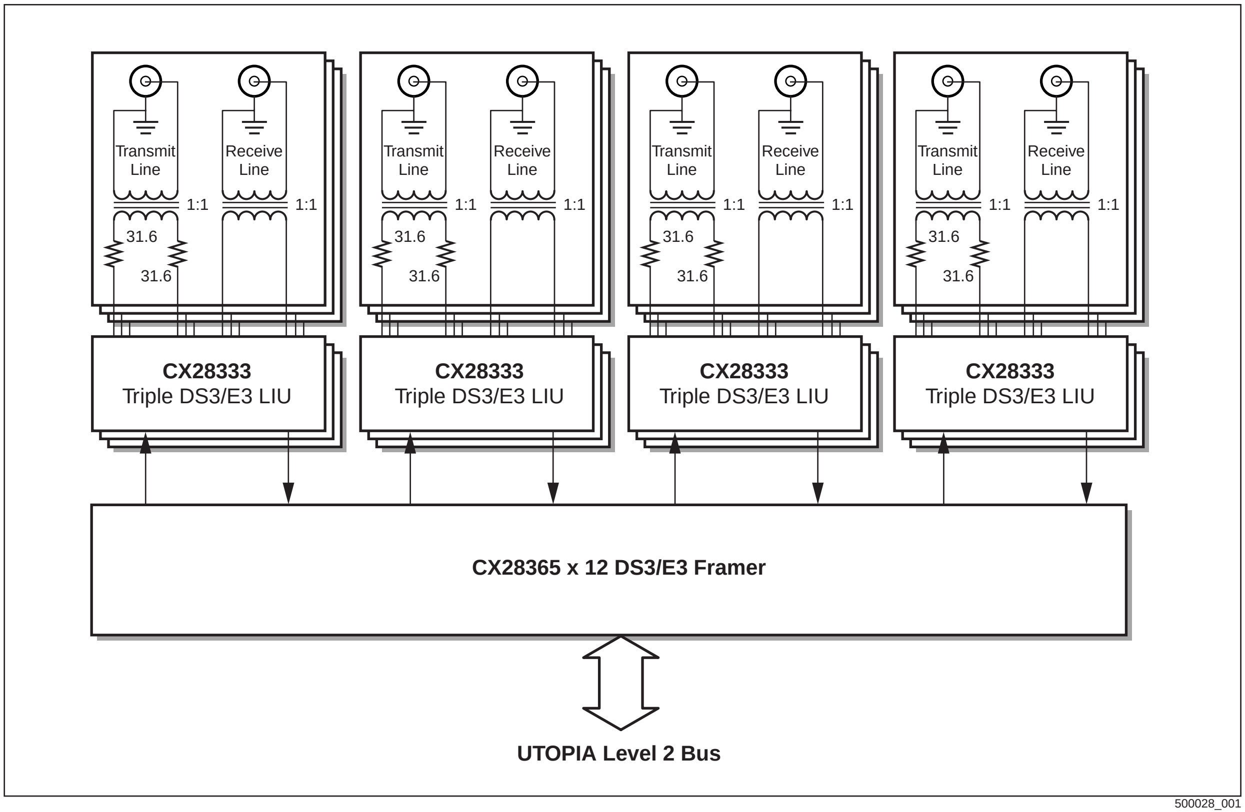
Revision History

Revision	Level	Date	Description
101104A	Advance	August 2000	Initial release.
101104B	Advance	February 2001	Added timing diagrams, tables, and functional description. General corrections. Deleted MDtack*.
101104C	Advance	February 2001	Added CX28366 and CX28364 versions. General corrections.
500028A	Advance	February 2001	Initial release under document number 500028A. Formerly document number 101104C.
500028B	Advance	February 2002	Incorporated changes from Errata document 500152B dated 12/13/01 and made general corrections.
500028C	Preliminary	May 2002	Incorporated Errata 500354A.

Functional Block Diagram



Typical Application—12 Port DS3 ATM Line Card



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1.0 Product Description

The CX2836x provides up to twelve DS3/E3 framers, each integrated with ATM physical layer processing functions. The framers support DS3-M13, DS3-C-bit parity, E3-G.751, and E3-G.832 transmission formats. Access is provided to the FEAC and TDL channels. The CX2836x integrates all the ATM Layer processing functions found in the *ATM Forum Cell-Based Transmission Convergence Sublayer* specification (af-phy-0043.000) in each of the twelve ports. The ATM cell processor is also referred to as the cell delineator. A UTOPIA Level 2 Multi-PHY interface connects the device to the host switch or terminal system and concentrates the ATM cell traffic onto a single bus interface.

Although designed primarily for DS3/E3 line applications, the ATM cell processor can be individually bypassed. Each port may be configured for operation at speeds from 64 Kbps to 52 Mbps, allowing a maximum aggregate bandwidth of 624 Mbps. Typical system implementations center around the concentration of multiple standard data rates such as T1 and E1 lines, DS3 and E3 lines, and multiple Digital Subscriber Line (DSL) formats such as HDSL, ADSL or VDSL. For each specific format, external devices perform the appropriate PMD (physical media dependant) layer functions and present the CX2836x with a payload bit stream. The CX2836x then performs all cell alignment functions on that bit stream. This gives system designers a simple, modular, and low-cost architecture for supporting all ATM interfaces below 52 Mbps. It also enables them to select the most integrated framer and LIU available, or reuse existing devices and software.

If the cell processor is bypassed, all framer signals are available, and the framer can be used as a standalone DS3/E3 framer. The CX2836x device allows for ease of configuration, while providing maximum flexibility to support the transmission and recovery of industry standard formats. It provides a flexible opportunity bit generation method to source Opportunity bits on an individual framer.

1.1 Application Overview

1.1.1 Logic Diagram

The CX2836x consists of the following interfaces:

- Framer Transmit and Receive Line Interface
- Framer Transmit and Receive System Interface
- ATM UTOPIA Transmit Interface
- ATM UTOPIA Receive Interface
- Programmable Input/Output Port
- Microprocessor Interface
- JTAG Interface

Logic Diagrams for the CX28365 are illustrated in Figures 1-1 and 1-2. Figure 1-1 includes signals that are present on the device if both framer and cell delineator are enabled. The cell delineator can be bypassed individually on a per port basis. Figure 1-2 illustrates this case.

The CX28366 and CX28364 devices are the same except for the number of ports.

Figure 1-1. CX28365 Logic Diagram, Framer, and Cell Delineator Enabled

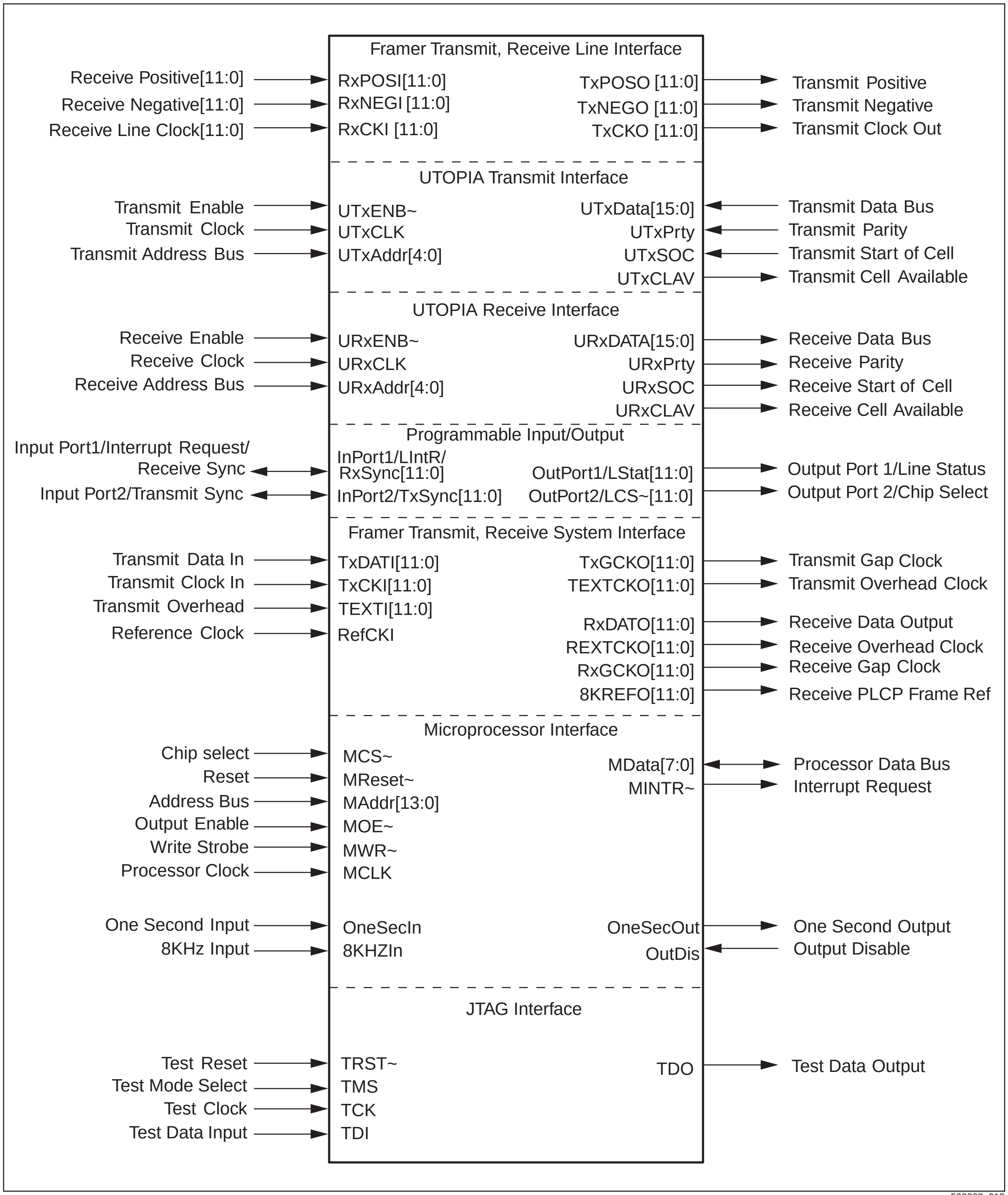
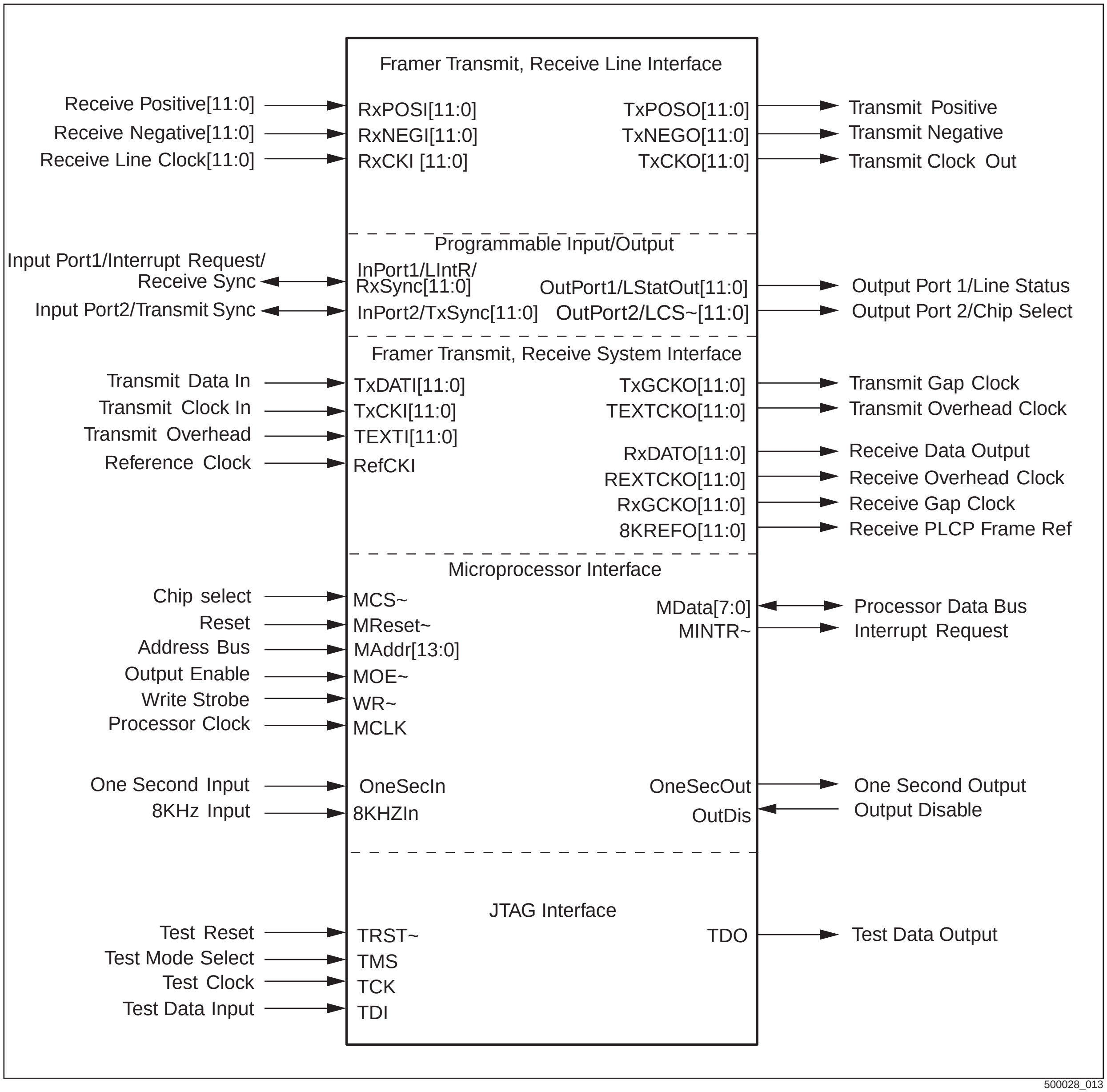


Figure 1-2. CX28365 Logic Diagram, Cell Delineator Bypassed



1.2 Pin Diagram and Definitions

The CX2836x is packaged in a 456-Pin Ball Grid Array (BGA) package with a body size of 35 mm × 35 mm and a pin pitch of 1.27 mm. Pin assignments are listed and described in Tables 1-1–1-7. Figures 1-3, 1-4, and 1-5 provide pinout diagrams.

Figure 1-3. CX28365 Pinout Diagram

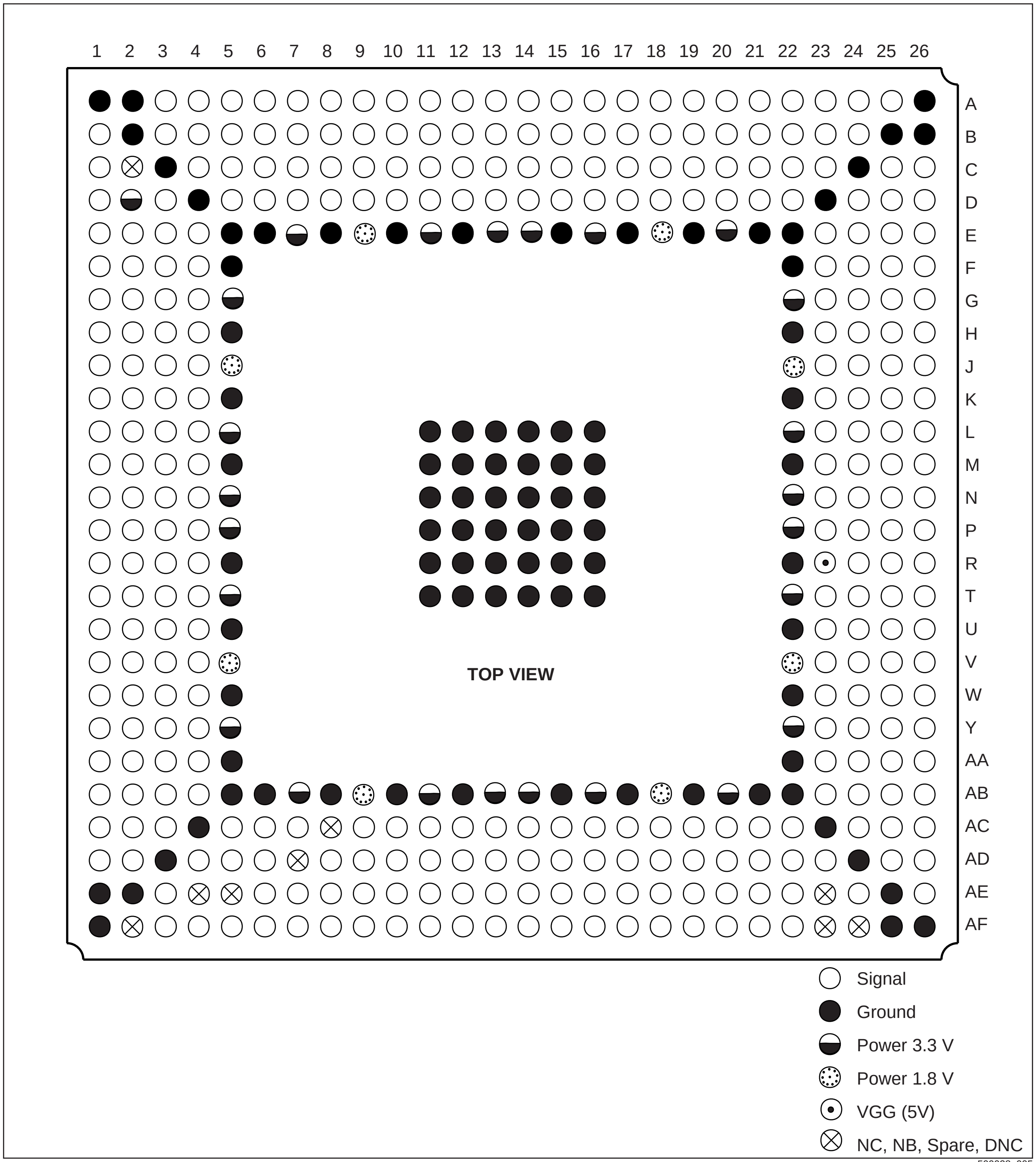


Figure 1-4. CX28366 Pinout Diagram

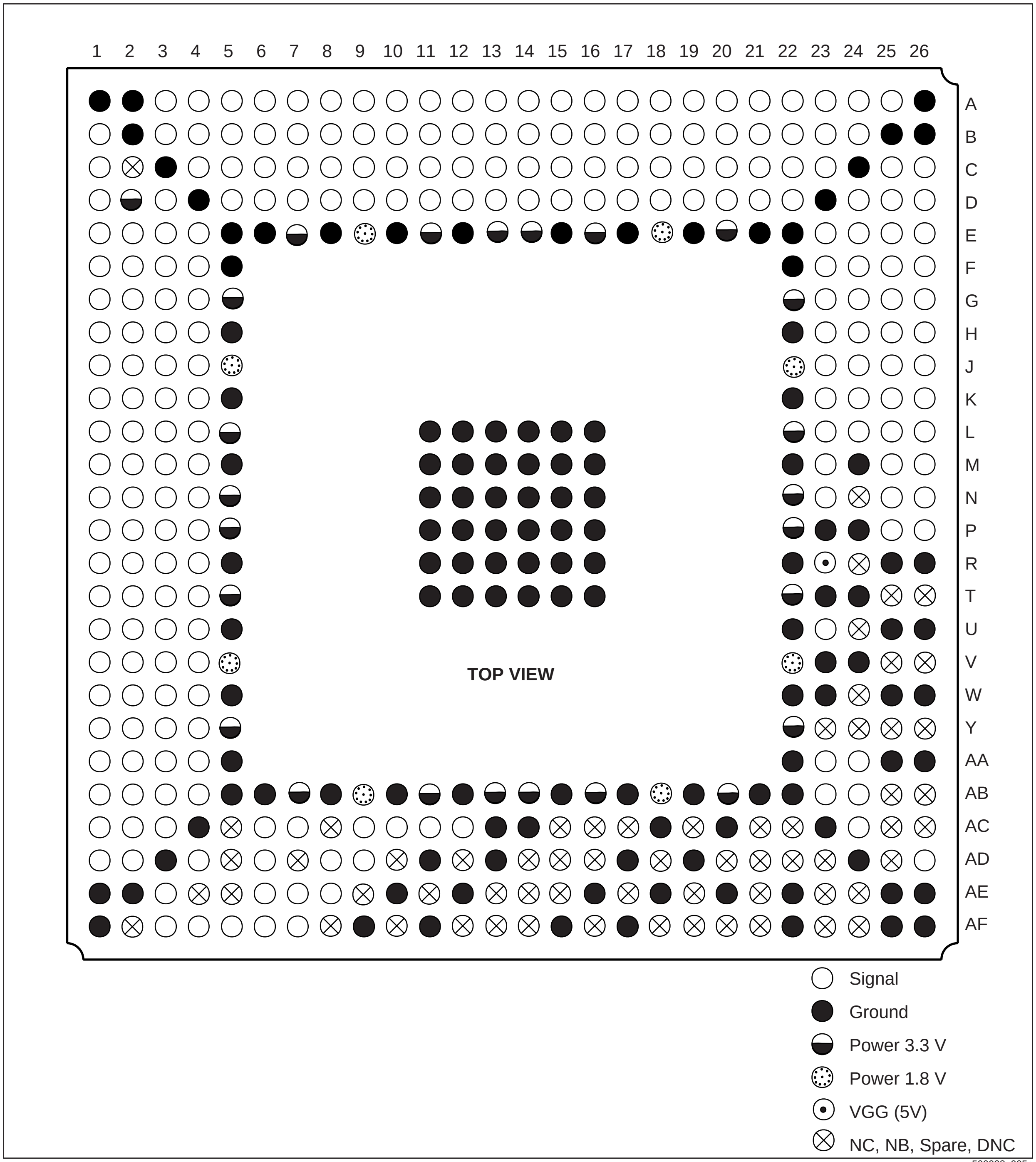
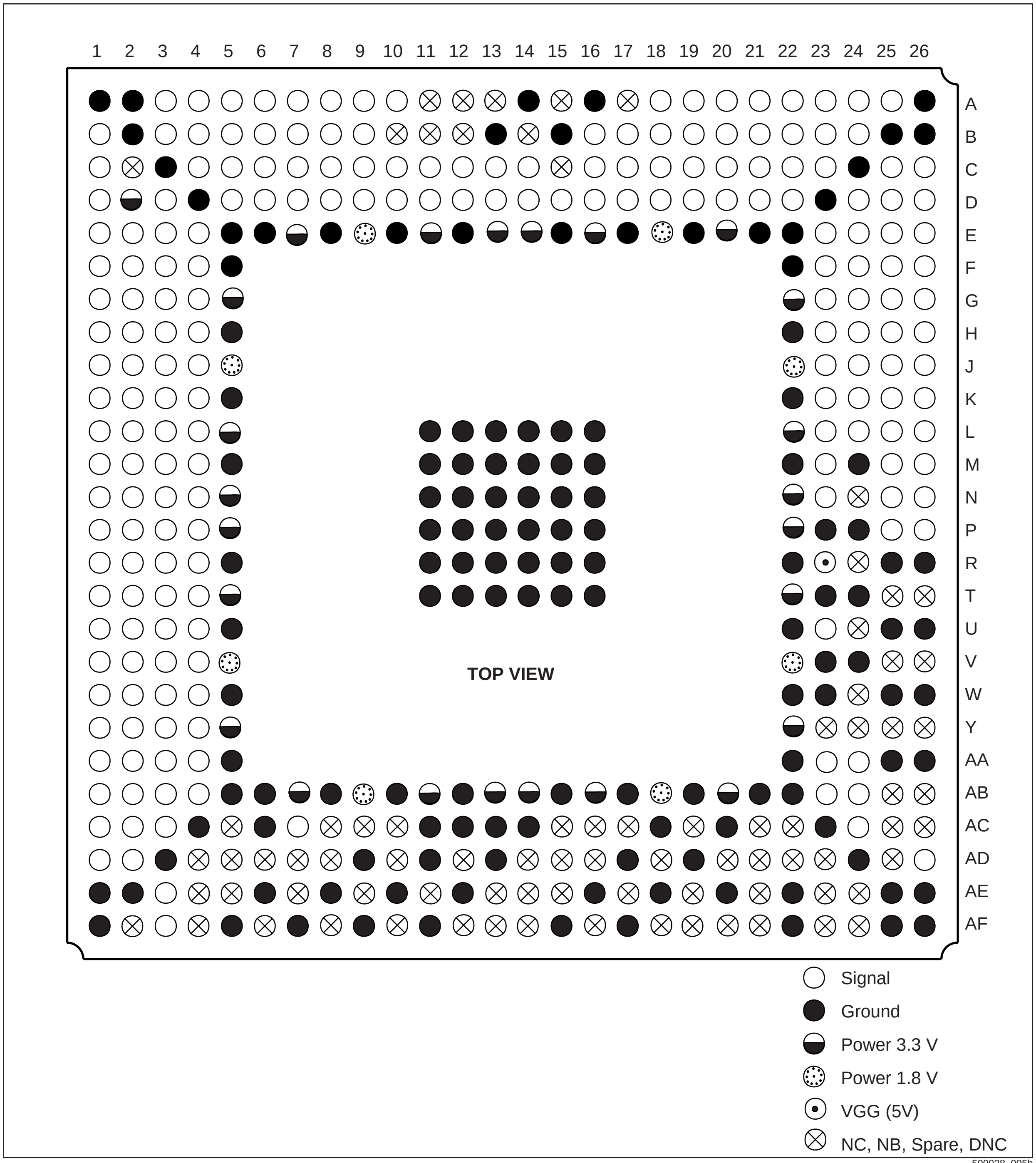


Figure 1-5. CX28364 Pinout Diagram



1.2.1 Pin Definitions

Table 1-1. Hardware Signal Definition, Microprocessor Interface (1 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
MReset*	Master Reset	A4	A4	A4	I	When active (low), all registers and counters are initialized to their default values. MReset operates in synchronous fashion and, therefore, requires that all line and system clocks are present during the reset period for a minimum of 30 cycles.
MCLK	Microprocessor Clock	E4	E4	E4	I	An 8-50 MHz clock signal input. The microprocessor interface inputs/outputs, address and data signals are sampled on the rising edge of this signal. This clock is also used to sample the input data on the Programmable InPort1 and InPort2 pins. Schmitt trigger input.
MOE*	Output Enable	E3	E3	E3	I	Enables MData outputs during a read operation when active low. When high, MData[7:0] outputs are high impedance.
MCS*	Chip Select	D3	D3	D3	I	Active-low enables the read/write decoder. A high ends the current read or write cycle and places MData[7:0] outputs in high impedance.
MWR*	Write Strobe	F4	F4	F4	I	Used by the microprocessor to indicate a write cycle if low.
MData[7] MData[6] MData[5] MData[4] MData[3] MData[2] MData[1] MData[0]	Microprocessor Data Bus (LSB)	F3 G4 F2 G3 H4 G2 H3 J4	F3 G4 F2 G3 H4 G2 H3 J4	F3 G4 F2 G3 H4 G2 H3 J4	I/O/Z	Eight-bit bidirectional bus used for connecting to a microprocessor system data bus and transferring data to/from registers.
MDTACK*	Data Transfer Acknowledge	C2	C2	C2	O/Z	Open drain, active low output signifiies in-progress data transfer cycle. Data-ready indication for read; transaction-end indication for write.

Table 1-1. Hardware Signal Definition, Microprocessor Interface (2 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
MAddr[13] MAddr[12] MAddr[11] MAddr[10] MAddr[9] MAddr[8] MAddr[7] MAddr[6] MAddr[5] MAddr[4] MAddr[3] MAddr[2] MAddr[1] MAddr[0]	Microprocessor Address Bus (LSB)	H2 J3 K4 J2 K3 L4 K2 L3 M4 L2 M3 N4 N3 P4	H2 J3 K4 J2 K3 L4 K2 L3 M4 L2 M3 N4 N3 P4	H2 J3 K4 J2 K3 L4 K2 L3 M4 L2 M3 N4 N3 P4	I	14-bit input bus used to identify a register for subsequent read/write data transfer cycle.
MINTR*	Interrupt Request	E2	E2	E2	O^P/Z	Open drain active low output signifies one or more pending interrupt requests. MINTR* goes to high impedance state after processor has serviced all pending interrupt requests.
8KHZIn	8 kHz Input	A5	A5	A5	I	Provides timing control for PLCP framing and can be used as the timing source to generate a one-second timer. Schmitt trigger input.
OneSecIn	One-Second Input	A7	A7	A7	I	Rising edge controls or marks one-second interval used for counter latching. This pin is internally pulled low.
OneSecOut	One-Second Output	A6	A6	A6	O	Rising edge indicates start of each one-second interval. It is derived from the 8 kHz input, (pulse width is one clock period).

Table 1-2. Hardware Signal Definition, Transmit/Receive Line Interface (1 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
TxCKO[0] TxCKO[1] TxCKO[2] TxCKO[3] TxCKO[4] TxCKO[5] TxCKO[6] TxCKO[7] TxCKO[8] TxCKO[9] TxCKO[10] TxCKO[11]	Framer Transmit Clock	P3 T3 V3 Y3 AD6 AD8 AD10 AD12 W24 U24 R24 N24	P3 T3 V3 Y3 AD6 AD8 — — — — — —	P3 T3 V3 Y3 — — — — — — — —	O/Z	Used to clock out the TxPOSO/ TxNRZ and TxNEGO framer transmit outputs. Data is clocked out on the rising or on the falling edge of TxCKO according to settings of bit LTxCkRis (Feature2 Control register).
TxPOSO/TxNRZ[0] TxPOSO/TxNRZ[1] TxPOSO/TxNRZ[2] TxPOSO/TxNRZ[3] TxPOSO/TxNRZ[4] TxPOSO/TxNRZ[5] TxPOSO/TxNRZ[6] TxPOSO/TxNRZ[7] TxPOSO/TxNRZ[8] TxPOSO/TxNRZ[9] TxPOSO/TxNRZ[10] TxPOSO/TxNRZ[11]	Framer Transmit Positive Rail or NRZ Data	N2 R2 U2 W2 AC10 AE7 AE9 AE11 AB25 Y25 V25 T25	N2 R2 U2 W2 AC10 AE7 — — — — — —	N2 R2 U2 W2 — — — — — — — —	O/Z	These pins are transmitter positive rail data (bipolar) or NRZ (unipolar nonreturn-to-zero) data outputs.
TxNEGO[0] TxNEGO[1] TxNEGO[2] TxNEGO[3] TxNEGO[4] TxNEGO[5] TxNEGO[6] TxNEGO[7] TxNEGO[8] TxNEGO[9] TxNEGO[10] TxNEGO[11]	Framer Transmit Negative Rail Data	M1 P1 T1 V1 AF4 AF6 AF8 AF10 AB26 Y26 V26 T26	M1 P1 T1 V1 AF4 AF6 — — — — — —	M1 P1 T1 V1 — — — — — — — —	O/Z	The negative output (bipolar) generated by the B3ZS/HDB3/AMI encoder. Not used in unipolar NRZ mode.
RxCKI[0] RxCKI[1] RxCKI[2] RxCKI[3] RxCKI[4] RxCKI[5] RxCKI[6] RxCKI[7] RxCKI[8] RxCKI[9] RxCKI[10] RxCKI[11]	Framer Receive Line Clock	R3 U3 W3 AA3 AC11 AD9 AD11 AD13 V24 T24 P24 M24	R3 U3 W3 AA3 AC11 AD9 — — — — — —	R3 U3 W3 AA3 — — — — — — — —	I	Used to clock in the RxPOSI and RxNEGI or RxNRZ signals. In the framer enable mode, the receiver line clock operates at 44.736 MHz (DS3 rate) or 34,368 MHz (E3 rate) Schmitt trigger input. Note: RxCKI must be present for proper register-read/writes.

Table 1-2. Hardware Signal Definition, Transmit/Receive Line Interface (2 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
RxPOSI/RxNRZ[0] RxPOSI/RxNRZ[1] RxPOSI/RxNRZ[2] RxPOSI/RxNRZ[3] RxPOSI/RxNRZ[4] RxPOSI/RxNRZ[5] RxPOSI/RxNRZ[6] RxPOSI/RxNRZ[7] RxPOSI/RxNRZ[8] RxPOSI/RxNRZ[9] RxPOSI/RxNRZ[10] RxPOSI/RxNRZ[11]	Framer Receive Positive Rail or NRZ Data	P2 T2 V2 Y2 AE6 AE8 AE10 AE12 AA25 W25 U25 R25	P2 T2 V2 Y2 AE6 AE8 — — — — — —	P2 T2 V2 Y2 — — — — — — — —	I	This pin is the framer receive positive rail data (bipolar mode) or NRZ (unipolar mode) data input and is sampled on the falling edge of RxCKI. This pin is internally pulled low.
RxNEGI/LCVI[0] RxNEGI/LCVI[1] RxNEGI/LCVI[2] RxNEGI/LCVI[3] RxNEGI/LCVI[4] RxNEGI/LCVI[5] RxNEGI/LCVI[6] RxNEGI/LCVI[7] RxNEGI/LCVI[8] RxNEGI/LCVI[9] RxNEGI/LCVI[10] RxNEGI/LCVI[11]	Framer Receive Negative Rail Data or Line Code Violation Indication	N1 R1 U1 W1 AF5 AF7 AF9 AF11 AA26 W26 U26 R26	N1 R1 U1 W1 AF5 AF7 — — — — — —	N1 R1 U1 W1 — — — — — — — —	I	This pin is the framer line receive negative rail data input (bipolar mode) or LCV input indication (unipolar NRZ mode). Data is sampled by RxCKI. The edge is programmable. This pin is internally pulled low.

Table 1-3. Hardware Signal Definition, Transmit/Receive Systems Interface (1 of 3)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
TEXTI[0] TEXTI[1] TEXTI[2] TEXTI[3] TEXTI[4] TEXTI[5] TEXTI[6] TEXTI[7] TEXTI[8] TEXTI[9] TEXTI[10] TEXTI[11]	Framer Transmit External Overhead Input	C4 C8 C12 B6 B13 A14 AF15 AF22 AE16 AE20 AD17 AC18	C4 C8 C12 B6 B13 A14 — — — — — —	C4 C8 C12 B6 — — — — — — — —	I	This input pin is used to insert externally supplied framer Opportunity bits into transmitted bit stream.
TEXTCKO[0] TEXTCKO[1] TEXTCKO[2] TEXTCKO[3] TEXTCKO[4] TEXTCKO[5] TEXTCKO[6] TEXTCKO[7] TEXTCKO[8] TEXTCKO[9] TEXTCKO[10] TEXTCKO[11]	Framer Transmit External Overhead Clock	C5 C9 C13 B7 B14 A15 AF16 AE24 AE17 AE21 AD18 AC19	C5 C9 C13 B7 B14 A15 — — — — — —	C5 C9 C13 B7 — — — — — — — —	O/Z	Used to indicate to the system when to insert new Opportunity bits on the TEXTI pin. This pin is internally pulled low.
TxDATI[0] TxDATI[1] TxDATI[2] TxDATI[3] TxDATI[4] TxDATI[5] TxDATI[6] TxDATI[7] TxDATI[8] TxDATI[9] TxDATI[10] TxDATI[11]	Framer Transmit Data Input	R4 U4 W4 AA4 AC6 AC12 AC13 AC14 W23 V23 T23 P23	R4 U4 W4 AA4 AC6 AC12 — — — — — —	R4 U4 W4 AA4 — — — — — — — —	I	MODE: CDBypass = 0 Not used. MODE: CDBypass = 1 Serial data input to the framer transmitter controlled by TxTimSel[1:0] bits in the corresponding port Mode Control register, PORTn. TxDATI is sampled on the falling edge of one of the following clock sources: REFCKI, TxCKI[11:0], RxCKI[11:0], or RxCKI[11:0]. This pin is internally pulled low.
TxCKI[0] TxCKI[1] TxCKI[2] TxCKI[3] TxCKI[4] TxCKI[5] TxCKI[6] TxCKI[7] TxCKI[8] TxCKI[9] TxCKI[10] TxCKI[11]	Transmit Clock Input	C6 C10 C14 B8 B15 A16 AF17 AE26 AE18 AE22 AD19 AC20	C6 C10 C14 B8 B15 A16 — — — — — —	C6 C10 C14 B8 — — — — — — — —	I	If selected as the transmitter clock source, it is used to clock transmit data from the cell delineator to the framer or from the TxDATI pin to the framer. The data inputs are sampled on the falling edge. Schmitt trigger input.

Table 1-3. Hardware Signal Definition, Transmit/Receive Systems Interface (2 of 3)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
TxGCKO[0] TxGCKO[1] TxGCKO[2] TxGCKO[3] TxGCKO[4] TxGCKO[5] TxGCKO[6] TxGCKO[7] TxGCKO[8] TxGCKO[9] TxGCKO[10] TxGCKO[11]	Framer Transmit Gapped Clock	C7 C11 D14 B9 C15 A17 AF18 AD25 AE19 AC22 AD20 AC21	C7 C11 D14 B9 C15 A17 — — — — — —	C7 C11 D14 B9 — — — — — — — —	O/Z	A gapped clock that is derived from the falling edge of the TxCKI clock. It is gapped during Opportunity bits which are not selected to be inserted with payload on TxDATI. Its polarity is programmable.
RxGCKO[0] RxGCKO[1] RxGCKO[2] RxGCKO[3] RxGCKO[4] RxGCKO[5] RxGCKO[6] RxGCKO[7] RxGCKO[8] RxGCKO[9] RxGCKO[10] RxGCKO[11]	Framer Receive Gapped Clock	D5 D8 D11 B3 B10 A11 AF12 AF19 AE13 AD21 AD14 AC15	D5 D8 D11 B3 B10 A11 — — — — — —	D5 D8 D11 B3 — — — — — — — —	O/Z	A gapped clock signal output that is used to indicate RxDATO serial data output. RxGCKO clock polarity and behavior are programmable and have several options.
REXTCKO[0] REXTCKO[1] REXTCKO[2] REXTCKO[3] REXTCKO[4] REXTCKO[5] REXTCKO[6] REXTCKO[7] REXTCKO[8] REXTCKO[9] REXTCKO[10] REXTCKO[11]	Framer Receive Overhead Clock Output	D7 D10 D13 B5 B12 A13 AF14 AF21 AE15 AD23 AD16 AC17	D7 D10 D13 B5 B12 A13 — — — — — —	D7 D10 D13 B5 — — — — — — — —	O/Z	Used to indicate chosen Opportunity bits that output on RxDATO. This output has a clock pulse for each position of chosen group of Opportunity bits for the specific DS3/E3 mode. Its polarity is programmable.
RxDATO[0] RxDATO[1] RxDATO[2] RxDATO[3] RxDATO[4] RxDATO[5] RxDATO[6] RxDATO[7] RxDATO[8] RxDATO[9] RxDATO[10] RxDATO[11]	Framer Receive Serial Data Output	D6 D9 D12 B4 B11 A12 AF13 AF20 AE14 AD22 AD15 AC16	D6 D9 D12 B4 B11 A12 — — — — — —	D6 D9 D12 B4 — — — — — — — —	O/Z	Serial receive data output from framer. Data is clocked out on the rising edge of RxGCKO clock.

Table 1-3. Hardware Signal Definition, Transmit/Receive Systems Interface (3 of 3)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
8KREFO[0] 8KREFO[1] 8KREFO[2] 8KREFO[3] 8KREFO[4] 8KREFO[5] 8KREFO[6] 8KREFO[7] 8KREFO[8] 8KREFO[9] 8KREFO[10] 8KREFO[11]	Receive PLCP Frame or 8 kHz Reference Output	AC3 AB3 AA2 Y1 AC9 AD4 AD5 AC5 AC26 AC25 Y24 Y23	AC3 AB3 AA2 Y1 AC9 AD4 — — — — — —	AC3 AB3 AA2 Y1 — — — — — — — —	O/Z	PLCP frame reference output from the receiver for each port (if the port is set to PLCP mode) or is an 8 kHz clock divided from the line input clock (if the port is not set to PLCP mode).
RefCKI	Common Transmit Reference Clock	AB4	AB4	AB4	I	Reference clock for framer transmitter. It operates either 34.368 MHz (E3 Rate) or 44.736 MHz (DS3 rate).Schmitt trigger input.

Table 1-4. Hardware Signal Definition, ATM UTOPIA Interface (1 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
UTxCLK	UTOPIA Transmit Clock	D25	D25	D25	I	Clock input used to synchronize transmitted data. Schmitt trigger input.
UTxENB*	Transmit Enable	C25	C25	C25	I	Enables data transmission when asserted low. Schmitt trigger input.
UTxAddr[0] UTxAddr[1] UTxAddr[2] UTxAddr[3] UTxAddr[4]	UTOPIA Transmit Address	M26 L25 H24 L26 K25	M26 L25 H24 L26 K25	M26 L25 H24 L26 K25	I	Address of the PHY device being selected for transmission. Address 1111 (31 decimal) indicates a null PHY port. Schmitt trigger input.
UTxData[0] UTxData[1] UTxData[2] UTxData[3] UTxData[4] UTxData[5] UTxData[6] UTxData[7] UTxData[8] UTxData[9] UTxData[10] UTxData[11] UTxData[12] UTxData[13] UTxData[14] UTxData[15]	UTOPIA Transmit Data	K26 J25 G24 J26 H25 F24 H26 G25 E24 D22 G26 F25 D24 F26 E25 C23	K26 J25 G24 J26 H25 F24 H26 G25 E24 D22 G26 F25 D24 F26 E25 C23	K26 J25 G24 J26 H25 F24 H26 G25 E24 D22 G26 F25 D24 F26 E25 C23	I	Transmit data from the ATM layer. Schmitt trigger input.
UTxPrty	UTOPIA Transmit Parity Input	D26	D26	D26	I	Parity calculated over the UTxData bus. BusWidth (bit 0) in the IOMODE register (0x0202) determines whether parity is checked over UTxData[7:0] or UTxData[15:0]. OddEven (bit 2) in the UTOP1 register (0x0D) determines whether this pin represents even or odd parity. Schmitt trigger input.
UTxSOC	UTOPIA Transmit Start of Cell	E26	E26	E26	I	Indicates the first byte of valid cell data transmitted when asserted high. Schmitt trigger input.
UTxCLAV	UTOPIA Transmit Cell Available	C26	C26	C26	O	Indicates a FIFO full condition or Cell Available condition, depending upon UTOPIA HandShake (bit 1) in the SYSBUS register (0xE01). An external pulldown resistor is required for this pin.
URxCLK	UTOPIA Receive Clock	C22	C22	C22	I	Clock input used to synchronize received data. Schmitt trigger input.
URxENB*	Receive Enable	D21	D21	D21	I	Enables data reception when asserted low. Schmitt trigger input.

Table 1-4. Hardware Signal Definition, ATM UTOPIA Interface (2 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
URxAddr[0] URxAddr[1] URxAddr[2] URxAddr[3] URxAddr[4]	UTOPIA Receive Address	A18 B18 B17 B16 C16	A18 B18 B17 B16 C16	A18 B18 B17 B16 C16	I	Address of the PHY device being selected for reception. The address range is 0–30. Address 11111(31 decimal) indicates a null PHY port. Schmitt trigger input.
URxData[0] URxData[1] URxData[2] URxData[3] URxData[4] URxData[5] URxData[6] URxData[7] URxData[8] URxData[9] URxData[10] URxData[11] URxData[12] URxData[13] URxData[14] URxData[15]	UTOPIA Receive Data	B24 B23 C21 D20 B22 C20 D19 B21 C19 D18 B20 C18 D17 B19 C17 D16	B24 B23 C21 D20 B22 C20 D19 B21 C19 D18 B20 C18 D17 B19 C17 D16	B24 B23 C21 D20 B22 C20 D19 B21 C19 D18 B20 C18 D17 B19 C17 D16	O/Z	These pins output the received data to the ATM layer.
URxPrty	UTOPIA Receive Parity Input	D15	D15	D15	O/Z	Parity calculated over the URxData bus. BusWidth (bit 0) in the SYSBUS register (0xE01) determines whether parity is calculated over URxData[7:0] or URxData[15:0]. OddEven (bit 2) in the UTOP1 register determines whether this pin represents even or odd parity.
URxSOC	UTOPIA Receive Start of Cell	A23	A23	A23	O/Z	When active high, this pin indicates the first byte of valid cell data received. An external pulldown resistor is required for this pin.
URxCLAV	UTOPIA Receive Cell Available	A24	A24	A24	O/Z	Indicates FIFO empty or Cell Buffer. Available, depending upon HandShake (bit 1) in the SYSBUS register (0xE01). An external pulldown resistor is required for this pin.

Table 1-5. Hardware Signal Definition, Programmable Input/Output Interface (1 of 2)

Pin Label	Signal Name	CX2836x Pin#	I/O	Definition
OutPort1[0] / LStatOut[0] OutPort1[1] / LStatOut[1] OutPort1[2] / LStatOut[2] OutPort1[3] / LStatOut[3] OutPort1[4] / LStatOut[4] OutPort1[5] / LStatOut[5] OutPort1[6] / LStatOut[6] OutPort1[7] / LStatOut[7] OutPort1[8] / LStatOut[8] OutPort1[9] / LStatOut[9] OutPort1[10] / LStatOut[10] OutPort1[11] / LStatOut[11]	General Purpose Output Port 1 Line Status Output	M2 L1 K1 J1 H1 G1 F1 E1 D1 C1 B1 A3	O/Z	These pins can be individually configured as general purpose output or status output pins. Refer to Port Mode Control registers, PORTn. As a general purpose output port, it reflects the corresponding bit setting in the OUTPORT1 register. As a Line status Output, it reflects one of the signals below depending upon the value of Out1Mode[1:0] field. <u>LstatOut</u> <u>Out1Mode[1:0]</u> LOCD (or PLCP LOF) 00 OOF from framer 01 Yellow Alarm from framer 10 OUTPORT1 register 11
OutPort2[0] / LCS*[0] OutPort2[1] / LCS*[1] OutPort2[2] / LCS*[2] OutPort2[3] / LCS*[3] OutPort2[4] / LCS*[4] OutPort2[5] / LCS*[5] OutPort2[6] / LCS*[6] OutPort2[7] / LCS*[7] OutPort2[8] / LCS*[8] OutPort2[9] / LCS*[9] OutPort2[10] / LCS*[10] OutPort2[11] / LCS*[11]	General Purpose Output Port 2 Line External Framer Chip Select	AD1 AC1 AB1 AA1 AD2 AC7 AF3 AE3 AD26 AC24 AB24 AA24	O/Z	These pins can be individually configured as general purpose output or chip select output pins. Refer to Port Mode Control registers, PORTn. As general purpose output pins, they reflect the corresponding bit values in the OUTPORT 2 register. As chip select outputs, an LCS pin is activated if the processor accesses an address within its range. The polarity of these signals is set by CsPol (bit 2) in the IOMODE registers.
InPort1[0] / LIntR[0]/RxSync[0] InPort1[1] / LIntR[1]/RxSync[1] InPort1[2] / LIntR[2]/RxSync[2] InPort1[3] / LIntR[3]/RxSync[3] InPort1[4] / LIntR[4]/RxSync[4] InPort1[5] / LIntR[5]/RxSync[5] InPort1[6] / LIntR[6]/RxSync[6] InPort1[7] / LIntR[7]/RxSync[7] InPort1[8] / LIntR[8]/RxSync[8] InPort1[9] / LIntR[9]/RxSync[9] InPort1[10] / LintR[10]/RxSync[10] InPort1[11] / LIntR[11]/ RxSync[11]	General Purpose Input Port 1 Interrupt Request Framer RxSync Output	N23 M23 L23 K23 J23 H23 G23 F23 E23 L24 K24 J24	I^{P}/O	The value on these 12 general purpose input pins can be read via registers IN1L and IN1H. These inputs can also be individually configured as interrupt inputs; refer to the PORTINTn register description. Internally pulled up. If configured as output pins, the corresponding RxSync from the framer block is available on these pins.

Table 1-5. Hardware Signal Definition, Programmable Input/Output Interface (2 of 2)

Pin Label	Signal Name	CX2836x Pin#	I/O	Definition
InPort2[0] / TxSync[0] InPort2[1] / TxSync[1] InPort2[2] / TxSync[2] InPort2[3] / TxSync[3] InPort2[4] / TxSync[4] InPort2[5] / TxSync[5] InPort2[6] / TxSync[6] InPort2[7] / TxSync[7] InPort2[8] / TxSync[8] InPort2[9] / TxSync[9] InPort2[10] / TxSync[10] InPort2[11] / TxSync[11]	General Purpose Input Port 2 Framer TxSync Output	AC2 AB2 AB23 AA23 P26 N26 M25 P25 N25 A8 A9 A10	I^{P}/O	These pins can be individually configured as general purpose inputs or framer TxSync outputs. See registers IN2CL and IN2CH. As input pins, InPort2[11:0] can be read via registers IN2L and IN2H. Internally pulled up. If configured as output pins, the corresponding TxSync from the framer block is available on these pins.

Table 1-6. Hardware Signal Definition, Power, and Ground (1 of 3)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
VGG	ESD Rail Voltage supply	R23	R23	R23	I	VGG must be connected to +5 V if 5 V tolerance on input pins is desired. If 5 V tolerance is not needed, connect this pin to 3.3 V.
VDDC	Core Supply voltage	AB9, AB18, E9, E18, J5, J22, V5, V22	AB9, AB18, E9, E18, J5, J22, V5, V22	AB9, AB18, E9, E18, J5, J22, V5, V22	I	Pins are provided for core supply power of 1.8 V.
VDDO	Output drivers supply voltage	AB7, AB11, AB13, AB14, AB16, AB20, D2, E7, E11, E13, E14, E16, E20, G5, G22, L5, L22, N5, N22, P5, P22, T5, T22, Y5, Y22	AB7, AB11, AB13, AB14, AB16, AB20, D2, E7, E11, E13, E14, E16, E20, G5, G22, L5, L22, N5, N22, P5, P22, T5, T22, Y5, Y22	AB7, AB11, AB13, AB14, AB16, AB20, D2, E7, E11, E13, E14, E16, E20, G5, G22, L5, L22, N5, N22, P5, P22, T5, T22, Y5, Y22	I	Pins are provided for I/O supply power of 3.3 V.

Table 1-6. Hardware Signal Definition, Power, and Ground (2 of 3)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
VSS	GND	A1, A2, A26, AA5, AA22, AB5, AB6, AB8, AB10, AB12, AB15, AB17, AB19, AB21, AB22, AC4, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26, B2, B25, B26, C3, C24, D4, D23, E5, E6, E8, E10, E12, E15, E17, E19, E21, E22, F5, F22, H5, H22, K5, K22, L11, L12, L13, L14, L15, L16, M5, M11–M16, M22, N11–N16, P11-P16, R5, R11-16, R22, T11–T16, U5, U22, W5, W22	A1, A2, A26, AA5, AA22, AB5, AB6, AB8, AB10, AB12, AB15, AB17, AB19, AB21, AB22, AC4, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26, B2, B25, B26, C3, C24, D4, D23, E5, E6, E8, E10, E12, E15, E17, E19, E21, E22, F5, F22, H5, H22, K5, K22, L11, L12, L13, L14, L15, L16, M5, M11–M16, M22, N11–N16, P11-P16, R5, R11-16, R22, T11–T16, U5, U22, W5, W22	A1, A2, A26, AA5, AA22, AB5, AB6, AB8, AB10, AB12, AB15, AB17, AB19, AB21, AB22, AC4, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26, B2, B25, B26, C3, C24, D4, D23, E5, E6, E8, E10, E12, E15, E17, E19, E21, E22, F5, F22, H5, H22, K5, K22, L11, L12, L13, L14, L15, L16, M5, M11–M16, M22, N11–N16, P11-P16, R5, R11-16, R22, T11–T16, U5, U22, W5, W22	I	Pins are provided for I/O ground.

Table 1-6. Hardware Signal Definition, Power, and Ground (3 of 3)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
VSS (Continued)	GND (Continued)	—	M24, P23, P24, R25, R26, T23, T24, U25, U26, V23, V24, W23, W25, W26, AA25, AA26, AC13, AC14, AC18, AC20, AD11, AD13, AD17, AD19, AE10, AE12, AE16, AE18, AE20, AE22, AE26, AF9, AF11, AF15, AF17, AF22	A14, A16, B13, B15, M24, P23, P24, R25, R26, T23, T24, U25, U26, V23, V24, W23, W25, W26, AA25, AA26, AC6, AC11, AC12, AC13, AC14, AC18, AC20, AD9, AD11, AD13, AD17, AD19, AE6, AE8, AE10, AE12, AE16, AE18, AE20, AE22, AE26, AF5, AF7, AF9, AF11, AF15, AF17, AF22	I	Pins are provided for I/O ground.

Table 1-7. Hardware Signal Definition, Test, and Control (1 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
TRST*	JTAG Test Reset	A25	A25	A25	I	When this pin is asserted, the internal boundary-scan logic is reset. This pin is internally pulled high.
TCK	JTAG Test Clock	A20	A20	A20	I	Samples the value of TMS and TDI on its rising edge in order to control the boundary scan operations (input clock).
TMS	JTAG Test Mode Select	A22	A22	A22	I	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin is internally pulled high.
TDI	JTAG Test Data Input	A21	A21	A21	I	Controls the boundary-scan Test Access Port (TAP) controller operation. This pin is internally pulled high.
TDO	JTAG Test Data Output	A19	A19	A19	I	Serial test data output.
TESTMOD[2] TESTMOD[1] TESTMOD[0]	Test mode control	Y4 V4 T4	Y4 V4 T4	Y4 V4 T4	I	Activates test modes. Factory use only. These pin must be connected to ground for normal operation.
OutDis	Output Disable Control	U23	U23	U23	I	When asserted high, all output pins are put into high impedance, three-state mode.
NC, NB	Spare	AC8, AD7, AE4, AE5, AE23, AF2, AF23, AF24	AC8, AD7, AE4, AE5, AE23, AF2, AF23, AF24	AC8, AD7, AE4, AE5, AE23, AF2, AF23, AF24	—	Not connected, not bonded.

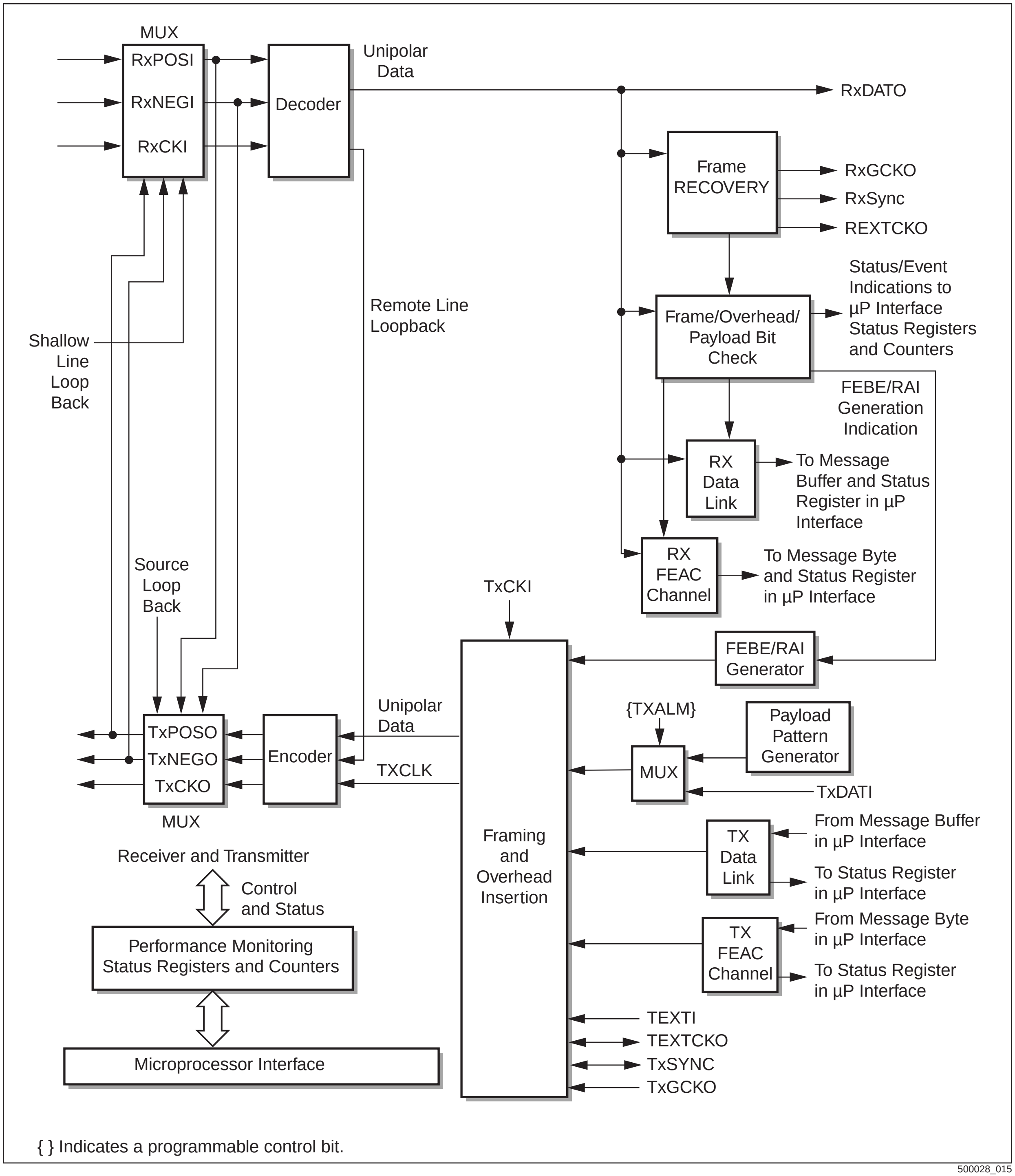
Table 1-7. Hardware Signal Definition, Test, and Control (2 of 2)

Pin Label	Signal Name	CX28365 Pin#	CX28366 Pin#	CX28364 Pin#	I/O	Definition
DNC	Do not connect.	C2	C2, N24, R24, T25, T26, U24, V25, V26, W24, Y23, Y24, Y25, Y26, AB25, AB26, AC5, AC15, AC16, AC17, AC19, AC21, AC22, AC25, AC26, AD5, AD10, AD12, AD14, AD15, AD16, AD18, AD20, AD21, AD22, AD23, AD25, AE9, AE11, AE13, AE14, AE15, AE17, AE19, AE21, AE24, AF21, AF8, AF10, AF12, AF13, AF14, AF16, AF18, AF19, AF20	A11, A12, A13, A15, A17, B10, B11, B12, B14, C2, C15, N24, R24, T25, T26, U24, V25, V26, W24, Y23, Y24, Y25, Y26, AB25, AB26, AC5, AC9, AC10, AC15, AC16, AC17, AC19, AC21, AC22, AC25, AC26, AD4, AD5, AD6, AD8, AD10, AD12, AD14, AD15, AD16, AD18, AD20, AD21, AD22, AD23, AD25, AE7, AE9, AE11, AE13, AE14, AE15, AE17, AE19, AE21, AE24, AF21, AF4	—	Internally connected. Do not connect.

2.0 Functional Description

This chapter describes the primary functions of the CX2836x, including the T3/E3 framer, ATM cell processor, the UTOPIA interface, and the microprocessor interface. Figure 2-1 is a functional block diagram for a single framer.

Figure 2-1. Framer Functional Block Diagram



2.1 T3/E3 Framer

The following describes the transmitter and receiver operation for a single framer. All features are the same for all the ports in the device.

2.1.1 Transmitter Operation

2.1.1.1 Line Signals

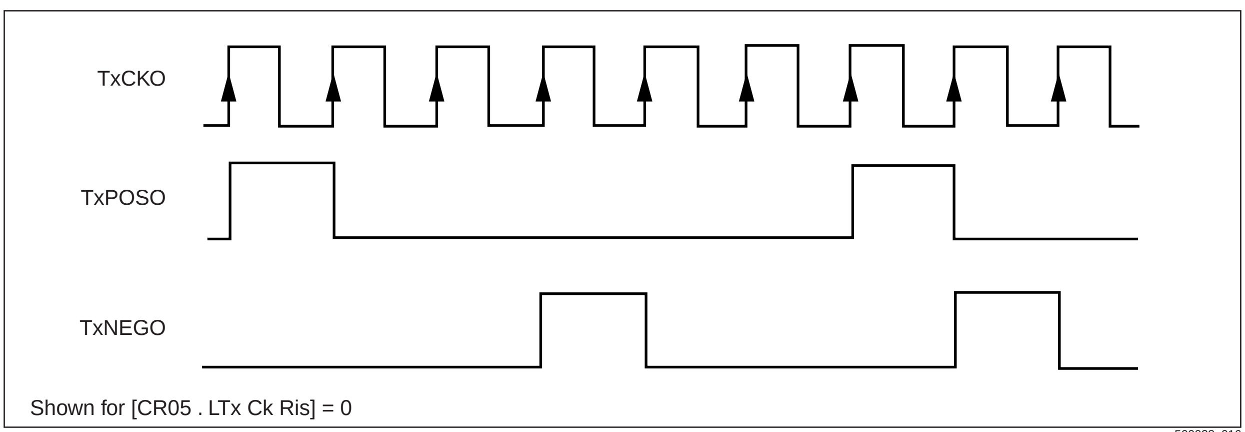
The transmit line side interface consists of three output pins: TxPOSO/TxNRZ, TxNEGO, TxCKO.

When bipolar mode is enabled, HDB3/B3ZS encoding is performed over all transmitted data. In this mode, encoded data is transmitted on TxPOSO (transmit positive polarity data) and TxNEGO (transmit negative polarity data). When AMI mode is enabled, data is transmitted without HDB3/B3ZS coding on TxPOSO and TxNEGO.

When NRZ mode is enabled, TxPOSO/TXNRZ transmits NRZ data, and TxNEGO is unused.

TxCKO is the clock reference output for TxPOSO/TxNRZ and TxNEGO output pins. Data outputs are a full-clock period wide and can change on positive or negative transitions of TxCKO signal. Figure 2-2 illustrates TxPOSO and TxNEGO changing on the rising edge of TxCKO.

Figure 2-2. Transmitter Line Outputs

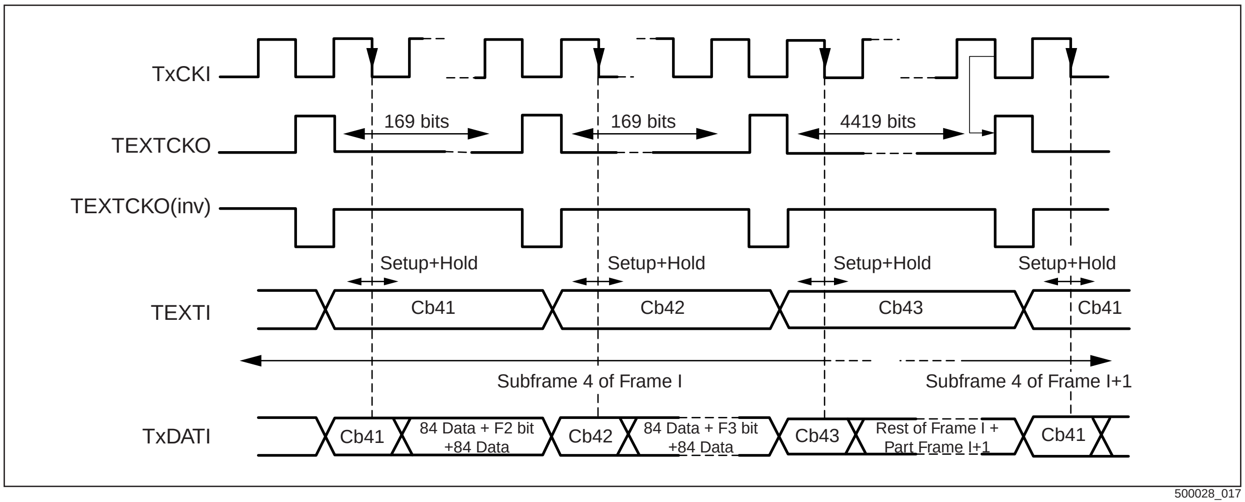


2.1.1.2 System Signals

The transmit system side interface for each framer consists of TxCKI, TxDATI, TxGCKO, TxSYNC, TEXTI, and TEXTCKO signals. Each of these pins are described in Section 1.2.1.

Figure 2-3 illustrates insertion of FEBE bits through the TEXTI pin in DS3 C-bit parity mode. In this example, ExtFEBE/Cj-bit of Transmitter Overhead Insertion register is set to 1, and all others are set to 0. In addition to the TEXTI overhead input and the TxCKI clock input, the response of TEXTCKO clock output is shown for normal and inverted modes of operation. With these settings, the TEXTCKO clock provides a clock pulse for the three C-bits in subframe 4 (FEBE bits). The FEBE bits are inserted through the TEXTI pin and sampled by the next falling edge of TxCKI clock after the pulse on TEXTCKO. This indicates, to the system, that the framer expects a new FEBE bit. The data on TEXTI must satisfy setup and hold times around the falling edge of TxCKI clock when it is sampled. TxDATI serial data input is also shown. TEXTI and TxDATI have the same timing.

Figure 2-3. Tx System Side External Overhead Insertion (DS3 FEBE-only Example)



There are three modes for the pin TxSync[i]. The modes are controlled by the Feature2 control register (CR05i) bits TXSYOut (b3) and TXSYIn (b2).

1. **Reset (**TXSYOut = 0 and TXSYIn = 0)

When the chip is in a reset condition, TxSync[i] is in a high Z state.

2. **Input (**TXSYOut = 0 and TXSYIn = 1)

At reset, the framer is not synchronized and does not provide internal synchronization. TEXTCK and TXGAPCK are disabled (long gap) until TxSync[i] is asserted. At least one TxSync[i] signal is expected to start the internal framer synchronization. It is sampled with the falling edge of the input clock TxCKI.

When asserted synchronously with the internal framer timing, no resynchronization occurs. There is a transition from low to high between the last sampling edge of frame N and the first sampling edge of frame N+1.

When asserted asynchronously with the internal framer timing, resynchronization occurs within one frame time.

In all cases, the first bit of the new frame is asserted on TXDATI at the same time and is available on the first or next sampling edge of TXCKI. The framer maintains synchronization from the last asserted TxSync[i] signal.

3) **Output** (TXSYOut = 1 and TXSYIn = 0)

There are two modes for the TxSync[i] pin when used for an output signal. The modes are controlled by the Feature2 control register (CR05i) TxOvhMrk bit (b4). In the output modes, it is sampled with the rising edge of the input clock TxCKI.

TxOvhMrk = 0, TxSync[i] is used for frame start indication. A transition from low to high occurs between the last sampling edge of frame N and the first sampling edge of frame N+1.

TxOvhMrk = 1, TxSync[i] is used for overhead bit indication including justification control bits and stuff opportunity bits. TxSync[i] samples low at the corresponding overhead bit with the sampling edge of TXCKI and samples high during all payload bits.

If TxSync[i] is not used but selected via the INPORT2 Control registers, set the pin to the output mode, TXSYOut = 1 and TXSYIn = 0.

NOTE: The state TXSYOut = 1 and TXSYIn = 1 is not allowed.

Figure 2-4 illustrates the behavior of TxSYNC as a frame start synchronization output signal. Also, payload bits only are inserted.

Figure 2-4. DS3 System Transmit Timing (TxSYNC Indicates Frame Start)

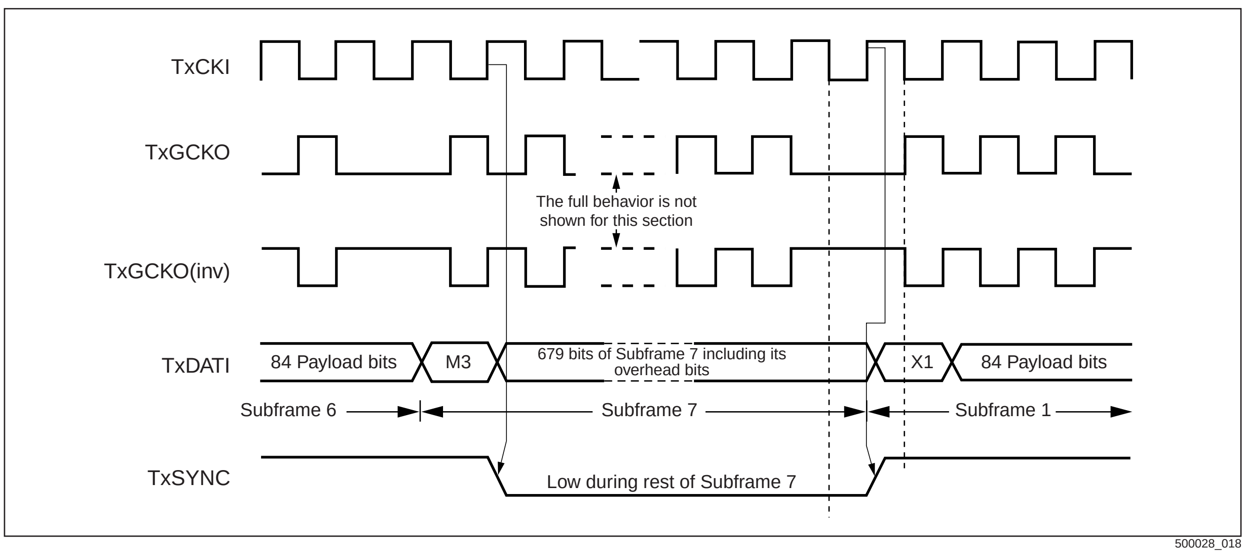


Figure 2-5 illustrates TxSYNC as an overhead indication output signal. Here TxSYNC is low during all overhead bits position and high during all payload data bit positions.

Figure 2-5. DS3 System Transmit Timing (TxSync Indicates Overhead Bits)

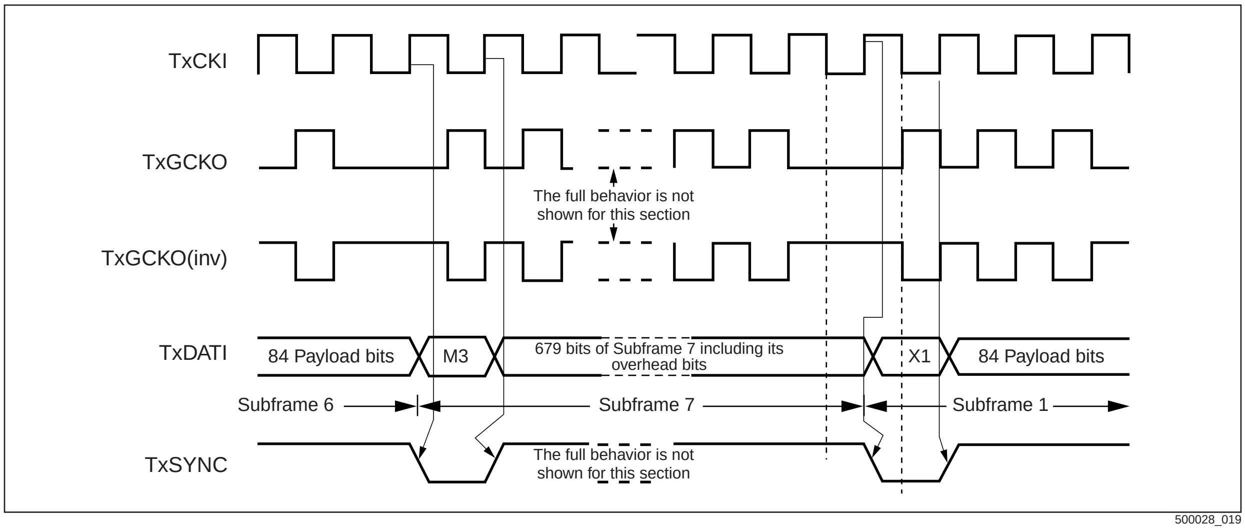
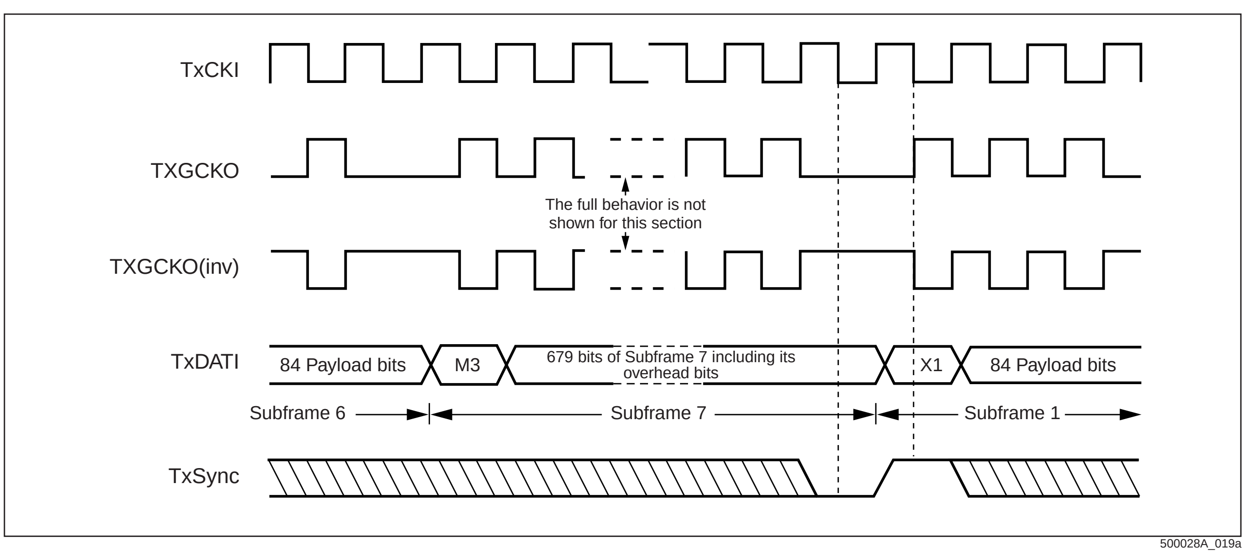


Figure 2-6 illustrates the TxSync[i] signal configured as a frame start synchronization input signal. The signal is sampled on the falling edge of TxCKI. The framer also expects the TxSync[i] signal to be low during the last bit of the previous frame before transitioning high during the first bit of the next frame.

The behavior of the TxGCKO signal is shown both in normal and inverted mode. Since none of the overheads are set to be inserted with the payload, TxGCKO is gapped during all overhead bits illustrated in Figures 2-4 through 2-6.

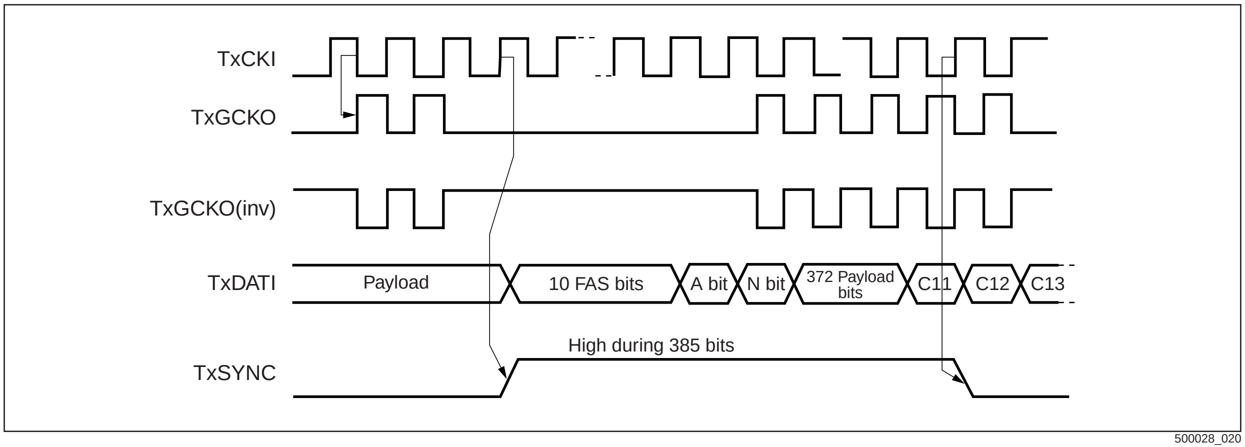
Figure 2-6. DS3 System Transmit Timing (TxSync[i] as Input Indicating Frame Start)



During E3-G.751 mode of operation, TxCKI pin is connected to a 34.368 MHz clock.

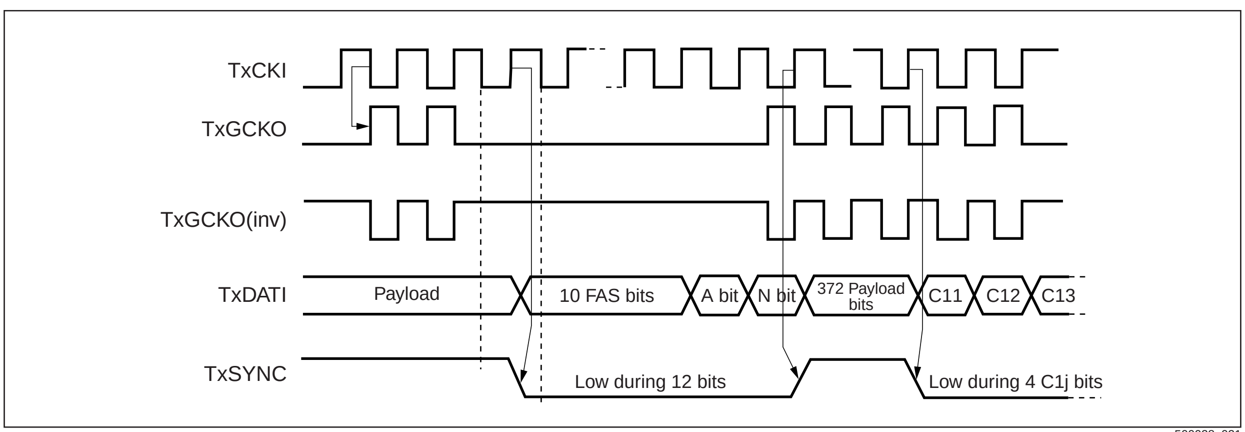
Figure 2-7 illustrates TxSYNC as a frame start synchronization indication and illustrates the TxGCKO clock behavior both in normal and in inverted mode. In this example, TxGCKO is gapped only during FAS, A, N-bits, and Stuff Opportunity bits, and supplies clock pulses during the payload and Justification Control bits (C_j1, C_j2, C_j3 where $_j$ = 1 to 4).

Figure 2-7. E3-G.751 System Transmit Timing (TxSYNC Indicates Frame Start)



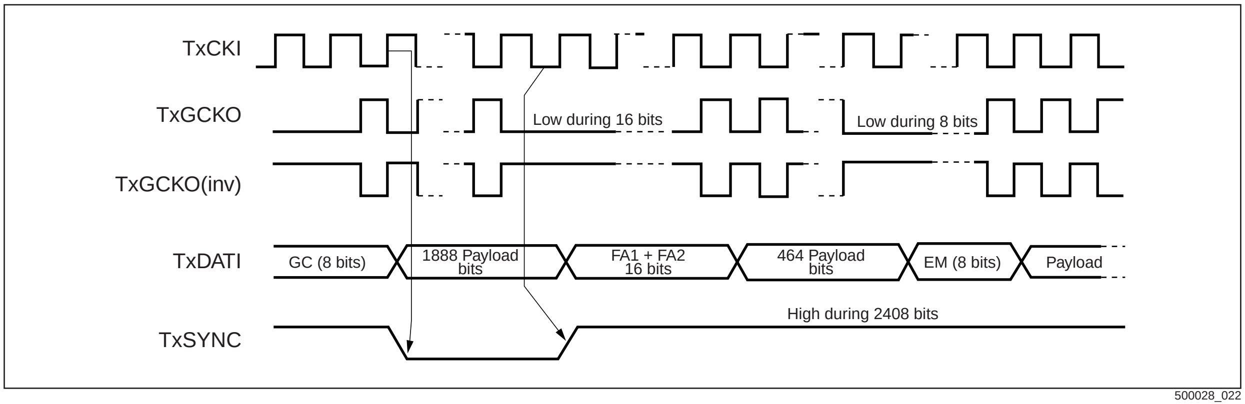
In Figure 2-8, TxSYNC is configured as an overhead indication signal and is low during all Opportunity bits and high during all data bits.

Figure 2-8. E3-G.751 System Transmit Timing (TxSYNC Indicates Overhead Bits)



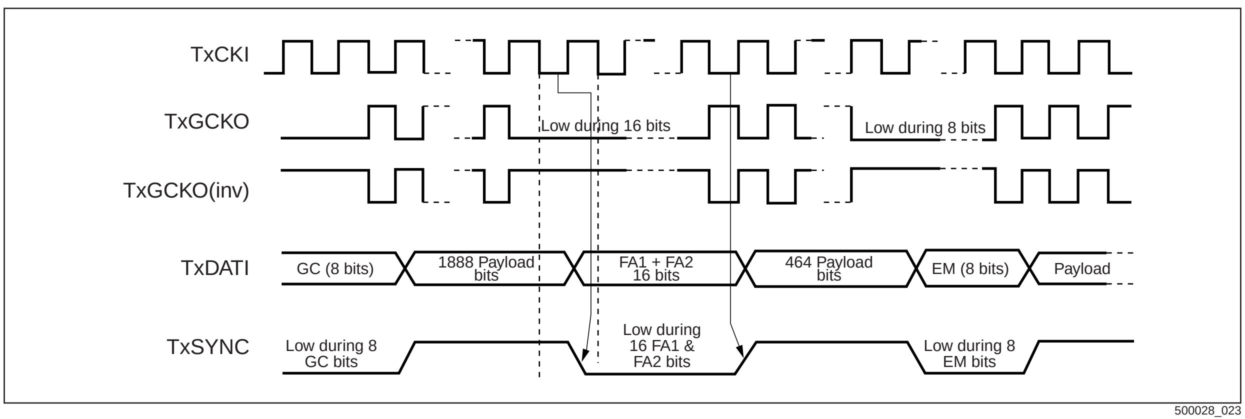
In the E3-G.832 mode, TxCKI pin is connected to a 34.368 MHz clock. In Figure 2-9, TxSYNC indicates frame start synchronization.

Figure 2-9. E3-G.832 System Transmit Timing (TxSYNC Indicates Frame Start)



In Figure 2-10, TxSYNC is low during all Opportunity bit positions (i.e., low during FA1, FA2, EM, TR, MA, NR, and GC bytes) and high during data bit positions regardless of the Opportunity bit source.

Figure 2-10. E3-G.832 System Transmit Timing (TxSYNC Indicates Overhead Bits)



2.1.1.3 Transmitter Overhead Bit Generation

The framer can use any of the following four techniques to insert framing and Opportunity bits:

1. Internal-Auto—Automatically generated by the internal circuitry, (e.g., automatic FEBE/REI).
2. Internal-Reg—Overhead bits are microprocessor-controlled.
3. External-Data—Overhead bits are supplied with the data stream.
4. External-Pin—Overhead bits are is input from an external pin (TEXTI) with the gapped clock (TEXTCKO).

The allocation of the Opportunity bits to one method is done for groups of overheads. The options vary for each one of the four main modes of operation. The Transmit Overhead Insertion 1 Control register and Transmit Overhead Insertion 2 Control register control the allocation. The register setting ability changes according to the framer mode of operation. Table 2-1 indicates the availability for the various Overhead bits in various modes.

Table 2-1. Overhead Sourcing Methods

Mode	Field	Technique			
		Internal-Auto	Internal-Reg	External-Data[(1)]	External-Pin
DS3	F-bits, M-bits (Frame)	•		•	•
	X-bits (RAI)		•	•	•
	P-bits (Parity)	•		•	•
	7 Stuff Opportunity bits[(2)]			•	•
	C-bits (Justification Control)[(2)]			•	•
	Cb11 (AIC)[(3)]	•		•	
	Cb13 (FEAC)[(3)]		•	•	•
	Cb3 (Path Parity)[(3)]	•		•	•
	Cb4 (FEBE)[(3)]	•		•	•
	Cb5 (DL)[(3)]	•	•	•	•
	Cb12, Cb2, Cb6–7[(3)]	•		•	•
E3-G.751	FAS (Frame)	•		•	•
	A-bit (RAI)	•	•	•	•
	N-bit (DL)	•	•	•	•
	C_j-bits (Justification Control)			•	•
	4 Stuff Opportunity bits			•	•
E3-G.832	FA1, FA2 (Frame)	•		•	•
	EM (BIP-8)	•		•	
	TR (Trail Trace)	•		•	•
	MA RDI	•	•	•	•
	MA REI	•		•	•
	MA PT		•	•	
	MA PD[(4)]		•	•	•
	MA MI[(5)]	•		•	•
	MA TM/SSM[(6)]		•	•	
	NR (DL)	•	•[(7)]	•	•
	GC (DL)	•	•[(7)]	•	•

GENERAL NOTE:
(1) Either all fields enter via data stream, or only Justification Control bits (in DS3 M13/M23 and E3-G.751), or Stuff Opportunity bits, or either justification control and stuff bits value or none.
(2) In M12/M23 mode.
(3) In C-bit Parity mode.
(4) In non-SSM mode.
(5) In SSM mode.
(6) In either SSM or non-SSM mode.
(7) Use only one overhead bit at a time to enable the LAPD datalink.

DS3 Mode

There are 56 frame Overhead bits in a DS3 M-frame structure. See Appendix B, for details.

The External-Data source option for the DS3 mode provides the ability to insert all frame Opportunity bits with the data stream. When the framer operates in C-bit parity mode, there is an option to either insert all the frame Opportunity bits with the data stream or none of them by setting bit ExtDat in the Transmit Overhead Insertion 1 Control register. When the framer operates in M13/M23 mode there are five options concerning the insertion of Opportunity bits with the data stream:

1. All Opportunity bits can be inserted with the data stream by setting ExtDat bit to 1.
2. Only C-bits (Justification Control bits) enter with the data stream and the 7 Stuff Opportunity bits are inserted via TEXTI by setting bit ExtDat to 0, ExtFEBE/Cj-bit to 0, and ExtStf to 1.
3. Only 7 Stuff Opportunity bits are inserted with the data stream while justification control bits are inserted from TEXTI by setting bit ExtDat to 0, ExtFEBE/Cj-bit to 1, and ExtStf to 0.
4. Both C-bits (Justification Control bits) and the 7 Stuff Opportunity bits are inserted with the data stream by setting bit ExtDat to 0, ExtFEBE/Cj-bit to 0, and ExtStf to 0.
5. None of the Opportunity bits are inserted with data (Justification Control and Stuff Opportunity bits enter through external pin, and other overload bits are internally generated) by setting ExtDat to 0, and ExtFEBE/Cj-bit to 1 and ExtStf to 1.

Table 2-2. Overhead Choice

Operation	Setting of External Data		
	ExtDat	ExtFEBE/Cj	ExtStf
1	1	0	0
2	0	0	1
3	0	1	0
4	0	0	0
5	0	1	1

When the Frame Overhead bits are not chosen to be inserted via the data stream, the following source options are provided: internally generated, taken from register, or entered through an external pin. For enabling sourcing options, the Frame Overhead bits are divided into groups where each group of overheads has its own sourcing options. Some groups and their source options are different for C-bit parity and M13/M23 mode of operation. The difference is in the C-bits, which are divided into more groups in C-bit parity mode.

C-Bit Parity and M13/M23 Modes of Operation

The following groups of overheads have the same options for both operational modes.

- Framing bits (F-bits and M-bits)—When the External-Data method is disabled, the three M-bits and the 28 F-bits can be either generated internally by the framer (when ExtFrmAl bit is 0) or inserted through TEXTI pin (when ExtFrmAl bit is 1).

- X-bits (RAI)—Can be either inserted through the TEXTI pin (controlled by bit ExtRAI in the Transmit Overhead Insertion 2 register) or can be generated by an internal register setting (controlled by TxAlm[1:0] bits). When TxAlm[1:0] is set to 01, bits X1 and X2 contain 0s regardless of other X-bits sourcing settings.
- P-bits (parity bits)—Can be either internally calculated or inserted from TEXTI pin (controlled by bit ExtP in the Transmit Overhead Insertion 2 register). When set to be calculated internally, the transmitter calculates the parity over 4704 payload bits of each M-frame (even parity calculation is used) and inserts the result into both P1 and P2 bits of the following M-frame.

The C-bits in M13/M23 modes are used as Justification Control bits and are all supplied from the same source. Their options are as follows:

- Either to be inserted with the data stream (with or without the rest of the Overhead bits) by setting ExtDat bit to 1 or ExtFEBE/Cj-bit to 0.
- To be inserted through the TEXTI external pin. This option is chosen by setting ExtDat bit to 0 and ExtFEBE/Cj-bit to 1.

C-Bit Parity Mode Only: Overhead Insertion

In the C-bit parity mode of operation, the C-bits are divided into groups with the following source options:

- AIC (Cb11)—Application Identification Channel. It is generated internally. The transmitter inserts 1 to the transmitted data at the C11 place to indicate that the line works with the C-bit parity application (a constant 1 at AIC-bit indicates C-bit parity application).
- FEAC (Cb13)—Far End Alarm Channel. When bit ExtFEAC/PD (Transmit Overhead Insertion 1 Control register) is set to 1, Cb13 value is inserted through the TEXTI input pin. When bit ExtFEAC/PD is set to 0, Cb13 is internally generated using the Transmit FEAC Channel Byte register and setting bit FEACSin (single or repetitive mode bit) at the Feature3 Control register.
- Path Parity (Cb3)—The three C-bits at subframe 3 can either be supplied to the transmitter circuit on TEXTI external input by setting bit ExtCP/TR in Transmit Overhead Insertion 1 Control register to 1, or internally generated by setting bit ExtCP/TR to 0. When internally generated, the transmitter calculates the parity over 4704 payload bits of each M-frame (even parity calculation is used) and inserts the result to Cb31, Cb32, and Cb33 bits of the next M-frame (they are all set to the same value as the P-bits when no error insertion occurs).
- FEBE (Cb4)—The three C-bits at subframe 4 (FEBE bits) can either be inserted through the TEXTI pin (when ExtFEBE/Cj-bit in the Transmit Overhead Insertion 1 Control register is set to 1), or can have an internal-automatic source (when ExtFEBE/Cj-bit is set to 0). The internal-auto sourcing of FEBE in DS3-C-bit parity mode is further described in Section 2.1.1.4.
- DL (Cb5)—The three C-bits in subframe 5 are assigned as a 28.2 Kb terminal-to-terminal path maintenance data link. Their values can be taken from the TEXTI input pin when bits DLMod[2] and DLMod[1] are set to 11. The bits can all be automatically set to 1 by setting bit DLMod[2] to 0 (DLMod[1] bit can be set to either 0/1), or they can be chosen internally by registers generated by setting DLMod[2] and DLMod[1] bits to 10. The last option uses an internal FIFO buffer and the HDLC formatting mechanism to implement LAPD data link channel on those bits. For details, see Section 2.1.1.6.
- Cb12, Cb2, and Cb6–7—Cb12 is an NR bit (network reserved bit). The C-bits in

the second, sixth, and seventh M-subframe are reserved bits—all together, they can either be generated internally or provided from an external pin. When bit DLMod[0] is set to 1, those bits are taken from the TEXTI pin. When this bit is set to 0, they are all internally generated and transmitted as 1.

E3–G.751 Mode

E3-G.751 frame structure has 24 frame Overhead bits, which are divided as follows:

- 10 frame alignment signal (FAS) bits
- Alarm indication to the remote digital multiplex equipment (A-bit) bit
- Bit reserved for national use (N-bit)
- 12 justification service bits (Cj-bits)

The External-Data source option for the E3-G.751 mode provides the following options of framing bits insertion with the data stream:

- All Overhead bits can be inserted with the data stream by setting bit ExtDat to 1.
- Only Cj-bits enter with the data stream and the 4 Stuff Opportunity bits are inserted via TEXTI by setting bit ExtDat to 0, bit ExtFEBE/Cj to 0, and ExtStf to 0. The rest of the Overhead bits (FAS, A, and N) source is set separately.
- Both Cj-bits and the 4 Stuff Opportunity bits are inserted with the data by setting ExtDat=0 and ExtFEBE/Cj = 0 and ExtStf = 0.
- None of the Overhead bits or stuff bits are inserted with data (they are either generated internally or enter through external pin) by setting bits ExtDat and ExtFEBE/Cj to 0 and 1 respectively, and ExtStf to 1.

When the frame Overhead bits are not chosen to be inserted via the data stream, the following source options are provided for each group of frame Overhead bits:

- FAS—Bits 1 to 10 of set 1 are used as the frame alignment signal. Those bits are generated automatically internally by the transmitter circuit and inserted at the beginning of each E3-G.751 frame transmission. The 10 FAS bits have the sequence 1111010000 (transmitted from left to right), or they can be inserted through the TEXTI pin by setting bit ExtFrmA1.
- A-bit—Bit 11 of set 1 is the alarm indication to the remote digital multiplex equipment bit (used to send RAI alarm signal). This bit can be automatically internally generated, controlled by a register or inserted through the TEXTI pin. Automatic RAI generation is enabled by setting bit AutoRAI in the Transmit Overhead Insertion 1 Control register to 1. In this mode, as long as a Loss of Signal (LOS) condition or loss of frame alignment (Out of Frame [OOF]) are detected at the RCV, the TRN automatically inserts 1 at the transmitted A-bit. When LOS and OOF conditions are not detected, the TRN sets the transmitted A-bit to 0 (no RAI alarm). When AutoRAI = 0, setting the ExtRAI bit in the Transmit Overhead Insertion 2 Control register to 1 causes A-bit insertion through the TEXTI pin. For as long as TxAlm[1] is set to 1, the A-bit contains 1 regardless of other A-bits sourcing settings.
- N-bit—Bit 12 of set 1 is reserved for national use. Its value can be taken from the TEXTI input pin when bits DLMod[2] and DLMod[1] in the Transmit Overhead Insertion 1 Control register are both set to 1. It can be automatically set to 1 by the framer when bit DLMod[2] is set to 0, or it can be chosen internally generated by registers when DLMod[2] and DLMod[1] are set to 10. The last option

implements a LAPD data link with HDLC formatting over the N-bit using an internal FIFO buffer. For more details about using the data link FIFO buffer, see Section 2.1.1.6.

- Cj-bits—The justification bits are provided either to the transmitter framer with the data stream, or by the TEXTI external overhead input pin (when ExtFEBE/Cj is set to 1) when the option of providing them with the data stream is disabled.

E3–G.832 Mode

E3-G.832 frame structure comprises seven octets of Opportunity bits divided into the following:

- FA1 and FA2 (2 octets)
- Error Monitoring byte (EM)
- Trail Trace byte (TR)
- Maintenance and Adaptation byte (MA)
- Network operator byte (NR)
- General purpose communication channel byte (GC)

In E3-G.832 mode, the framer provides two options for the insertion of the frame Opportunity bytes within the data stream: either all frame Overhead bits are inserted with the data stream (by setting bit ExtDat to 1), or none of the Overhead bits are inserted via the data stream (setting bit ExtDat to 0).

When the frame Overhead bits are not chosen to be inserted via the data stream, the following source options are provided for each group of frame Overhead bits:

- FA1 and FA2—The frame alignment bytes that have the value of FA1 = 11110110 (transmitted left to right), FA2 = 00101000 (transmitted left to right) are automatically inserted by the framer's transmitter circuit at the beginning of each frame, or inserted from the TEXTI pin by setting ExtFrm A1 bit.
- EM—Error monitoring, BIP-8 byte. When not all overheads are inserted via the data stream, this byte is generated automatically by the transmitter circuit. The transmitter calculates a BIP-8 code using even parity. The BIP-8 is calculated over all bits, including the Overhead bits, from the previous frame. The computed BIP-8 is placed in the EM byte of the current transmitted E3-G.832 frame.
- TR—The trail trace byte to be transmitted can be either supplied externally on the TEXTI pin (by setting ExtCP/TR bit in the Transmit Overhead Insertion 1 Control register to 1) or disabled and automatically transmitted as all 0s (by setting ExtCP/TR bit to 0).
- MA RDI—Bit 1 of the MA field is the remote defect indicator. This bit value can either be generated automatically, controlled by a register or inserted through the TEXTI pin, depending on AutoRAI, TxAlm, and ExtRAI bit settings. If AutoRAI = 1, automatic RDI is enabled. In this mode, for as long as Loss of Signal (LOS) or loss of frame alignment (Out of Frame [OOF]) conditions are detected at the receiver, the transmitter automatically inserts 1 at the transmitted RDI-bit. Otherwise, the RDI-bit is transmitted as 0. RDI insertion is also controlled by TxAlm[1] bit at the Mode Control register. Normally, the transmitter sends 0 as the RDI-bit. When AutoRAI = 0, setting the ExtRAI bit at the Transmit Overhead Insertion 2 Control register to 1 causes the RDI-bit insertion through TEXTI pin. For as long as TxAlm[1] is set to 1, RDI-bit contains 1, regardless of other RDI-bit sourcing settings.
- MA REI—Bit 2 of the MA field is the remote error indication. It can be either

generated internally or supplied on the TEXTI pin to the transmitter circuit. If bit ExtFEBE/Cj in Transmit Overhead Insertion 1 Control register is set to 1, the REI-bit is inserted to the transmitter via the TEXTI pin. If bit ExtFEBE/Cj is set to 0, REI is internally generated automatically. In the internal-automatic mode, the REI-bit is set by the transmitter as a reaction to an error detected in a received BIP-8 code (in EM field). In this mode, if the received BIP-8 code at the current frame does not equal the calculated BIP-8 code over the previously received frame, the transmitter inserts 1 at the REI-bit for one frame at the first opportunity. As long as no BIP-8 errors are detected at the received frame, the transmitter inserts 0 at the transmitted REI-bit.

- MA PT—(payload type) Bits 3 to 5 of the MA byte are the payload type field. The 3-bit payload type pattern to be transmitted is contained in bits FEBEC/PT[1:3] at the Feature1 Control register. Writing a new payload type to the register affects the next transmitted frame.
- MA PD/MI—Bits 6 and 7 of the MA byte are the payload- dependent/multiframe indicator bits. There are two modes of operation for these bits: SSM mode, and the normal mode. When bit SSMEn in Feature4 (I) Control register is set to 1, SSM mode is enabled. In this mode, the MA PD/MI bits act as multiframe indicator bits (MI). They can be supplied by either an external circuit on TEXTI bit input, or they can be automatically generated internally by setting of bit ExtFEAC/PD (when set to 0, it is automatically generated; when set to 1, it is supplied through the TEXTI pin). When multiframe indication bits are supplied automatically, a 2-bit rollover counter is implemented. The counter is incremented each frame and its value is transmitted on MI bits (The MI counter is reset to 00 when enabling automatic generation of MI bit in SSM mode). When bit SSMEn is set to 0, SSM mode is disabled and the PD/MI bits act as the payload- dependent bits. When SSM mode is not set, those bits can be either supplied by external circuitry on the TEXTI pin by setting bit ExtFEAC/PD bit in the Transmit Overhead Insertion 1 register to 1, or the value to be transmitted can be taken from bits MAPD[1:2] in register Feature4 (I) Control register by setting bits ExtFEAC/PD and SSMEn to 0.
- MA TM/SSM—Bit 8 of the MA byte is the timing marker/SSM bit. There are two modes of operation for these bits: SSM mode, and the normal mode that is controlled by the settings of bit SSMEn in Feature4 (I) Control register. If bit SSMEn is set to 1, SSM mode is enabled. Otherwise, SSM mode is disabled. In both SSM and normal mode, the bits to be transmitted are written to the register. When SSM mode is disabled, the TM value to be transmitted is taken from bit SSM[1]/TM in the Feature4 Control register. When SSM mode is enabled, the 4-bit SSM message to be transmitted is stored in bits SSM[1]/TM, SSM[2:4] in Feature4 Control register. In this mode, the bit of the SSM message to be transmitted is selected according to the value of MI transmitted bits (supplied through the TEXTI pin or automatically generated).

NOTE: There are eight options for setting NR and GC sources using the DLMod[2:0] bits setting at the Transmit Overhead Insertion 1 Control register in a E3-G.832 mode of operation. The framer is capable of implementing one LAPD data link using an internal FIFO buffer at a time. In E3-G.832 mode a LAPD data link can either be implemented on GC or NR, but not on both at the same time.

- NR (DL)—The network operator byte source is determined by bits DLMod[2], DLMod[1], and DLMod[0] at the Transmit Overhead Insertion 1 Control register. It can be supplied externally on TEXTI. It can be transmitted as all-1s (data link disabled). The framer is also capable of implementing LAPD data link using an internal FIFO buffer, as specified in Section 2.1.1.6.

- GC (DL)—The general purpose communication channel bytes source is determined by DLMod[2], DLMod[1], and DLMod[0] at the Transmit Overhead Insertion 1 Control register together with the NR byte. It can be supplied externally on the TEXTI pin or transmitted as all 1s (data link disabled). The framer is also capable of implementing an LAPD data link using an internal FIFO buffer, as specified in Section 2.1.1.6.

2.1.1.4 Alarm Signal Generation

Each framer is provided with an alarm signal generation mechanism. Some alarms can be either generated automatically as a reaction to receive conditions, or initiated by the user (set by bits, inserted via external interface or with the data stream). All alarm signals initiated by the user are implemented as an activate/deactivate mechanism in which the user is responsible for activating and deactivating the alarm signal generation bit. The alarms that can be generated are specified for each available mode of operation.

For all DS3/E3 modes of operation bits, TxAlm1 and TxAlm0 in the Mode (i) Control register are responsible for alarm generation.

During alarm generation and transmission, the system interface is not influenced, and thus, all clocks and signals remain the same.

Loss of Signal Generation

For all modes of operation, the transmit mechanism provides the user with a programmable option to transmit LOS to the line side by setting bit TxLOS at the Feature2 Control register. When bit TxLOS is set to 1, the transmit mechanism generates 0 on the line side data interface outputs (TxPOSO and TxNEGO are transmitted as 0)—regardless of inserted payload and Overhead bit settings.

DS3 Mode

In DS3 M13/M23 and C-bit parity modes, RAI, AIS, and IDLE alarm signals can be generated on the outgoing DS3 stream by setting the TxAlm1 and TxAlm0 bit pair in the Mode (i) Control register for each framer individually. Table 2-3 summarizes the alarms. In C-bit parity mode, a FEBE alarm is also generated. The various alarms are described in the following paragraphs.

Table 2-3. DS3 Mode Alarm Signal Setting

Bits		Type Alarm
TxAlm0	TxAlm1	
0	0	Normal
0	1	Yellow
1	0	IDLE
1	1	AIS

RAI (Yellow Alarm)

The Yellow alarm is contained in the X1 and X2 bits (by setting them to 0). The Yellow alarm is controlled by TxAlm[1:0] regardless of X bits source settings. Setting the TxAlm bit pair to 01 sends the Yellow alarm. X1 and X2 bits are sent as 0 as long as the TxAlm bit pair is set to 01. The start and termination of RAI occur in the next frame after setting the TxAlm[1:0] bits.

AIS

The DS3 AIS signal has a valid M-frame alignment channel, a valid M-subframe alignment channel and valid P-bits, all C-bits set to 0 regardless of DS3 framing mode (M13/M23 or C-bit parity), both X-bits set to 1, and the payload set to a 1010... pattern starting with 10 after each Overhead bit.

Generation and transmission of the AIS signal is enabled by setting the TxAlm[1:0] bit pair to 11. It continues as long TxAlm[1:0] bits are set to 11. When TxAlm[1:0] bit pair is set to 11, the transmit line output is replaced with the DS3 AIS pattern. The pattern is generated internally regardless of the inserted data and Overhead bits insertion method from the system side, which is ignored by the framer.

NOTE: When the transmitter starts generating the AIS alarm, it continues keeping the old M-frame's synchronization. The start and termination of AIS generation are frame-aligned (AIS transmission initiates with the beginning of the next frame after setting the TxAlm[1:0] bit pair to 11, and terminates at the beginning of the next frame after setting TxAlm[1:0] bit pair to other than 11).

IDLE

The DS3 IDLE signal has valid framing and parity. With both X-bits set to 1, the payload is set to a 1100... pattern, starting with 11 after each Overhead bit. The C-bits in M-subframe 3 are set to 0, and the remaining C-bits can individually be a 1 or a 0, and can vary with time.

The transmission of idle code is enabled by setting the TxAlm[1:0] bit pair to 10 for each framer individually, and continues as long as those bits are set to 10. The start and termination of IDLE generation are frame-aligned (IDLE transmission initiates with the beginning of the next frame after setting the TxAlm[1:0] bit pair to 10, and terminates at the beginning of the next frame after setting the TxAlm[1:0] bit pair to other than 10).

In both DS3 framing modes (M13/M23 or C-bit parity), when IDLE code generation is enabled, the framer's transmitter line output is replaced with the DS3 IDLE pattern. It is internally generated regardless of the inserted data. The C bits are handled as follows: the C bits in M-subframe 3 are set to 0 and the remaining C bits are set according to their method of generation setting (from Internal-Auto, from Internal-Reg, from External-data, or from External-Pin) that are set for each mode, described in Section 2.1.1.3. The remaining Overhead bits are generated according to IDLE code specifications. When the transmitter starts generating the IDLE alarm, the transmitter keeps the previous M-frame's synchronization.

Handling of the C-bits in IDLE code generation is such to allow full use of the remaining C-bits, e.g., use terminal data link and transmit FEAC channel in C-bit parity mode during transmission of IDLE code.

FEBE

The FEBE alarm in DS3 is defined for C-bit parity application only. The three C bits in M-subframe 4 are used as FEBE bits.

In C-bit parity mode, when the ExtFEBE/Cj-bit in the Transmit Overhead Insertion 1 Control register is set to 0, the FEBE bits are not expected on the TEXTI input pin. FEBE alarms are automatically generated in the transmitter when the receiver detects either a frame bit error (F or M-bit error) or a path parity error in an M-frame. The 3-bit FEBE pattern that is transmitted is contained in the FEBE Pattern Bit Field (FEBEC/PT[1:3]) of the Feature1 Control register of each framer respectively. When no alarm condition is present, the FEBE channel contains all 1s. To prevent disabling proper FEBE operation during the Internal-Auto method of FEBE, the FEBE field should be written to any combination other than 111.

NOTE: FEBE transmission is performed at the first opportunity after framing error or CP error detection. Automatic FEBE transmission also remains operational (if set) during receiver OOF, LOS, AIS, or IDLE conditions. When FEBE bits are inserted from an external pin or with data, the automatic FEBE insertion is disabled and Pattern Bit Field settings have no meaning—FEBE bits are inserted externally.

E3-G.751 Mode

When E3-G.751 mode is set, two alarms can be generated: RAI (Yellow Alarm) and AIS according to the G.751 standard.

RAI (Yellow Alarm)

Bit 11 set 1 of E3-G.751 frame structure is the A-bit and used to transmit the remote alarm indication (RAI). RAI alarm is defined as transmitting 1 on A-bit.

Each framer has an option to insert the A-bit:

- With payload (when the method of overhead insertion is all with the data stream)
- From TEXTI pin
- Automatically generate it
- Force RAI alarm sending by a control register

If automatic RAI is enabled (by setting AutoRAI in Transmit Overhead Insertion 1 Control register to 1), as long as LOS condition or OOF are detected at the receiver, the transmitter automatically inserts 1 at the transmitted A-bit (starting and stopping at first opportunity). When LOS and OOF conditions are no longer detected, the transmitter sets the transmitted A-bit to 0 (no RAI alarm). In the automatic RAI mode the transmitter side sends automatic RAI as long as OOFAlm or LOSAlm bits at the Maintenance Status register are set. Detection of LOS and OOF are specified in Section 2.1.2.4.

Forcing a RAI alarm can also be done by setting TxAlm[1] to 1. As long as TxAlm[1] is set to 1, A-bit contains 1, regardless of other A-bits sourcing settings.

AIS

E3 AIS is defined as unframed all 1s.

In E3 mode, transmission of AIS is enabled by setting TxAlm0 high. When AIS is enabled, the framer ignores the inserted data and Overhead bit settings and transmits an all-1s code as long as TxAlm0 bit is set to 1. Start of AIS transmission and termination in E3 is immediate with the setting of TxAlm0.

E3-G.832 Mode

In E3-G.832 mode, three alarms are generated: Remote Defect Indicator (RDI), Remote Error Indicator (REI), and Alarm Indication Signal (AIS).

RDI

Bit 1 of MA field at E3-G.832 34.368 Mbps frame structure is used to transmit RDI.

Transmission of RDI in E3-G.832 mode is similar to RAI in E3-G.751 mode. Each framer has an option to insert the RDI bit:

- With payload (when the method of overhead insertion is all with data)
- From TEXTI pin
- Automatically generate it
- Force RDI alarm sending by a control register

If automatic RDI is enabled (by setting bit AutoRAI in Transmit Overhead Insertion 1 Control register to 1), as long as LOS or OOF conditions are detected at the receiver, the transmitter automatically inserts 1 at the transmitted RDI bit. When LOS and OOF conditions are no longer detected, the transmitter sets the transmitted RDI bit to 0 (no RDI alarm). In the automatic RDI mode, the transmitter side sends automatic RDI as long as OOFAlm or LOSAlm bits at the Maintenance Status register are set.

Forcing a RDI alarm can also be done by setting TxAlm[1] to 1. As long as TxAlm[1] is set to 1, RDI bit contains 1, regardless of other RDI bit source settings.

NOTE: Automatic RDI transmission does not react to TR mismatch because the framer does not check TR mismatches. When the method of overhead insertion is all with data, setting AutoRAI or ExtRAI has no influence on the transmitted RDI-bit.

REI

REI is transmitted in bit 2 of the MA octet at the E3-G.832 34.386 Kb frame structure.

For each framer this bit can be either externally supplied (with the data stream or from an external pin) or internally generated automatically.

If the REI bit is selected to be generated internally, the transmitter sets this bit to 1 (generate REI signal) if one or more errors are detected by BIP-8 code received in the EM field. The REI bit is otherwise transmitted as 0 (no BIP-8 errors). During receiver LOS or AIS, automatic REI remains active. During receiver OOF condition, REI is transmitted as 0 in this mode.

AIS

The ability to transmit an all-1s AIS code is also supplied for the E3-G.832 mode (similar to the E3-G.751 mode).

In E3-G.832 mode, transmission of AIS (unframed all 1s) is enabled by setting TxAlm0 high. When AIS is enabled, the framer ignores the inserted data and Overhead bit settings and transmits an all 1s code, as long as TxAlm0 bit is set to 1. Start of AIS transmission and termination in E3-G.832 is immediate with the setting of TxAlm0.

2.1.1.5 Terminal Data Link Transmission

A terminal data link channel can be implemented over the 3 C-bits in subframe 5 in DS3, C-bit parity mode, over the N-bit in E3-G.751 mode, and over GC byte or the NR byte in E3-G.832 mode of operation (either GC or NR not both).

The transmitted data link bits for each mode of operation can be supplied to the transmitter circuit externally via the data stream or on TEXTI (external overhead input pin). They can be processed internally using an internal FIFO buffer, which is accessed via a microprocessor-controlled interface. When the data link is disabled and its bits are not supplied externally, the transmitter circuit automatically inserts a default value to the transmitted data link bits: i.e., in DS3 C-bit parity mode, the 3 C-bits in subframe 5 are transmitted as 1; in E3-G.751 mode, N-bit is transmitted as 1; and in E3-G.832 when the data link is disabled on NR or GC (or both), those bytes are transmitted as 1.

The following sections describe the transmit side terminal data link implementation using an internal FIFO buffer. Setting bits DLMod[2:0] in the Transmit Overhead Insertion 1 Control register Feature Control registers, can enable this mode for each rate.

For this mode of operation, the framer is controlled internally by a FIFO buffer and LAPD/HDLC formatting circuitry to implement a LAPD/HDLC terminal data link transmission according to ITU-T Q.921 and ISO/IEC 3309 standards.

HDLC/LAPD Formatting Circuitry

The HDLC/LAPD formatting circuitry includes the following:

- Automatic generation of FLAG sequences (01111110) when no message is being transmitted and between messages
- Zero insertion mechanism for transparency (a 0 bit is inserted after all sequences of five continuous 1 bits in a message between two FLAGs including the FCS to differ data from FLAG transmission)
- Automatic generation of abort sequence (a sequence of 16 continuous 1 bits)

The formatting circuitry has the capability of calculating the 16-bit Frame Check Sequence (FCS) and transmitting it at the end of the message. Transmitting of FCS is software-selectable by the settings of TxFCSEn in the Transmit Data Link Control register.

FIFO Buffer Control Circuitry

The transmit data link side (TDL) of each framer includes a 128-byte FIFO buffer that is additional to a 128-byte receiver-side data link FIFO buffer (RDL). The FIFO buffer is filled by the microprocessor with the data bytes to be transmitted for each message, and also provides interrupts and status bits to indicate its condition.

Writing to the FIFO Buffer

The FIFO buffer is written using the microprocessor interface. Writing a byte each time to the Transmit Data Link Message Byte register (TxDLMsg [7:0] byte) fills the FIFO buffer with a new message. The writing of the message byte adds it to the FIFO buffer.

The Transmit Data Link Message Byte register has two addresses. The low address is used to write all message bytes except the last byte; the high address is used to write the last byte of the message. The writing to the high address marks the written byte as the end of message byte (EOM). The next byte written to the FIFO buffer belongs to a new message.

TDL FIFO Buffer Related Interrupts

All TDL FIFO interrupts are maskable individually. Settings in the Transmit Data Link Control register control the enabling and disabling of the interrupts.

The TDL FIFO provides the following three interrupts:

1. TDL FIFO Near-Empty—(interrupt enabled by setting the TxNEIE bit to 1)
   - Turned on when the number of data bytes that remains to be transmitted in the FIFO buffer becomes equal to or falls below the programmable Near-Empty threshold level and the Near-Empty indication is not set.
   - Turned off when the number of data bytes that remained to be transmitted in the FIFO buffer becomes higher than the programmable Near-Empty threshold level.
   - The range of Near-Empty threshold settings is 0 to 126, and is set in the TxNEThr[6:0] bit at the Transmit Data Link Threshold Control register. Setting Near-Empty threshold to NE = 0 to 126, means that Near-Empty event is declared when the number of data bytes remaining in the FIFO buffer is equal or less than NE.
2. TDL FIFO Underrun—(interrupt enabled by setting the TxURIE bit to 1)
   - Turned on when the FIFO buffer is empty, if the last message byte that was transmitted did not indicate an end of message byte, and the inner HDLC circuitry requests the FIFO buffer for another byte to transmit.
   - Turned off when the Transmit Data Link FEAC Status register is read.
3. TDL Message Transmitted —(interrupt enabled by setting the TxMsgIE bit to 1)
   - Turned on when the last bit of the closing FLAG of a message is transmitted.
   - Turned off when the TxMsg status bit at the Transmit Data Link FEAC Status register is read.

TDL FIFO Related Status Bits

The TDL FIFO status indications are available at the Transmit Data Link FEAC Status register to be read by the microprocessor. They are as follows:

- TDL FIFO Near-Empty—(set and cleared with the interrupt) (indicated by the TxNE bit)
- TDL FIFO Empty—Indicates that the FIFO buffer is empty and has no message bytes written to it (indicated by the TxEmpty bit).
- TDL FIFO Underrun—(set and cleared with interrupt) (indicated by the TxUR bit)
- TDL Message Transmitted—(set and cleared with interrupt). Indicates that a full message was transmitted including its closing FLAG (indicated by the TxMsg bit).
- TDL FIFO Full—An indication bit that is set and stays set as long as the FIFO buffer is full—128 bytes are stored inside the FIFO buffer. The FIFO Full status can be used in polling mode to check if the FIFO buffer is full and there is no point in writing to it (indicated by the TxFull bit).

Initial Setup of Transmit Data Link

The TDL is disabled on reset, with no interrupts active. Bits DLMod [2:0] in the Transmit Overhead Insertion 1 Control register control TDL enabling for each mode.

Set the desired interrupt settings for the Near-Empty FIFO threshold and the TDL-related options to the desired values through the Transmit Data Link and the Transmit Data Link Threshold Control registers. The insertion of the FCS is software-selectable by setting the TxFCSEn field of the Transmit Data Link Control register.

When only the Data Link is disabled, the FIFO buffer is cleared, and the Near-Empty and Empty status bits are read. If the Near-Empty interrupt is enabled, a Near-Empty interrupt is generated. Before disabling the Data Link, the user should mask its interrupts. If the channel is enabled when disabling the Data Link a repetitive 1s signal is sent. While the Data Link is disabled, the FIFO buffer can still be written.

When both the Data Link and the channel are enabled, if the FIFO buffer is not reset and is not empty, a new message starts after sending two FLAG sequences. If the FIFO buffer is empty, FLAG sequences are automatically transmitted until a new message byte is written to the FIFO buffer.

When the entire channel is enabled after reset or disabled (while data link is enabled), the FIFO buffer is cleared, the Near-Empty and Empty status bits are cleared, and if the Near-Empty interrupt is enabled, a Near-Empty interrupt is generated.

When the whole channel is disabled, the following occurs:

- Data Link activities are terminated.
- Data link control settings at the Transmit Data Link and the Transmit Data Link Threshold Control registers are not affected (interrupt enables, Near-Empty threshold, FCS transmission, etc.).
- The channel’s old status at the Transmit Data Link FEAC Status register is maintained (status bits maintain their old values and so do interrupts if not disabled earlier).
- The FIFO buffer is not emptied.

Sending Message Using the FIFO—Normal Operation

In normal operation, when the TDL FIFO buffer is empty, the TDL circuitry generates IDLE flags. When the system has a message to transmit on the data link, it must write it to the FIFO buffer, one byte each time, by writing all data bytes (except the last message byte) to the low address of the Transmit Data Link Message Byte register (TxDLMsg[7:0]). The last byte of the message must be written to the high address of the Transmit Data Link Message Byte register indicating to the TDL circuit that it is the last byte of the message (EOM byte). After EOM, if the FIFO buffer is not FULL, another message can be written following the last EOM byte.

There is no limit to the length of each message, and the FIFO buffer can contain more than one message written to it at a time.

EMPTY and FULL status bits are provided to help the system evaluate the FIFO buffer’s content, and message transmission status, Near-Empty Threshold and Status, Transmitted Message Status indication and interrupt. With the help of these data bits, the system can TDL FIFO buffer accesses.

The internal logic terminates sending FLAG messages as soon as a new message byte is written to the FIFO buffer. The new message is sent until an EOM byte is encountered, which is followed by sending FCS (if enabled) and two FLAG sequences. After sending the closing FLAG of each message, an indication of transmitted message and an interrupt (if enabled) is provided. The next message immediately starts if the FIFO buffer is not empty. If the last transmitted octet was an EOM, FLAG sequences continue to be generated and transmitted.

From the system point of view, there are two TDL modes: Interrupt Driven mode and Polling mode.

Interrupt Driven Mode

Unmasking at least one FIFO-related interrupt (Near-Empty, Underrun, or Message Transmitted) enables interrupt driven mode.

Once an interrupt occurs, the microprocessor reads the Source Channel Status register to identify which framer is the interrupt's originator, then read the framer's Interrupt Source (i) Status register to identify which block raised the interrupt at the particular framer (TDL in this case—bit TxDLFEACItr is high). It then reads the Transmit Data Link FEAC Status register to identify the type of interrupt (Underrun, Near-Empty, or Message Transmitted).

There are many available settings and methods of handling interrupts. The proposed handling for normal operation is to read the Transmit Data Link FEAC Status register as the interrupt occurs. If the TDL Near-Empty indication is set, a new block of data bytes are written and transmitted (maximum 128 Near-Empty threshold bytes to safely fill the FIFO buffer). After servicing this interrupt, the system waits for another interrupt.

Polling Mode

Polling mode is effective when TDL function interrupts are masked. In Polling mode, the service routine is executed based on timers. Here, after writing a message byte or a message block of several bytes, the service routine waits for N milliseconds (based on the data link rate and the block size written) and polls or samples the Transmit Data Link FEAC Status register to check whether the FIFO buffer is empty or near empty, and if so, writes another block. In this mode, TDL status is read before writing to the FIFO buffer.

2.1.1.6 FIFO Special Events

End of Message Event

The system indicates End of Message (EOM) by writing the last byte of the message to the high address of the Transmit Data Link Message Byte register. When the TDL circuitry encounters the EOM indication set for a byte in the FIFO buffer, and after transmitting the last byte, it checks whether FCS sequence sending is set (bit TxFCSEn is set to 1 in Transmit Data Link Control register). If set, FCS bytes are sent, followed by at least two FLAG sequences before starting transition of the next message in the FIFO buffer (if there is one).

If the EOM byte is the last byte in the FIFO buffer, the TDL circuitry continues transmitting FLAG sequences (after transmitting the last byte and FCS, if enabled) until a new message byte is written to the FIFO buffer.

Near-Empty Event

The Near-Empty event is declared when the number of bytes remaining in the TDL FIFO buffer is less than or equal to the number programmed at the Near-Empty threshold, the value of which can be set to 0 to 126. The Near-Empty event results in an interrupt, if enabled. It is used to help the system control and use the FIFO buffer with minimum need to access the FIFO status bits.

FIFO Underrun

A FIFO underrun condition is caused when the internal transmit logic has emptied the FIFO buffer without encountering an end of message and the transmit logic request for the next byte to be transmitted. This causes an ABORT sequence (16 consecutive 1s) to be transmitted followed by at least two FLAG sequences. After an ABORT + two FLAG sequences, the transmit internal circuitry is ready to start transmitting a new message as soon as it is written to the FIFO buffer.

As soon as an underrun condition is declared internally, an interrupt is issued (if enabled) and the FIFO buffer prevents additional data bytes from being written to it. The underrun interrupt is cleared upon reading the Transmit Data Link FEAC Status register. Writing to the FIFO buffer is enabled again only after the interrupt is cleared.

The system checks the amount of data bytes that may have been written and lost between the time the first underrun interrupt occurred and the system reads the FIFO status register and senses a underrun condition.

Writing to FIFO when FIFO is Full

When the FIFO buffer is full, writing to the FIFO buffer by the microprocessor is ignored by the circuit, and no indication for ignoring written data during a FIFO Full condition is supplied. Neither data bytes and pointers of the FIFO buffer, nor the HDLC formatting and message providing mechanisms are affected by writing into the FIFO during FIFO full condition.

FLAG Transmission

The TDL machine generates and transmits a flag sequence (01111110) automatically in the following cases:

1. After enabling the data link, FLAG sequences are transmitted automatically until a new message starts. At least two FLAG sequences are transmitted before the new message begins.
2. Between two consecutive transmitted messages, two FLAG sequences are automatically inserted. In the FIFO buffer contains more than one message (after the FCS is transmitted, if FCS transmission is enabled), the transmitter sends two FLAG sequences after the last byte of the previous message is sent before starting transmission of the first byte of the new message (the next byte to be transmitted in the FIFO buffer after an EOM byte).
3. If the current message is the last message in the FIFO buffer (FIFO is empty, and the last byte is indicated as an EOM byte), the transmitter sends FLAG sequences continuously after the end of the message and as long as the FIFO buffer is empty.
4. After sending one abort sequence (sixteen 1s in underrun condition), the transmitter automatically starts transmitting FLAG sequences for as long as the FIFO buffer is empty (at least two FLAG sequences are transmitted before starting a new message).

ABORT Message Transmission

ABORT is defined in ISO-3309 as a sequence of seven or more continuous 1s.

The ABORT message generated by the transmit circuitry is a sequence of 16 continuous 1s. It is generated automatically as a result of an underrun condition. When underrun occurs, the transmit generates only one abort sequence followed by at least two FLAG sequences before transmitting the next message.

For the system to intentionally send an ABORT sequence during a message transmission without damaging other messages stored in the TDL FIFO buffer, the system must stop writing new data bytes to the FIFO buffer. In addition, the system must not write an EOM data byte, and wait until the FIFO buffer is emptied. When the FIFO buffer is emptied, an underrun occurs which results in sending the desired ABORT sequence.

2.1.1.7 FEAC Channel Transmission

A description of a FEAC channel is applicable to each framer on the device.

There are three sources available for transmission of FEAC bits in DS3 C-bit parity mode that are set at the Transmit Overhead Insertion 1 Control register by bits ExtDat and ExtFEAC/PD for each framer individually: 1. from data, 2. from an external pin, or 3. generated internally using the Transmit FEAC Channel Byte register and the microprocessor. When TxFEAC bits are sourced from data (ExtDat = 1) or from an external pin (ExtFEAC/PD = 1 and ExtDat = 0), no operation is done by the framer except inserting TxFEAC bits to the transmitter data stream at the proper time (when TxFEAC bits are inserted from an external pin). When TxFEAC is generated internally (ExtFEAC/PD = 0 and ExtDat = 0), the code word to be transmitted at the TxFEAC is taken from the Transmit FEAC Channel Byte register.

When TxFEAC is generated internally, the Transmit FEAC Channel Byte register controls the byte to be transmitted on the TxFEAC channel. All messages transmitted on this channel are in the form 0xxxmmm011111111. The right-most bit of this sequence is the first bit transmitted on the channel. Only the 0xxxmmm0 byte of the 16-bit message is written to the Transmit FEAC Channel Byte register; the eight consecutive 1s of the FEAC message are transmitted automatically.

The transmitter FEAC mechanism provides the microprocessor with an interrupt and a status bit indicating that the interrupt's source is the TxFEAC (transmit FEAC channel Interrupt bit [TxFEACltr] at the Transmit Data Link FEAC Status register). The setting of bit TxFEACIE at the Feature3 Control register can mask the interrupt. The transmitter FEAC interrupt indicates that the last message was sent and a new message byte can be written to the Transmit FEAC Channel Byte register.

A reset or returning to enable after a disable clears the TxFEAC interrupt (if it was issued). A new interrupt is not issued until a new FEAC message is written and sent, and until then, repetitive 1s are sent.

Activating transmission of AIS in C-bit parity mode in the middle of a FEAC message transmission terminates the FEAC message. The FEAC state machine returns to IDLE state, and no transmitter FEAC interrupt is issued. When AIS transmission is deactivated, the transmitter sends IDLE sequence (repetitive 1s) on the FEAC channel until a new message byte is written to Transmit FEAC Channel Byte register controls.

Transmission of Yellow Alarm or DS3 IDLE code in C-bit parity mode has no effect on TxFEAC channel transmission.

Two modes of transmitting a FEAC message available using the Transmit FEAC Channel Byte register are the single code-word mode and the repetitive code-word mode. These are set by bit FEACSin in the Feature3 Control register.

Single Code-Word Mode

In this mode, to initiate transmission of a message byte in the TxFEAC channel, the desired byte, in the form 0mmmxxx0 is written into the Transmit FEAC Channel Byte register (TxFEAC[7:0]).

Each time a FEAC written message is sent (eight consecutive 1s, followed by TxFEAC written byte), an interrupt is issued on the MINTR* output pin (if interrupt is enabled) to indicate that the last message was sent and to request a new byte from the processor. The transmit FEAC channel Interrupt bit (TxFEACltr) at the Transmit Data Link FEAC Status register is set high. The Transmit Data Link FEAC Status register must be read to clear the interrupt. After sending a written message, if a new message byte is not written to Transmit FEAC Channel Byte register, the old message is continuously issuing an interrupt for each time the message is sent. Interrupts from the TxFEAC channel occur at a rate of approximately one interrupt per 1.7 ms. If a 1 is written in either the MSB or LSB position of the TxFEAC field, continuous transmission of idle flags (repetitive 1s) is enabled (starting after the current message transmission is complete). No interrupts are issued until a byte of the proper format is written to the Transmit FEAC Channel Byte register. Interrupts from the TxFEAC channel transmitter are indicated by appearing on Transmit FEAC Channel Interrupt bit of the framer that generated the interrupt (TxFEACltr bit).

Repetitive Code-Word Mode

In this mode, each new code word that is written to the Transmit FEAC Channel Byte register is transmitted repetitively (eight consecutive 1s, followed by TxFEAC written byte). Every 10 consecutive times the message is transmitted, an interrupt is issued on the MINTR* output pin (if transmitter FEAC interrupt is enabled) to request a new byte from the processor. TxFEACltr bit at the Transmit Data Link FEAC Status register is high. The interrupt is cleared with the reading of the Transmit Data Link FEAC Status register. If a new byte is not written to the Transmit FEAC Channel Byte register after an interrupt was issued, the old message is transmitted continuously (it is repeated for another 10 times until the Transmit FEAC circuitry checks again whether a new message byte was written to Transmit FEAC Channel Byte register). If a new message byte is written, the transmitter first finishes sending the old message and then starts sending the new written message. If a 1 is written in either the MSB or LSB position of the TxFEAC field, continuous transmission of idle flags (repetitive 1s) is enabled (after transmitting the last message 10 times). Interrupts are not issued until a byte of the proper format is written to the Transmit FEAC Channel Byte register.

NOTE: There is no TxFEAC channel transmission in either E3 mode or DS3 M13/M23 modes.

2.1.1.8 Test Equipment —Error Insertion

The CX2836x framer provides the ability to insert errors intentionally in the transmitted data stream (for each framer individually) by using the Error Insertion Control registers. The Error Insertion Control registers contain a control bit for each available error. Setting the relevant bit at the Error Insertion Control registers causes insertion of one requested error at the next valid opportunity for each error. Once the error is inserted, the relevant control bit is automatically cleared. Several different error insertions can be set at the same time by setting more than one error control bit; each error selection is cleared when the appropriate error is inserted. Before setting the control bits for another error insertion, they must be polled for the desired errors and the relevant control bits, must be checked for zero. Writing zero to the control bits does not affect their settings.

The errors that can be inserted, and their effect on the transmitted data, are specified for each basic mode of operation.

DS3 Mode

In DS3 mode (both in M13/M23 and in C-bit parity mode), errors listed in Table 2-4 can be transmitted by setting bits at the Error Insertion1 Control register.

Table 2-4. Setting the Error Insertion1 Control Register in DS3 Mode

Error	Bit	Set To	Description
Framing F	FrmErrF	1	A single F-bit error is inserted by inverting the next transmitted F-bit (only one bit).
Framing M	FrmErrM	1	A single M-bit error is inserted by inverting the next transmitted M-bit (one M-bit).
P-bit parity	ParErr	1	Transmission of incorrect value in the two P-bits (i.e., incorrect parity calculation over the previous frame). In this case, the next two P-bits of a single frame to be transmitted are inverted.
P-bit parity disagreement	ParDgrErr	1	Transmission of unequal P-bits at the next opportunity (performed by inverting the next transmitted P-bit).
CP bit error (path parity)(1)	CPErr	1	Transmission of an incorrect value in the three CP bits in an M-frame. It is performed by inverting the three CP bits of a single M-frame at the next opportunity.
RAI	YelErr	1	Transmission of the opposite value of the M-frame X-bits than the expected or set value. This is performed by inverting the two X-bits transmitted in a single M-frame at the next opportunity. Thus, if RAI is set to be transmitted, the X-bits are set to 1 (instead of 0). If RAI alarm is not set to be transmitted, both X-bits are transmitted as 0 (instead of 1).
X-bit disagreement	XdgrErr	1	Transmission of opposite values of both X-bits in an M-frame. The setting of XdgrErr to 1 causes the two X-bits of a single M to be transmitted with opposite values by inverting the next X-bit to be transmitted.
FEBE(2)	FEBEErr	1	Transmission of opposite of the expected code in FEBE bits (the three C-bits in Subframe 4). When FEBE bits are set to be internally-automatically generated, setting a FEBE error insertion results in transmission of a 111 code (no error code) in FEBE bits of a single M-frame (at the next opportunity) if a frame error or a C-bit parity error is detected. Otherwise, it transmits the value stored in FEBEC/PT[1:3] in the Feature1 Control register.

FOOTNOTE:
(1) In DS3 C-bit parity mode.
(2) Active in C-bit parity only.

E3-G.751 Mode

In the E3-G.751 mode of operation, setting bits at the Error Insertion1 Control register can generate the errors listed in Table 2-5.

Table 2-5. Setting the Error Insertion1 Control Register in E3-G.751 Mode

Error	Bit	Set to	Description
FAS	FrmErrF	1	Causes one bit of the next FAS sequence to be inverted.
RAI	YelErr	1	Transmission of the opposite value of A-bit than expected or set. In this case the next transmitted A-bit is cleared to 0 if an RAI should be transmitted, and set to 1 if RAI is not expected (done by inverting the next A-bit before transmission).

E3-G.832 Mode

In the E3-G.832 mode of operation, setting bits at the Error Insertion1 Control register can generate errors listed in Table 2-6.

Table 2-6. Setting the Error Insertion1 Control Register in E3-G.832 Mode

Error	Bit	Set to	Description
Framing Error (FA error)	FrmErrF	1	Transmission of one framing bit error. This causes one bit of the next FA sequence to be inverted.
BIP-8 parity	ParErr	1	Transmission of a single incorrect bit in the next BIP-8 sequence by inverting it before transmission.
RDI	YelErr	1	Transmission of the value opposite of the RDI bit than expected or set. The next transmitted RDI bit is cleared to 0 if an RDI should be transmitted, and set to 1 if RDI is not expected (done by inverting the next RDI bit before transmission).
REI (FEBE)	FEBEErr	1	Transmission of the value opposite from the expected one (by automatic generation or its inserted value from external pin or with payload) at the next MA REI bit position. This is done by inverting the next transmitted MA REI bit.

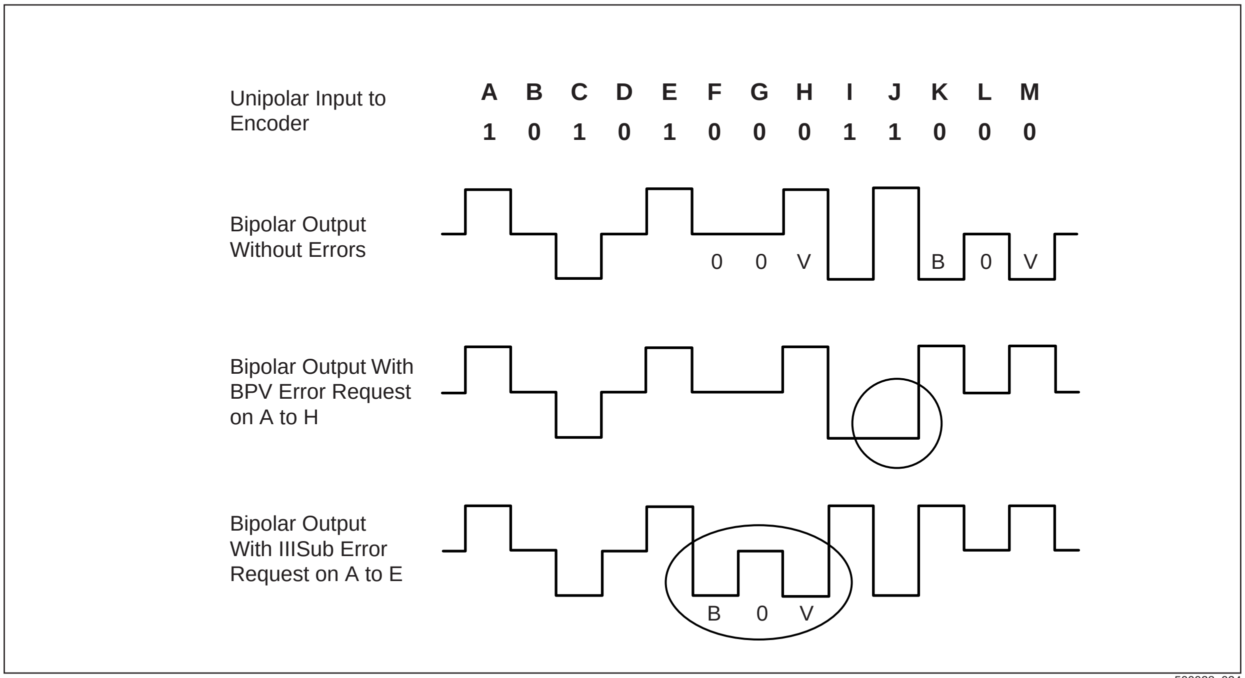
NOTE: Error insertion can be performed by the system only on Overhead bits that are set to be automatically generated or taken from a register. Setting error insertion on Overhead bits where the source is set to be from TEXTI pin, or inserted with payload, produces undefined results.

Line Coding Errors

In all basic modes of operation, line code errors can be forced when the transmitter line side is operating in AMI or rail (HDB3/B3ZS encoding) mode.

In AMI or rail mode, a bipolar violation (BPV) can be inserted by setting the LCVBPV bit in the Error Insertion2 Control register. The next 11 arriving after the bit is set is changed to 1V (this restriction, rather than just reversing the next 1, prevents inadvertently creating a zero-substitution sequence). Then, the encoding circuitry adjusts itself to the reversed signal, causing the following output to be opposite from the one that would have been produced had this error not been introduced; otherwise, each error insertion would result in two consecutive BPVs. Figure 2-11 illustrates an example.

Figure 2-11. Line Coding Error Insertion



In rail mode, an illegal substitution (IllSub) can be inserted by setting the LCVIllSub bit in Error Insertion2 Control register. The next 000 (in DS3) or 0000 (in E3) arriving after the bit is set is reversed (00V to 10V or vice versa in DS3; 000V to 100V or vice versa in E3). Then the encoding circuitry adjusts itself to the reversed signal, causing the following output to be the reverse of the one that would have been produced had this error not been introduced; otherwise, each error insertion would also result in a BPV.

Figure 2-11 illustrates the possible bipolar outputs (in DS3 B3ZS) resulting from a given unipolar input (assumes ideal conditions where there is no delay between the error insertion request and its execution):

- Unipolar input (from transmitter circuitry to encoder) of 13 bits, marked A to M
- Bipolar output (from encoder to line) without errors
- Bipolar output with BPV error insertion requested on bits A to H
- Bipolar output with IllSub error insertion requested on bits A to E

NOTE: The actual erroneous bits are circled in the Figure 2-11. Bits following an error insertion are reversed compared to the original line 2 (i.e., bits K–M in line 3, and I–M in line 4).

2.1.2 Receiver Operation

2.1.2.1 Line Signals

The line receive interface consists of three input signals:

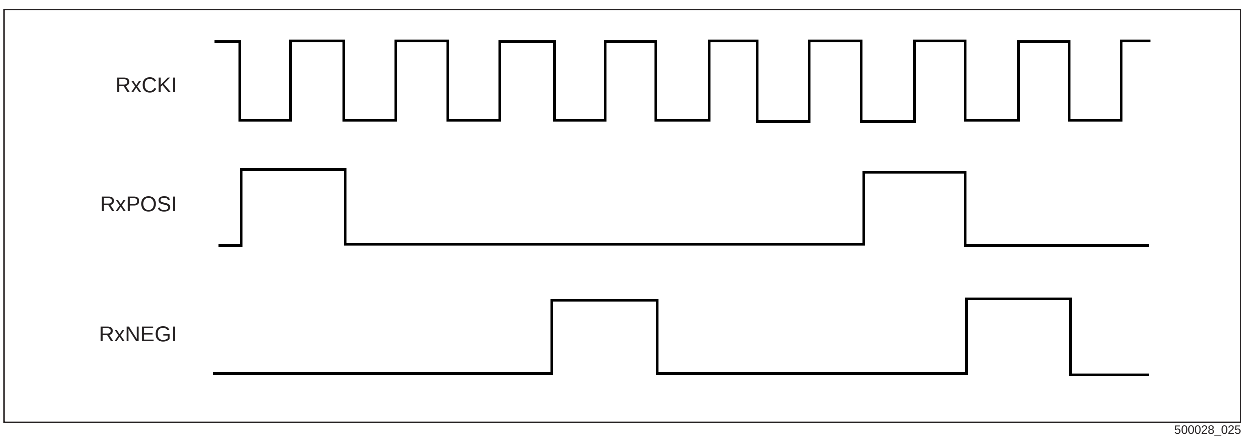
1. RxCKI—Receive clock derived from incoming data (44.736MHz or 34.368 MHz).
2. RxPOSI/RxNRZ—In Bipolar mode, is positive polarity data. In Unipolar mode, is NRZ data.
3. RxNEGI/LCVI—In Bipolar mode, is negative polarity data. In Unipolar mode, reports an LCV (or tied to ground).

The line interface can be placed in Bipolar or Unipolar mode and the RxAMI field of the Feature1 line code can be selected as AMI or B3ZS/HDB3. See register CR04.

The data stream is sampled from the data (RxPOSI and RxNEGI, or RxNRZ and LCVI) pins on either the rising or the falling edge of RxCKI (CR08 register). Figure 2-12 illustrates the relation between data (100100110) and clock assuming data is sampled on the rising edge of the clock.

The CX2836x decoder converts the bipolar signal to a unipolar stream based on AMI/ B3ZS/HDB3 line code and detects LCV, if any. The decoder is bypassed in NRZ (unipolar) mode.

Figure 2-12. Receiver Line Input Timing



2.1.2.2 System Signals

The system-side receive interface consists of four output signals:

- RxGCKO—Data clock, gapped during Opportunity bits (programmable)
- RxDATO—Data (all payload and overhead)
- REXTCKO—Receive supplementary clock, (programmable)
- RxSync—Frame synchronization output signal

RxCKI clocks the internal circuits and drives both output clocks (RxGCKO and REXTCKO). Output signals (RxDATO and RxSync) change on either the rising or falling edge of the output clocks (as defined in the CR08 register).

RxGCKO functionality is software-selectable to one of five modes:

1. Ungapped (identifies every payload and Overhead bit)
2. Overhead gapped (identifies every Payload bit)
3. Non-Cj gapped (identifies every Payload and Justification Control bit)
4. Non-stuff gapped (identifies every Payload and Stuff Opportunity bit)
5. Non-Cj and stuff gapped (identifies every payload bit, Justification Control bit, and Stuff Opportunity bit)

The RxSync output signal has two modes based on the selection of the RxOvhMrk field of the CR08 register:

1. As a frame synchronization signal, it rises from low to high on the first bit of each frame. It returns to low after the third M-bit in DS3; mode it returns to low after the first Cj-bit in E3-G.751 mode, and it returns to low after the last bit of the GC byte in E3-G.832 mode.
2. As an overhead marker signal, it is low on all Overhead bits and high on all Payload bits.

NOTE: Justification Control and Stuff Opportunity bits are viewed as Overhead bits.

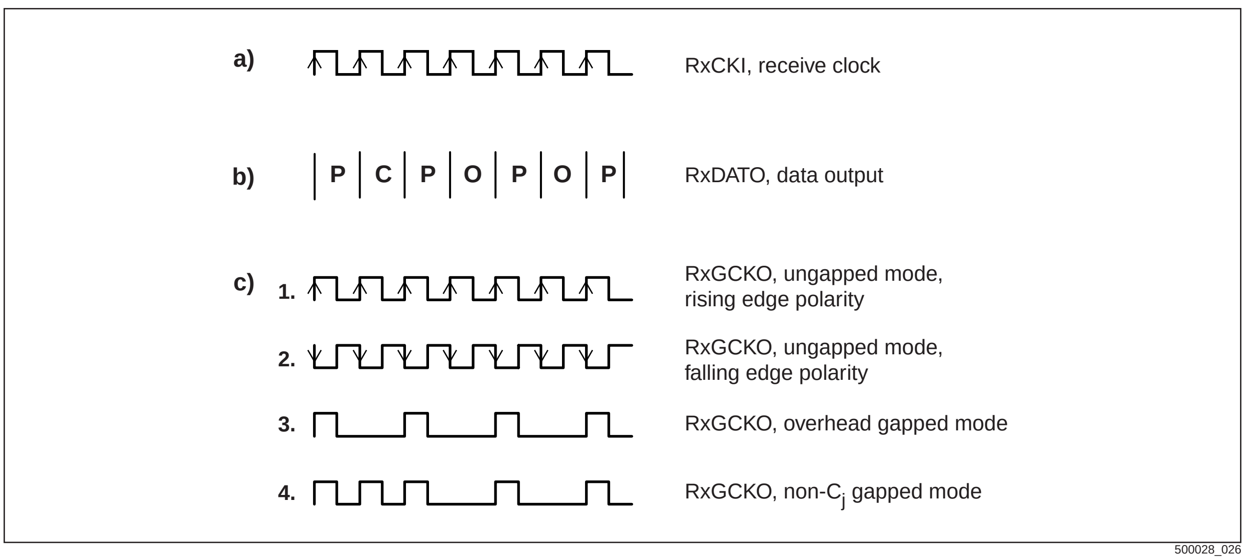
Figure 2-13 illustrates the ideal behavior of system-side outputs, in several modes, for a general data stream that represents seven bits (bits 1, 3, 5, and 7: payload [P]; bit 2: Cj overhead [C]; bits 4 and 6: non-Cj overhead [O]; bit 3 is the last bit of one frame, bit 4 is the first bit of the next frame).

a) RxCKI, internally-used receiver clock.

b) RxDATO, data output.

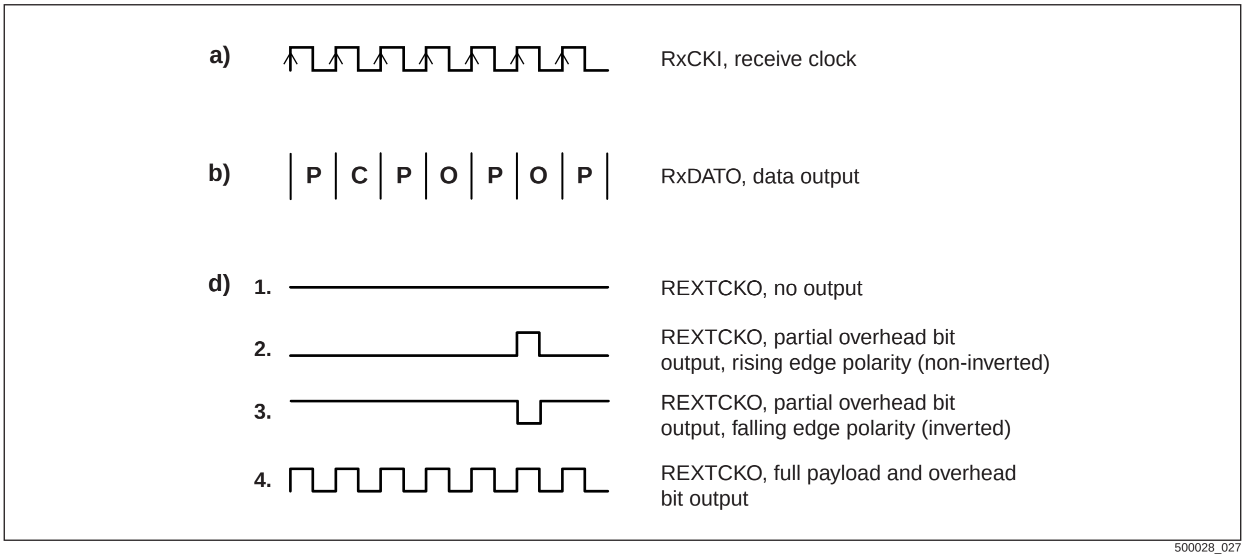
c) RxGCKO, in three of the five modes (ungapped, overhead gapped, and non-C_j gapped), each available at either rising or falling edge polarity (only shown for ungapped, but valid for all five modes).

Figure 2-13. Receiver System Side Outputs [RxGCKO]



d) REXTCKO, in three representative selections (no output, partial Overhead bit output, and full Payload and Overhead bit output). Each is available at either rising or falling edge. Figure 2-14 illustrates partial Overhead bit output, but it is valid for all selections.

Figure 2-14. Receiver System Side Outputs [REXTCKO]

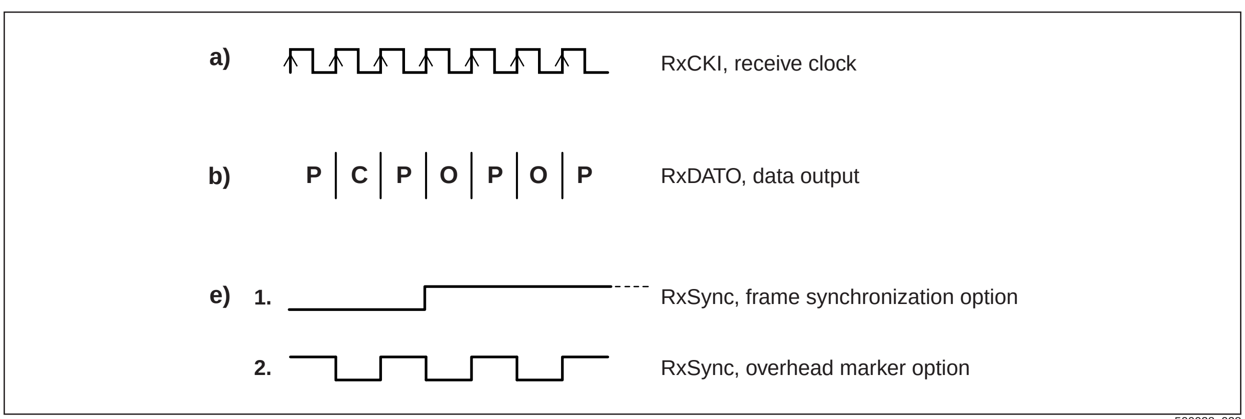


e) Figure 2-15 illustrates two options of RxSync signal, frame synchronization signal, and overhead marker signal.

Options are available (via the RxAll1 and RxAIS fields of the CR08 register) to produce either an all 1s or an AIS output, respectively, on the RxDATO pin, completely masking the received input. In addition, automatic assertion of an all 1s stream is available (via the RxAutoAll1 mode control bit in CR08 register). In this case, detection of one or more of the following events produces an all 1-s sequence: LOS, OOF, AIS, Idle in DS3 mode, and LOS, OOF, AIS in E3 mode.

Termination of these events, terminates the all-1s stream assertion. The received data is otherwise normally handled and results in all expected indications and performance monitoring.

Figure 2-15. Receiver System Side Outputs



NOTE: During an OOF condition, the system-side interface continues to function relative to the previous framing position (the RxSync, RxGCKO, and REXTCKO signals are relative to the previous framing position) until a new framing template is located, and the OOF condition is turned off.

2.1.2.3 Overhead Bit Recovery

The bit stream arriving from the line side is functionally divided into two categories, payload and overhead. See Appendix B.

Processing of Overhead Bits

The Overhead bits are processed as follows:

External-Data—All overhead and payload bits exit on the RxDATO pin; a gapped clock is supplied for skipping Overhead bits, RxGCKO (see Figure 2-13). This clock's gaps come in one of five types: 1. all Overhead bits, 2. all Overhead bits except Justification Control bits, 3. all Overhead bits except Stuff Opportunity bits, 4. all Overhead bits except justification control and Stuff Opportunity bits, 5. or none are gapped (software-selectable by setting the AllOVHDat and RxCjDat fields of the Receive Overhead Control register).

Internal—Several fields are internally evaluated for alarm and status detection (framing bits, RAI/RDI, FEBE/REI, parity, and path parity bits) or supplied to the system via microprocessor-side buffers or registers (DL, FEAC, PT, PD/MI, TM/SSM, and AIC).

External-Extended—All overhead and payload bits exit on the RxDATO pin; a clock is supplied for marking various sets of overhead and payload bits (REXTCKO) (see Figure 2-14). The output is based on the settings of REXTCKO Control register fields:

- In DS3 C-bit parity, the eight independently-selectable field combinations are as follows:
  - F-bits + M-bits + X-bits + P-bits
  - Cb11 (AIC)
  - Cb13 (FEAC)
  - Cb3 (Path Parity)
  - Cb4 (FEBE)
  - Cb5 (Data Link)
  - Cb12 + Cb2 + Cb6 + Cb7 (Reserved)
    - All Overhead bits + all the payload (effectively a full serial stream)
- In DS3 M13/M23, the four independently-selectable field combinations are as follows:
  - F-bits + M-bits + X-bits + P-bits
  - C-bits
  - Stuff bits
  - All Overhead bits + all the payload (effectively a full serial stream)
- In E3-G.751, the six independently-selectable field combinations are as follows:
  - FAS
  - A-bit
  - N-bit

  - Cj-bits
  - Stuff bits
  - All Overhead bits + all the payload (effectively a full serial stream)
- In E3-G.832, the eight independently-selectable field combinations are as follows:
  - FA + EM + RDI + PT
  - TR
  - REI
  - PD/MI
  - TM/SSM
  - NR
  - GC
  - All Overhead bits + all the payload (effectively a full serial stream)

NOTE: These modes are not mutually exclusive, i.e., the modes set for REXTCKO and RxGCKO do not interfere in any way with each other or with the internal processing of overheads).

Internal Processing of Overhead Bits

The internal logic is responsible for continuously identifying and monitoring the framing bits (i.e., F-bits, M-bits, FAS, and FA) to recover, maintain, and identify loss of frame alignment. The analysis of these bits governs identification of the Framing Bit Error (FBE), Out of Frame (OOF), and Severely Errored Frame (SEF) indications. DS3's maximum average reframe time is less than 1.5 ms, and E3's maximum average reframe time is less than 1 ms.

Control over the frame-search mechanism is available through the RefrmStp bit in the Feature5 Control register:

- When this bit is set (i.e., a 1), no frame-search is conducted (regardless of OOF status)
- When this bit has been cleared (i.e., 0 is written over a previous 1), frame-search resumes, shifted forward by one bit from the current frame position, until a new framing is located
- When this bit is clear (i.e., a 0), searching occurs in response to an OOF status

To produce a forced reframe, the microprocessor usually needs two write cycles, the first to write a 1 to the bit, the next to write a 0 to it. Note: activating this forced reframe does not transfer the receiver into OOF. The receiver circuit actually moves its framing template due to forced reframe only after the criteria for in frame have been met for the new position. The status of the frame-search mechanism is open to inspection through the ReFrm bit of the Maintenance Status register.

RAI/RDI bits (i.e., X-bits, A-bit, and RDI) are continuously monitored and their value mirrored through the RAI/RDI indication. Similarly, FEBE/REI bits (i.e., Cb4 and REI) are monitored and their value mirrored through the FEBE/REI indication. In case of X-bits, any disagreement between the two bits is also noted through the X-bit disagreement indication.

For each frame, parity is calculated according to the definitions for that frame type, and is compared to that found in the parity/path-parity bits (i.e., P-bits, Cb3, and EM). Any discrepancy is flagged through the parity error and path-parity error indications. In case of P-bits, any disagreement between the two bits is noted via the P-bit disagreement indication.

The AIC bit (Cb11) in DS3 C-bit parity is always 1; while the same bit in DS3 M13/M23, being a justification bit, is either 0 or 1. An 8-bit register (ReceiveAICByte Status register) containing the AIC bits from eight consecutive frames is provided for polling and system verification of the bit.

Internal processing of the terminal data link bits (i.e., Cb5, N-bit, NR, and GC) as HDLC/LAPD channels makes their contents available to the system through an internal 128-byte FIFO buffer; this mechanism is fully described in Section 2.1.2.5. It is not possible to use this internal mechanism for non-HDLC channels.

Messages flowing on the FEAC (Cb13) channel are supplied to the system via a dedicated register.

Non-alarm fields of the MA byte (i.e., PT, PD/MI, and TM/SSM) are available for inspection through the microprocessor interface. Their contents (three bits for PT, two bits for PD/MI, one bit for TM, and four bits for SSM) are saved on every E3-G.832 frame in dedicated registers (RxMAPT, RxMAPD, and RxMATM fields of the E3-G.832 MAFields Status register; RxSSM field of the E3-G.832 SSMField Status register). The host processor poll these fields to detect changes in their values. The RxSSM field, on a multiframe boundary (i.e., when MI is 11), stores the 4-bit SSM field, spread over a four-framed multiframe based on the MI field. Selection of whether the framer functions in TM or SSM mode is through the SSMEn field of the Feature4 Control register.

There is no internal processing of justification control, Stuff Opportunity, reserved, and TR fields.

2.1.2.4 Performance Monitoring

The performance monitoring function is available through event indicators, counters, and interrupts. An event indicator represents an event, such as parity error, or a change of status, such as out-of-frame. These event indicators can be the cause for an interrupt or the increment of a event counter. The event indicators are BPV, EXZ, LCV, FBE, PER, PBD, PPER, XBD, FEBE/REI, LOS, OOF, SEF, AIS, IDLE, and RAI/RDI.

These event indicators are externally identifiable through interrupts, counters, or the status registers they affect. All counters used to count the events are 16 bits long except the LCV counter, which is 24 bits long. If these counters are read once per second, the size of the counters guarantees non-saturation in normal conditions (assuming a BER ≤1E3).

Depending on the settings of the Counter Interrupt Control register, the counters function either in saturation mode or rollover mode.

If the interrupt associated with a specific counter is masked, the counter operates in saturation mode. In this mode, the counter counts up to the highest possible value and turns on a saturation indication bit in the Counter Interrupt Status register. The counter and the indication bits are cleared when read.

If the interrupt associated with a specific counter is unmasked, the counter operates in the rollover mode and resumes counting from zero after counting up to the highest value. An interrupt is generated, and an interrupt identification bit is set in the Counter Interrupt Status register. The counter and the status register are cleared when read.

NOTE: In reading 16-bit/24-bit counters, software should read the low byte first and then the high byte/bytes. The counters do not miss or double count any errors during the microprocessor reads. At reset all counters are cleared.

When the MINTR* pin is active, an appropriate interrupt identification bit is active or set. Unless otherwise qualified, the interrupt is associated with the identification bit, and both are cleared when the identification bit is read. The status indication bits often parallel the interrupts and can be used for applications preferring polling to interrupts. Once an interrupt occurs the microprocessor should read the SrcChnl1-SrcChnl4 fields of the Source Channel Status register to identify the interrupt originating channel. Once the channel is identified and read, the Interrupt Source Status register identifies which sub-block initiated the interrupt. The interrupt identification fields of the Status Indication register for that sub-block identifies the type of interrupt. All interrupts are masked on reset. They are unmasked or made active by setting the appropriate fields in the AlarmStartInterrupt and AlarmEndInterrupt registers.

NOTE: The presence of one event indicator does or inhibit the other events from occurring or inhibit the other data channels (Data Link or FEAC). For example, FBE is still active in OOF, and internal datalink processing is still active in AIS.

The following sections describe the various event indicators encountered in DS3/E3.

Bipolar Violation (BPV), Excessive Zeros (EXZ), and Line Code Violation (LCV)

A BPV is defined as the occurrence of a signal of the same polarity as the previous one in an AMI mode or rail mode pulse sequence. An EXZ is defined as the occurrence in rail mode of more than two DS3 or three E3 consecutive 0s, regardless of the length of the zero string.

A LCV is defined as the occurrence of either EXZ or BPV, excluding those that are part of the zero substitution code in DS3 mode. In E3 mode, the LCV is defined as the occurrence of two consecutive BPVs of the same polarity.

In rail mode (B3ZS/HDB3), LCV and EXZ events are counted. In AMI mode, BPV events are used to increment the LCV counter. In unipolar mode, only LCV is valid, and the LCV (defined as a pulse on RxNEGI/LCVI pin) counter is updated.

Loss of Signal (LOS)

In DS3, LOS is declared when there are no signal pulses of either polarity over a period of 100 contiguous pulse intervals in rail mode. The LOS event is terminated when the pulse density equals or exceeds 33% over a period of 100 contiguous pulse intervals. The same is true in AMI mode.

In E3 mode, an LOS is declared when there are no signal pulses of either polarity over a period of 100 contiguous pulse intervals in rail mode. The LOS event is terminated when the pulse density equals or exceeds 25% over a period of 100 contiguous pulse intervals. The same definition is true in AMI mode. In unipolar mode, an LOS event is undefined.

When a LOS is initiated, it generates a LOSStrt interrupt indication and sets the LOS status indication bit (the LOSAlm field of the Maintenance Status register). Upon the termination of the LOS event, the LOS event generates a LOSEnd interrupt indication and clears the LOS status indication bit.

In the presence of LOS in the E3 and DS3 modes, if the Auto RAI field is set in the Transmit Overhead Insertion 1 Control register, RAI/RDI is transmitted on the transmit stream.

In the presence of LOS in the E3 and DS3 modes, if the RxAutoAll1 field is set in the Feature5 Control register, an all-1s sequence is transmitted on RxDATO towards the receive system side.

Framing Bit Error (FBE)

In E3, an FBE event occurs when a framing bit (FAS, F, M, or FA) in the receive stream is different from the expected value. The FBE event increments a FBE counter.

In DS3 C-bit parity mode, an FBE event is valid and counted. If internal FEBE generation is programmed for the transmitter by clearing the ExtFEBE/Cj-bit in the TransmitOverheadInsertion1 Control register, the detection of a framing bit error in the receiver causes transmission of FEBE error code by the transmitter.

Out of Frame (OOF)

In DS3 mode, an OOF event is declared if, in the receive data stream, there are three or more F-bit framing bit errors in sixteen consecutive F-bits or one or more M-bit FBEs per frame in two or more of four consecutive frames. The OOF is terminated upon the non-occurrence of FBEs in three consecutive frames. The checking of F-bits is done in batches of 16 F-bits and not as a sliding window.

In E3-G.751 mode, an OOF event is declared if, in the receive data stream, there is one or more FBEs per frame in four consecutive frames. The OOF is terminated if there are no FBEs in three consecutive frames.

In E3-G.832 mode, an OOF event is declared if, in the receive data stream, there is one or more FBEs per frame in four consecutive frames. An OOF event is also declared if there are PER in 986 or more frames in a block of 1000 frames. The OOF is terminated if there are no FBEs in three consecutive frames.

The OOF event generates an OOFStrt interrupt indication and sets the OOF status indication bit in the OOFAlm field of the Maintenance Status register. Terminating the OOF event generates an OOFEnd Interrupt and clears the OOF status indication bit.

NOTE: While the framer is searching for a new framing template, the old one is maintained for ongoing performance monitoring (e.g., FBE) and output signaling (e.g., RxSync).

In E3 mode, in the presence of OOF, RAI/RDI is transmitted on the transmit stream if the AutoRAI field in the TransmitOverheadInsertion 1 Control register is set.

In both E3 and DS3 modes, in the presence of OOF, an all-1s sequence is transmitted on the RxDATO toward the receive system side if the RxAutoAll1 field in Feature5 Control register is set.

Severely Errored Frame (SEF)

In DS3, an SEF event is declared when there are three or more F-bit FBEs in sixteen consecutive F-bits. This is terminated when the framer is in frame (i.e., OOF end). This is not specified in E3 mode.

The SEF event generates a SEFStrt interrupt indication. Because the termination criteria for SEF is identical to OOF, there is no SEF-end interrupt indication.

Alarm Indication Signal (AIS)

In DS3, AIS event is declared when the receiver recognizes the AIS pattern (i.e., payload set to a 1010... sequence, with C-bits set to 0, X-bits set to 1, and F-, M-, and P-bits all valid) for two consecutive frames with ten or less deviations per frame and when OOF is off. The AIS event is terminated, if in the receive data stream, there are eleven or more deviations per frame for two consecutive frames or OOF is on.

An E3-G.751 AIS event is declared when four or fewer 0s are received by the receiver per frame period for two consecutive frame periods regardless of OOF. If OOF is off, no more than two 0s can be present in the FAS bits in order to differentiate framed and unframed all 1s. The AIS event is terminated if the receiver sees five or more 0s for two consecutive frame periods.

In E3-G.832, AIS event is declared when nine or fewer 0s are received per frame period, for two consecutive frame periods regardless of OOF. If OOF is off no more than two 0s can be present in the FA bytes in order to differentiate framed and unframed all 1s. The AIS event is terminated if the receiver sees ten or more 0s per frame period for two consecutive frames.

The AIS event generates an AISStrt interrupt indication and sets the AIS status indication bit (AISDet) in the Maintenance Status register. When the AIS event terminates, AISEnd interrupt indication is generated, and the AIS status indication bit is cleared.

In the presence of AIS event, (in both DS3 and E3) an all-1s sequence is transmitted on the RxDATO pin if the RxAutoAll1 filed in the Feature5 Control register is set.

Idle Signal (IDLE)

In DS3, an IDLE event is declared when the receiver recognizes the IDLE pattern (i.e., payload set to a 11001100... sequence, with Cb3 bits set to 0, X-bits set to 1, and F-, M- and P-bits all valid) for two consecutive frames with ten or fewer deviations per frame when OOF is off. The IDLE event is terminated if the receiver has eleven or more deviations from the expected IDLE pattern per frame for two consecutive frames or OOF is on.

The IDLE event generates an Idlestrt interrupt indication and sets the IDLE status indication bit in the Maintenance Status register. When the IDLE event terminates, IdleEnd interrupt indication is generated and the IDLE status indication bit is cleared.

In the presence of an IDLE event (only in DS3), an all-1s sequence is transmitted on the RxDATO pin if the RxAutoAll1 field in the Feature5 Control register is set.

Parity Error (PER) and P-Bit Disagreement (PBD)

In DS3, as per ANSI T1.231-1997, the PER event is declared when at least one of the two P-bits differs in value from the expected value as calculated from the previous frame. The PBD event is declared when the receive data has two p-bits which are not equal.

Similarly, in the E3-G.832, the PER event is declared if, in the receive data, at least one of the eight EM bits differs from the expected value calculated on the previous frame and OOF is off. PBD is not defined in E3-G.832. Both PER and PBD are undefined in E3-G.751. The PER event increments the PER counter and the PBD event increments the PBD counter.

If the ExtFEBE/Cj field in the TransmitOverheadInsertion1 Control register is enabled, REI is transmitted on the transmit stream upon a PER event in E3-G.832 mode.

Path Parity Error (PPER)

In DS3 C-bit parity mode, the PPER event is declared when at least two of the three Cb3 bits differ in value from the expected value as calculated from the previous frame. The PPER event increments the PPER counter.

If the ExtFEBE/Cj field of the TransmitOverheadInsertion 1 Control register is enabled, FEBE is transmitted on the transmit stream upon a PPER event.

Remote Alarm/Defect Indication (RAI/RDI), X-bit disagreement (XBD)

In DS3, an RAI/RDI event is declared when both X-bits of a receive frame are 0. The RAI/RDI event is terminated when both X-bits are 1. The XBD event is declared when the two X-bits are not equal.

In E3, an RAI/RDI event is declared when two consecutive receive frames have an A/RDI bit with the value 1. The RAI/RDI event is terminated when two consecutive frames have an A/RDI bit with the value 0. The XBD event is not defined.

The RAI/RDI also generates a YelStrt interrupt indication and sets the YelDet status indication bit in the Maintenance Status register. Upon terminating, the RAI/RDI event generates a YelEnd interrupt indication and clears the YelDet status indication bit. The XBD event increments the XBD counter.

Far-End Block Error/Remote Error Indication (FEBE/REI)

The FEBE/REI event is defined only in DS3 C-bit parity mode and E3-G.832 mode. In DS3 C-bit parity mode, it is declared when at least one of the three Cb4 bits is 0. In E3-G.832 mode, it is declared when the REI-bit is 1. The FEBE/REI event increments the FEBE/REI counter.

2.1.2.5 Terminal Data Link Reception

The terminal data link channel (DL) resides on the C5 bits of DS3 C-bit Parity frames, which is approximately 28.195 Kbps (3/4760 bits at 44.736 Mbps). On the N-bit of E3-G.751 frames, it is approximately 22.375 Kbps (1/1536 bits at 34.368 Mbps). On the NR or GC (but not both) bytes of E3-G.832 frames, it is approximately 64 Kbps (1/537 bytes at 34.368 Mbps). The DL contents are generally available via one or more of three routes the data stream (marked with other overheads by RxGCKO), marked by REXTCKO, or through a FIFO-buffered microprocessor interface the first two are specified in Section 2.1.2.3; this section describes the details of the third mode.

The internal circuitry [Receive Data Link (RDL) block] provides logic and FIFO buffering for implementing LAPD/HDLC terminal data link reception according to ITU-T Q.921 and ISO/IEC 3309 standards. The logic is responsible for flag and abort sequence detection, 16-bit frame check sequence (FCS) checking and transparency zero removal, and managing the internal FIFO buffer. Each channel contains a 128-byte Receive Data Link FIFO buffer, distinct from the Transmit Data Link FIFO buffer, to reduce the amount of intervention required from the system in accessing the data link contents. The FIFO buffer contents are accessed via the microprocessor interface either in interrupt-driven mode, using maskable interrupts to synchronize data flow into and out of the FIFO buffer, or in status-polling mode.

The RDL FIFO buffer contains two types of information, data bytes and status bytes. Data bytes are the actual data extracted from the DL channel (all flag-bounded bytes except flag and abort sequences and zeros for transparency). Status bytes contain additional information qualifying the data bytes following them.

A data block within the FIFO buffer is one status byte followed by 0 to 127 data bytes.

When a new block starts, the RDL reserves one byte for status and then fills data bytes, as required, until the end of the block. At the end, status information is written into the reserved byte and a new block is started.

A block terminates and a new one starts in conjunction with one of the following:

- A FIFO near-full interrupt
- A message received interrupt
- A FIFO overrun interrupt

Before the status byte is read from the RxMsgByte Status register, the user must read the RDL Status register and get the RxGoodBlk field value. This bit defines the type of the status byte to be read from the RxMsgByte Status register.

For types a1 and a2, the RxGoodBlk is set; for type b it is cleared. Refer to Table 2-7.

Table 2-7. Status Byte Description

RxGoodBlk Field Value	MSB	Type	Description	Additional Information (Bits 0–6)
Set	Set	a1	End of message (detection of flag sequence) with correct FCS	Number of data bytes in block (range = 0 to 127)
—	Cleared	a2	Partially-received message, FIFO near-full, message data continue in next block	—
Cleared	Undefined	b	Errored block cases: end of message with incorrect FCS, or end of message with number of bits indivisible by 8 (alignment error), or aborted message (detection of abort sequence), or overrun error. Priority of error type is bad FCS, align error, abort, overrun (from low to high). Only one type of error can be indicated.	—
GENERAL NOTE: In type b, the number of data bytes in the block is always 0, as the data bytes are of no significance and therefore discarded by the RDL. Also, if one or more a2 blocks is followed by a b block, all the data bytes of the previously read a2 blocks belong to the same erroneous/aborted message.				

The available RDL-related interrupt events are as follows:

- FIFO near-full:
  - Turned on when the number of bytes in the FIFO buffer is equal to or more than the programmable Near-Full FIFO threshold (range = 2 to 127). A type a2 block ends when this interrupt is turned on, and another block of this type is not be produced until the interrupt is turned off].
  - Turned off when there are no more unread complete blocks left in the FIFO buffer, i.e., when the last byte of the last complete data block has been read: If, after reading all pending complete blocks from the FIFO buffer, the number of

bytes in the remaining incomplete block is again equal to or more than the threshold, a new interrupt is generated and another type, a2, block terminated).

- Message received:
  - Turned on when an end-of-message flag sequence or an abort sequence is detected. A type a1 or b block ends when this interrupt is turned on.
  - Turned off when the message received status indication is read (unless these interrupts are promptly and consistently read and cleared, this interrupt means that one or more message received events have occurred since the last read)
- FIFO overrun:
  - Turned on when the FIFO buffer is full and another byte must be written to it. A type b block (with overrun error-type) ends when this interrupt is turned on, and another block of this type is not produced until the interrupt is turned off.
  - Turned off when there are no more unread complete blocks left in the FIFO buffer, i.e., when the last byte of the last complete data block has been read (because all input is discarded by the RDL until the overrun is cleared, this is the status byte of the incoming message within whose data the overrun error has occurred).

These interrupts are independently enabled by setting the RxNFIE, RxMsgIE, and RxOVRIE fields in the Receive Data Link Control register, and are differentiated by reading the Status Indication register (Receive Data Link Status register).

The RDL-related status indications available are as follows:

- FIFO near-full (set and cleared with the interrupt)
- Message received (set and cleared with the interrupt)
- FIFO overrun (set and cleared with the interrupt)
- Data block in FIFO buffer (set if there is ≤ 1 complete data block in the FIFO buffer, otherwise cleared)
- Type of next FIFO byte (set if status, cleared if data, undefined if the data block in FIFO indication is not set)

These indications are detected by examining RxNF, RxMsg, RxOVR, RxBlk, and StatByte fields (respectively) of the Receive Data Link Status register.

Initial Setup

On reset, the RDL is disabled, with no interrupts active. Prior to enabling the RDL, the desired interrupt enables the Near-Full FIFO threshold, and the RDL-related options must be set to the desired values through the Receive Data Link and the Receive Data Link Threshold Control registers. Checking the 16-bit FCS is software-selectable by setting the RxFCSEn field of the Receive Data Link Control register. If the channel is functioning in E3-G.832 mode, the NRDL field of the Receive Data Link Control register should be set to identify which of the two possible overhead bytes (NR or GC) is processed by the RDL.

Setting the RxDLEn field of the Receive Data link Control register activates the RDL. Once active, the HDLC-related functionality (flag and abort detection, zero removal) of the RDL is automatically executed on all DL data flowing through the FIFO buffer. Once the RDL is enabled, it assumes the channel is idle and starts looking for HDLC flag sequences.

To modify the basic settings of the RDL (i.e., Near-Full FIFO threshold, FCS checking, E3-G.832 NR/GC source), the system should first disable the RDL (by clearing the RxDLEn field of the Receive Data Link Control register).

After disabling the RDL, when accompanied by an immediate termination of all its activities, the following enable causes discard of all the FIFO buffer contents and update of the status indications to represent a new status (i.e., all interrupt indications clear, no data blocks in the FIFO buffer).

Writing Messages into the FIFO

Data arriving on the data link channel is automatically written into the FIFO buffer by the RDL. Type a1, a2, and b block description references found below are explained in Table 2-7.

Normal Message

A new data block starts filling up when the RDL detects a transition from flag sequence 01111110 to stuffed-zero data (≤5 consecutive 1s). Each octet of message data (i.e., between flag sequences), following stuffed-zero removal (i.e., discarding a 0 directly following five contiguous 1s), is stored in a FIFO byte. A transition from zero-stuffed data back to flag sequence marks the end of the message and results in an interrupt with the indication message received.

NOTE: For each message, all octets between the initial and terminal flags—not including the flags but including the FCS—are placed in the FIFO buffer.

If the number of data bits collected is not divisible by eight, or if FCS checking is enabled and the FCS is incorrect, a type b block is marked in the block type field of the data block's status byte (the first byte of the block), the error type is noted in the same byte, all the data bytes are discarded, and a new block is started on the byte following the current status byte. Otherwise, a type a1 block is marked, the block length in the status byte is set to the number of data octets stored, and a new block is started on the byte following the last data byte stored.

Because consecutive messages can share the flag between them, the next message can start as soon as new zero-stuffed data is detected, regardless of the number of flags between the messages.

NOTE: Two flags with a shared zero between them are treated as two valid flags.

A sequence of five 1s not followed by 0 (i.e., 01111101111110) is faulty and produces a type b block (with alignment error-type).

Aborted Message

A transition from zero-stuffed data to abort sequence (≤ 7 consecutive 1s) marks an aborted message and results in an interrupt with the indication message received. A type b block is marked in the block type field, the error type is noted in the same byte, all the data bytes are discarded, and a new block is started on the byte following the current status byte. The next message starts only after at least one flag sequence is located and new zero-stuffed data follows.

Near-Full FIFO Event

A Near-Full FIFO event occurs when the number of bytes in the FIFO buffer is equal to or more than the Near-Full FIFO threshold and the FIFO near-full interrupt is off (the byte whose writing leads to this event is referred to as the threshold byte). This results in an interrupt with the indication FIFO near-full. A type a2 block is marked in the block type field, block length is set to the number of data octets stored, and a new block is started on the byte following the last data byte stored.

If the first octet to arrive after the threshold byte is a flag sequence (i.e., the threshold byte was the last byte of the FCS), the new block is a type a1 block with a length of 0 or a type b block. If the first octet to arrive after the threshold byte is an abort sequence, the new block is a type b block. Otherwise, the new block contains the upcoming bytes of the same message.

If the last octet to arrive before the threshold byte is a flag or abort sequence (i.e., the threshold byte is the status byte of an upcoming message), the type a2 block has a length of 0, and the new block contains the actual data of the new message; i.e., the system receives a message received interrupt (on the byte before the threshold byte) and, shortly afterwards, a Near-Full FIFO interrupt (on the threshold byte).

FIFO Overrun

If the FIFO buffer is full when another byte must be written to it, and the FIFO overrun interrupt is off, an overrun error occurs, resulting in an interrupt with the indication FIFO overrun. If the new byte is a data byte, it is lost (i.e., data bytes already present in the FIFO buffer are not overwritten), and the data block is immediately terminated and marked as a b block. If the new byte is a status byte, its writing to the FIFO buffer is postponed until at least one byte has been read from the FIFO buffer, and it is guaranteed to be a type b status byte.

While the RDL is in overrun state (i.e., until the indication is turned off), all incoming data bytes are discarded and nothing is written to the FIFO buffer except the status byte of the message where the overrun error occurred. New data is written to the FIFO buffer only upon detection of a transition from flag sequence to zero-stuffed data following the clearing of the interrupt.

Reading Messages from the FIFO

The system reads the contents of the FIFO buffer by accessing the Receive Data Link Message Byte Status register; each access returns the next byte from the FIFO buffer.

The Receive Data Link(i) Status register is read before a new status is read. This is done to make sure there are data blocks in the FIFO buffer (RxBlk) and that the type of the next status byte a1, a2, or type b are fetched from RxGoodBlk.

The FIFO buffer contains zero or more complete data blocks at any time, plus zero or more bytes of the current incomplete block.

At no time are the bytes of the current incomplete block accessible by the system. After reading the Receive Data Link(i) Status register, the status itself is read and understood according to the RxGoodBlk field value.

The data block in the FIFO status indication bit (the RxBlk field in the Receive Data Link Status register) is cleared if there are 0 complete blocks, otherwise it is set. Attempting to read the FIFO buffer when this bit is not set returns an undefined value, but the FIFO read pointer is not incremented.

Although there is a bit in the Status Indication register (Receive Data Link Status register), that can be queried to inform the system if the next byte to be read from the FIFO buffer is a status or a data byte (StatByte field), the bit in the Status Indication register is not strictly needed for reading from the FIFO buffer. The first byte read from the FIFO buffer after the RDL is enabled is a status byte, which indicates the number of data bytes following it, 0 for (b) blocks, additional information field for a1 and a2 blocks. After this, another status byte is again guaranteed, and so forth. The next FIFO byte type bit is supplied only for systems that do not want to maintain a count of data bytes after reading each status byte, and would rather query this bit before reading every single byte in the FIFO buffer.

Interrupt-Driven Mode

The interrupt-driven FIFO buffer reading mode is enabled by unmasking at least one of the two functional interrupts related to the RDL (FIFO near-full and message received). The third interrupt (FIFO overrun) is useful for error condition monitoring. Once an interrupt occurs, the microprocessor reads the SrcChnl1 to SrcChnl4 fields of the Source Channel Status register to identify which channel is the interrupt's originator. It then reads that channel's Interrupt Source Status register to identify which part of the chip raised the interrupt (RDL in this case, namely RxDLItr field). It then reads the interrupt identification fields of the Status Indication register for this channel's RDL (the RxNF, RxMsg, and RxOVR fields of the Receive Data Link Status register) to identify the type of interrupt.

Before reading a status byte from the FIFO buffer, the RDL Status Indication register (Receive Data Link Status register) is read, the first time after an interrupt to identify the interrupt's source, every other time to make sure there are data blocks in the FIFO buffer still left to read.

Beyond this, options of handling the interrupt are numerous, but one would expect the microprocessor to read one or more data blocks and/or one or more bytes from the FIFO buffer. What follows is a possible routine:

- The E3-G.832 framer in question has all its RDL interrupts set to active, with the near-full threshold set to 32 bytes.
- After identifying the source and type of interrupt, if the interrupt type is
  - Message received: If the microprocessor is busy, do nothing but return; if it is not busy, read one entire block from the FIFO buffer, then check if the data-block-in-FIFO indication is set; if not, return, otherwise repeat
  - FIFO near-full: Read one entire block from the FIFO buffer, check if the data-block-in-FIFO indication is set; if not, return, otherwise repeat
  - FIFO overrun: Inform the network management that the system was unable to cope with the data link throughput, then act as per FIFO near-full.

NOTE: In this example, from the time a FIFO near-full interrupt occurs until the FIFO buffer fills up, a minimum period of 12 ms (96 bytes at 8 KB) passes.

Polling Mode

Polling mode is effective when both RDL functional interrupts have been masked. Polling mode differs from interrupt-driven mode only in that the entry into the service routine is timer-dependent rather than interrupt-driven. The rest of the handling is similar to interrupt-driven mode.

2.1.2.6 Far-End Alarm and Control Channel Reception

The FEAC channel resides on the C13 bit of DS3 C-bit Parity frames. There are three ways to access FEAC contents: 1. through the data stream (marked with other overheads by RxGCKO), 2. through the data stream marked by REXTCKO, 3. through a register-based microprocessor interface. Section 2.1.2.3 discusses the first two; this section describes the third.

FEAC messages are in the form of 16-bit code words, with a pattern of 0xxxxxx011111111 (right-to-left). The code word overhead are the 10 fixed bits. The code word proper are the six x bits. The entire 16 bits are represented as the complete code word pattern. When no alarm or control signal is present, the channel carries an all-1s (idle) pattern. Internal circuitry (Receive FEAC [RFEAC] block) provides logic and a register for implementing FEAC message identification. As this channel is undefined in DS3 M13/M23 and E3 modes, the RFEAC is automatically disabled in these modes.

The RFEAC comes in two modes (selectable through the FEACSin field of the Feature3 Control register), 1. single code word detection (makes no assumptions about FEAC messages repetitions) 2. multiple code word detection (assumes each FEAC message is repeated at least 10 times).

In single code word detection, a valid code word is detected when one complete code word pattern is located.

In multiple code word detection, a valid code word is detected when nine complete code word patterns with the same code word proper are located, using the following algorithm F:

F1. [Initiation]

Locate a complete code word pattern, store its code word proper (cp1) in a 6-bit register (termed the tentative code word), set a 4-bit counter to 1, and go to step F2.

F2. [Tentative]

Locate another complete code word pattern and compare its code word proper (cp2) with the tentative code word:

- **a.** If identical, add 1 to the counter, and go to step F5
- **b.** If not, store cp2 in another 6-bit register (termed the alternative code word) and go to step F3.

F3. [Tentative and Alternative]

Locate another complete code word pattern and compare its code word proper (cp3) with the tentative code word:

- **a.** If identical, add 2 to the counter (for cp2 and cp3), and go to step F5
- **b.** If not, go to step F4.

F4. [Alternative]

Compare cp3 with the alternative code word:

- **a.** If identical, store the alternative code word in the tentative code word register, set the counter to 2 (for cp2 and cp3) and return to step F2
- **b.** If not, store the alternative code word in the tentative code word register, set the counter to 1, store cp3 in the alternative code word register, and return to step F3.

F5. [Possible Termination]

If counter ≤ 9 declare a valid code word and end algorithm, if not go to step F2.

> **NOTE:** When comparing code word propers, the number of bits differing between the two is of no importance, just their identity or lack of identity.

In both modes, no allowance is made for bit errors in the code overhead. Complete code word patterns can be separated from one another by any amount of data (whether all 1s or not), which are ignored by the RFEAC logic.

In both detection schemes, a valid idle signal is detected when 16 consecutive 1s are located.

The RFEAC is always in one of two internal states, namely idle state (the initial state) or message state:

- In idle state, the RFEAC scans for a valid code word (according to one of the two definitions given above). Once this is found, the valid code word proper (plus the two 0s) is written to the Receive FEAC Byte Status register, and a new FEAC message interrupt (with the RxFEACItr indication of the Receive Data Link FEAC Status register) is generated (it is cleared once the code word proper is read from Receive FEAC Byte Status register). This moves the RFEAC to message state.
- In message state, the RFEAC scans for either a valid code word or a valid idle signal. If a valid code word is found, processing is the same as in idle state. If a valid idle signal is detected instead, a reversion to idle interrupt (with the RxFEAC Idle indication of the Receive Data Link FEAC Status register) is generated (it is cleared once the interrupt indication is read); this moves the RFEAC back to idle state.

As a FEAC message takes 16 DS3 frames, new FEAC message interrupts arrive at a maximum rate of 1 per 1.7 ms for single code word detection, and at a maximum rate of 1 per 17 ms for multiple code word detection.

> **NOTE:** There is no buffering of messages; if the system fails to read the code word proper from the Receive FEAC Byte Status register before a new one is located, the old code word is overwritten.

There is no facility for disabling the RFEAC circuitry; systems that do not need to receive this information should not enable the two RFEAC interrupts. Similarly, systems that work by polling should also mask the interrupts and poll the interrupt identification bits. Masking and unmasking is performed by setting the RxFEACIE and RxFEAC IdleIE fields of the Feature3 Control register.

In addition to the interrupt based FEAC mechanism described above, a three-stage FIFO buffer (the FEAC stack) for FEAC messages is provided to allow for a more relaxed and flexible FEAC channel processing.

The FEAC stack mechanism provides a register (Receive FEAC Stack Byte) for the stacks' FEAC message with two extra bits. One extra bit signaling that the data is valid and has not been read and another bit signaling that there are more valid messages in the stack. If the valid bit is off, it forces the more bit to zero and the six FEAC message bits are set to undefined.

If the more bit is off, it means there are no more valid messages. An indication that the stack is not empty is provided by and implemented in the FEAC Status register bit RxFEACSNE. When this status bit is set, an interrupt is generated unless the interrupt has been masked (the RxFEACSNEIE bit in the Feature3 Control register is off). The stack has no alert on underrun and overrun. A word shifted into a full stack can overrun an old word that has not been read yet. Reading an empty stack results in reading an undefined code word except for valid bit and more bit which are zero.

Writing into the FEAC Stack

A code word is shifted in to the stack for one of three reasons:

1. If the code word is different from the previous code word.
2. If the stack was empty (either after reset or after channel enable).
3. When the FEAC channel comes out of Idle state (all 1s in the FEAC channel).

Writing a new word into the FEAC stack causes shifting of old code words, possibly overrunning the oldest code word.

Reading from the FEAC Stack

The messages are read from the FEAC stack in FIFO style. Reading FEAC stack can be done by either polling or interrupt modes.

The sequence of operation in interrupt mode is as follows:

1. Wait for an interrupt, read the RxFEACSNE before the first read.
2. Read the FEAC stack message only if RxFEACSNE is on.
3. If the more bit in the read word is off, go to step 1 (wait for the next interrupt) or else go to step 2.

The sequence of operation in polling mode is as follows:

1. Read the FEAC FIFO register. The word read is valid only if the valid bit is on.
2. If the more bit is on, the next word read is also valid.

The FEAC stack logic cannot be disabled. Host systems using the interrupt mode to read the FEAC messages should not enable the FEAC stack interrupts. The masking is performed by setting the RxFEACSNEIE in Feature3 Control register. Systems using the polling mode should not read the FEAC Stack register.

2.2 ATM Cell Processor

The CX2836x's ATM cell receiver block is responsible for recovering cell alignment, performing detection/correction, and descrambling the payload octets. The resulting ATM cells are then passed to the ATM layer via the UTOPIA interface. Simultaneously, the ATM transmitter block is receiving data from the ATM layer, optionally inserting header fields, optionally calculating the HEC, and sending the cells to the framers. If no data is being received from the ATM layer, the cell processor generates idle cells based on the data programmed into the associated registers.

Transmitted cells can be directly mapped into the framer payload or framed using the Physical Layer Convergence Protocol (PLCP) defined by the ATM Forum DS3 Physical Interface Specification: af-phy-0054.000 (1996) for T3 applications and by ETSI Standard ETS 300 214 for E3 applications. The cell receiver, accordingly, can recover cell alignment (also called cell delineation) using the HEC octet when direct mapping is used or can find PLCP frame alignment when that method is used. The following paragraphs describe direct cell mapping and PLCP framing is described in Sections 2.2.3 through 2.2.5.

The Cell Processor has all counters needed for capturing ATM error events and performs payload CRC calculations as required by the AAL formats. It generates cell status events, cell counts, and error counts.

2.2.1 ATM Cell Transmitter

The ATM cell transmitter controls the generation and formatting of 53-octet ATM cells sent to the framer (Line) Transmit ports. This block formats an octet stream containing ATM data cells from the ATM layer device when those cells are available. All 53 octets of the data cells may be obtained from the external data source and formatted into the outgoing octet stream.

This block calculates the HEC octet in the outgoing cell from the header field. The calculated HEC octet can be inserted in place of the incoming data octet by writing DisHEC (bit 7) in the CGEN register (0x08) to a logical 0. For testing purposes, this HEC octet can be corrupted by XORing the calculated value with a specific error pattern input set in the ERRPAT register (0x0B). This HEC error is achieved by writing ErrHEC (bit 4) in the CGEN register (0x08) to a logical 1. The remaining 48-octet payload field of the outgoing cell is obtained from the external data source. The payload can be scrambled.

When there is no data from the ATM layer device, the cell processor inserts idle cells automatically in the outgoing octet stream. The 4-octet header field for these idle cells comes from the TXIDL1–4 registers (0x14–17). The HEC octet is calculated and inserted automatically. The payload field is filled with the octet contained in the IDLPAY register (0x0A).

In normal operation, the 4-octet header field in the outgoing cell is passed on from the ATM layer device. Header patterns can be modified in the TXHDR1–4 registers (0x10–13) and inserted into outgoing cells in place of header bytes received from the ATM layer. Whether the original header cells or replacement cells are sent is controlled by bits 0–4 in the HDRFIELD (0x09) register.

2.2.1.1 HEC Generation

In normal operation, the cell processor calculates the HEC for the four header bytes of each cell coming from the ATM layer. It then adds the HEC coset (55 hex, by ATM standards) and inserts the result in octet 5 of the outgoing cell. HEC calculation can be disabled by setting bit 7 of CGEN (0x08) to 1. When HEC is disabled, the cell processor leaves the contents of the HEC field unchanged and transmits whatever data is placed in that field by the ATM layer.

The HEC coset is used to maintain a value other than 0 in the HEC field. If the first four bytes in the header are 0, the HEC derived from these bytes is also 0. When this occurs and there are strings of 0s in the data, the receiver cannot determine cell boundaries. Therefore, it is recommended that the value 55 hex be added to the HEC before transmission. To enable the HEC coset on the transmit side, set bit 6 in register CGEN (0x08) to 1. To enable the receive HEC coset, set bit 5 in register CVAL (0x0C) to 1.

2.2.2 ATM Cell Receiver

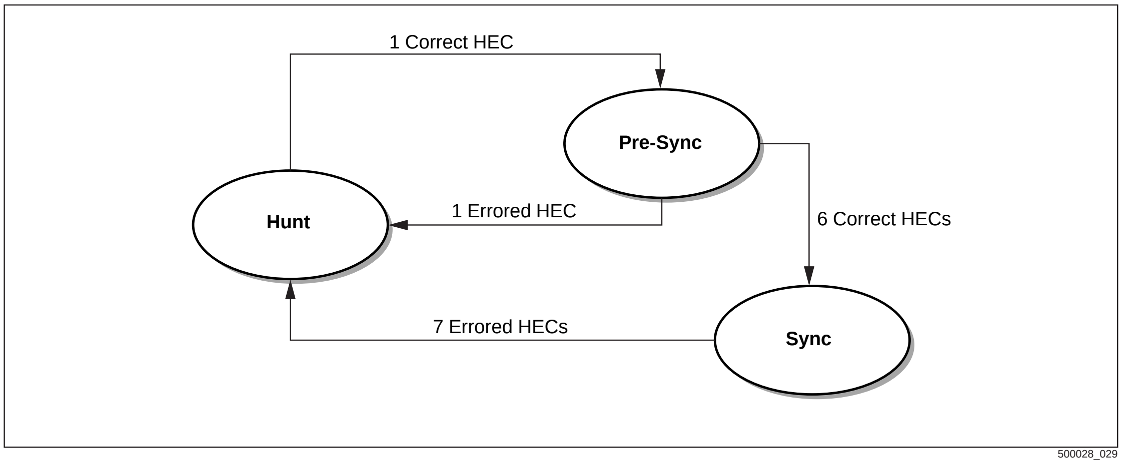
The ATM cell receiver performs cell delineation on incoming data cells by searching for the position of a valid HEC field within the cell. The HEC coset can be either active or inactive; this is determined in bit 5 in the CVAL (0x0C) register.

NOTE: The cell delineator can receive cells when the receive framer indicates OOF. Although the cells are good unless the CD reports the contrary, the cells must be considered suspect. The CD must be disabled when in the OOF state. This is accomplished by asserting the port logic reset, bit 9, in the PORTn Mode Control registers at offsets 0xE80Q–0xE8B of the Common register group.

2.2.2.1 HEC Based Cell Delineation

The ATM block receives octets from the framers and recovers ATM cells by means of cell delineation. Cell delineation is achieved by aligning ATM cell boundaries using the HEC algorithm. Four consecutive bytes are chosen and the HEC value is calculated. The result is compared with the value of the following byte. This hunt is continued by shifting this four-byte window, one byte at a time, until the calculated HEC value equals the received HEC value. When this occurs, a pre-sync state is declared and the next 48 bytes are assumed to be payload. The ATM block calculates HEC on the four bytes following this payload, assuming that a new cell has begun. If seven consecutive header blocks are found, synchronization is declared. If any HEC calculation fails in the pre-sync state, the process begins again (see Figure 2-16). Synchronization is held until seven consecutive incorrect HECs are received. At this time, the hunt state is reinitiated.

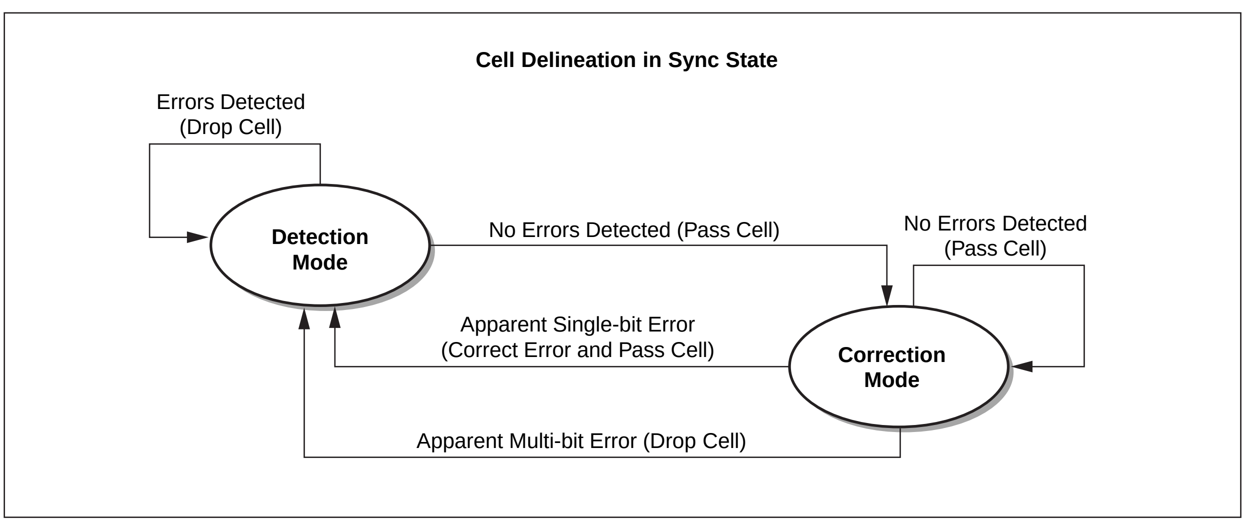
Figure 2-16. Cell Delineation Process



During the sync state of cell delineation, cells are passed to the UTOPIA interface if the HEC is valid. If a single-bit error in the header is detected, the error is corrected (optionally), and the cell is passed to the UTOPIA interface. If HEC checking is enabled and HEC correcting is disabled (bit 3 in the CVAL register [0x0C]), cells with single-bit HEC errors are discarded. If a multi-bit error is detected, the cell is dropped. Once either type of error is noted, all subsequent errored cells are dropped until a valid cell is received. This rule applies even for single-bit errors that could be corrected. Once a valid cell is detected, the process begins again. (See Figure 2-17).

When LOCD occurs, an interrupt is generated and the cell processor automatically enters the hunt mode. However, the cell is still being scrambled by the far-end transmitter, leaving only the headers unscrambled. This means that the only repetitive byte patterns in the data stream that meet the cell delineation criteria are valid headers.

Figure 2-17. Header Error Check Process



2.2.3 PLCP Cell Generation for Transmit

In PLCP formats, the PLCP overhead generation consists of the framing octets A1 and A2, the Path Overhead Identifier (POI) octets, the path overhead (POH) octets, and the trailer nibbles. The framing, POI, and POH octets are generated by the PLCD transmit circuitry, but can be selectively disabled if desired. Applicable specifications regarding DS3 PLCP operation are the BISDN Physical Layer UNI Specification: ANSI T1.646 (1995) and the ATM Forum DS3 Physical Layer Interface Specification: af-phy-0054.000 (1996), and TR-TSV-000773.

The A1 and A2 octets are generated with the normal 0xF6/0x28 pattern as the default. The POI octets are determined by the particular line rate that is selected, but in each case they consist of a slot count and a parity bit. The DS3 PLCP has 12 slots per frame, the DS1 and E1 PLCP have 10, and the E3 PLCP has 9. In each case, the POI octets provide a backwards count of the PLCP slots in the frame, along with a parity bit. Generation of the A1, A2, POI, B1, and C1 octets can be disabled (written to 0x00) via the Overhead Control [bits 7-4] of PLCPOVH register [addr 0x01]. All path overhead growth octets Zn are forced to zero. The path user channel F1 is forced to zero as a default but can be modified using register TXF1 [addr 0x03].

The B1 octet is populated with a BIP-8 code that is calculated over each PLCP frame. The BIP Error Insert [bit 1] of PLCPOVH controls insertion of BIP-8 errors in the generated PLCP. If errors are to be inserted, a non-zero value written to the ERRPAT [addr 0x0B] register inverts the corresponding bits of the B1 octet from that calculated by the BIP-8 circuit in the following PLCP frame. Insert control bits are cleared after each frame when the errors are inserted. PLCPOVH can be read to determine if this has occurred, so the microprocessor can insert BIP-8 errors as desired in each PLCP frame.

This capability can be used to verify far-end FEBE operation. BIP generation can be disabled via the Overhead Control bits. The fields of the G1 octet (PLCP Path Status) are controlled by the TXG1 [addr 0x02] register, the AutoFEBE control bit in PLCPOVH, and the InsFebeErr control bit in PLCPOVH. The FEBE bits occupy the upper nibble of G1. The FEBE controls operate as shown in Table 2-8.

Table 2-8. FEBE Controls

InsFebeErr	AutoFEBE	TxFEBE	FEBE Field Value
0	1	x x x x	According to BIP-8 Errors Received
0	0	a b c d	a b c d
1	x	x x x x	Upper nibble of ERRPAT

The Yellow Alarm bit in the G1 octet is set to the value contained in TxYellow [bit 3] in TXG1.

The C1 octet is under control of PhyType[2:0] bits in PMODE [addr 0x04] register, 8kLock[1:0] bits in PLCPSEL [addr 0x00] register, and DisC1 bit in PLCPOVH [addr 0x01] register as shown in Table 2-9.

Table 2-9. C1 Octet

DisC1	PhyType[2:0]	8kLock[1:0]	C1 Octet Value
1	x	x x	00
0	DS1, E1	x x	00
0	DS3, E3	b_{1b0}	Per Selected 8 kHz Reference

The trailer content (except in E1 mode where there is no trailer) has each nibble set to 1100.

2.2.4 PLCP Cell Validation for Receive

In PLCP framed modes, the PLCP receiver processes a serial stream to find PLCP framing. Octet synchronization is provided externally in DS1 and E1 modes. Internal or external E3 octet synchronization and DS3 nibble synchronization are provided to the PLCP framer. Physical layer framing patterns are automatically removed before recovery of the octet data.

The 57-octet PLCP framing state machine contains three states: in-frame, out-of-frame, and loss-of-frame. Valid framing is found when two consecutive valid path overhead octets in sequence are observed after the A1, A2 framing octets. The out-of-frame state is entered only from the in-frame state, when there are errors in both the A1 and A2 octets or when there are two consecutive Pn errors. This event is an OOF event, and is counted. The LOF state is entered after eight consecutive PLCP frames in the out-of-frame state.

Stuffing and destuffing are provided according to the line type setting in 57-octet formats. Cycle stuffing is used at the transmit PLCP for DS3 and E3 whenever the receive PLCP is in the LOF state or Receiver Hold Enable is high, and this function is enabled with the HldEn bit in PLCPSEL register.

NOTE: When the framing mode is dynamically modified between direct mapping and PLCP framing, the CX2836x goes into an OOF state. Dynamic switching should only be used if necessary.

2.2.4.1 PLCP Status

Errors in either the A1 or A2 PLCP framing octets cause an indication in the PLCPFrmErr bit in the PLCPSTAT [addr0x04] register. PLCP OOF events are indicated by the PLCPOOF bit in PLCBSTAT. PLCP LOF events (OOF for eight consecutive PLCP frames) are indicated by the PLCPLOF bit in PLCBSTAT. Loss of cell delineation in direct mapped modes (non-PLCP) and in PLCP modes is indicated by the LOCD bit in the RXCELL [addr 0x2F] register and counted in LOCDCNT [addr 0x33].

The PLCP Yellow Alarm status bit (PLCPYellow) is set high after 10 consecutive frames with a PLCP Yellow Alarm value (RAI bit in POH octet G1) of one and cleared after 10 consecutive frames of a value of zero.

Errors detected in the receiver BIP-8 code checking circuit cause BIP-8 Error (PLCPBIPErr bit in PLCPSTAT register) to be set and counted (BICNTL/BICNTH [addr 0x08/0x09] registers). FEBE Error (PLCPFebeErr bit in PLCPSTAT register) is set if any FEBE-error value (0000 to 1000) is received. This condition is also counted in the FEBE Error Counter (FEBECNTL/FEBECNTH addr[0x0C/0x0D]). Invalid FEBE (InvalFEBE bit in PLCBSTAT) is set if any invalid FEBE value (1001 through 1111) is received; a value of 1111 also causes All Ones FEBE (AllOnesFEBE bit in PLCBSTAT) to be set. This value is used to indicate that the FEBE calculation is not supported at the far end of the circuit.

Bits 7,6, and 5 in PLCPSTAT register indicated the current state. All other bits are latched until read and then automatically cleared.

2.2.5 PLCP Transmit/Receive Synchronization

PLCP frames must be transmitted at the same rate as they are received. For DS1 and E1, long-term synchronization of the bit clock rates establish this. For DS3 and E3 rates, the payload data rate is independent of the line rate, and a separate timing/synchronization mechanism is required.

The DS3 and E3 PLCPs both have a 125 µs frame period. The reference clock for this frame is taken from the received signal, or alternatively from an external reference supplied to the 8 kHz clock input pin, 8KHZIn. In either case, the transmit circuit generates one PLCP frame per reference frame.

All PLCP frame structures are based on a 125 µs period; consequently, no stuffing is required to synchronize the transmit and receive segments.

Clock and control inputs consist of the following:

- An external 8 kHz reference input for the PLCP at E3 and DS3
- An external 8 kHz receiver output for the PLCP at E3 and DS3
- A one-second input to synchronize status collection timing in multiple-port applications
- A reset input

A one-second clock output is provided to allow synchronization of status collection for multiple CX2836x devices or for CX2836x devices and external line framers. When a single CX2836x is used, OneSecOut should be connected to OneSecIn. This timing output is derived from the external 8 kHz reference clock input on 8KHZIn.

2.2.6 Cell Screening

The cell processor provides two optional types of cell screening. The first type, idle cell rejection, prevents idle cells from being passed on. The second type, user traffic screening, compares incoming bits to the values in the receive cell header registers. Cells are rejected or accepted based on the bit patterns of their headers.

Idle cell rejection is enabled in bit 6 of the CVAL register (0x0C). If this bit is set to 1, all incoming cells that match the contents of the Receive Idle Cell Header Control registers, RXIDL1–4 (0x20–23), are rejected. Individual bits in the Receive Idle Cell Mask Control registers, IDLMSK1–4 (0x24–27), can be set to 1 or Don’t Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their value. If idle cell rejection is disabled, cells pass directly to user traffic screening.

User traffic cell screening is similar to idle cell screening in that the incoming cells are compared to the Receive Cell Header Control registers, RXHDR1–4 (0x18–1B). Individual bits in the Receive Cell Mask Control registers, RXMSK1–4 (0x1C–1F), can be set to 1 or Don’t Care, causing the corresponding bits of the incoming cell to be treated as matching, regardless of their values.

The RejHdr bit (bit 7) in the CVAL register (0x0C) determines whether matching cells are rejected or accepted; if it is set to 0, matching cells are accepted. If it is set to 1, matching cells are rejected. See Tables 2-10 and 2-11.

Table 2-10. Cell Screening—Matching

Receive Cell Mask Bit	Receive Cell Header Bit	Incoming Bit	Result
0	0	0	Match
0	0	1	Fail
0	1	0	Fail
0	1	1	Match
1	x	x	Match

Table 2-11. Cell Screening—Accept/Reject Cell

Cell	Reject Header	Result
Match	0	Accept Cell
Match	1	Reject Cell
Fail	0	Reject Cell
Fail	1	Accept Cell

2.2.7 Cell Scrambler

The ATM standard requires cell scrambling to ensure that only valid headers are found in the cell delineation process. Scrambling randomizes any repeated patterns or other data strings that could be mistaken for valid headers. The Cell Processor supports Self Synchronizing Scrambler (SSS) as defined by ITU-T I.432:

2.2.7.1 SSS Scrambling

SSS scrambling uses the polynomial $X^{43} + 1$ to scramble the payload, leaving the five header bytes untouched. It can be enabled in EnTxCellScr, bit 5, of the CGEN register (0x08).

Descrambling uses the same polynomial to recover the 48-byte cell payload. It can be enabled in EnRxCellScr, bit 4, of the CVAL register (0x0C). SSS scrambling runs at up to 45 Mbps.

2.3 UTOPIA Interface

The CX2836x uses the ATM Forum's UTOPIA interface as its host interface to communicate with the ATM layer device. This interface is UTOPIA Level 2-compliant and UTOPIA Level 1-compatible. In brief, these two specifications are described as follows:

1. UTOPIA Level 1: This is an 8- or 16-bit interface designed for data rates up to 200 Mbps. Both octet-level and cell-level handshaking are supported at a clock rate of 25 MHz. Octet-level handshaking requires the PHY to guarantee the acceptance of at least 4 bytes before it asserts the TxFull control line. In cell-level, it must guarantee the transfer of at least one entire 53-byte cell.
2. UTOPIA Level 2: This interface provides all the features of Level 1, plus several enhancements. Level 2 defines multi-PHY functionality, allowing up to 31 PHYs to interface to one ATM layer device. This interface uses either 8-bit or 16-bit wide data buses and cell-level handshaking. The 16-bit mode, which can run at 50 MHz, supports data rates up to 800 Mbps.

NOTE: PHY refers to a physical layer ATM port. Consequently, the CX2836x is a 12-PHY device.

2.3.1 UTOPIA Transmit and Receive FIFOs

The CX2836x's UTOPIA block has two sections, transmit and receive, each of which has a 4-cell FIFO buffer. ATM cell data is placed in the transmit FIFO buffers where it can then be passed to the ATM cell processing block. On the receive side of the UTOPIA interface, incoming cells are placed in the receive FIFO buffer until sent.

NOTE: By convention, data being transferred from the PHY to the ATM layer is labeled received data, while data from the ATM layer to the PHY is called transmitted data.

2.3.2 UTOPIA 8-bit and 16-bit Bus Widths

The CX2836x has two bus width options, 8-bit or 16-bit, which are selected in BusWidth, bit 2, of the MODE register (0x0202). The protocols and timing are the same in both modes, except that 8-bit mode uses only the lower half of the data bus (UTxData[7:0] and URxData[7:0]) and parity is only generated or checked over those bits.

In 8-bit mode, each ATM cell consists of 53 bytes, as listed inTable 2-12. The first five bytes are used for header information. The remaining bytes are used for payload.

Table 2-12. Cell Format for 8-bit Mode

Bit 7	...	Bit 0
Header 1		
Header 2		
Header 3		
Header 4		
UDF1 (HEC) (byte 5)		
Payload 1		
...		
Payload 48		

In 16-bit mode, the cells consists of 54 bytes, as listed in Table 2-13. The first five bytes contain header information. The sixth byte, UDF2, is required to maintain alignment but is not read by the CX2836x. The remaining bytes are used for payload.

Table 2-13. Cell Format for 16-bit Mode

Bit 15	...	Bit 8	Bit7	...	Bit 0
Header 1			Header 2		
Header 3			Header 4		
UDF1 (HEC) (byte 5)			UDF2 (0) (byte 6)		
Payload 1			Payload 2		
...			...		
Payload 47			Payload 48		

NOTE: Normally, the HEC is calculated by the PHY and put in byte 5, UDF1. However, setting bit 7 of the CGEN register (0x08) to 1 disables HEC calculation. In this case, data inserted by the ATM layer into byte 5 is transmitted by the PHY.

2.3.3 UTOPIA Parity

The CX2836x supports even and odd parity, which is selected by OddEven, bit 2, in the UTOP1 register (0x0D). The parity on received data is generated for either 8 bits or 16 bits, according to the selected bus width in bit 0 of the MODE register (0x0202). The result is output on URxPrty (pin V14).

Likewise, the parity on transmitted data is checked for either 8 bits or 16 bits, according to the selected bus width. The calculated result should match the bit present on UTxPrty (pin W11). If it does not match, a parity error has occurred. This error can be observed either in the ParErr bit (bit 7) in the TXCELL register (0x2E) or in the ParErrInt bit (bit 7) in the TXCELLINT register (0x2C). Systems that do not use parity should disable the generation of interrupts caused by parity errors by writing bit 7 of the ENCELLT register (0x28) to 0.

2.3.4 UTOPIA Multi-PHY Operation

The CX2836x supports multi-PHY operation as described in the UTOPIA Level specification (af-phy-0039.000, see http://www.atmforum.com). Three primary functions are involved in this operation: polling, selection, and data transfer. These functions are basically the same for both the transmit and receive sides of the UTOPIA bus. The following example describes the transmit functions.

The ATM layer UTOPIA controller polls the connected PHY ports by transmitting the port addresses on the UTxAddr lines. If a port is ready to transfer data, it asserts UTxCLAV. The controller determines which port is to transfer data and selects that port by transmitting its address. The controller then asserts UTxEnb* to allow the PHY to transfer data on the UTxData lines. UTxEnb* is deasserted when the transfer is completed. Polling can continue during the data transfer process but not during port selection. It operates independently of the state of UTxEnb*.

To pause the data transfer, UTxEnb* can be deasserted. To continue the transfer, the controller must reselect the port by transmitting its address one clock cycle before asserting UTxEnb*. The controller must ensure that the cell transfer from this port has been completed, to avoid a start-of-cell error.

The CX2836x has a UTOPIA receiver output disable feature which allows the user to set up redundant or back-up PHYs with the same UTOPIA address on the same UTOPIA bus. In this setup, both PHYs' transmitters are enabled, sending out identical data streams. Both PHYs' receivers are enabled, but only one is transferring data to the ATM device. The receiver output is disabled in the backup PHY by writing the UtopDis, bit 5, in the UTOP2 register (0x0E) to a logical 1. This disable places five of the backup PHY's signals, URxData, URxPrty, URxSOC, URxCLAV, and UTxCLAV, in a high-impedance state, preventing data and control signals from being passed to the ATM layer device. The disabled receiver flushes its FIFO buffers at the same rate as the enabled one, but all data it has received, except the last four cells, is lost. If the primary PHY device encounters an unacceptable error rate, software quickly enables the backup PHY and disables the primary PHY, reducing cell loss in the transition.

NOTE: To facilitate multi-PHY operation, the CX2836x assigns a different address to each of its twelve ports by default.

2.3.5 UTOPIA Addressing

The UTOPIA address for each port is stored in bits 0–4 of the UTOP2 register (0x0E). The default for this value is the port number. For example, the UTOP2 register for port 4 (0x10E [with the offset]) defaults to 04 hex. However, the value can be changed to any value from 00–1E hex by programming the register to accommodate multiple devices on the same UTOPIA bus. The value 1F hex is reserved for the null address. The UTOPIA address should be changed only when the device or port is in the reset state.

UTOPIA bus conflicts can occur if different CX2836x ports are programmed with the same multi-PHY address. Under these circumstances, a bus conflict may occur if data is being transferred through these ports at the same time. A bus conflict generates an error in BusCnflct (bit 2) of the TXCELL register (0x2E). During a data collision, data will be transmitted according to port priority the lowest port number has highest priority.

2.3.6 Handshaking

The CX2836x provides both cell- and octet-level handshaking on its UTOPIA interface (only cell-level is used in Level 2). Octet-level sends and receives four octets at a time, while cell-level sends and receives a full cell at a time, depending on FIFO buffer size and availability. In octet-level handshaking, UTxCLAV is an active low, FIFO full indicator. In cell-level, it is an active high, cell buffer available indicator. These two options are selectable in the Handshake bit, bit 1, of the MODE register (0x0202).

UTxCLAV (transmit cell available): The CX2836x implementation of UTxCLAV is designed to provide a “look ahead” feature to allow the ATM layer to anticipate when the FIFO buffers are full. The UTOPIA layer polls the port to determine if that port has room for a cell. In response, the port asserts (logic1) the UTxCLAV line if it has room and deasserts (0) the line if it does not have room. The threshold is controlled by bits [1:0] in the UTOP1 register and, UTOP1[TxFill]. For maximum performance when using a standard ATM layer device, Mindspeed recommends leaving these set to 0s.

0 0 The UTxCLAV is asserted if the UTOPIA FIFO buffer can accept at least one more complete cell

0 1 The UTxCLAV line is asserted if the UTOPIA FIFO buffer has room for at least two more cells.

0 1 The UTxCLAV line is asserted if the UTOPIA FIFO buffer has room for at least three more cells.

1 1 The UTxCLAV line is asserted if the UTOPIA FIFO buffer can accept at least three more cells.

2.4 Interfacing

2.4.1 Microprocessor Interface

The microprocessor interface transfers control and status information in 8-bit data transfers between the external microprocessor and CX2836x by means of write and read access to internal registers. This interface allows the microprocessor to configure the CX2836x by writing various control registers. These control registers can also be read for configuration confirmation. This interface also provides the ability to read the device's current condition via its status registers and counters. Summary status is available for rapid interrupt identification.

The MPU interface consists of the following pins: MCs*, MOE*, MR/W*, MData[7:0], MAddr[13:0], MINTR*, MReset*, 8KHZIn, OneSecIn, OneSecOut, and MCLK. A detailed description of the MPU pins is provided in Table 1-1.

2.4.1.1 Resets

Software Reset

There are four register controlled reset functions, two at the device level and two at the port level. The two levels allow a user to reset either the entire CX2836x with one command or only a port within the device. The two logic resets allow the user to keep the device or port in a reset state while the control registers are being programmed. When the reset bit is de-asserted, all changes to the registers take place simultaneously.

At the device level, the register bit GLOB[MasterReset] restarts all device logic functions and sets the control and status registers to their default values. The GLOB[DevLogReset] bit restarts cell delineator device logic functions but leaves all control registers unaffected. Table 2-14 summarizes the effect of each reset source.

At the port level, the PMODE[PrtMstRst] bit restarts cell delineator port logic functions and sets the cell delineator port registers to their default values. The PORTn[PortReset] bit restarts cell delineator functions but leaves the control registers unaffected.

Hardware Reset

MReset* is an active low, level activated, synchronous reset pin. While MReset* is active, RxCKI and TxCKI on all ports must be present for a minimum of 30 clock cycles. During MReset* the system side outputs are high impedance, 3-state. After MReset*, all ports are disabled and all control registers and counters are set to their default values.

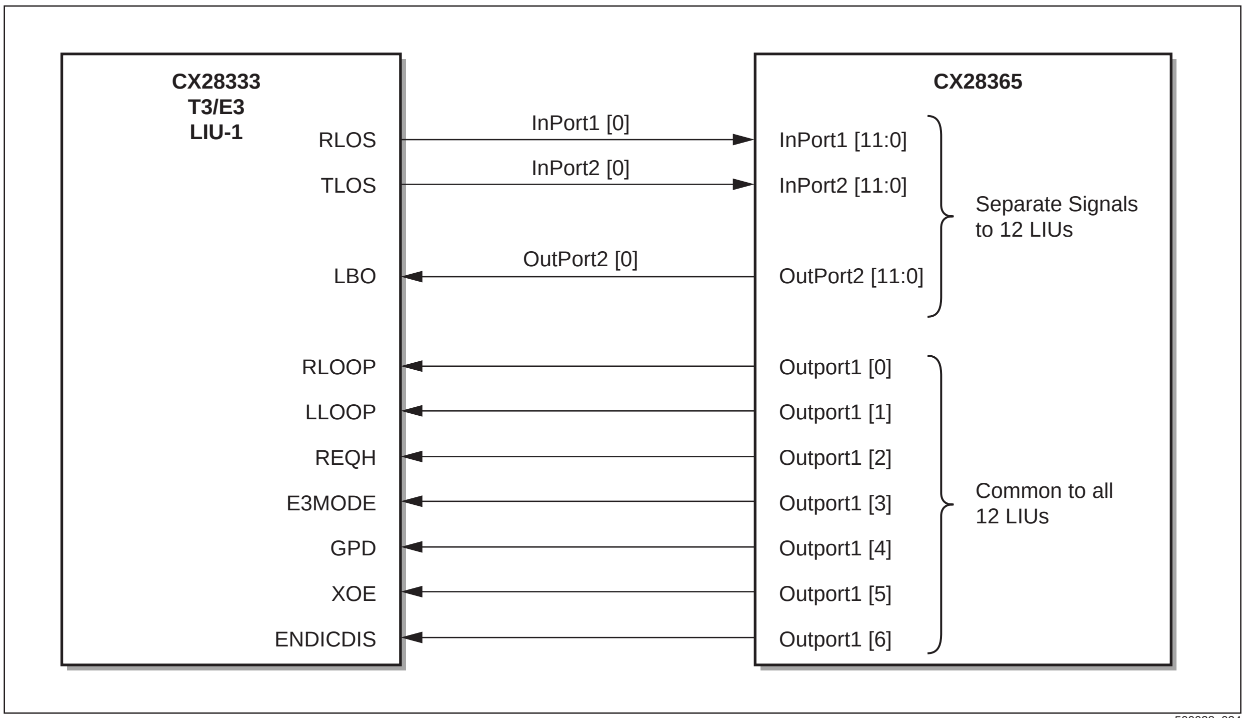
Table 2-14. Reset Control

Reset	Cell Delineator Logic	Set Cell Delineator Register Defaults	Framer Logic	Set Framer Register Defaults	Set Global Register Defaults
MReset* pin	X	X	X	X	X
GLOB[MasterReset]	X	X	X	X	X
GLOB[DevLogReset]	X	—	—	—	—
PMODE[PrtMstRst]	X	X	—	—	—
PORTn[PortReset]	X	—	—	—	—

2.4.2 Input/Output Ports

The CX2836x provides 48 multi-purpose input/output pins arranged as four 12-bit ports. InPort1 and InPort2 are 12-bit bidirectional ports and can be used as general purpose inputs or as framer RxSync and TxSync outputs. OutPort1 and Outport2 are 12-bit output ports. OutPort1 can be used as general purpose output pins or as framer or cell processor status outputs. OutPort2 can be used as general purpose output pins or as chip select outputs between external framers and the cell processor when the internal framer is bypassed. Figure 2-18 illustrates an application example using the Input/Output ports to control and monitor external LIUs. These four ports are 12-bits wide regardless of the device (CX28365, CX28366, or CX28364). RxSync and TxSync, however, are applicable only for ports which exist.

Figure 2-18. Input/Output Ports Application Example (LIU Control)



2.4.3 Counters

There are counters in the cell delineator block that record events within the cell delineator. Two types of events are recorded: error events, such as section BIP. errors, and transmission events, such as transmitted ATM cells.

Counters comprised of more than one register must be accessed by reading the least significant byte (LSB) first. This guarantees that the value contained in each component register accurately reflects the composite counter value at the time the LSB was read, because the counter may be updated while the component registers are being read.

Each counter is large enough to accommodate the maximum number of events that may occur within a one-second interval. The counters are cleared after being read. Therefore, if the counters are read every second, the application will receive an accurate recording of all events.

2.4.4 One-Second Latching

The CX2836x's implementation of one-second latching ensures the integrity of the statistics being gathered by network management software. Internal statistics counters can be latched at one-second intervals, which are synchronized to the OneSecIn pin. Therefore, the data read from the statistics counters represents the same one second of real-time data, independent of network management software timing.

The CX2836x implements one-second latching for both status signals and counter values. When the GLOB[EnStatLat] bit is written to a logical 1, a read from any status register returns the state of the device at the time of the previous OneSecIn pin assertion. When the GLOB[EnCntrLat] bit is written to a logical 1, a read from any counter returns the state of the device at the time of the previous OneSecIn pin assertion. Every second, the counter is read, moved to the latch, and the counter is cleared. The latch is cleared when read.

OneSecIn is intended to be asserted at one-second intervals. This can be achieved by connecting the OneSecIn pin to the OneSecOut pin. The OneSecOut signal is derived from the 8kHzIn pin. This signal is asserted for one 8kHzIn period, every 8,000 8kHzIn periods. If 8kHzIn is being driven by an 8 kHz clock, the OneSecOut signal is asserted every second.

NOTE: When latching is disabled and a counter is wider than one byte, the LSB should be read first to retain the values of the other bytes for a subsequent read.

2.4.5 External Framer Interrupts and Chip Selects

The CX2836x can interface directly with a maximum of twelve external framers, reducing the amount of external logic and address decode circuitry. Its twelve interrupt inputs (MINTR*[0:11]) and twelve chip select outputs (LCS*[0:11]) provide this function. Furthermore, the user can program the LCS* pins in IOMODE[CsPol] to be either active high or active low to match the framer's chip select input polarity.

When an external framer generates an interrupt, it asserts the associated LIntR* pin. Each LIntR* pin is mapped to a corresponding ExInt bit in the appropriate Port's SUMINT register and the interrupt is forwarded, as described in Section 2.4.6. An LCS* pin is asserted when an address within its range appears on the microprocessor address bus and the MCS* pin is asserted. This output selects the external framer being addressed. The framer's address decoding logic further determines which specific address is being accessed. Table 3-8 lists the LCS* pins and their address ranges.

2.4.6 Interrupts

The CX2836x's interrupt indications can be classified as either single- or dual-event; a single-event interrupt is triggered by a status assertion; a dual-event interrupt is triggered by either a status assertion or deassertion. Both types of interrupts are further described in the following examples.

Single-event interrupt: When a parity error occurs on the UTOPIA transmit data bus, an interrupt is generated on TXCELLINT[ParErrInt]. This bit is cleared when read.

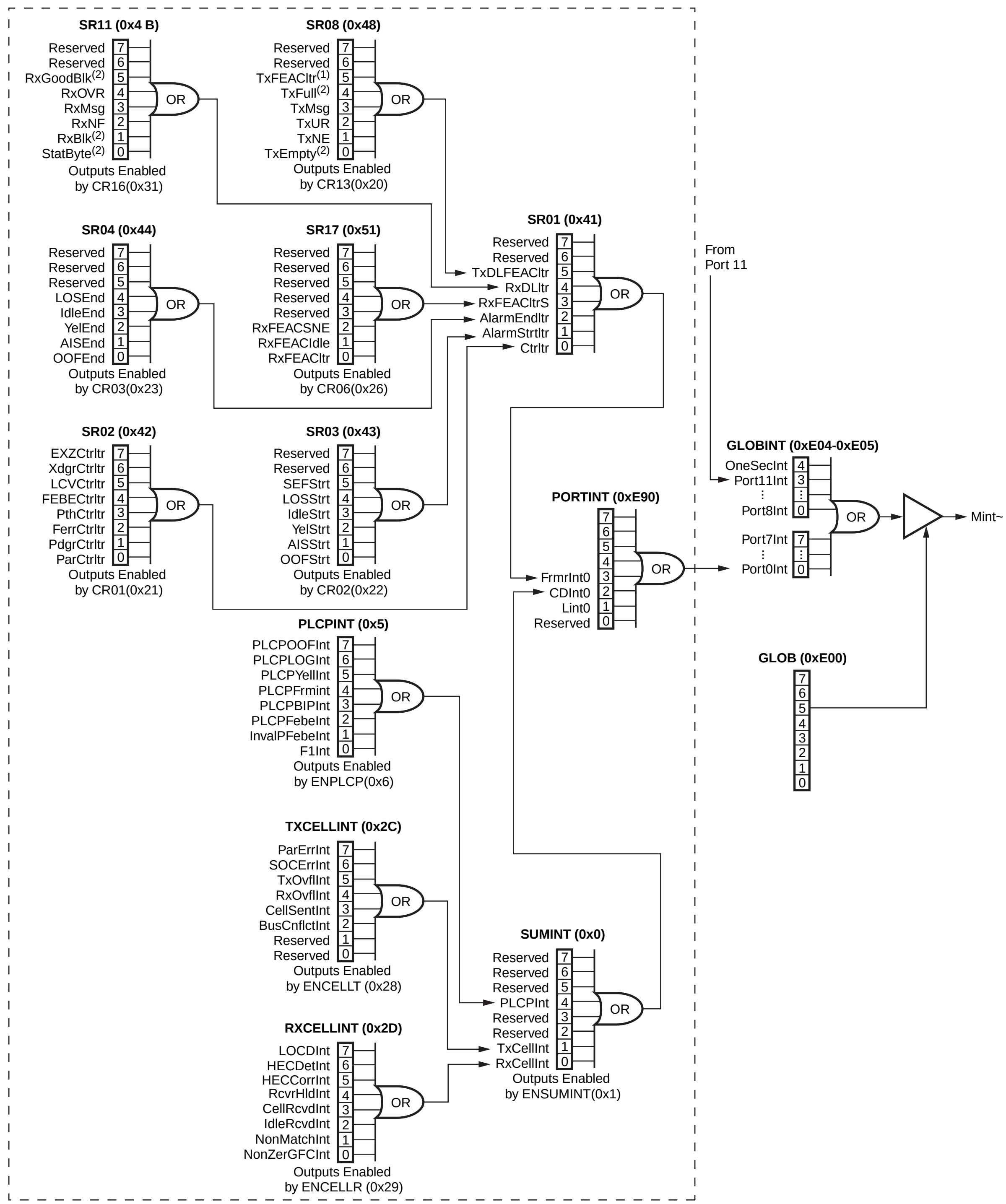
Dual-event interrupt: When LOCD occurs, TXCELLINT[LOCD] is set to 1. This bit is cleared when the register is read. Once cell delineation is recovered, TXCELLINT[LOCD] is set to 1 again, generating another interrupt.

All interrupt bits have a corresponding enable bit. This allows software to disable or mask interrupts as required.

NOTE: The interrupt bits in the Cell Delineator register group do not latch status unless the respective interrupts are enabled. The affected registers are SUMINT (offset 0x00), TXCELLINT (offset 0x2C), and RCXCELLINT (offset 0x2D).

2.4.6.1 Interrupt Routing

Figure 2-19. Input/Output Ports Application Example (Framer and LIU Control)



NOTE(S):

(1) TxFEACltr bit is enabled by TxFEACIE (bit 6) in CR06 (0x26).

(2) These bits are status bits only. No interrupt is linked to them.

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The CX2836x uses four levels of interrupt indications as illustrated in Figure 2-19. The first level consists of interrupts from the 12 ports plus the one-second interrupt as indicated in the Global Interrupt Status registers [GLOBINTL and GLOBINTH]. The second level indicates interrupts pending in the framer, cell delineator, or external framer of the interrupting port.

If there are interrupts pending in the cell delineator, the third level consists of receive, transmit or PLCP interrupt indications, which correspond to specific events on a specific port. Finally the fourth level indicates the interrupting source in the PLCP, TXCELLINT, and RXCELLINT area respectively.

If there are interrupts pending in the framer area, the Interrupt Status register (SR01 addr; 0x41) which represents the third level of interrupt indication, identifies the reason for the interrupt assertion. The six possible sources of interrupt are from TxDLFEACItr, RxDLltr, RxFEACltrS, AlarmEndItr, AlarmStrtItr, and Ctrltr. Finally, the fourth level indicates the interrupting source in SR02, SR03, SR04, SR08, SR11, and SR17, respectively.

2.5 Loopback

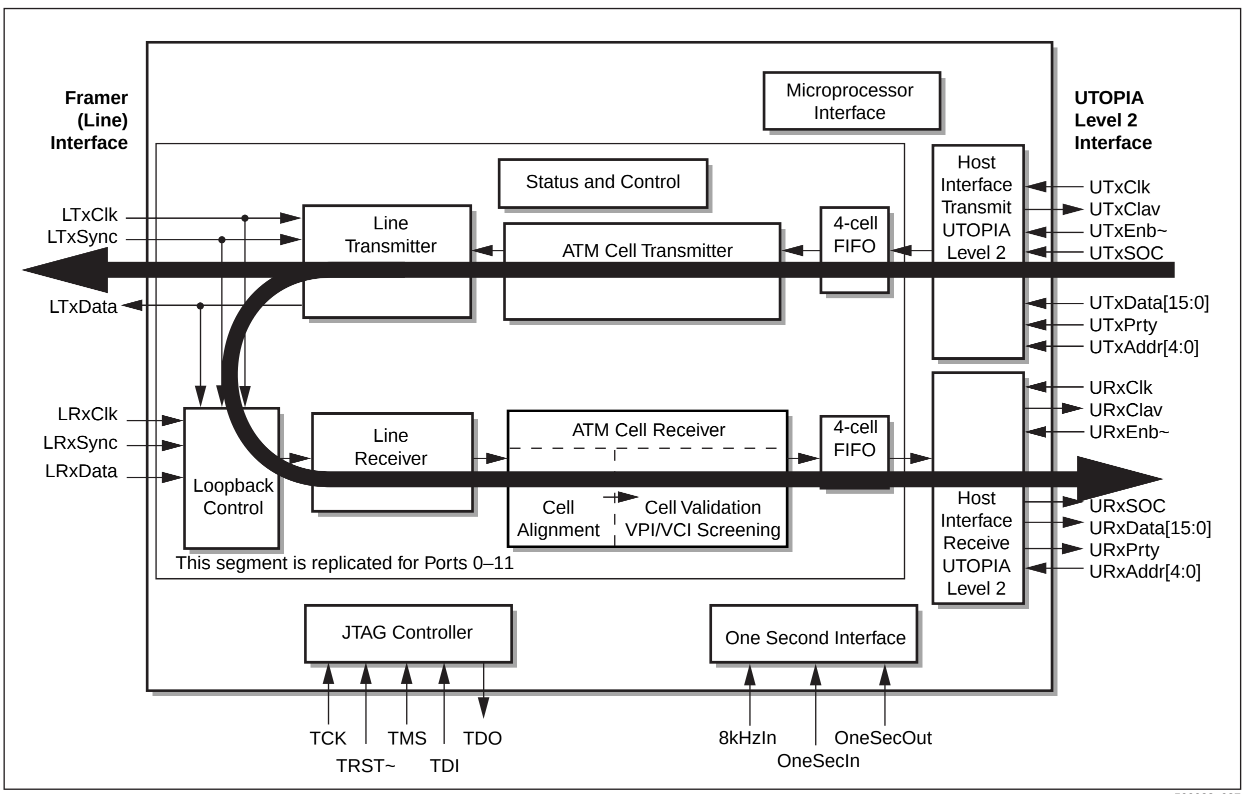
There are two source loopback mechanisms in the CX2836x device, one in the cell delineators and one in the framers.

2.5.1 Cell Delineator Source Loopback

For the Cell Delineator loopback, the Source loopback checks that the host (the ATM layer) is communicating with the PHY. It is enabled and disabled in bit 5 of the PMODE register (0x04). When the Source loopback is enabled for a given port, all data transmitted by the CX2836x on that port is also looped back through the Receive Line interface. Data from the Framer interface is ignored.

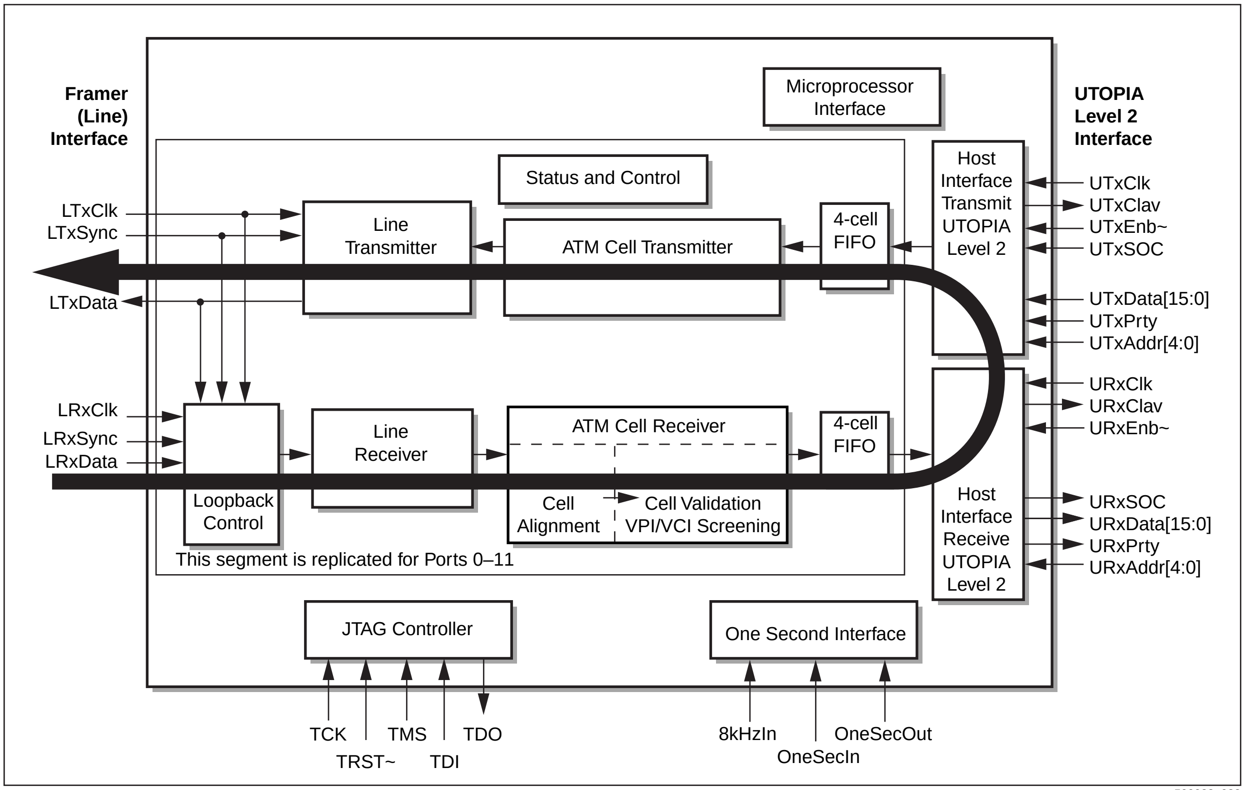
NOTE: LTxClk, LRxClk, LTxSync, and LRxSync must be present for the Loopback mode to function properly for a given port.

Figure 2-20. Source Loopback Diagram



2.5.2 Far-End Line Loopback

Figure 2-21. Far-End Line Loopback Diagram



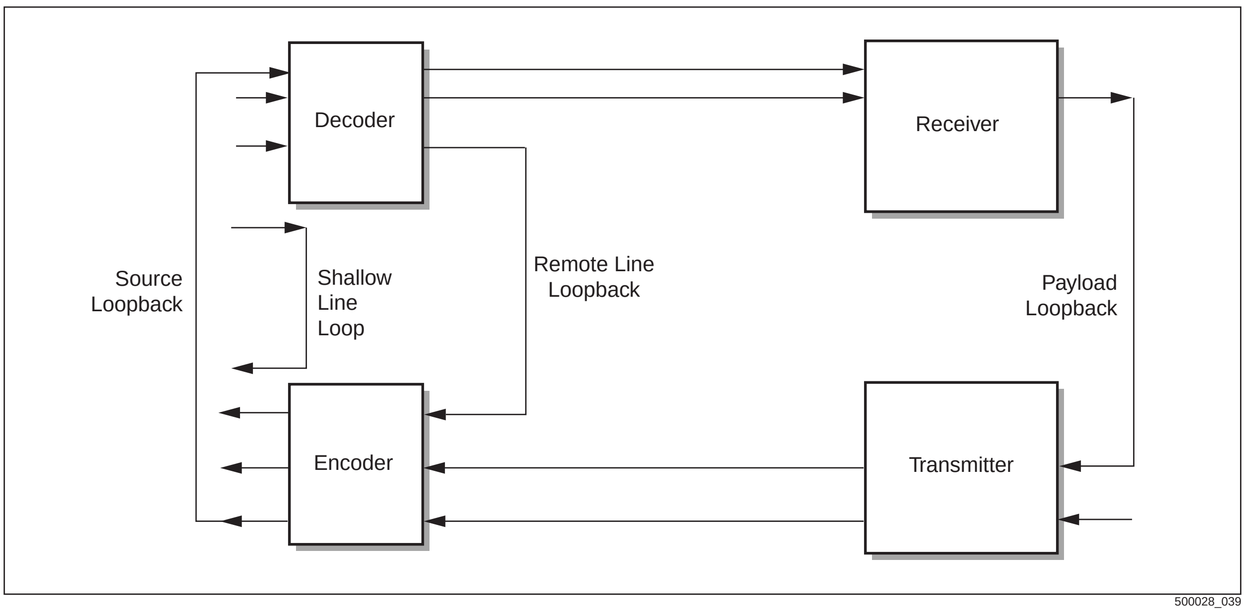
When the Far-End Line Loopback control bit is set, PMODE[FELNLOOP], a UTOPIA loopback is enabled. Received cells are processed normally up to the UTOPIA block but are sent to the UTOPIA transmit block rather than output. Cells from the UTOPIA transmit bus are ignored.

NOTE: When configuring the device for CD far-end loopback, continuous Start of Cell (SOC) errors occur. These errors are incorrect because the UTOPIA interface is not being used. The SOC interrupts must be disabled during the CD far-end loopback. Clear EnSOCErrInt, bit 6, in the ENCELLT control register in the Cell Delineator group.

2.5.3 Framer Loopbacks

The framer provides a complete set of loopbacks for diagnostics, maintenance, and troubleshooting of each channel. All loopbacks perform clock and data switching, if necessary. The activation and deactivation of a specific loopback are done through programmable control bits. Because activation and deactivation of a loopback causes internal circuits to switch between clocks, after writing to a loopback control bit, the microprocessor should not access any of the device registers (read or write) for the 20 slowest clock cycles.

Figure 2-22. Loopback Types



2.5.3.1 Shallow Line Loopback

The Shallow Line loopback loops the receiver inputs before B3ZS/HDB3 decoding back to the line through the transmitter outputs. The Shallow Line loopback provides LCV transparency, i.e., LCVs are transmitted exactly as received. The receiver data path is not affected by activation of this loopback, and the received data is still present on the RxDATO pin (it can be replaced by an all-1s or AIS stream by programming RxAll1 or RxAIS bits in the Feature5 Control register).

The entire transmitter circuit works with the receiver clock (RXCKI); therefore, the system interface clock outputs (TxGCKO and TEXTCKO) cannot be related to TxCKI in this mode and are inactive. TxSYNC is also inactive. Error insertion on the looped framer is not valid.

When the TxLOS bit in Feature2 Control register is set, an all-0s signal is output on the transmitter and overrides the content of the frame looped from the receiver.

This loopback is activated by setting LineLp bit in the Mode Control register.

When the receiver and the transmitter are programmed to be in shallow line loopback, and the line code is set to unipolar (NRZMod bit in Feature Control register is set), the

TxNEGO output pin is forced to 0. Therefore, TxNEGO does not reflect RxNEGI in unipolar mode.

NOTE: The Shallow Line loopback and Source loopback cannot be operated simultaneously.

2.5.3.2 Remote Line Loopback

The remote line loopback loops receive data after B3ZS/HDB3 decoding and before frame recovery back to the line. The decoder output is connected to transmitter B3ZS/HDB3 encoder input. The remote line loopback provides some LCV error correction due to the path through the decoder and the encoder. Activation of this loopback does not affect the receiver data path. The received data is still present on RxDATO pin (it can be replaced by an all-1s or AIS stream by programming the RxAll1 or RxAIS bits in the Feature5 Control register). Error insertion on the looped frame is not valid.

The entire transmitter circuit works with the receiver clock (RxCKI). System interface clock outputs (TxGCKO and TEXTCKO) cannot be related to TxCKI in this mode and are inactive. TxSYNC is also inactive.

Overwriting the looped frame by an AIS pattern and transmission of AIS to the line is enabled by programming TxAlm bits in the Mode Control register. However, the generated pattern is not aligned to the looped frame boundaries and is initiated and terminated once TxAlm bits change. Idle pattern and RAI transmission due to TxAlm bits are not enabled during this loopback.

When TxLos bit in Feature2 Control register is set, an all-0s signal is output to the transmitter and overrides the content of the frame looped from the receiver.

This loopback is activated by setting RlineLp bit in the Feature3 Control register.

2.5.3.3 Payload Loopback

The payload loopback loops the received frame from the frame recovery circuit output through the transmitter frame generation circuit input back to the line. The transmitter is programmed through the Transmit Overhead Insertion1&2 registers to an internal generation of the Overhead bits, i.e., nothing is inserted via TxDATI or TEXTI pins. The only exception is that justification control and Stuff Opportunity bits should be selected to be driven with the data stream, enabling the transmitter to receive them from the receiver with the payload. The entire transmitter circuit works with the receiver clock (RxCKI). The system interface clock outputs (TxGCKO and TEXTCKO) cannot be related to TxCKI in this mode and are inactive. The transmitter circuit gets the frame alignment signal from the receiver with the data that is looped. TxSYNC is inactive.

The payload loopback provides framing bits and some LCV error correction due to the path through the decoder, frame recovery, frame generation, and encoder. Activation of this loopback does not affect the receiver data path. The received data is present on RxDATO pin (it can be replaced by an all-1s or AIS stream by programming RxAll1 or RxAIS bits in Feature5 Control register). Error insertion on the looped frame is valid in this mode. Overwriting the looped frame by an AIS pattern and transmission of AIS to the line is enabled by programming TxAlm bits in the Mode Control register. The generated pattern is aligned to the looped frame boundaries, and initiated and terminated similarly to normal operation (i.e., when not in loopback). Idle pattern and RAI transmission due to TxAlm bits are also valid during this loopback.

NOTE: The transmitter does not generate an AIS or Idle pattern independently due to AIS or Idle detection in the receiver during this loopback. The microprocessor must program the transmitter to generate an AIS/Idle according to the receiver detection.

When TxLOS bit in the Feature2 Control register is set, an all-0s signal is output on the transmitter and overrides the content of the frame looped from the receiver.

This loopback is activated by setting PayldLp bit in the Feature3 Control register.

Framer Source Loopback

The source loopback loops the transmitter encoder outputs back to the system through the receiver decoder inputs.

The transmitter data path is not affected by activation of this loopback and the transmitted data is still present on the TxPOSO and TxNEGO pins. The transmitted frame can be overwritten by an AIS pattern by setting TxAlm bits in the Mode Control register to AIS control state. Doing this affects only TxPOSO and TxNEGO and not the looped frame. Therefore, the AIS pattern is not looped by the transmitter. The same behavior applies to TxLOS bit, i.e., when TxLOS is set during source loopback, the TxPOSO and TxNEGO are forced to zero, and the looped frame is unaffected. When an AIS or LOS pattern is generated, error insertion is invalid. Idle pattern and RAI are not supported in this mode like AIS, i.e., they can overwrite the looped frame by setting TxAlm bits as in normal operation.

Setting SourceLp bit in the Mode Control register activates this loopback.

NOTE: The shallow line loopback and source loopback cannot be operated simultaneously.

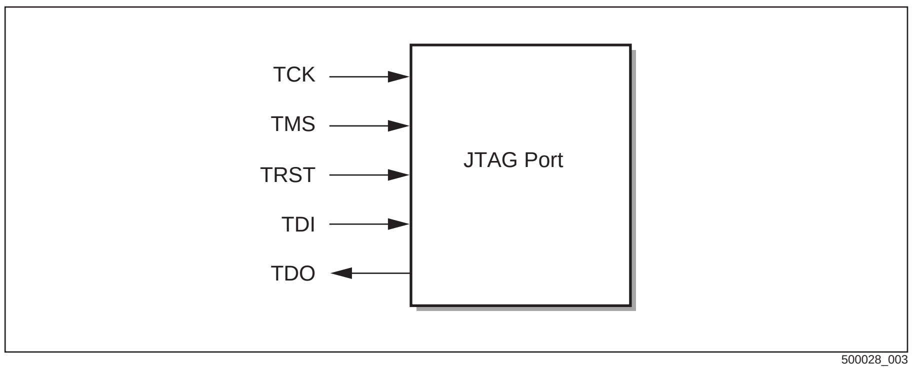
2.6 Joint Test Access Group (JTAG) Interface

The CX2836x incorporates printed circuit board testability circuits in compliance with IEEE Standard *P1149.1a–1993*, IEEE Standard Test Access Port and Boundary–Scan Architecture, commonly known as JTAG (Joint Test Action Group).

The JTAG includes a Test Access Port (TAP) and several data registers. The TAP provides a standard interface through which instructions and test data are communicated, see Figure 2-23. A Boundary Scan Description Language (BSDL) file for the CX28344 is available from Mindspeed upon request.

The TAP consists of TDI, TCK, TMS, TDO, and TRST* pins. The TRST* control bit must be manually operated to take the JTAG port in and out of reset.

Figure 2-23. TAP Diagram



2.6.1 Instructions

In addition to the required BYPASS, SAMPLE/PRELOAD, and EXTEST instructions, an IDCODE instruction is supported. Table 2-15 lists the JTAG instructions and their codes.

Table 2-15. JTAG Instruction Codes

Instruction	Code
EXTEST	000
SAMPLE/PRELOAD	001
BYPASS	111
IDCODE	010
HIGHZ	100

2.6.2 Device Identification Register

The JTAG ID register consists of a 4-bit version, 16-bit part number, and 11-bit manufacturer number (see Table 2-16).

Table 2-16. CX28394 Device Identification JTAG Register

<table>
<tr><th></th><th colspan="4">Version(1)</th><th colspan="16">Part Number</th><th colspan="12">Manufacturer ID</th></tr>
<tr><td></td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>CX28365</td><td colspan="4">0x02</td><td colspan="16">0x8365</td><td colspan="11">0X013</td><td></td></tr>
<tr><td>CX28366</td><td colspan="4">0x02</td><td colspan="16">0x8366</td><td colspan="11">0x013</td><td></td></tr>
<tr><td>CX28364</td><td colspan="4">0x02</td><td colspan="16">0x8364</td><td colspan="11">0x013</td><td></td></tr>
<tr><td></td><td colspan="4">4 bits</td><td colspan="16">16 bits</td><td colspan="11">11 bits</td><td></td></tr>
</table>

TDO

FOOTNOTE:
(1) Consult factory for current version number.
Device revision A: Version = 0001
Device revision B: Version = 0010

3.0 Registers

The CX2836x registers control and observe the device's operations. Registers are of three types: Control, Status, and Counters. Control registers are used for configuration. Status registers report events such as alarms and errors. Counters count events and performance errors in the received signal and data path. Counters are automatically cleared when read.

Some Control registers can be modified whether a port is disabled or enabled (dynamic modification). Some Control registers can only be modified when a port is disabled (static modification). When a register with mixed bits (both dynamic and static bits in the same register) is modified while a port is enabled, the software may modify the dynamic bits, but must leave the static bits unchanged.

Data Link static (DL-static) bits can be modified dynamically only if the internal data link mechanism is disabled:

- Rx bits: when the RxDLEn field in the Receive Data Link Control register is cleared
- Tx bits: when the DLMod fields in the Transmit Overhead Insertion Control register is set, so that HDLC and FIFO mechanism is disabled and does not affect the DL channel

3.1 Register Map

The register map contains the following groups of register addresses:

- Cell Delineator (CD) registers (Tables 3-1 and 3-2)
- PLCP Registers (Tables 3-3 and 3-4)
- Framer Registers (Tables 3-5 and 3-7)
- Common Registers (Table 3-7)
- External Chip Select Addresses (Table 3-8)

The CD, PLCP, and framer register groups each include sets of registers which are replicated for each of twelve ports. To determine the exact address of a specific register, add the register group base address to the register offset address (all numbers are hexadecimal). For example:

For the Cell Delineator Port 3, IOMODE register (from Table 3-1 and Table Table 3-2):

> 0x00C0 (port 3 base address) + 0x05 (IOMODE register offset address) = 0x00C5 (exact register address)

Common Registers (in Table 3-7) are not associated with a specific port and are considered global. The External Chip Select addresses are defined in Table 3-8 and are applicable if OUTPORT2 pins are configured to output Line Chip Select signals. LCS*[n] is activated when the address bus, MAddr[13:0], is within the address range specified in Table 3-8. All registers are 8 bits wide. All control registers can be read to verify contents.

NOTE: Control bits that do not have a documented function are reserved and must be written to a logical 0.

Table 3-1. Cell Delineator Register Map

Base Address	Register Group
0x0000	Cell Delineator Port 0 Control and Status
0x0040	Cell Delineator Port 1 Control and Status
0x0080	Cell Delineator Port 2 Control and Status
0x00C0	Cell Delineator Port 3 Control and Status
0x0100	Cell Delineator Port 4 Control and Status
0x0140	Cell Delineator Port 5 Control and Status
0x0180	Cell Delineator Port 6 Control and Status
0x01C0	Cell Delineator Port 7 Control and Status
0x0200	Cell Delineator Port 8 Control and Status
0x0240	Cell Delineator Port 9 Control and Status
0x0280	Cell Delineator Port 10 Control and Status
0x02C0	Cell Delineator Port 11 Control and Status

The registers listed in Table 3-2 are replicated for each port.

Table 3-2. Cell Delineator Control and Status Registers (1 of 3)

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x00	SUMINT	R	—	Summary Interrupt Status Register	3-27
0x01	ENSUMINT	R/W	—	Summary Interrupt Control Register	3-27
0x02	—	—	—	Reserved, set to a logic 0	—
0x03	—	—	—	Reserved, set to a logic 0	—
0x04	PMODE	R/W	—	Port Mode Control Register	3-11
0x05	IOMODE	R/W	—	Input/Output Mode Control Register	3-12
0x06	—	—	—	Reserved. Set to a logic 0	—
0x07	—	—	—	Reserved. Set to a logic 0	—
0x08	CGEN	R/W	—	Cell Generation Control Register	3-13
0x09	HDRFIELD	R/W	—	Header Field Control Register	3-13
0x0A	IDLPAY	R/W	—	Transmit Idle Cell Payload Control Register	3-14
0x0B	ERRPAT	R/W	—	Error Pattern Control Register	3-14
0x0C	CVAL	R/W	—	Cell Validation Control Register	3-18

Table 3-2. Cell Delineator Control and Status Registers (2 of 3)

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x0D	UTOP1	R/W	—	UTOPIA Control Register 1	3-25
0x0E	UTOP2	R/W	—	UTOPIA Control Register 2	3-25
0x0F	RXUDF2	R/W	—	Receive UTOPIA UDF2 Octet Register	3-26
0x10	TXHDR1	R/W	—	Transmit Cell Header Control Register 1	3-14
0x11	TXHDR2	R/W	—	Transmit Cell Header Control Register 2	3-15
0x12	TXHDR3	R/W	—	Transmit Cell Header Control Register 3	3-15
0x13	TXHDR4	R/W	—	Transmit Cell Header Control Register 4	3-15
0x14	TXIDL1	R/W	—	Transmit Idle Cell Header Control Register 1	3-16
0x15	TXIDL2	R/W	—	Transmit Idle Cell Header Control Register 2	3-16
0x16	TXIDL3	R/W	—	Transmit Idle Cell Header Control Register 3	3-16
0x17	TXIDL4	R/W	—	Transmit Idle Cell Header Control Register 4	3-17
0x18	RXHDR1	R/W	—	Receive Cell Header Control Register 1	3-19
0x19	RXHDR2	R/W	—	Receive Cell Header Control Register 2	3-19
0x1A	RXHDR3	R/W	—	Receive Cell Header Control Register 3	3-20
0x1B	RXHDR4	R/W	—	Receive Cell Header Control Register 4	3-20
0x1C	RXMSK1	R/W	—	Receive Cell Mask Control Register 1	3-20
0x1D	RXMSK2	R/W	—	Receive Cell Mask Control Register 2	3-21
0x1E	RXMSK3	R/W	—	Receive Cell Mask Control Register 3	3-21
0x1F	RXMSK4	R/W	—	Receive Cell Mask Control Register 4	3-21
0x20	RXIDL1	R/W	—	Receive Idle Cell Header Control Register 1	3-22
0x21	RXIDL2	R/W	—	Receive Idle Cell Header Control Register 2	3-22
0x22	RXIDL3	R/W	—	Receive Idle Cell Header Control Register 3	3-22
0x23	RXIDL4	R/W	—	Receive Idle Cell Header Control Register 4	3-23
0x24	IDLMSK1	R/W	—	Receive Idle Cell Mask Control Register 1	3-23
0x25	IDLMSK2	R/W	—	Receive Idle Cell Mask Control Register 2	3-23
0x26	IDLMSK3	R/W	—	Receive Idle Cell Mask Control Register 3	3-24
0x27	IDLMSK4	R/W	—	Receive Idle Cell Mask Control Register 4	3-24
0x28	ENCELLT	R/W	—	Transmit Cell Interrupt Control Register	3-28
0x29	ENCELLR	R/W	—	Receive Cell Interrupt Control Register	3-28
0x2A	—	—	—	Reserved, set to a logic 0	—
0x2B	—	—	—	Reserved, set to a logic 0	—
0x2C	TXCELLINT	R	—	Transmit Cell Interrupt Indication Control Register	3-29
0x2D	RXCELLINT	R	—	Receive Cell Interrupt Indication Control Register	3-29
0x2E	TXCELL	R/W	√(1)	Transmit Cell Status Control Register	3-30

Table 3-2. Cell Delineator Control and Status Registers (3 of 3)

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x2F	RXCELL	R	√(1)	Receive Cell Status Control Register	3-31
0x30	IDLECNTL	R	√(2)	Receive idle cell counter (low byte)	3-32
0x31	IDLECNTM	R	√(2)	Receive idle cell counter (middle byte)	3-32
0x32	IDLECNTH	R	√(2)	Receive idle cell counter (high byte)	3-32
0x33	LOCDCNT	R	√(2)	LOCD Event Counter	3-32
0x34	TXCNTL	R	√(2)	Transmitted Cell Counter (low byte)	3-33
0x35	TXCNTM	R	√(2)	Transmitted Cell Counter (mid byte)	3-33
0x36	TXCNTH	R	√(2)	Transmitted Cell Counter (high byte)	3-33
0x37	CORRCNT	R	√(2)	Corrected HEC Error Counter	3-33
0x38	RXCNTL	R	√(2)	Received Cell Counter (low byte)	3-34
0x39	RXCNTM	R	√(2)	Received Cell Counter (mid byte)	3-34
0x3A	RXCNTH	R	√(2)	Received Cell Counter (high byte)	3-34
0x3B	UNCCNT	R	√(2)	Uncorrected HEC Error Counter	3-34
0x3C	NONCNTL	R	√(2)	Nonmatching Cell Counter (low byte)	3-35
0x3D	NONCNTH	R	√(2)	Nonmatching Cell Counter (high byte)	3-35
0x3E	—	—	—	Reserved, set to a logic 0	—
0x3F	—	—	—	Reserved, set to a logic 0	—

FOOTNOTE:
(1) One-second latching is enabled by setting EnStatLat (bit 7) in the Global Control register (0xE00) to a logic 1.
(2) One-second latching is enabled by setting EnCntrLat (bit 6) in the Global Control register (0xE00) to a logic 1.

Table 3-3. PLCP Register Map

Base Address	Register Group
0x0300	PLCP Port 0 Control and Status
0x0340	PLCP Port 1 Control and Status
0x0380	PLCP Port 2 Control and Status
0x03C0	PLCP Port 3 Control and Status
0x0400	PLCP Port 4 Control and Status
0x0440	PLCP Port 5 Control and Status
0x0480	PLCP Port 6 Control and Status
0x04C0	PLCP Port 7 Control and Status
0x0500	PLCP Port 8 Control and Status
0x0540	PLCP Port 9 Control and Status
0x0580	PLCP Port 10 Control and Status
0x05C0	PLCP Port 11 Control and Status

Table 3-4. PLCP Registers

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x00	PLCPSEL	R/W	—	PLCP Mode Select Register	3-36
0x01	PLCPOVH	R/W	—	PLCP Overhead Control Register	3-36
0x02	TXG1	R/W	—	Transmit G1 Control Register	3-37
0x03	TXF1	R/W	—	Transmit F1 Control Register	3-37
0x04	PLCPSTAT	R	—	Receive PLCP Status Register	3-37
0x05	PLCPINT	R	—	PLCP Interrupt Status Register	3-38
0x06	ENPLCP	R/W	—	PLCP Interrupt Enable Control Register	3-38
0x07	RXF1	R/W	—	Receive F1 Status Register	3-39
0x08	B1CNTL	R	—	PLCP BIP Error Counter (low byte)	3-39
0x09	B1CNTH	R	—	PLCP BIP Error Counter (high byte)	3-39
0x0A	FEBECNTL	R	—	PLCP FEBE Error Counter (low byte)	3-39
0x0B	FEBECNTH	R	—	PLCP FEBE Error Counter (high byte)	3-39

Table 3-5. Framer Register Map

Base Address	Register Group
0x0800	Framer channel 0 Control and Status
0x0880	Framer channel 1 Control and Status
0x0900	Framer Channel 2 Control and Status
0x0980	Framer Channel 3 Control and Status
0x0A00	Framer Channel 4 Control and Status
0x0A80	Framer Channel 5 Control and Status
0x0B00	Framer Channel 6 Control and Status
0x0B80	Framer Channel 7 Control and Status
0x0C00	Framer Channel 8 Control and Status
0x0C80	Framer Channel 9 Control and Status
0x0D00	Framer Channel 10 Control and Status
0x0D80	Framer Channel 11 Control and Status

Table 3-6. Framer Registers

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x20	CR00	R/W	—	Mode Control Register	3-40
0x21	CR01	R/W	—	Counter Interrupt Control Register	3-41
0x22	CR02	R/W	—	Alarm Start Interrupt Control Register	3-42
0x23	CR03	R/W	—	Alarm End Interrupt Control Register	3-43
0x24	CR04	R/W	—	Feature1 Control Register	3-44
0x25	CR05	R/W	—	Feature2 Control Register	3-45
0x26	CR06	R/W	—	Feature3 Control Register	3-46
0x27	CR07	R/W	—	Feature4 Control Register	3-47
0x28	CR08	R/W	—	Feature5 Control Register	3-48
0x29	CR09	R/W	—	Transmit Overhead Insertion1 Control Register	3-50
0x2A	CR10	R/W	—	Transmit Overhead Insertion2 Control Register	3-52
0x2B	CR11	R/W	—	REXTCK Control Register	3-53
0x2C	CR12	R/W	—	Receive Overhead Control Register	3-55
0x2D	CR13	R/W	—	Transmit Data Link Control Register	3-56
0x2E	CR14	R/W	—	Transmit Data Link Threshold Control Register	3-56
0x2F	CR15	R/W	—	Transmit Data Link Message Byte—low	3-57
0x30	CR15	R/W	—	Transmit Data Link Message Byte—high	3-57

Table 3-6. Framer Registers

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x31	CR16	R/W	—	Receive Data Link Control Register	3-58
0x32	CR17	R/W	—	Receive Data Link Threshold Control Register	3-59
0x33	CR18	R/W	—	Transmit FEAC Channel Byte	3-59
0x34	CR19	R/W	—	Error Insertion1 Control Register	3-60
0x35	CR20	R/W	—	Error Insertion2 Control Register	3-61
0x40	SR00	R	—	DS3/E3 Maintenance Status Register	3-62
0x41	SR01	R	—	Interrupt Source Status Register	3-63
0x42	SR02	R	—	Counter Interrupt Status Register	3-64
0x43	SR03	R	—	Alarm Start Interrupt Status Register	3-65
0x44	SR04	R	—	Alarm End Interrupt Status Register	3-66
0x45	—	—	—	Reserved	—
0x46	SR06	R	—	E3-G.832 MA FINTIds Status Register	3-67
0x47	SR07	R	—	E3-G.832 SSM FINTId Status Register	3-67
0x48	SR08	R	—	Transmit Data Link Status Register	3-68
0x49	SR09	R/W	—	Reserved	—
0x4A	SR10	R/W	—	Reserved	—
0x4B	SR11	R	—	Receive Data Link Status Register	3-69
0x4C	SR12	R	—	Receive Data Link Message Byte	3-70
0x4D	SR13	R/W	—	Reserved	—
0x4E	SR14	R/W	—	Reserved	—
0x4F	SR15	R	—	Receive FEAC Byte	3-71
0x50	SR16	R	—	Receive FEAC Stack Byte	3-71
0x51	SR17	R	—	Receive FEAC Status Register	3-72
0x52	SR18	R	—	Receive AIC Byte	3-72
0x60	Ctr00	R/W	—	DS3/E3 Parity Error Counter—low	3-73
0x61	Ctr00	R/W	—	DS3/E3 Parity Error Counter—high	3-73
0x62	Ctr01	R/W	—	DS3 Parity Disagreement Counter—low	3-74
0x63	Ctr01	R/W	—	DS3 Parity Disagreement Counter—high	3-74
0x64	Ctr02	R/W	—	DS3 X Disagreement Counter—low	3-74
0x65	Ctr02	R/W	—	DS3 X Disagreement Counter—high	3-74
0x66	Ctr03	R/W	—	DS3/E3 Frame Error Counter—low	3-74
0x67	Ctr03	R/W	—	DS3/E3 Frame Error Counter—high	3-75

Table 3-6. Framer Registers

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x68	Ctr04	R/W	—	DS3 Path Parity Error Counter—low	3-75
0x69	Ctr04	R/W	—	DS3 Path Parity Error Counter—high	3-75
0x6A	Ctr05	R/W	—	DS3/E3 FEBE Event Counter—low	3-75
0x6B	Ctr05	R/W	—	DS3/E3 FEBE Event Counter—high	3-76
0x6C	Ctr06	R/W	—	DS3/E3 Excessive Zeros Counter—low	3-76
0x6D	Ctr06	R/W	—	DS3/E3 Excessive Zeros Counter—high	3-76
0x6E	Ctr07	R/W	—	DS3/E3 LCV Counter—low	3-76
0x6F	Ctr07	R/W	—	DS3/E3 LCV Counter—mid	3-77
0x70	Ctr07	R/W	—	DS3/E3 LCV Counter—high	3-77

Table 3-7. Common Registers (1 of 2)

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x0E00	GLOB	R/W	—	Global Control Register	3-78
0x0E01	SYSBUS	R/W	—	System Bus Control Register	3-78
0x0E02	VERSION	R/W	—	Part Number/Version Register	3-79
0x0E03	—	R/W	—	Reserved	—
0x0E04	GLOBINTL	R/W	—	Global Interrupt Status Register (low byte)	3-79
0x0E05	GLOBINTH	R/W	—	Global Interrupt Status Register (high byte)	3-80
0x0E06	—	R/W	—	Reserved	—
0x0E07	—	R/W	—	Reserved	—
0x0E08	OUT1L	R/W	—	OUTPORT1 Control Register (low byte)	3-80
0x0E09	OUT1H	R/W	—	OUTPORT1 Control Register (high byte)	3-81
0x0E0A	OUT2L	R/W	—	OUTPORT2 Control Register (low byte)	3-81
0x0E0B	OUT2H	R/W	—	OUTPORT2 Control Register (high byte)	3-82
0x0E0C	IN1L	R/W	—	INPORT1 Status Register (low byte)	3-82
0x0E0D	IN1H	R/W	—	INPORT1 Status Register (high byte)	3-83
0x0E0E	IN2L	R/W	—	INPORT2 Status Register (low byte)	3-83
0x0E0F	IN2H	R/W	—	INPORT2 Status Register (high byte)	3-84
0x0E10	INCL	R/W	—	INPORT Control Register (low byte)	3-84
0x0E11	INCH	R/W	—	INPORT Control Register (high byte)	3-85
0x0E12–0x0E7F	—	R/W	—	Reserved	—

Table 3-7. Common Registers (2 of 2)

Register Offset Address	Name	Type	One-second Latching	Description	Page Number
0x0E80	PORT0	R/W	—	Port0 Mode Control Register	3-85
0x0E81	PORT1	R/W	—	Port1 Mode Control Register	3-85
0x0E82	PORT2	R/W	—	Port2 Mode Control Register	3-85
0x0E83	PORT3	R/W	—	Port3 Mode Control Register	3-85
0x0E84	PORT4	R/W	—	Port4 Mode Control Register	3-85
0x0E85	PORT5	R/W	—	Port5 Mode Control Register	3-85
0x0E86	PORT6	R/W	—	Port6 Mode Control Register	3-85
0x0E87	PORT7	R/W	—	Port7 Mode Control Register	3-85
0x0E88	PORT8	R/W	—	Port8 Mode Control Register	3-85
0x0E89	PORT9	R/W	—	Port9 Mode Control Register	3-85
0x0E8A	PORT10	R/W	—	Port10 Mode Control Register	3-85
0x0E8B	PORT11	R/W	—	Port11 Mode Control Register	3-85
0x0E8C–0x0E8F	—	R/W	—	Reserved	—
0x0E90	PORTINT0	R/W	—	Port0 Interrupt Control/Status Register	3-86
0x0E91	PORTINT1	R/W	—	Port1 Interrupt Control/Status Register	3-86
0x0E92	PORTINT2	R/W	—	Port2 Interrupt Control/Status Register	3-86
0x0E93	PORTINT3	R/W	—	Port3 Interrupt Control/Status Register	3-86
0x0E94	PORTINT4	R/W	—	Port4 Interrupt Control/Status Register	3-86
0x0E95	PORTINT5	R/W	—	Port5 Interrupt Control/Status Register	3-86
0x0E96	PORTINT6	R/W	—	Port6 Interrupt Control/Status Register	3-86
0x0E97	PORTINT7	R/W	—	Port7 Interrupt Control/Status Register	3-86
0x0E98	PORTINT8	R/W	—	Port8 Interrupt Control/Status Register	3-86
0x0E99	PORTINT9	R/W	—	Port9 Interrupt Control/Status Register	3-86
0x0E9A	PORTINT10	R/W	—	Port10 Interrupt Control/Status Register	3-86
0x0E9B	PORTINT11	R/W	—	Port11 Interrupt Control/Status Register	3-86
0x0E9C–0x0FFF	—	R/W	—	Reserved	—

Table 3-8. External Chip Select Address Map

Address Range	External Chip Select Pin (Refer to OUTPORT2 Hardware Description)
0x1000–0x11FF	LCS[0]
0x1200–0x13FF	LCS[1]
0x1400–0x15FF	LCS[2]
0x1600–0x17FF	LCS[3]
0x1800–0x19FF	LCS[4]
0x1A00–0x1BFF	LCS[5]
0x1C00–0x1DFF	LCS[6]
0x1E00–0x1FFF	LCS[7]
0x2000–0x21FF	LCS[8]
0x2200–0x23FF	LCS[9]
0x2400–0x25FF	LCS[10]
0x2600–0x27FF	LCS[11]

3.2 Cell Delineator Registers

3.2.1 Mode Control Registers

0x04—PMODE (Port Mode Control Register)

The PMODE register controls the port-level software resets, source loopback, and physical layer interface mode.

7	6	5	4	3	2	1	0
PrtMstRst	—	SrcLoop	FELNLOOP	—	PhyType[2]	PhyType[1]	PhyType[0]

Default after reset: 00

Modification:
bits 0–2, 4, 5: static
bit 7: dynamic

PrtMstRst When written to a logical 1, this bit initiates a Port Master Reset. All cell delineator internal state machines associated with this port are reset and all cell delineator control registers for this port, assume their default values.

SrcLoop(1) When written to a logical 1, this bit enables a source loopback. The line transmit clock and data outputs are connected to the line receive clock and data inputs.

FELNLOOP(1) When written to a logical 1, this bit enables the far end line loopback.

PhyType[2:0](1) These bits determine the Physical Layer Interface mode:
000 = T1 mode
001 = E1 mode
010 = DS3 mode
011 = E3 mode
100 = Reserved, do not use
101 = Reserved, do not use
110 = Reserved, do not use
111 = Power Down

0x05—IOMODE (Input/Output Mode Control Register)

The IOMODE register controls the line interface signal polarities and status outputs.

7	6	5	4	3	2	1	0
—	LRxMRKPol	RxCKIPol	LTxMRKPol	TxCKIPol	CsPol	—	—

Default after reset: 00

Modification:
bits 2–4, 6: static
bit 5: dynamic

LRxMRKPol This bit determines the Receiver Synchronization Input Polarity. When written to a logical 1, the active level on the LRxMRK input is high. When written to a logical 0, the active level is low.

RxCKIPol This bit determines the Receiver Clock Input Polarity. When written to a logical 1, the active edge on the RxCKI input is the falling edge. When written to a logical 0, the active edge is the rising edge.

LTxMRKPol This bit determines the Transmitter Synchronization Input Polarity. When written to a logical 1, the active level on the LTxMRK input is high. When written to a logical 0, the active level is low.

TxCKIPol This bit determines the Transmitter Clock Input Polarity. When written to a logical 1, the active edge on the TxCKI input is the falling edge. When written to a logical 0, the active edge is the rising edge.

CsPol This bit determines the Chip Select Output Polarity. When written to a logical 1, the active level on the LCs output pin is high. When written to a logical 0, the active level is low.

NOTE: For normal operation, the IOMODE register must be set to 0x70. This affects RxSyncPol, RxClkPol, and TxSyncPol.

3.2.2 Cell Transmit Registers

This section describes the control registers used for traffic transmission.

0x08—CGEN (Cell Generation Control Register)

The CGEN register controls the device's cell generation functions.

7	6	5	4	3	2	1	0
DisHEC	EnTxCos	EnTxCellScr	ErrHEC	—	—	0	0

Default after reset: 60

Modification: dynamic

DisHEC When written to a logical 1, this bit disables internal generation of the HEC field. When disabled, the HEC field from the UTOPIA interface remains unchanged in the transmitted cell. When written to a logical 0, HEC is internally calculated and inserted in the transmitted cell.

EnTxCos When written to a logical 1, this bit enables the Transmit HEC Coset. When written to a logical 0, the HEC Coset is disabled.

EnTxCellScr When written to a logical 1, this bit enables the Transmit Cell Scrambler. When written to a logical 0, the Transmit Cell Scrambler is disabled.

ErrHEC When written to a logical 1, this bit causes the ERRPAT register to be XORed with the calculated HEC byte for one transmit cell. These bits are cleared automatically by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register.

0x09—HDRFIELD (Header Field Control Register)

The HDRFIELD register controls the header insertion elements.

7	6	5	4	3	2	1	0
—	—	—	InsGFC	InsVPI	InsVCI	InsPT	InsCLP

Default after reset: 00

InsGFC When written to a logical 1, this bit inserts a Generic Flow Control (GFC) field in the outgoing header from the TXHDR registers. When written to a logical 0, the GFC field is not changed prior to transmission.

InsVPI When written to a logical 1, this bit inserts a Virtual Path Identifier (VPI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VPI field is not changed prior to transmission.

InsVCI When written to a logical 1, this bit inserts a Virtual Channel Identifier (VCI) field in the outgoing header from the TXHDR registers. When written to a logical 0, the VCI field is not changed prior to transmission.

InsPT When written to a logical 1, this bit inserts a Payload Type (PT) field in the outgoing header from the TXHDR registers. When written to a logical 0, the PT field is not changed prior to transmission.

InsCLP When written to a logical 1, this bit inserts a Cell Loss Priority (CLP) bit in the outgoing header from the TXHDR registers. When written to a logical 0, the CLP field is not changed prior to transmission.

0x0A—IDLPAY (Transmit Idle Cell Payload Control Register)

The IDLPAY register contains the Transmit Idle Cell Payload.

7	6	5	4	3	2	1	0
IdlPay[7]	IdlPay[6]	IdlPay[5]	IdlPay[4]	IdlPay[3]	IdlPay[2]	IdlPay[1]	IdlPay[0]

Default after reset: 6A

IdlPay[7:0] These bits hold the Transmit Idle Cell Payload values for outgoing idle cells.

0x0B—ERRPAT (Error Pattern Control Register)

The ERRPAT register provides the error pattern for the HEC error insertion function. ErrHEC (bit 4) in the CGEN register (0x08) enables this function. Each bit in the error pattern register is XORed with the corresponding bit of the calculated HEC byte to be errored.

7	6	5	4	3	2	1	0
ErrPat[7]	ErrPat[6]	ErrPat[5]	ErrPat[4]	ErrPat[3]	ErrPat[2]	ErrPat[1]	ErrPat[0]

Default after reset: 00

ErrPat[7:0] Error pattern

0x10—TXHDR1 (Transmit Cell Header Control Register 1)

The TXHDR1 register contains the first byte of the Transmit Cell Header. It controls the header value that is inserted in the transmitted cell. This header consists of 32 bits divided among four registers (TXHDR1–4). These bits hold the Transmit Header values for Octet 1 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09).

7	6	5	4	3	2	1	0
TxHdr1[7]	TxHdr1[6]	TxHdr1[5]	TxHdr1[4]	TxHdr1[3]	TxHdr1[2]	TxHdr1[1]	TxHdr1[0]

Default after reset: 00

TxHdr1[7:4] GFC/VPI bits (for UNI they are GFC bits, for NNI they are VPI bits).

TxHdr1[3:0] VPI bits

0x11—TXHDR2 (Transmit Cell Header Control Register 2)

The TXHDR2 register contains the second byte of the Transmit Cell Header. (See 0x10—TXHDR1.) These bits hold the Transmit Header values for Octet 2 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09).

7	6	5	4	3	2	1	0
TxHdr2[7]	TxHdr2[6]	TxHdr2[5]	TxHdr2[4]	TxHdr2[3]	TxHdr2[2]	TxHdr2[1]	TxHdr2[0]

Default after reset: 00

TxHdr2[7:4] VPI bits

TxHdr2[3:0] VCI bits

0x12—TXHDR3 (Transmit Cell Header Control Register 3)

The TXHDR3 register contains the third byte of the Transmit Cell Header. (See 0x10—TXHDR1.) These bits hold the Transmit Header values for Octet 3 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09).

7	6	5	4	3	2	1	0
TxHdr3[7]	TxHdr3[6]	TxHdr3[5]	TxHdr3[4]	TxHdr3[3]	TxHdr3[2]	TxHdr3[1]	TxHdr3[0]

Default after reset: 00

TxHdr3[7:0] VCI bits

0x13—TXHDR4 (Transmit Cell Header Control Register 4)

The TXHDR4 register contains the fourth byte of the Transmit Cell Header (see 0x10—TXHDR1). These bits hold the Transmit Header values for Octet 4 of the outgoing cell. Insertion of the bits is controlled by the HDRFIELD register (0x09).

7	6	5	4	3	2	1	0
TxHdr4[7]	TxHdr4[6]	TxHdr4[5]	TxHdr4[4]	TxHdr4[3]	TxHdr4[2]	TxHdr4[1]	TxHdr4[0]

Default after reset: 00

TxHdr4[7:4] VCI bits

TxHdr4[3:1] Payload Type Indicator bits

TxHdr4[0] Cell Loss Priority bit

0x14—TXIDL1 (Transmit Idle Cell Header Control Register 1)

The TXIDL1 register contains the first byte of the Transmit Idle Cell Header. It controls the header value that is inserted in the transmitted idle cells. This header consists of 32 bits divided among four registers. These bits hold the Transmit Idle Cell Header values for Octet 1 of the outgoing cell.

7	6	5	4	3	2	1	0
TxIdl1[7]	TxIdl1[6]	TxIdl1[5]	TxIdl1[4]	TxIdl1[3]	TxIdl1[2]	TxIdl1[1]	TxIdl1[0]

Default after reset: 00

TxIdl1[7:4] GFC/VPI bits (for UNI they are GFC bits, for NNI the are VPI bits)

TxIdl1[3:0] VPI bits

0x15—TXIDL2 (Transmit Idle Cell Header Control Register 2)

The TXIDL2 register contains the second byte of the Transmit Idle Cell Header (see 0x14—TXIDL1). These bits hold the Transmit Idle Cell Header values for Octet 2 of the outgoing cell.

7	6	5	4	3	2	1	0
TxIdl2[7]	TxIdl2[6]	TxIdl2[5]	TxIdl2[4]	TxIdl2[3]	TxIdl2[2]	TxIdl2[1]	TxIdl2[0]

Default after reset: 00

TxIdl2[7:4] VPI bits

TxIdl2[3:0] VCI bits

0x16—TXIDL3 (Transmit Idle Cell Header Control Register 3)

The TXIDL3 register contains the third byte of the Transmit Idle Cell Header (see 0x14—TXIDL1). These bits hold the Transmit Idle Cell Header values for Octet 3 of the outgoing cell.

7	6	5	4	3	2	1	0
TxIdl3[7]	TxIdl3[6]	TxIdl3[5]	TxIdl3[4]	TxIdl3[3]	TxIdl3[2]	TxIdl3[1]	TxIdl3[0]

Default after reset: 00

TxIdl3[7:0] VCI bits

0x17—TXIDL4 (Transmit Idle Cell Header Control Register 4)

The TXIDL4 register contains the fourth byte of the Transmit Idle Cell Header (see 0x14—TXIDL1). These bits hold the Transmit Idle Cell Header values for Octet 4 of the outgoing cell.

7	6	5	4	3	2	1	0
TxIdl4[7]	TxIdl4[6]	TxIdl4[5]	TxIdl4[4]	TxIdl4[3]	TxIdl4[2]	TxIdl4[1]	TxIdl4[0]

Default after reset: 01

TxIdl4[7:4] VCI bits

TxIdl4[3:1] Payload Type Indicator bits

TxIdl4[0] Cell Loss Priority bit

3.2.3 Cell Receive Registers

This section describes the Traffic Reception control registers.

0x0C—CVAL (Cell Validation Control Register)

The CVAL register controls the validation of incoming cells.

7	6	5	4	3	2	1	0
RejHdr	DelIdle	EnRxCos	EnRxCellScr	EnHECCorr	DisHECChk	DisCellRcvr	DisLOCD

Default after reset: 70

RejHdr When written to a logical 1, this bit enables the Rejection of certain Header cells. When enabled, cells with headers matching the RXHDRx/RXMSKx definition are rejected and all others are accepted. When written to a logical 0, cells with matching headers are accepted and cells with non-matching headers are rejected.

DelIdle When written to a logical 1, this bit enables the Deletion of Idle Cells. When enabled, cells matching the RXIDL/IDLMSK definition are deleted from the received cell stream. When written to a logical 0, idle cells are included in the received stream.

EnRxCos When written to a logical 1, this bit enables the Receive HEC Coset. When written to a logical 0, the HEC Coset is disabled.

EnRxCellScr When written to a logical 1, this bit enables the Receive Cell Scrambler. When written to a logical 0, the Receive Cell Scrambler is disabled.

EnHECCorr When written to a logical 1, this bit enables HEC Correction. When written to a logical 0, HEC Correction is disabled.

DisHECChk When written to a logical 1, this bit disables HEC Checking. When written to a logical 0, HEC checking is performed as a cell validation criterion.

DisCellRcvr When written to a logical 1, this bit disables the Cell Receiver. When disabled, all cell reception is disabled on the next cell boundary. When written to a logical 0, cell reception begins or resumes on the next cell boundary.

DisLOCD When written to a logical 1, this bit disables Loss of Cell Delineation. When disabled, cells are passed even if cell delineation has not been found. When written to a logical 0, cells are passed only while cell alignment has been achieved.

The CX2836x contains two independent HEC Check state machines. The cell delineator (CD) state machine is used to find cell delineation and conversely to declare LOCD (loss of cell delineation). The cell valid (CV) state machine is used to validate the cells that are passed to the UTOPIA FIFOs.

These state machines are controlled by two register bits that allow the CX2836x to be programmed for special applications. The control bit function is shown in Table 3-9.

Table 3-9. Control Bit Function

DisLOCD Setting	DisHECChk Setting	Effect
0	0	Normal operation; used for standard ATM traffic. Cells are output to the UTOPIA FIFO only after cell delineation is found. Only cells with valid HECs are passed (this includes cells with single bit errors that have been corrected).
0	1	Ignore HEC Errors mode; used for IMA applications. The cell delineator state machine is active and looking for valid ATM cells. It follows the ATM Forum's cell delineation process. However, since the cell valid state machine is turned off, the CX2836x passes all cells, including those with HEC errors, to the UTOPIA FIFOs. The CX2836x does not transfer cells during LOCD.
1	0	Not supported.
1	1	

0x18—RXHDR1 (Receive Cell Header Control Register 1)

The RXHDR1 register contains the first byte of the Receive Cell Header. The header values direct ATM cells to the UTOPIA port if an incoming ATM cell header matches the value in the header register. Receive Header Mask Registers further qualify ATM cell reception. This header consists of 32 bits divided among four registers.

7	6	5	4	3	2	1	0
RxHdr1[7]	RxHdr1[6]	RxHdr1[5]	RxHdr1[4]	RxHdr1[3]	RxHdr1[2]	RxHdr1[1]	RxHdr1[0]

Default after reset: 00

RxHdr1[7:0] These bits hold the Receive Header values for Octet 1 of the incoming cell.

0x19—RXHDR2 (Receive Cell Header Control Register 2)

The RXHDR2 register contains the second byte of the Receive Cell Header (see 0x18—RXHDR1).

7	6	5	4	3	2	1	0
RxHdr2[7]	RxHdr2[6]	RxHdr2[5]	RxHdr2[4]	RxHdr2[3]	RxHdr2[2]	RxHdr2[1]	RxHdr2[0]

Default after reset: 00

RxHdr2[7:0] These bits hold the Receive Header values for Octet 2 of the incoming cell.

0x1A—RXHDR3 (Receive Cell Header Control Register 3)

The RXHDR3 register contains the third byte of the Receive Cell Header (see 0x18—RXHDR1).

7	6	5	4	3	2	1	0
RxHdr3[7]	RxHdr3[6]	RxHdr3[5]	RxHdr3[4]	RxHdr3[3]	RxHdr3[2]	RxHdr3[1]	RxHdr3[0]

Default after reset: 00

RxHdr3[7:0] These bits hold the Receive Header values for Octet 3 of the incoming cell.

0x1B—RXHDR4 (Receive Cell Header Control Register 4)

The RXHDR4 register contains the fourth byte of the Receive Cell Header (see 0x18—RXHDR1).

7	6	5	4	3	2	1	0
RxHdr4[7]	RxHdr4[6]	RxHdr4[5]	RxHdr4[4]	RxHdr4[3]	RxHdr4[2]	RxHdr4[1]	RxHdr4[0]

Default after reset: 00

RxHdr4[7:0] These bits hold the Receive Header values for Octet 4 of the incoming cell.

0x1C—RXMSK1 (Receive Cell Mask Control Register 1)

The RXMSK1 register contains the first byte of the Receive Cell Mask. It modifies ATM cell screening, which compares the Receive Cell Header Registers to the incoming cells. Setting a bit in the Mask Register causes the corresponding bit in the received ATM cell header to be disregarded for screening. For example, setting RXMSK1 bit 0 to 1 causes ATM cells to be accepted with either 1 or 0 in the octet 1, bit 0 position. Combinations of Receive Header Mask bits can select groups of ATM VPI/VCIs for reception. This mask consists of 32 bits divided among four registers.

7	6	5	4	3	2	1	0
RxMsk1[7]	RxMsk1[6]	RxMsk1[5]	RxMsk1[4]	RxMsk1[3]	RxMsk1[2]	RxMsk1[1]	RxMsk1[0]

Default after reset: FF

RxMsk1[7:0] These bits hold the Receive Header Mask for Octet 1 of the incoming cell.

0x1D—RXMSK2 (Receive Cell Mask Control Register 2)

The RXMSK2 register contains the second byte of the Receive Cell Mask (see 0x1C—RXMSK1).

7	6	5	4	3	2	1	0
RxMsk2[7]	RxMsk2[6]	RxMsk2[5]	RxMsk2[4]	RxMsk2[3]	RxMsk2[2]	RxMsk2[1]	RxMsk2[0]

Default after reset: FF

RxMsk2[7:0] These bits hold the Receive Header Mask for Octet 2 of the incoming cell.

0x1E—RXMSK3 (Receive Cell Mask Control Register 3)

The RXMSK3 register contains the third byte of the Receive Cell Mask (see 0x1C—RXMSK1).
.

7	6	5	4	3	2	1	0
RxMsk3[7]	RxMsk3[6]	RxMsk3[5]	RxMsk3[4]	RxMsk3[3]	RxMsk3[2]	RxMsk3[1]	RxMsk3[0]

Default after reset: FF

RxMsk3[7:0] These bits hold the Receive Header Mask for Octet 3 of the incoming cell.

0x1F—RXMSK4 (Receive Cell Mask Control Register 4)

The RXMSK4 register contains the fourth byte of the Receive Cell Mask (see 0x1C—RXMSK1).

7	6	5	4	3	2	1	0
RxMsk4[7]	RxMsk4[6]	RxMsk4[5]	RxMsk4[4]	RxMsk4[3]	RxMsk4[2]	RxMsk4[1]	RxMsk4[0]

Default after reset: FF

RxMsk4[7:0] These bits hold the Receive Header Mask for Octet 4 of the incoming cell.

0x20—RXIDL1 (Receive Idle Cell Header Control Register 1)

The RXIDL1 register contains the first byte of the Receive Idle Cell Header. It defines ATM idle cells for the cell receiver. Idle cells are discarded from the received stream if register CVAL (0x0C) bit 6 is set to 1. This header consists of 32 bits divided among four registers.

7	6	5	4	3	2	1	0
RxIdl1[7]	RxIdl1[6]	RxIdl1[5]	RxIdl1[4]	RxIdl1[3]	RxIdl1[2]	RxIdl1[1]	RxIdl1[0]

Default after reset: 00

RxIdl1[7:0] These bits hold the Receive Idle cell header for Octet 1 of the incoming cell.

0x21—RXIDL2 (Receive Idle Cell Header Control Register 2)

The RXIDL2 register contains the second byte of the Receive Idle Cell Header (see 0x20—RXIDL1).

7	6	5	4	3	2	1	0
RxIdl2[7]	RxIdl2[6]	RxIdl2[5]	RxIdl2[4]	RxIdl2[3]	RxIdl2[2]	RxIdl2[1]	RxIdl2[0]

Default after reset: 00

RxIdl2[7:0] These bits hold the Receive Idle cell header for Octet 2 of the incoming cell.

0x22—RXIDL3 (Receive Idle Cell Header Control Register 3)

The RXIDL3 register contains the third byte of the Receive Idle Cell Header (see 0x20—RXIDL1).

7	6	5	4	3	2	1	0
RxIdl3[7]	RxIdl3[6]	RxIdl3[5]	RxIdl3[4]	RxIdl3[3]	RxIdl3[2]	RxIdl3[1]	RxIdl3[0]

Default after reset: 00

RxIdl3[7:0] These bits hold the Receive Idle cell header for Octet 3 of the incoming cell.

0x23—RXIDL4 (Receive Idle Cell Header Control Register 4)

The RXIDL4 register contains the fourth byte of the Receive Idle Cell Header (see 0x20—RXIDL1).

7	6	5	4	3	2	1	0
RxIdl4[7]	RxIdl4[6]	RxIdl4[5]	RxIdl4[4]	RxIdl4[3]	RxIdl4[2]	RxIdl4[1]	RxIdl4[0]

Default after reset: 01

RxIdl4[7:0] These bits hold the Receive Idle cell header for Octet 4 of the incoming cell.

0x24—IDLMSK1 (Receive Idle Cell Mask Control Register 1)

The IDLMSK1 register contains the first byte of the Receive Idle Cell Mask. It modifies ATM cell screening, which compares the Receive Idle Cell Header Registers to the incoming cells. Setting a bit in the Mask Register causes the corresponding bit in the received ATM idle cell header to be disregarded for screening. For example, setting IDLMSK1 bit 0 to 1 causes cells to be accepted as ATM idle cells with either 1 or 0 in Octet 1, bit 0 position. This header consists of 32 bits divided among four registers.

7	6	5	4	3	2	1	0
IdlMsk1[7]	IdlMsk1[6]	IdlMsk1[5]	IdlMsk1[4]	IdlMsk1[3]	IdlMsk1[2]	IdlMsk1[1]	IdlMsk1[0]

Default after reset: 00

IdlMsk1[7:0] These bits hold the Receive Idle cell header mask for Octet 1 of the incoming cell.

0x25—IDLMSK2 (Receive Idle Cell Mask Control Register 2)

The IDLMSK2 register contains the second byte of the Receive Idle Cell Mask (see 0x24—RXMSKL1).

7	6	5	4	3	2	1	0
IdlMsk2[7]	IdlMsk2[6]	IdlMsk2[5]	IdlMsk2[4]	IdlMsk2[3]	IdlMsk2[2]	IdlMsk2[1]	IdlMsk2[0]

Default after reset: 00

IdlMsk2[7:0] These bits hold the Receive Idle cell header mask for Octet 2 of the incoming cell.

0x26—IDLMSK3 (Receive Idle Cell Mask Control Register 3)

The IDLMSK3 register contains the third byte of the Receive Idle Cell Mask (see 0x24—RXMSKL1).

7	6	5	4	3	2	1	0
IdlMsk3[7]	IdlMsk3[6]	IdlMsk3[5]	IdlMsk3[4]	IdlMsk3[3]	IdlMsk3[2]	IdlMsk3[1]	IdlMsk3[0]

Default after reset: 00

IdlMsk3[7:0] These bits hold the Receive Idle cell header mask for Octet 3 of the incoming cell.

0x27—IDLMSK4 (Receive Idle Cell Mask Control Register 4)

The IDLMSK4 register contains the fourth byte of the Receive Idle Cell Mask (see 0x24—RXMSKL1).

7	6	5	4	3	2	1	0
IdlMsk4[7]	IdlMsk4[6]	IdlMsk4[5]	IdlMsk4[4]	IdlMsk4[3]	IdlMsk4[2]	IdlMsk4[1]	IdlMsk4[0]

Default after reset: 00

IdlMsk4[7:0] These bits hold the Receive Idle cell header mask for Octet 4 of the incoming cell.

3.2.4 UTOPIA Registers

0x0D—UTOP1 (UTOPIA Control Register 1)

The UTOP1 register controls the UTOPIA resets, parity orientation, and the transmit FIFO fill-level threshold.

7	6	5	4	3	2	1	0
TxReset	RxReset	—	—	—	OddEven	TxFill[1]	TxFill[0]

Default after reset: 00

TxReset When written to a logical 1, this bit resets the transmit FIFO pointers. This reset should only be used as a test function because it can create short cells.

RxReset When written to a logical 1, this bit resets the receive FIFO pointers. This reset should only be used as a test function because it can create short cells.

OddEven(1) This bit determines Odd/Even Parity. When written to a logical 1, even parity is generated and checked. When set to a logical 0, odd parity is generated and checked.

TxFill[1:0](1) These bits set the Transmit FIFO Fill-level threshold for UTxCLAV pin
00 = UTxCLAV indicates full after 1 more cell
01 = UTxCLAV indicates full after 2 more cells
10 = UTxCLAV indicates full after 3 more cells
11 = UTxCLAV indicates full after 4 more cells

NOTE: (1) These bits should only be changed when the device or port logic reset is asserted.

0x0E—UTOP2 (UTOPIA Control Register 2)

The UTOP2 register contains the multi-PHY address value for the device.

7	6	5	4	3	2	1	0
—	—	UtopDis	MphyAddr[4]	MphyAddr[3]	MphyAddr[2]	MphyAddr[1]	MphyAddr[0]

Default after reset: UtopDis set to 1, MphyAddr[4:0] see notes

UtopDis(1) When written to a logical 1, this bit disables UTOPIA outputs for this port.

MphyAddr[4:0](1) These bits are the Multi-PHY Device Address. Each CX2836x port should have a unique address. These bits correspond to the URxAddr and UTxAddr pins. When the pin matches the bit values, the port is accessed. This port ignores any transactions meant for another port or PHY device.

NOTE: (1) These bits should only be changed when the Device or Port Logic reset is asserted.
The default for MphyAddr4 is 0 and the default for MphyAddr[3:0] is the port number for each port. (0000–Port 0, 0001–Port 1, 0010–Port2, 0011–Port 3, 0100–Port 4, 0101–Port 5, 0110–Port 6, 0111–Port 7, 1000–Port 8, 1001–Port 9, 1010–Port10, 1011–Port 11).

0x0F—RXUDF2 (RXUDF2 Octet Control)

The UTOP2 register contains the multi-PHY address value for the device.

7	6	5	4	3	2	1	0
RXUDF2[7]	RXUDF2[6]	RXUDF2[5]	RXUDF2[4]	RXUDF2[3]	RXUDF2[2]	RXUDF2[1]	RXUDF2[0]

Default after reset: (port number)

These eight bits are written into the Receive UTOPIA UDF2 octet when in 16-bit UTOPIA mode. RXUDF2[7:0] is set to the port number, same as UTOP[MphyAddr]. All bits are read/write so the default can be overwritten.

3.2.5 Status and Interrupt Registers

These registers contain interrupt enables, interrupt indications, and status information.

NOTE: The interrupt bits in the Cell Delineator register group do not latch status unless the respective interrupts are enabled. The affected registers are SUMINT (offset 0x00), TXCELLINT (offset 0x2c), and RXCELLINT (offset 0x2D).

0x00—SUMINT (Summary Interrupt Indication Status Register)

The SUMINT register indicates the Cell Delineator port summary interrupts.

7	6	5	4	3	2	1	0
—	—	—	PLCPInt	—	—	TxCellInt	RxCellInt

PLCPInt Active-high interrupt from PLCP circuit.

TxCellInt(1) When a logical 1 is read, this bit indicates a Transmit Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the TxCellInt register (0x2C).

RxCellInt(1) When a logical 1 is read, this bit indicates a Receive Cell Interrupt. This interrupt is a summary interrupt and signifies that an interrupt indication occurred in the RxCellInt register (0x2D).

NOTE: (1) This bit is a summary indication of any interrupt events that occurred in the indicated registers. This bit is a pointer to the next interrupt indication register to be read. This bit is cleared when the interrupt bits in the corresponding interrupt indication registers are read and automatically cleared.

0x01—ENSUMINT (Summary Interrupt Control Register)

The ENSUMINT register controls which of the interrupts listed in the SUMINT register (0x00) appear in the SUMPORT register (0xE04 and 0xE05) and on the MINTR* (pin E2).

7	6	5	4	3	2	1	0
—	—	—	EnPLCPInt	—	—	EnTxCellInt	EnRxCellInt

Default after reset: 00

EnPLCPInt Active-high enable of PLCP interrupt.

EnTxCellInt When written to a logical 1, this bit enables the transmit cell interrupts located in the TxCellInt register (0x2C). These interrupts can appear on the MINTR* pin (pin E2), provided that EnPortInt in the ENSUMPORT register (0x0201) and the CDInten in the PORTINT register (0xE90) are enabled for that port and the EnIntpin in the GLOB register (0xE00) is enabled.

EnRxCellInt When written to a logical 1, this bit enables the receive cell interrupts located in the RxCellInt register (0x2D). These interrupts can appear on the MInt* pin (pin B19), provided that EnPortInt in the ENSUMPORT register (0x00201) and the CDInten in the PORTINT register (0xE90) are enabled for that port and the EnIntpin in the GLOB register (0xE00) is enabled.

0x28—ENCELLT (Transmit Cell Interrupt Control Register)

The ENCELLT register controls which of the interrupts listed in the TxCellInt register (0x2C) appear on CDInt (bit 2) of the PORTINTn Interrupt Control/Status register (0xE90–0xE9B).

7	6	5	4	3	2	1	0
EnParErrInt	EnSOCErrInt	EnTxOvflInt	EnRxOvflInt	EnCellSentInt	EnBusCnflctInt	—	—

Default after reset: FC

EnParErrInt When written to a logical 1, this bit enables the Parity Error Interrupt.

EnSOCErrInt When written to a logical 1, this bit enables the Start of Cell Error Interrupt.

EnTxOvflInt When written to a logical 1, this bit enables the Transmit FIFO Overflow Interrupt.

EnRxOvflInt When written to a logical 1, this bit enables the Receive FIFO Overflow Interrupt.

EnCellSentInt When written to a logical 1, this bit enables the Cell Sent Interrupt.

EnBusCnflctInt When written to a logical 1, this bit enables the Bus Conflict Interrupt.

0x29—ENCELLR (Receive Cell Interrupt Control Register)

The ENCELLR register controls which of the interrupts listed in the RxCellInt register (0x2D) appear on CDInt (bit 2) of the PORTINTn Interrupt Control/Status register (0xE90–0xE9B).

7	6	5	4	3	2	1	0
EnLOCDInt	EnHECDetInt	EnHECCorrInt	EnRcvrHldInt	EnCellRcvdInt	EnIdleRcvdInt	EnNonMatchIn t	EnNonZerGFCI nt

Default after reset: FF

EnLOCDInt When written to a logical 1, this bit enables a Loss of Cell Delineation Interrupt.

EnHECDetInt When written to a logical 1, this bit enables a HEC Error Detected Interrupt.

EnHECCorrInt When written to a logical 1, this bit enables a HEC Error Corrected Interrupt.

EnRcvrHldInt When written to a logical 1, this bit enables a Receiver Hold Interrupt.

EnCellRcvdInt When written to a logical 1, this bit enables a Cell Received Interrupt.

EnIdleRcvdInt When written to a logical 1, this bit enables an Idle Cell Received Interrupt.

EnNonMatchInt When written to a logical 1, this bit enables a Non-matching Cell Received Interrupt.

EnNonZerGFCInt When written to a logical 1, this bit enables a Non-zero GFC Received Interrupt.

0x2C—TXCELLINT (Transmit Cell Interrupt Indication Status Register)

The TXCELLINT register indicates that a change of status has occurred within the Transmit Status signals.

7	6	5	4	3	2	1	0
ParErrInt	SOCErrInt	TxOvflInt	RxOvflInt	CellSentInt	BusCnflctInt	—	—

ParErrInt(1) When a logical 1 is read, this bit indicates that a Parity Error occurred.

SOCErrInt(1) When a logical 1 is read, this bit indicates that a Start of Cell Error occurred.

TxOvflInt(1) When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow occurred.

RxOvflInt(1) When a logical 1 is read, this bit indicates that a Receive FIFO Overflow occurred.

CellSentInt(1) When a logical 1 is read, this bit indicates that a cell has been sent.

BusCnflctInt(1) When a logical 1 is read, this bit indicates that a Bus Conflict occurred.

NOTE: (1) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

0x2D—RXCELLINT (Receive Cell Interrupt Indication Status Register)

The RXCELLINT register indicates that a change of status has occurred within the Receive Status signals.

7	6	5	4	3	2	1	0
LOCDInt	HECDetInt	HECCorrInt	—	CellRcvdInt	IdleRcvdInt	NonMatchInt	NonZerGFCInt

LOCDInt(1) When a logical 1 is read, this bit indicates that a Loss of Cell Delineation has occurred.

HECDetInt(2) When a logical 1 is read, this bit indicates that a HEC Error was detected.

HECCorrInt(2) When a logical 1 is read, this bit indicates that a HEC Error was corrected.

CellRcvdInt(2) When a logical 1 is read, this bit indicates that a cell has been received.

IdleRcvdInt(2) When a logical 1 is read, this bit indicates that an Idle Cell has been received.

NonMatchInt(2) When a logical 1 is read, this bit indicates that a Non-matching Cell has been received.

NonZerGFCInt(2) When a logical 1 is read, this bit indicates that a Non-zero GFC has been received.

NOTE: (1) Dual event—Either a 0 to 1 or a 1 to 0 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

(2) Single event—A 0 to 1 transition on the corresponding status bit causes this interrupt to occur, provided that this interrupt has been enabled by the corresponding enable bit. Reading this interrupt register clears this interrupt.

0x2E—TXCELL (Transmit Cell Status Register)

The TXCELL register contains status for the cell transmitter.

7	6	5	4	3	2	1	0
ParErr	SOCErr	TxOvfl	RxOvfl	CellSent	BusCnflct	—	DisTxIdle

Default after reset: DisTxIdle set to 0

ParErr(1) When a logical 1 is read, this bit indicates that a parity error was received on the transmit UTOPIA input data octet.

SOCErr(1) When a logical 1 is read, this bit indicates that a Start of Cell Error was received on the UTxSOC pin (pin W12).

TxOvfl(1) When a logical 1 is read, this bit indicates that a Transmit FIFO Overflow condition occurred in the transmit UTOPIA FIFO.

RxOvfl(1) When a logical 1 is read, this bit indicates that a Receive FIFO Overflow condition occurred in the receive UTOPIA FIFO.

CellSent(1) When a logical 1 is read, this bit indicates that a non-idle cell was formatted and transmitted.

BusCnflct(1) When a logical 1 is read, this bit indicates that a UTOPIA bus conflict has occurred, which means that a duplicate multi-PHY address has been programmed for this port. Check the contents of the UTOP2 register (0x0E).

DisTxIdle When written to 1, this bit enables the last cell value transmitted prior to an idle period to be output repeatedly until new data is available (the last value replaces what would be idle cells). When set to 0 (default), idle cells are transmitted when there is a gap in the data stream.

NOTE: (1) This status shows an event that has occurred since the register was last read.

0x2F—RXCELL (Receive Cell Status Register)

The RXCELL register contains status for the cell receiver.

7	6	5	4	3	2	1	0
LOCD	HECDet	HECCorr	—	CellRcvd	IdleRcvd	NonMatch	NonZerGFC

LOCD(1) When a logical 1 is read, this bit indicates a Loss of Cell Delineation.

HECDet(2) When a logical 1 is read, this bit indicates that an uncorrected HEC Error was detected.

HECCorr(2) When a logical 1 is read, this bit indicates that a HEC Error was corrected.

CellRcvd(2) When a logical 1 is read, this bit indicates that a cell with a header matching the receive header value and mask criteria was received.

IdleRcvd(2) When a logical 1 is read, this bit indicates that a cell with a header matching the receive idle cell header value and mask criteria was received.

NonMatch(2) When a logical 1 is read, this bit indicates that a cell with a header not matching either the receive cell or idle cell criteria was received.

NonZerGFC(2) When a logical 1 is read, this bit indicates that a cell with a Non-zero GFC field in the header was received.

NOTE: (1) This status reflects the current state of the circuit.
(2) This status indicates an event that occurred since the register was last read.

3.2.6 Counters

This section describes the CX2836x's counters. When the counters fill, they saturate and do not rollover. The counts have been sized to ensure against saturation within a one-second interval. Therefore, when one-second latching is enabled, the counters are read and cleared before they can saturate. All counters are cleared when read.

0x30—IDLECNTL (Receive Idle Cell Counter—Low Byte)

Receive idle cell counter.

7	6	5	4	3	2	1	0
IDLECNTL[7]	IDLECNTL[6]	IDLECNTL[5]	IDLECNTL[4]	IDLECNTL[3]	IDLECNTL[2]	IDLECNTL[1]	IDLECNTL[0]

IDLECNTL[7:0] Receive idle cell counter low byte.

0x31—IDLECNTM (Receive Idle Cell Counter—Middle Byte)

Receive idle cell counter.

7	6	5	4	3	2	1	0
IDLECNTM[7]	IDLECNTM[6]	IDLECNTM[5]	IDLECNTM[4]	IDLECNTM[3]	IDLECNTM[2]	IDLECNTM[1]	IDLECNTM[0]

IDLECNTM[7:0] Receive idle cell counter middle byte.

0x32—IDLECNTH (Receive Idle Cell Counter—High Byte)

Receive idle cell counter.

7	6	5	4	3	2	1	0
—	—	—	—	—	IDLECNTH[2]	IDLECNTH[1]	IDLECNTH[0]

IDLECNTH[7:0] Receive idle cell counter high byte.

0x33—LOCDCNT (LOCD Event Counter)

The LOCDCNT counter tracks the number of LOCD events.

7	6	5	4	3	2	1	0
LOCDCnt[7]	LOCDCnt[6]	LOCDCnt[5]	LOCDCnt[4]	LOCDCnt[3]	LOCDCnt[2]	LOCDCnt[1]	LOCDCnt[0]

LOCDCnt[7:0] LOCD event counter.

0x34—TXCNTL (Transmitted Cell Counter—Low Byte)

The TXCNTL counter tracks the number of transmitted cells. This byte of the counter should be read first.

7	6	5	4	3	2	1	0
TxCnt[7]	TxCnt[6]	TxCnt[5]	TxCnt[4]	TxCnt[3]	TxCnt[2]	TxCnt[1]	TxCnt[0]

TxCnt[7:0] Transmitted cell counter low byte.

0x35—TXCNTM (Transmitted Cell Counter—Mid Byte)

The TXCNTM counter tracks the number of transmitted cells.

7	6	5	4	3	2	1	0
TxCnt[15]	TxCnt[14]	TxCnt[13]	TxCnt[12]	TxCnt[11]	TxCnt[10]	TxCnt[9]	TxCnt[8]

TxCnt[15:9] Transmitted cell counter mid-byte.

0x36—TXCNTH (Transmitted Cell Counter—High Byte)

The TXCNTH counter tracks the number of transmitted cells.

7	6	5	4	3	2	1	0
—	—	—	—	—	TxCnt[18]	TxCnt[17]	TxCnt[16]

TxCnt[18:16] Transmitted cell counter bit high byte.

0x37—CORRCNT (Corrected HEC Error Counter)

The CORRCNT counter tracks the number of corrected HEC errors.

7	6	5	4	3	2	1	0
CorrCnt[7]	CorrCnt[6]	CorrCnt[5]	CorrCnt[4]	CorrCnt[3]	CorrCnt[2]	CorrCnt[1]	CorrCnt[0]

CorrCnt[7:0] Corrected HEC Error counter.

0x38—RXCNTL (Received Cell Counter—Low Byte)

The RXCNTL counter tracks the number of received cells. This byte of the counter should be read first.

7	6	5	4	3	2	1	0
RxCnt[7]	RxCnt[6]	RxCnt[5]	RxCnt[4]	RxCnt[3]	RxCnt[2]	RxCnt[1]	RxCnt[0]

RxCnt[7:0] Received cell counter low byte.

0x39—RXCNTM (Received Cell Counter—Mid Byte)

The RXCNTM register tracks the number of received cells.

7	6	5	4	3	2	1	0
RxCnt[15]	RxCnt[14]	RxCnt[13]	RxCnt[12]	RxCnt[11]	RxCnt[10]	RxCnt[9]	RxCnt[8]

RxCnt[15:8] Received cell counter mid-byte.

0x3A—RXCNTH (Received Cell Counter—High Byte)

The RXCNTH counter tracks the number of received cells.

7	6	5	4	3	2	1	0
—	—	—	—	—	RxCnt[18]	RxCnt[17]	RxCnt[16]

RxCnt[18:16] Received cell counter bit 16.

0x3B—UNCCNT (Uncorrected HEC Error Counter)

The UNCCNT counter tracks the number of uncorrected HEC errors.

7	6	5	4	3	2	1	0
UncCnt[7]	UncCnt[6]	UncCnt[5]	UncCnt[4]	UncCnt[3]	UncCnt[2]	UncCnt[1]	UncCnt[0]

UncCnt[7:0] Uncorrected HEC Error Counter

0x3C—NONCNTL (Non-matching Cell Counter—Low Byte)

The NONCNTL counter tracks the number of non-matching cells. This byte of the counter should be read first.

7	6	5	4	3	2	1	0
NonCnt[7]	NonCnt[6]	NonCnt[5]	NonCnt[4]	NonCnt[3]	NonCnt[2]	NonCnt[1]	NonCnt[0]

NonCnt[7:0] Non-matching cell counter low byte.

0x3D—NONCNTH (Non-matching Cell Counter—High Byte)

The NONCNTH counter tracks the number of non-matching cells.

7	6	5	4	3	2	1	0
NonCnt[15]	NonCnt[14]	NonCnt[13]	NonCnt[12]	NonCnt[11]	NonCnt[10]	NonCnt[9]	NonCnt[8]

NonCnt[15:8] Non-matching cell counter high byte.

3.3 PLCP Registers

The control/status register name assignments are the same for each port and are shown below with the offset from the base address listed in the CX2836x address map.

0x00—PLCPSEL (PLCP Mode Select Register)

7	6	5	4	3	2	1	0
PLCPSel	8kLock[1]	8kLock[0]	—	—	—	—	—

Default after reset: 00

PLCPSel When written to 1, PLCP mapping mode is selected; when written to 0, direct cell mapping mode is selected.

8kLock[1:0] 00 = the transmit PLCP frame is locked to the receive PLCP frame reference
01 = the transmit PLCP frame is locked to the external 8 kHz reference input
10 = the transmit PLCP frame is generated with cycle stuffing for a nominal 8 kHz frame rate
11 = the transmit PLCP frame is locked to the external 8 kHz reference input

0x01—PLCPOVH (PLCP Overhead Control Register)

7	6	5	4	3	2	1	0
DisA1A2	DisPOI	DisB1	DisC1	AutoFEBE	InsFrmErr(1)	InsBIPErr(1)	InsFebeErr(1)

Default after reset: 08

DisA1A2 When written to 1, the A1 and A2 overhead octets in the PLCP frame are generated as 00h.

DisPOI When written to 1, the POI octets in the PLCP frame are generated as 00h.

DisB1 When written to 1, the B1 octet in the PLCP frame are generated as 00h.

DisC1 When written to 1, the C1 octet in the PLCP frame are generated as 00h.

AutoFEBE When written to 1, the FEBE field in the G1 octet are generated automatically in response to received BIP errors; when written to 0, the FEBE field in the G1 octet are from the upper nibble of the TXG1 register.

InsFrmErr[(1)] When written to 1, all A1 octets are inverted from the normal value for 1 PLCP frame.

InsBIPErr[(1)] When written to 1, the B1 octet are XORed with the value in the ERRPAT register for one frame.

InsFebeErr[(1)] When written to 1, the upper nibble of the G1 octet are the value in the upper nibble of the ERRPAT register for one frame.

NOTE: [(1)] These bits are cleared automatically by internal circuitry after the indicated error insertion has taken place. Clearing takes precedence over a simultaneous write operation to this register.

0x02—TXG1 (Transmit G1 Control Register)

7	6	5	4	3	2	1	0
TxFEBE[3]	TxFEBE[2]	TxFEBE[1]	TxFEBE[0]	TxYellow	TxLSS[2]	TxLSS[1]	TxLSS[0]

Default after reset: F0

TxFEBE[3:0] Transmit value when auto FEBE generation is disabled. Default value indicates to far-end that FEBE calculation is not supported.

TxYellow Transmit value for PLCP Yellow alarm bit in the G1 octet. When this bit is changed, the new value is transmitted in the corresponding G1 bit for at least 20 PLCP frames.

TxLSS[2:0] Transmit value for the LSS field in the G1 octet.

0x03—TXF1 (Transmit F1 Control Register)

7	6	5	4	3	2	1	0
TXF1[7]	TXF1[6]	TXF1[5]	TXF1[4]	TXF1[3]	TXF1[2]	TXF1[1]	TXF1[0]

Default after reset: 00

TXF1[7:0] Transmit value for the F1 octet.

0x04—CPSTAT (Receive PLCP Status Register)

7	6	5	4	3	2	1	0
PLCPOOF	PLCPLOF	PLCPYellow	PLCPFrmErr	PLCPBIPErr	PLCPFebeErr	AllOnesFEBE	InvalFEBE

PLCPOOF(2) PLCP Out Of Frame indication is set when the PLCP framing state machine cannot locate correct PLCP frame structure.

PLCPLOF(2) PLCP Loss Of Frame indication is set when PLCPOOF is active for 8 frames. Indication is cleared when valid framing is found.

PLCPYellow(2) PLCP Yellow alarm indication set when the received Yellow Alarm bit in the G1 octet is high for 10 consecutive PLCP frames. This bit is cleared when the received Yellow Alarm bit in the G1 octet is low for 10 consecutive PLCP frames.

PLCPFrmErr(1) PLCP Frame Error indication is set when an A1, A2, or POI octet error is detected.

PLCPBIPErr(1) PLCP BIP Error indication is set when a B1 BIP error is detected.

PLCPFebeErr(1) PLCP FEBE Error indication is set when a FEBE error is detected in the G1 octet. Only received error values from 0001 through 1000 are indicated in this status bit.

AllOnesFEBE(1) This indication is set when a FEBE value of 1111 is received in the G1 octet.

InvalFEBE(1) This indication is set when a FEBE value of 1001 through 1110 is received in the G1 octet.

NOTE: (1) This status shows an event that has occurred since the register was last read.
(2) This status reflects the current state of the circuit.

0x05—PLCPINT (PLCP Interrupt Status Register)

7	6	5	4	3	2	1	0
PLCPOOFInt	PLCPLOFInt	PLCPYellInt	PLCPFrmInt	PLCPBIPInt	PLCPFebeInt	InvalFEBEInt	F1Int

PLCPOOFInt[(2)] This bit indicates that a PLCPOOF interrupt has occurred.

PLCPLOFInt[(2)] This bit indicates that a PLCPLOF interrupt has occurred.

PLCPYellInt[(2)] This bit indicates that a PLCP Yellow Alarm interrupt has occurred.

PLCPFrmInt[(1)] This bit indicates that a PLCP Frame Error interrupt has occurred.

PLCPBIPInt[(1)] This bit indicates that a PLCP BIP Error interrupt has occurred.

PLCPFebeInt[(1)] This bit indicates that a PLCP FEBE Error interrupt has occurred.

InvalFEBEInt[(1)] This bit indicates that an invalid or all-1s FEBE interrupt has occurred.

F1Int[(1)] This bit indicates that a new RXF1 value has been received.

NOTE: [(1)] Single event interrupt-only a positive transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.
[(2)] Dual event interrupt-either a positive or negative transition on the corresponding status bit causes this interrupt to occur. Reading the interrupt register clears the interrupt.

0x06—ENPLCP (PLCP Interrupt Enable Control Register)

7	6	5	4	3	2	1	0
EnPLCPOOF	EnPLCPLOF	EnPLCPYell	EnPLCPFrm	EnPLCPBIP	EnPLCPFebe	EnInvalFEBE	EnF1

Default after reset: 00

EnPLCPOOF This bit enables the PLCPOOF interrupt.

EnPLCPLOF This bit enables the PLCPLOF interrupt.

EnPLCPYell This bit enables the PLCP Yellow Alarm interrupt.

EnPLCPFrm This bit enables the PLCP Frame Error interrupt.

EnPLCPBIP This bit enables the PLCP BIP Error interrupt.

EnPLCPFebe This bit enables the PLCP FEBE Error interrupt.

EnInvalFEBE This bit enables the invalid FEBE interrupt.

EnF1 This bit enables the RXF1 interrupt.

0x07—RXF1 (Receive F1 Status Register)

7	6	5	4	3	2	1	0
RXF1[7]	RXF1[6]	RXF1[5]	RXF1[4]	RXF1[3]	RXF1[2]	RXF1[1]	RXF1[0]

RXF1[7:0] Receive value for the F1 octet.

0x08—B1CNTL (PLCP BIP Error Counter—low byte)

7	6	5	4	3	2	1	0
B1Cnt[7]	B1Cnt[6]	B1Cnt[5]	B1Cnt[4]	B1Cnt[3]	B1Cnt[2]	B1Cnt[1]	B1Cnt[0]

B1Cnt[7:0] PLCP BIP error counter low byte.

0x09—B1CNTH (PLCP BIP Error Counter—high byte)

7	6	5	4	3	2	1	0
B1Cnt[15]	B1Cnt[14]	B1Cnt[13]	B1Cnt[12]	B1Cnt[11]	B1Cnt[10]	B1Cnt[9]	B1Cnt[8]

B1Cnt[15:8] PLCP BIP error counter high byte.

0x0A—FEBECNTL (PLCP FEBE Error Counter—low byte)

7	6	5	4	3	2	1	0
FEBECnt[7]	FEBECnt[6]	FEBECnt[5]	FEBECnt[4]	FEBECnt[3]	FEBECnt[2]	FEBECnt[1]	FEBECnt[0]

FEBECnt[7:0] PLCP FEBE error counter low byte.

0x0B—FEBECNTH (PLCP FEBE Error Counter—high byte)

7	6	5	4	3	2	1	0
FEBECnt[15]	FEBECnt[14]	FEBECnt[13]	FEBECnt[12]	FEBECnt[11]	FEBECnt[10]	FEBECnt[9]	FEBECnt[8]

FEBECnt[15:8] PLCP FEBE error counter high byte.

3.4 Framer Registers

0x20—CR00 (Mode Control Register)

7	6	5	4	3	2	1	0
LineLp	SourceLp	TxAlm1	TxAlm0	—	—	E3Frm	CbitP/832

Default after reset: 00

Direction: Read/Write

Modification: Bits 4–7: dynamic, bits 0–1: static

LineLp Shallow Line Loopback Enable—Set to enable loopback in the external direction (back to network). This loopback connects the received data stream before B3ZS/HDB3 decoding to the transmitter. All data and Opportunity bits are looped, and Bipolar Code Violations (BPVs) are fully preserved per ANSI standard T1.404. The received data is presented to all receiver blocks, and is present on the receiver output pins.

A dynamic change of this bit can cause loss of data for a few clock cycles, until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks. After writing this bit, the microprocessor should not access any of the device registers (read/write) for 20 slowest clock cycles.

SourceLp Source Loopback Enable—Set to enable the loopback in the internal direction. This loopback connects the encoded transmitter data and clock directly to receiver B3ZS/HDB3 decoder. Transmission of data on the line is not affected by this loopback.

A dynamic change of this bit can cause loss of data for a few clock cycles, until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks. After writing to this bit, the microprocessor should not access any of the device registers (read or write) for 20 slowest clock cycles.

TxAlm1,0 Transmit Alarm Control—Used to control transmission of various alarm signals. In DS3 mode, AIS, idle, and Yellow Alarm signals on the outgoing DS3 stream are controlled as follows:

TxAlm1	TxAlm0	Alarm Action
0	0	Normal, No Alarms Transmitted
0	1	Yellow Alarm (X-bits low) Transmitted
1	0	Idle Code Transmitted
1	1	AIS Transmitted

In E3-G.751 and E3-G.832 modes, the TxAlm0 bit is set high to transmit the E3 AIS signal. The TxAlm1 bit is set high to transmit the E3 Yellow Alarm (A-bit or RDI bit high). TxAlm0 bit has precedence in E3 mode.

E3Frm E3 Framing Mode—Enables the E3 mode framing and transmission circuitry. When cleared, DS3 mode is active. The specific framing format is defined according to CbitP/832 bit.

CbitP/832 C-Bit Parity/E3-G.832 Mode—Selects which type of framing is present on the transmitted DS3/E3 signal.

E3Frm	CbitP/832	Framing Mode
0	0	DS3-M13/M23
0	1	DS3-C-Bit Parity
1	0	E3-G.751
1	1	E3-G.832

0x21—CR01 (Counter Interrupt Control Register)

The Counter Interrupt Control register is provided to enable or disable individual interrupt sources. To enable an interrupt for a particular counter, the control bit corresponding to that counter must be set high in the Interrupt Control register. This enables the interrupt from that source to be asserted on the MINTR* output pin. If a counter has its interrupt control bit set low, interrupts from this counter are masked from asserting on MINTR*.

7	6	5	4	3	2	1	0
EXZCtrlE	XDgrCtrlE	LCVCtrlE	FEBECtrlE	PthCtrlE	FerrCtrlE	PDgrCtrlE	ParCtrlE

Default after reset: 00

Direction: Read/Write

Modification: Dynamic

EXZCtrlE Excessive Zeros Counter Interrupt Enable—A control bit that allows interrupts from the DS3/E3 EXZ Counter to appear on MINTR* pin.

XDgrCtrlE X-bits Disagreement Counter Interrupt Enable—A control bit that allows interrupts from the DS3/Disagreement Counter to appear on MINTR* pin.

LCVCtrlE Line Code Violation Counter Interrupt Enable—A control bit that allows interrupts from the DS3/E3LCV Counter to appear on MINTR* pin.

FEBECtrlE FEBE Event Counter Interrupt Enable—A control bit that allows interrupts from the DS3 FEBE/E3-G.832 REI Event Counter to appear on MINTR* pin.

PthCtrlE Path Parity Error Counter Interrupt Enable—A control bit that allows interrupts from the Path Parity Error Counter to appear on MINTR* pin.

FerrCtrlE Frame Error Counter Interrupt Enable—A control bit that allows interrupts from the Frame Error Counter to appear on MINTR* pin.

PDgrCtrlE Disagreement Counter Interrupt Enable—A control bit that allows interrupts from the DS3 P Disagreement Counters to appear on the MINTR* output pin.

ParCtrlE Parity Error Counter Interrupt Enable—A control bit that allows interrupts from the DS3 Parity/E3-G.832 BIP-8 Error Counter to appear on MINTR* pin.

0x22—CR02 (Alarm Start Interrupt Control Register)

7	6	5	4	3	2	1	0
—	—	SEFStrtIE	LOSStrtIE	IdleStrtIE	YelStrtIE	AISStrtIE	OOFStrtIE

Default after reset: 00

Direction: Read/Write

Modification: Dynamic

SEFStrtIE Severely Errored Frame Start Interrupt Enable—Set to enable interrupts to be asserted on MINTR* pin due to detection of SEF event start in DS3 mode. When the receiver detects an SEF condition start, the interrupt is asserted and the SEFStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of SEF start sets the appropriate status bit; however, an interrupt is not activated. This bit has no effect in E3-G.751 and E3-G.832 modes.

LOSStrtIE Loss of Signal Start Interrupt Enable—Set to enable interrupts to be asserted on MINTR* pin, due to a detection of LOS condition start in all modes. When a LOS condition start is detected, the interrupt is asserted, and the LOSStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of LOS start sets the appropriate status bit; however, an interrupt is not activated.

IdleStrtIE Idle Interrupt Start Enable—Set to enable interrupts to appear on MINTR* due to detection of Idle event start in DS3 mode. When the receiver detects an Idle start, the interrupt is asserted, and the IdleStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of Idle start sets the appropriate status bit; however, an interrupt is not activated. This bit has no effect in E3-G.751 and E3-G.832 modes.

YelStrtIE Yellow Alarm Start Interrupt Enable—Set to enable interrupts to be asserted on MINTR* due to detection of RAI/RDI event start in all modes. When the receiver detects an RAI/RDI event start, the interrupt is asserted, and YelStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of RAI/RDI start sets the appropriate status bit; however, an interrupt is not activated.

AISStrtIE Alarm Indication Signal Start Interrupt Enable—Set to enable interrupts to be asserted on MINTR* due to detection of AIS event start in all modes. When the receiver detects an AIS event start, the interrupt is asserted, and AISStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of AIS start sets the appropriate status bit; however, an interrupt is not activated.

OOFStrtIE Out of Frame Start Interrupt Enable—Set to enable interrupts to be asserted on MINTR* pin due to detection of OOF condition start in all modes. When the receiver detects an OOF condition start, the interrupt is asserted, and OOFStrt bit in Alarm Start Interrupt Status register is set. When this bit is cleared, detection of OOF start sets the appropriate status bit; however, an interrupt is not activated.

0x23—CR03 (Alarm End Interrupt Control Register)

NOTE: Reserved bits in Control registers must be set to 0.

7	6	5	4	3	2	1	0
—	—	—	LOSEndIE	IdleEndIE	YelEndIE	AISEndIE	OOFEndIE

Default after reset: 00

Direction: Read/Write

Modification: Dynamic

LOSEndIE Loss of Signal End Interrupt Enable—Set to enable interrupts to be asserted on MINTR* pin due to detection of LOS condition end in all modes. When a LOS condition end is detected, the interrupt is asserted, and LOSEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of LOS end sets the appropriate status bit; however, an interrupt is not activated.

IdleEndIE Idle Interrupt End Enable—Set to enable interrupts be asserted on MINTR* pin due to detection of Idle event end in DS3 mode. When the receiver detects an Idle end, the interrupt is asserted, and IdleEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of Idle end sets the appropriate status bit; however, an interrupt is not activated. This bit has no effect in E3-G.751 and E3-G.832 modes.

YelEndIE Yellow Alarm End Interrupt Enable—Set to enable interrupts to be asserted on MINTR* pin due to detection of RAI/RDI event end in all modes. When the receiver detects an RAI/RDI event end, the interrupt is asserted, and YelEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of RAI/RDI end sets the appropriate status bit; however, an interrupt is not activated.

AISEndIE Alarm Indication Signal End Interrupt Enable—Set to enable interrupts to be asserted on MINTR* pin due to detection of AIS event end in all modes. When the receiver detects an AIS event end, the interrupt is asserted, and AISEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of AIS end sets the appropriate status bit; however, an interrupt is not activated.

OOFEndIE Out of Frame End Interrupt Enable—Set to enable interrupts be asserted on MINTR* pin due to detection of OOF condition end in all modes. When the receiver detects an OOF condition end, the interrupt is asserted, and OOFEnd bit in Alarm End Interrupt Status register is set. When this bit is cleared, detection of OOF end sets the appropriate status bit; however, an interrupt is not activated.

3.4.1 Feature Control Registers

0x24—CR04 (Feature1 Control Register)

7	6	5	4	3	2	1	0
TxAMI	RxAMI	NRZMod	—	—	FEBEC/PT[1]	FEBEC/PT[2]	FEBEC/PT[3]

Default after reset: 07

Direction: Read/Write

Modification: Bits 0–2: dynamic; bits 5–7: static

TxAMI Transmit AMI Mode—Set high to enable AMI line coding on TxPOSO and TxNEGO (no B3ZS/HDB3 encoding or decoding). When cleared, B3ZS/HDB3 line coding is used on these pins.

NOTE: This bit is effective only when NRZMod bit is cleared.

RxAMI Receive AMI Mode—Set high to enable AMI line coding on RxPOSI and RxNEGI (no B3ZS/HDB3 encoding or decoding). When cleared, these pins use B3ZS/HDB3 line coding.

NOTE: This bit is effective only when NRZMod bit is cleared.

NRZMod NRZ Mode—Set high to disable bipolar (B3ZS/HDB3 or AMI) encoding or decoding and provide a unipolar NRZ line code on TxPOSO/TxNEGO and RxPOSI/RxNEGI. Setting this bit disables and bypasses the encoder and decoder circuits. The unipolar output appears at the TxPOSO pin while TxNEGO pin is continuously low, and the clock is available on TCLKO pin. The unipolar input should appear on RxPOSI, while RxNEGI can be tied to the LCV output of the LIU and be used as an increment control of the LCV counter.

NRZMod	RxAMI	TxAMI	Description
0	0	X	B3ZS/HDB3 encoded data on RxPOSI, RxNEGI
0	1	X	AMI encoded data on RxPOSI, RxNEGI
0	X	0	B3ZS/HDB3 encoded data on TxPOSO, TxNEGO
0	X	1	AMI encoded data on TxPOSO, TxNEGO
1	X	X	NRZ data on TxPOSO, RxPOSI; TxNEGO is set to 0; RxNEGI is used as an LCV input from the LIU (if unused, should be tied low)

FEBEC/PT[1:3] FEBE Pattern/Payload Type Bit Field—In DS3 mode set to the 3-bit sequence that is sent each time a FEBE indication is transmitted in C-bit parity mode. This pattern is automatically transmitted when the ExtFEBE/Cj-bit in the Transmit Overhead Insertion 1 Control register is cleared, and the receiver detects a framing or path parity error. This pattern must not be all 1s to indicate a FEBE to the far end. An all-1s pattern disables FEBE transmission and should not be used for any other purpose. In E3-G.832 mode set to the 3-bit pattern that is transmitted every frame in the payload type field in the MA byte.

In both modes, FEBEC/PT[1] bit is transmitted first and FEBEC/PT[3] bit is transmitted last. In both modes, writing a new value to this byte takes effect only starting from the next transmitted frame. In DS3-M13/M23 and E3-G.751 modes, this field has no effect.

0x25—CR05 (Feature2 Control Register)

7	6	5	4	3	2	1	0
—	—	TxLOS	TxOvhMrk	TXSYOut	TXSYIn	TxInvClk	LtxCkRis

Default after rest: 01

Direction: Read/Write

Modification: Bit 5: dynamic, bits 0–4: static

TxLOS Transmit Loss of Signal—When set, this bit results in the generation of all-0s (LOS) on the transmit line side. Setting this bit overrides any other programmed or inserted payload and overhead pattern with 0s.

TxOvhMrk Transmit Overhead Bits Mark—This bit controls the behavior of TxSync pin when programmed to be driven as an output. When set, TxSync marks the bit positions of all Opportunity bits. When cleared, TxSync marks the beginning of a new frame.

TXSYOut TxSync Pin Output Control—When set, the TxSync pin is an output. The transmitter circuit generates its own frame synchronization mechanism and signals the frame start or the Opportunity bit positions (according to TxOvhMrk bit) on TxSync pin to the system. When cleared, TxSync can be an input or undefined according to the value of TXSYIn bit in this register.

NOTE: TXSYOut and TXSYIn bits must not be set at the same time.

TXSYIn TxSync Pin Input Control—When set, the TxSync pin is an input. The system generates a synchronization pulse and the transmitter circuit acts according to it. When cleared, TxSync can be an output or undefined according to the value of TXSYOut bit in this register.

NOTE: TXSYOut and TXSYIn bits must not be set at the same time.

TxInvClk Transmit System Side Inverted Clocks—This bit controls the polarity of TXGAPCK and TEXTCK output clocks. When the bit is cleared, TXGAPCK and TEXTCK rising edges are derived from TxCKI falling edge. In this mode, both clock gaps are active-low. When this bit is set, TXGAPCK and TEXTCK are inverted, TXGAPCK and TEXTCK falling edges are derived from TxCKI falling edge. In this mode, both clock gaps are active-high.

LTxCkRis LIU Transmit Clock Polarity Control—Used to define the TxCKO edge upon which the transmitter output data on TxPOSO and TxNEGO pins are sampled by the LIU. When set, the data are clocked out by the chip on the falling edge of TxCKO. It is sampled by the LIU on the rising edge of TxCKO. When cleared, the data are clocked out by the chip on the rising edge of TxCKO. It is sampled by the LIU on the falling edge of TxCKO.

0x26—CR06 (Feature3 Control Register)

7	6	5	4	3	2	1	0
PayldLp	RlineLp	TxFEACIE	FEACSin	—	RxFEACSNEIE	RxFEACIdleIE	RxFEACIE

Default after reset: 00

Direction: Read/Write

Modification: Bit 4: static, bits 0–2, 5–7: dynamic

PayldLp Payload Loopback Enable—Set to enable a payload loopback from the receiver circuit through the transmitter circuit back to the network. This loopback connects the received payload (after decoding, frame recovery and overhead extraction) to the transmitter input, where it is framed and encoded again. The received data is still present on the receiver output pins. A dynamic change of this bit can cause loss of data for a few clock cycles, until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks. After writing to this bit the microprocessor should not access any of the device registers (read/write) for 20 slowest clock cycles.

RlineLp Remote Line Loopback Enable—Set to enable loopback after decoding or encoding back to the network. Data output of the B3ZS/HDB3 decoder connects to the transmitter encoder input. Line Code Violations (LCV) are not preserved in this loopback. The received data is still presented to all receiver blocks and is present on the receiver outputs.

A dynamic change of this bit can cause loss of data for a few clock cycles until the channel is internally synchronized. Activation or deactivation of a loopback causes internal circuits to switch between clocks, after writing to this bit the microprocessor should not access any of the device registers (read or write) for 20 slowest clock cycles.

TxFEACIE Transmit FEAC Interrupt Enable—A control bit that allows interrupts from the FEAC transmitter to be asserted on MINTR* pin when in DS3-C-Bit Parity mode. When in single mode, the interrupt is asserted after every transmission of the code word written in the Transmit FEAC Channel Byte register. When in repetitive mode, the interrupt is asserted once the code word is transmitted 10 times.

FEACSin FEAC Channel in Single Mode—In DS3-C-Bit Parity mode set to enable FEAC channel (in the transmitter and the receiver) in a single mode, i.e., assert an interrupt after a single reception or transmission of a code word. When clear, repetitive mode is enabled, i.e., an interrupt is asserted after completion of 10 repetitions of code word reception or transmission. In DS3-M13/M23, E3-G.751, and E3-G.832 modes, this bit has no effect.

RxFEACSNEIE Receive FEAC Stack Not Empty Interrupt Enable—A control bit that allows interrupts to appear on MINTR* pin due to detection of the FEAC stack being not empty (i.e., Receive FEAC stack byte is holding valid data). This bit is active both in single and repetitive modes.

RxFEACIdleIE Receive FEAC channel Idle Interrupt Enable—A control bit that allows interrupts to be asserted on MINTR* pin due to detection of the start of an idle pattern over FEAC channel by the receiver circuit. This bit is active both in single and repetitive modes.

RxFEACIE Receive FEAC Interrupt Enable—A control bit that allows interrupts from the FEAC receiver to appear on MINTR* pin when in DS3-C-Bit Parity mode. When a legal code word is detected by the receiver (see Far-End Alarm and Control Channel Reception paragraph) this interrupt is asserted.

0x27—CR07 (Feature4 Control Register)

NOTE: This control register has an effect only in E3-G.832 mode. In DS3 and E3-G.751 modes the content of this register is ignored.

7	6	5	4	3	2	1	0
—	SSMEn	SSM[1]/TM	SSM[2]	SSM[3]	SSM[4]	MAPD[1]	MAPD[2]

Default after reset: 00

Direction: Read/Write

Modification: Bits 0–5: dynamic, bit 6: static

SSMEn SSM Mode Enable—Set to enable usage of bit 8 in the MA byte as an SSM field and of bits 6–7 in the MA byte as a multiframe indicator (MI) field. When cleared, bit 8 in the MA byte is the timing marker (TM) field and bits 6–7 in the MA byte are used as payload dependent (PD) field.

SSM[1]/TM SSM MSB/Timing Marker Bit Field—When SSM mode is enabled (SSMEn bit is set), this bit is the MS bit (transmitted first) to be sent in the SSM field (bit 8 in MA byte). When MI field has a value of 00, SSM [1] is inserted in the frame. When SSM mode is disabled (SSMEn bit is cleared), this bit is the timing marker. It is inserted on every frame in bit 8 position in the MA byte.

SSM[2:4] SSM Bit Field—When SSM mode is enabled (SSMEn bit is set), set to the three LS bits pattern to be sent in the SSM field (bit 8 of MA byte) according to the multiframe phase indicated by MI field. When MI field has a value of 01, SSM [2] is inserted in the frame. When MI field has a value of 10, SSM [3] is inserted in the frame. When MI field has a value of 11, SSM [4] is inserted in the frame. When SSM mode is disabled, this field is ignored.

MAPD[1:2] Payload Dependent Field in MA byte—When SSM mode is disabled (SSMEn bit in this register is cleared) and ExtFEAC/PD bit in Transmit Overhead Insertion register 1 is cleared, this field is sent in every frame in bits 6–7 of the MA byte. MAPD [1] bit transmits first. If SSM mode is enabled or ExtFEAC/PD is set, this field is ignored.

0x28—CR08 (Feature5 Control Register)

7	6	5	4	3	2	1	0
RxAutoAll1	RefrmStp	RxAIS	RXAll1	RxOvhMrk	0	RxInvClk	LRxCkRis

Default after rest: 00

Direction: Read/Write

Modification: Bits 0–3: static, bits 4–6: dynamic, bit 7: static

RxAutoAll1 Receive Automatic All 1s—Set to enable automatic generation of an all-1s stream on RXDAT pin in response to a fault detection. When set and a LOS, OOF, AIS, or Idle are detected in DS3 mode or LOS, OOF, or AIS are detected in E3 mode, the data received on RXPOS, RXNEG is presented to the receiver circuit, but is not present on RXDAT pin. It is overwritten by an all-1s stream. The assertion of all 1s continues as long as one or more of these conditions is valid. When clear, all-1s sequence on RXDAT pin occurs due to RxAll1 bit in this register. RxAll1 and RxAIS bits have precedence over the RxAutoAll1 bit.

RefrmStp Reframe Mechanism Stop—This bit controls the behavior of the frame-search mechanism. When this bit is set, no frame-search is conducted regardless of OOF status. When it has been cleared, frame-search resumes shifted forward by one bit from the current frame position, until a new frame is located. When it is cleared, searching occurs in response to an OOF status.

NOTE: To produce a forced reframe, the microprocessor usually needs two write cycles, the first to write 1 to the bit, and then to write 0 to it.

RxAIS Receive Data Stream AIS—When set, enables driving of an AIS pattern in all DS3 and E3 modes on RXDAT pin. Data received on RXPOS, RXNEG is presented to the receiver circuit but is not present on RXDAT pin. Detection and the count of errors, alarms, and events continue while this mode operates. When cleared, data received on RXPOS, RXNEG, and processed by the receiver circuit is present on RXDAT pin. If both RxAll1 and RxAIS are active, a data stream of all 1s is generated.

RxAll1 Receive Data Stream is All 1s—When set, enables driving an all-1s stream on RXDAT pin. Data received on RXPOS, RXNEG is presented to the receiver circuit, but is not present on RXDAT pin. Detection and the count of errors, alarms, and events continue while this mode operates. When cleared, the data received on RXPOS, RXNEG, and processed by the receiver circuit is present on RXDAT pin. If both RxAll1 and RxAIS are active, data stream of all 1s is generated.

RxOvhMrk Receive Overhead Bits Mark—This bit controls behavior of the RxSYNC pin. When set, RxSYNC marks the bit positions of all Opportunity bits. When cleared, RxSYNC marks the beginning of a new frame.

RxInvClk Receive System Side Inverted Clocks—This bit controls the polarity of RxGCKO and REXTCKO output clocks. When the bit is cleared, RxGCKO and REXTCKO rising edges are in parallel to the data change on RXDAT pin. In this mode, both clock gaps are active low. When this bit is set, RxGCKO and REXTCKO are inverted. The RxGCKO and REXTCKO falling edges are in parallel to the data change on RxDATO pin. In this mode, both clock gaps are active high.

LRxCkRis LIU Receive Clock Polarity Control—Used to define the RxCKI edge upon which the receiver input data on RxPOSI, RxNEGI pins are clocked out by the LIU. When set, data are sampled by the device on the falling edge of RxCKI, therefore it is clocked out by the LIU on the rising edge of RxCKI. When clear, data are sampled by the chip on the rising edge of RxCKI, therefore it is clocked out by the LIU on the falling edge of RxCKI.

3.4.2 Transmitter Registers

The Transmit Overhead Insertion Control registers CR09 and CR10 are provided to enable insertion of different overhead fields from these sources:

- Internal automatic generation
- Internal registers programmed by the microprocessor
- The system via the data stream
- The system via TEXTI[11:0] pins

NOTE: Not all sources are available for every overhead field in every mode. Some control bits have no effect in a specific mode. Some bits have multiple meanings; it depends on the working mode.

0x29—CR09 (Transmit Overhead Insertion1 Control Register)

7	6	5	4	3	2	1	0
DLMod[2]	DLMod[1]	DLMod[0]	AutoRAI	ExtFEBE/Cj	ExtCP/TR	ExtFEAC/PD	ExtDat

Default after reset: 00

Direction: Read/Write

Modification: Bits 0–2, 4: static, bits 6–7: dynamic, bit 5: dynamic for DL (G.832) and static for reserved C-bits (DS3), bit 3: dynamic for Cj and static for FEBE

DLMod[2:0] Data Link Mode—This field is interpreted differently in different working modes. In E3-G.832 mode, it is a three-bit field that determines the source of NR and GC bytes. In E3-G.751, only DLMod [2:1] determines the source of the N-bit, while DLMod [0] has no effect. In DS3-C Bit Parity mode DLMod [2:1] determines the source of the data link (Cb5), and DLMod [0] determines the source of the reserved C-bits. In DS3-M13/M23, this field has no effect.

NOTE: If the system wants to change the source of the data link (i.e., internal FIFO to TEXTI pin), it must first disable the data link and then enable it by setting the appropriate mode. Another example is that when changing the type of byte processed by the internal HDLC circuit (NR to GC or vice versa) in E3-G.832 mode, the data link must be disabled first for both (by writing 0 to all three bits).

Tables 3-10 and 3-11 detail the interpretation of this field in the different modes.

Table 3-10. DS3-C-Bit Parity/E3-G.751 Mode Field Interpretation

DLMod[2]	DLMod[1]	Description
0	X	Transmit Data Link circuit is disabled, and the framer automatically sends the all-1s pattern on Cb5 bits/N-bit.
1	0	Data link data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit.
1	1	Data link data is inserted through the TEXTI pin and is unaffected by the internal HDLC circuit.

DS3-C Bit Parity

DLMod [0] controls the reserved C-bits (C12, Cb2, Cb6, and Cb7) generation. When set, these bits are inserted via the TEXTI pin. When cleared, these bits are automatically generated as all 1s. In this mode, the bit is static.

Table 3-11. E3-G.832 Mode Field Interpretation

DLMod[2]	DLMod[1]	DLMod[0]	Description
0	0	0	Data link on the NR byte is disabled and the chip automatically generates an FF(h) pattern on these bits. Data link on the GC byte is disabled and the chip automatically generates an FF(h) pattern on these bits.
0	0	1	Data link on the NR byte is disabled, and the chip automatically generates an FF(h) pattern on these bits. GC data is inserted via the TEXTI pin and is unaffected by the internal HDLC circuit.
0	1	0	Data link on the NR byte is disabled and the chip automatically generates an FF(h) pattern on these bits. GC data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit.
0	1	1	NR data is inserted via the TEXTI pin, it is unaffected by the internal HDLC circuit. Data link on GC byte is disabled and the chip automatically generates FF(h) pattern on these bits.
1	0	0	NR data is inserted via the TEXTI pin; it is unaffected by the internal HDLC circuit. GC data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit.
1	0	1	NR data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit. GC data is inserted via the TEXTI pin and is unaffected by the internal HDLC circuit.
1	1	0	NR data is inserted through the Transmit Data Link FIFO buffer and is processed by the internal HDLC circuit. Data link on GC byte is disabled and the chip automatically generates an FF(h) pattern on these bits.
1	1	1	Both NR and GC data are inserted via the TEXTI pin; they are unaffected by the internal HDLC circuit.

AutoRAI Automatic RAI/RDI Generation Control—Set to enable automatic generation of the RAI or RDI alarm in response to a fault detection. When set, an automatic assertion of the RAI bit in E3-G.751 mode or RDI bit in E3-G.832 mode occurs once the receiver detects a LOS or OOF condition. The automatic assertion continues as long as one or more of these conditions is valid. The TxAlm [1] bit in the Mode Control register still effects RAI/RDI generation in E3 mode while this bit is set. When clear, RAI and RDI generation occurs due to the TxAlm [1] bit in the Mode Control register and there is no automatic generation.

NOTE: This bit has no effect in DS3 mode. Generation of an RAI alarm in DS3 mode is controlled only by TxAlm bits.

ExtFEBE/Cj External FEBE/Justification Control—Set to enable insertion of FEBE or Justification Control bits via the TEXTI pin. In DS3-C-Bit Parity mode, setting this bit enables insertion of FEBE field via TEXTI pin. In DS3-M13/M23 mode, setting this bit enables insertion of all C-bits (used for Justification Control) via TEXTI pin. In E3-G.751 mode, setting this bit enables insertion of all Cj-bits (used for Justification Control) via TEXTI pin. In E3-G.832 mode, setting this bit enables insertion of REI bit in MA byte via TEXTI pin. When this bit is cleared, FEBE bits are transmitted automatically upon detection of framing or CP error by the receiver according to the contents of FEBEC/PT field described in the Feature1 Control register, DS3-C-Bit Parity mode. In DS3-M13/M23 mode or E3-G.751 mode, Justification Control bits are inserted via the data stream when this bit is cleared. In E3-G.832 mode, the REI bit is set automatically by the transmitter upon detection of BIP-8 error if this bit is cleared.

ExtCP/TR External CP/Trail Trace Control—Set to enable insertion of CP-bits or TR byte via TEXTI pin. In DS3-C-Bit Parity mode, setting this bit enables insertion of CP field via TEXTI pin. In E3-G.832 mode, setting this bit enables insertion of Trail Trace byte via TEXTI pin. In E3-G.832, when this bit is cleared, the transmitter automatically transmits 00(h) on TR byte. In DS3-M13/M23 and E3-G.751 modes, this bit has no effect.

ExtFEAC/PD External FEAC/Payload Dependent/Multiframe Indicator Field Control—Set to enable insertion of FEAC channel or payload dependent field via TEXTI pin. In DS3-C-Bit Parity mode, setting this bit enables insertion of FEAC channel via TEXTI pin. In E3-G.832 mode, setting this bit enables insertion of payload dependent, multiframe indicator field in MA byte via TEXTI pin. When this bit is cleared, FEAC channel is inserted through a programmable register (Transmit FEAC Channel Byte) in DS3-C-Bit Parity mode. In E3-G.832, payload dependent field is inserted through a programmable register (MAPD field in Feature4 control register) when this bit is cleared and SSMEn bit (in Feature4 Control register) is also cleared. If SSMEn is set, i.e., bits 6–7 in MA byte are used as a multiframe indicator, the MI is internally produced cycling through the values 00, 01, 10, and 11 on an arbitrarily defined, 4-frame multiframe. In DS3-M13/M23 and E3-G.751 modes, this bit has no effect.

ExtDat External Data Control—Set to enable all Opportunity bits to be inserted via the data stream. When set, this bit overrides the rest of the control bits in this register and in the Transmit Overhead Insertion2 Control register. It disables internal generation of Opportunity bits (automatic or through programmable registers) and forces the device to use the Opportunity bits inserted in the data stream. When clear, overhead configuration is determined by the rest of the control bits as described above. This bit affects all modes. Setting of TxAlm [1:0] bits is effective even during ExtDat = 1.

0x2A—CR10 (Transmit Overhead Insertion2 Control Register)

7	6	5	4	3	2	1	0
—	—	—	—	ExtStf	ExtFrmAl	ExtP	ExtRAI

Default after reset: 00

Direction: Read/Write

Modification: Static

ExtStf External Stuff Bits—Set to enable insertion of Stuff Opportunity bits via TEXTI pin in DS3-M13/M23 and E3-G.751 modes. When clear, stuff bits are inserted with the payload. This bit has no affect in DS3-C-bit parity and E3-G.832 modes.

ExtFrmAl External Frame Alignment Bits—Set to enable insertion of F and M-bits (DS3 mode), FAS (E3-G.751), FA1 and FA2 (E3-G.832) bits via TEXTI pin. When clear, the frame alignment bits are automatically generated by the internal circuitry.

ExtP External P-Bit Control—Set to enable insertion of P-bits via TEXTI pin in DS3-C-Bit Parity and DS3-M13/M23 modes. When clear, P-bits are automatically calculated by the internal circuitry. In E3-G.751 and E3-G.832 modes, this bit has no effect.

ExtRAI External X/A/RDI-Bit Control—Set to enable insertion of X-bits (in DS3), A-bit (in E3-G.751), and RDI (in E3-G.832) via TEXTI pin. It affects E3 when AutoRAI bit is clear.

3.4.3 Receiver Registers

0x2B—CR11 (REXTCK Control Register)

The REXTCK Control register provides enabled marking of different fields through REXTCKO pin. Presentation of a field through REXTCKO pin does not prevent it from being ticked upon by the RxGCKO pin or from being processed via the microprocessor interface. Setting a bit in this register does not affect other control bits set in other registers. This enables monitoring of certain fields for testing, in addition to being processed by another mechanism. If a specific field should be presented only through the REXTCKO pin, it should be disabled from being presented on RxGCKO/ microprocessor interface in another control register.

7	6	5	4	3	2	1	0
ExtReserved/ GC	ExtDL/NR	ExtFEBE/A	ExtCP/TM	ExtFEAC/PD/ Stf	ExtAIC/Cj/TR	ExtFrm	AllRxExt

Default after reset: 00

Direction: Read/Write

Modification: Static

ExtReserved/GC External Reserved C-bits/GC Byte—Set to enable presentation of reserved C-bits (C12, C2, C6, C7) in DS3-C-Bit Parity mode or presentation of GC byte in E3-G.832 mode through REXTCKO pin. In DS3-M13/M23 and E3-G.751 modes, this bit is ignored.

ExtDL/NR External Data Link/NR Byte—Set to enable presentation of data link data through REXTCKO pin. The bits are output exactly as they were received (i.e., the HDLC circuit is bypassed). In DS3-C-Bit Parity mode, this bit enables presentation of C5 bits through REXTCKO pin. In E3-G.751 mode, this bit enables presentation of N-bit through REXTCKO pin. In E3-G.832 mode, this bit enables presentation of NR byte through REXTCKO pin. In DS3-M13/M23, this bit is ignored.

ExtFEBE/A External FEBE/REI/A-Bit—Set to enable presentation of FEBE field in DS3-C-Bit Parity mode or REI bit field in E3-G.832 mode through the REXTCKO pin. In E3-G.751 mode, set to enable presentation of A-bit through REXTCKO pin. In DS3-M13/M23 mode, this bit is ignored.

ExtCP/TM External Path Parity/Timing Marker/SSM—Set to enable presentation of CP field in DS3-C-Bit Parity mode or Timing Marker/SSM bit field in E3-G.832 mode through REXTCKO pin. In DS3-M13/M23 and E3-G.751 modes, this bit is ignored.

ExtFEAC/PD/Stf External FEAC/Payload Dependent/Multiframe Indicator/Stuff Opportunity Bits—Set to enable presentation of FEAC channel in DS3-C-Bit Parity mode or payload dependent/ multiframe indicator field in E3-G.832 mode or Stuff Opportunity bits in DS3 M13/M23 and in E3-G.751 modes through REXTCKO pin.

ExtAIC/Cj/TR External AIC/Justification Control/Trail Trace—In DS3-C-Bit Parity mode, set to enable presentation of application identification channel through REXTCKO pin. In DS3-M13/M23 and E3-G.751 modes, set to enable presentation of the Justification Control bits through the REXTCKO pin. In E3-G.832 mode, set to enable presentation of Trail Trace byte through REXTCKO pin.

ExtFrm External Framing Fields—In DS3 modes, set to enable presentation of M, F, X, and P-bits through the REXTCKO pin. In E3-G.751 mode, set to enable presentation of FAS field through the REXTCKO pin. In E3-G.832 mode, set to enable presentation of FA1, FA2, EM, RDI, and PT fields through REXTCKO pin.

AllRxExt All Received Data is External—Set to enable presentation of the complete frame; i.e., payload and Opportunity bits, through REXTCKO pin. This bit is available in all framing modes. When this bit is set, it overrides the rest of the bits in this register. Presentation of Opportunity bits through the RxGCKO pin or through the microprocessor interface in parallel to REXTCKO is determined by the Receive Overhead Control register and by the RxDLEn bit in Receive Data Link Control register.

0x2C—CR12 (Receive Overhead Control Register)

7	6	5	4	3	2	1	0
—	—	—	—	—	RxStfDat	RxCjDat	AllOVHDat

Default after reset: 00

Direction: Read/Write

Modification: Static

RxStfDat Received Stuff Opportunity Bits in the Data Stream—Set to enable presentation of the Stuff Opportunity bits in the Data Stream over RxDATO pin in DS3-M13/M23 and E3-G.751 modes. When set, RXGCKO is not gapped over the Stuff Opportunity bit positions. When clear, the Stuff Opportunity bits are not extracted (i.e., RXGCKO is gapped over their bit positions). When AllOVHDat bit in this register is set, this bit is ignored. In DS3-C-Bit Parity and E3-G.832 modes, this bit is ignored.

RxCjDat Received Justification Control Bits in the Data Stream—Set to enable presentation of the Justification Control bits in the data stream over RxDATO pin in DS3-M13/M23 and E3-G.751 modes. When set, RXGCKO is not gapped over the Justification Control bit positions. When clear, the Justification Control bits are not extracted (i.e., RXGCKO is gapped over their bit positions). When AllOVHDat bit in this register is set, this bit is ignored. In DS3-C-Bit Parity and E3-G.832 modes, this bit is ignored.

AllOVHDat All Overhead Bits Are in the Data Stream—Set to enable presentation of the complete frame in the data stream over RxDATO pin (i.e., RxGCKO is a nominal clock, it is not gapped). This bit is available in all framing modes. When this bit is set, it overrides RxCjDat and RxStfDat bits in this register. When this bit is cleared, presenting the Justification Control bits on RxDATO (RxGCKO gapping over Cj-bit positions) is determined by RxCjDat bit in this register, and presenting the Stuff Opportunity bits in RxDATO (RxGCKO gapping over Stuff bits positions) is determined by RxStfDat bit in this register. Other Opportunity bits are not presented on RxDATO pin when this bit is cleared (i.e., RxGCKO is gapped accordingly).

The following table details RxGCKO output behavior in different modes according to these bit settings:

RxStfDat	RxCjDat	AllOVHDat	RxGCKO Output Behavior
X	X	1	Nominal
0	0	0	Tick on Payload bits only (also not on Stuff Opportunity bits)
0	1	0	Ticks only on Payload bits and on Justification Control bits (in DS3-M13/M23 and in E3-G.751)
1	0	0	Ticks only on Payload bits and on Stuff Opportunity bits (in DS3-M13/M23 and in E3-G.751)
1	1	0	Ticks on Payload, Stuff Opportunity, and Justification Control bits (in DS3-M13/M23 and in E3-G.751)

3.4.4 Data Link Registers

0x2D—CR13 (Transmit Data Link Control Register)

The Transmit Data Link Control register (CR13) enables different modes and interrupts in the Transmit Data Link operation.

NOTE: Reserved bits, (—) in Control registers must be set to 0.

7	6	5	4	3	2	1	0
—	—	—	—	TxMsgIE	TxURIE	TxNEIE	TxFCSEn

Default after reset: 00

Direction: Read/Write

Modification: Bits 1–3: dynamic, bit 0–DL: static

TxMsgIE Transmit Data Link Message Transmitted Interrupt Enable—Set to enable interrupt assertion on MINTR* pin due to end of transmission of a full message.

TxURIE Transmit Data Link FIFO Underrun Interrupt Enable—Set to enable interrupt assertion on MINTR* pin due to Data Link FIFO underrun error.

TxNEIE Transmit Data Link FIFO Near-Empty Interrupt Enable—Set to enable interrupt assertion on MINTR* pin due to the FIFO buffer being near empty.

TxFCSEn Transmit Data Link FCS Calculation Enable—Set to enable FCS calculation over the transmitted message and add it to the end of the transmitted message. When cleared, the FCS calculation and addition are executed by the software.

0x2E—CR14 (Transmit Data Link Threshold Control Register)

7	6	5	4	3	2	1	0
—	TxNEThr[6]	TxNEThr[5]	TxNEThr[4]	TxNEThr[3]	TxNEThr[2]	TxNEThr[1]	TxNEThr[0]

Default after reset: 00

Direction: Read/Write

Modification: DL—static

TxNEThr[6:0] Transmit Data Link FIFO Near Empty Threshold—Set to the threshold value, used to indicate a Near-Empty FIFO event. The range of values available for this purpose is 0–126, where 00(h) is interpreted as 0, 01(h) is 1, etc. and 7E(h) is interpreted as 126.

0x2F—CR15 (Transmit Data Link Message Byte, Low Address)

0x30—CR15 (Transmit Data Link Message Byte, High Address)

7	6	5	4	3	2	1	0
TxDLMsg[7]	TxDLMsg[6]	TxDLMsg[5]	TxDLMsg[4]	TxDLMsg[3]	TxDLMsg[2]	TxDLMsg[1]	TxDLMsg[0]

Default after reset: Undefined

Direction: Read/Write

Modification: Dynamic

TxDLMsg [7:0] Transmit Data Link Message Byte—This byte is loaded with data to be written into the Data Link FIFO buffer, which is later transmitted by the Data Link Transmitter circuit. Two addresses are allocated for this register. During the whole message, except the last byte, the lower address is used to access this register. When the last byte of the message is written to this register, the higher address is used. The higher address indicates the end of the message to the transmitter circuit. TxDLMsg [0] bit is transmitted first and TxDLMsg [7] bit is transmitted last. Reading this register causes latching of the content of the FIFO stage pointed by the Transmit Data Link Read pointer into this register.

0x31—CR16 (Receive Data Link Control Register)

The Receive Data Link Control register enables operation of the receiver terminal data link circuit, defines the FCS mode, and enables interrupt assertion due to data link events.

NOTE: Reserved bits in control registers must be set to 0.

7	6	5	4	3	2	1	0
—	—	NRDL	RxOVRIE	RxMsgIE	RxNFIE	RxFCSEn	RxDLEn

Default after reset: 00

Direction: Read/Write

Modification: Bits 0, 2–4: dynamic, bits 1, 5: DL-static

NRDL NR Byte Over the Data Link—This bit is effective only in E3-G.832 mode. When set, selects NR byte to be processed by the receiver data link HDLC and FIFO circuits. When cleared, selects GC byte to be processed by the receiver data link HDLC and FIFO circuits.

RxOVRIE Receive Data Link FIFO Overrun Interrupt Enable—Set to enable interrupt assertion due to Data Link FIFO overrun error.

RxMsgIE Receive Data Link Message Interrupt Enable— Set to enable interrupt assertion due to a message received event.

RxNFIE Receive Data Link FIFO Near-Full Interrupt Enable—Set to enable interrupt assertion due to the FIFO near-full event.

RxFCSEn Receive Data Link FCS Check Enable—Set to enable execution of an FCS check on the received message. When cleared, the FCS check is executed by software; therefore, no interrupt or status due to bad FCS appears.

RxDLEn Receive Data Link Enable—Set to enable operation of the Receive Data Link FIFO buffer and HDLC/LAPD circuits over the selected data link channel (Cb5, N-bit, NR, or GC). When cleared, the data link channel data is left unchanged (may be presented on the data stream via the REXTCKO and RxGCKO clocks), and no receive datalink interrupts (enabled in this register) are asserted.

0x32—CR17 (Receive Data Link Threshold Control Register)

7	6	5	4	3	2	1	0
—	RxNFThr[6]	RxNFThr[5]	RxNFThr[4]	RxNFThr[3]	RxNFThr[2]	RxNFThr[1]	RxNFThr[0]

Default after reset: 7F

Direction: Read/Write

Modification: DL—static

RxNFThr [6:0] Receive Data Link FIFO Near Full Threshold—Set to the threshold value; used to indicate a near-full FIFO event. The range of values available for this purpose is 2–127, where 02(h) is interpreted as 2 and 7F(h) is interpreted as 127.

0x33—CR18 (Transmit FEAC Channel Byte)

7	6	5	4	3	2	1	0
TxFEAC[7]	TxFEAC[6]	TxFEAC[5]	TxFEAC[4]	TxFEAC[3]	TxFEAC[2]	TxFEAC[1]	TxFEAC[0]

Default after reset: FF

Direction: Read/Write

Modification: Dynamic

TxFEAC[7:0] Transmit FEAC Channel Message Byte—If the mode is set to DS3-C-Bit Parity, this register is used as the data byte for the transmit FEAC channel transmitter. When this byte is in the form 0xxxxxx0 it is transmitted after every flag. If there is a 1 in either the most significant or least significant bit of this register, an all-1s (idle) is transmitted on FEAC channel. An interrupt is associated with this channel and is enabled by TxFEACIE bit in Feature3 Control register. For interrupt activation. TxFEAC [0] bit is transmitted first and TxFEAC [7] bit is transmitted last.

3.4.5 Error Insertion Control Registers

Error insertion registers, CR19 and CR20, enable single insertion of different errors. Setting the relevant bit causes insertion of the requested error at the next valid opportunity. The relevant control bit clears once the error is inserted. Therefore, the control bits have to be polled before setting them for the next error insertion. Several Error Insertion Control bits can be set at the same time; each one of them is cleared when the appropriate error is inserted.

NOTE: The software can only set the Error Insertion bits. Writing 0 to these bits leaves them unaffected. Some of the bits are valid only in certain modes. When not valid, setting the bits has no effect and they are not cleared. Reserved bits are cleared to 0. Value after enabling Error Insertion Control bits = 0.

0x34—CR19 (Error Insertion1 Control Register)

7	6	5	4	3	2	1	0
FEBEErr	XdgrErr	YelErr	CPErr	ParDgrErr	ParErr	FrmErrM	FrmErrF

Default after reset: 00

Direction: Read/Write

Modification: Dynamic

FEBEErr FEBE Error Insertion Control—Causes insertion of a FEBE error at the next opportunity.

In DS3 C-bit Parity mode, a FEBE error is the transmission of any combination of 1s and 0s except 111. When a frame bit error or a C-bit parity is detected, transmission of the FEBE error code, written in the FEBEC/PT field in Feature1 control register, takes place.

In E3-G.832 mode, REI (FEBE) bit is cleared to 0 when a BIP-8 error is detected in the EM byte and set to 1 when the parity check in the EM byte is correct.

XDgrErr X-Bits Disagreement Error Insertion Control—Causes insertion of X-bits disagreement (i.e., the two X-bits in an M-frame are not equal) at the next opportunity. Valid in only DS3 mode.

YelErr Yellow Alarm Error Insertion Control—Causes insertion of RAI/RDI error at the next opportunity. RAI error means transmission opposite of the expected value.

In DS3 mode, the two X-bits are set to 1 if an RAI should be transmitted and cleared to 0 if RAI is not expected.

In E3-G.751 mode, The A-bit is cleared to 0 if an RAI should be transmitted and set to 1 if a RAI is not expected.

In E3-G.832 mode, RDI bit clears to 0 if an RAI should be transmitted, and set to 1 if an RAI is not expected.

CPErr C-Bit Parity Error Insertion Control—Causes insertion of a CP error at the next opportunity. A CP error means transmission of an incorrect value in the three CP-bits. Valid only in DS3 C-Bit Parity mode.

ParDgrErr Parity Bits Disagreement Error Insertion Control—Causes insertion of P-bits disagreement (i.e., the two P-bits in an M-frame are not equal) at the next opportunity. Valid only in DS3 mode.

ParErr Parity Error Insertion Control—Causes insertion of a parity error at the next opportunity.

In DS3 mode, the error means transmission of an incorrect value in the two P-bits.

In E3-G.832 mode, the error means transmission of a single incorrect bit in BIP-8 field (EM byte).

FrmErrM Frame Error in M-Bit Insertion Control—Causes insertion of a single error (inversion) in one M-bit at the next opportunity. Valid only in DS3 mode.

FrmErrF Frame Error in F/FAS/FA Insertion Control—Causes insertion of a single frame error at the next opportunity.

In DS3 mode, causes inversion of a single F-bit.

In E3-G.751 mode, causes inversion of a single bit in the next FAS field.

In E3-G.832 mode, causes inversion of a single bit in the next FA field.

0x35—CR20 (Error Insertion2 Control Register)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	LCVIllSub	LCVBPV

Default after reset: 00

Direction: Read/Write

Modification: Dynamic

LCVIllSub LCV Illegal Substitution Insertion Control—Causes insertion of an illegal substitution at the next opportunity. Illegal substitution is defined as an opposite polarity substitution at the next B3ZS/HDB3 substitution. This means that a B0V/B00V pattern is replaced with a 00V/000V pattern or vice versa.

LCVBPV LCV Bipolar Violation Error Insertion Control—Causes insertion of a bipolar violation at the next opportunity. A bipolar violation is defined as a second pulse with the same polarity as the previous one.

3.4.6 Framer Channel Status Registers

0x40—SR00 (DS3/E3 Maintenance Status Register)

The DS3/E3 Maintenance Status register contains the major DS3/E3 maintenance indicators.

7	6	5	4	3	2	1	0
ReFrm	—	—	LOSAlm	IdleDet	YelDet	AISDet	OOFAlm

Value after reset: 81

Direction: Read only

Value after enable: If RefrmStp bit is clear—81
If RefrmStp bit is set—01

ReFrm Reframe in Progress—Set while the framing circuit searches for a valid framing pattern in either DS3 or E3 modes.

LOSAlm Loss-of-Signal Alarm—Indicates that the received signal has been lost prior to B3ZS/HDB3 decoding. This signal is set as soon as the receiver detects the loss-of-signal condition and clears when the receiver detects a legal signal.

IdleDet Idle Code Detect—Set if an idle pattern is found. This bit is low in E3 modes, since there is no defined E3 idle signal.

YelDet Yellow Alarm Detect—Set when a RAI/RDI event is detected in the receiver.

AISDet Alarm Indication Signal Detect—Set if the receiver detects an AIS event.

OOFAlm Out of Frame Alarm—Set when an OOF condition is detected by the receiver. This condition initiates a reframe.

NOTE: RefrmStp—Bit 6 in CR08, Feature 5 Control register.

0x41—SR01 (Interrupt Source Status Register)

This register identifies which status registers reports the reason for the interrupt assertion. If a framer interrupt has occurred (PORTINTn[FrmrInt]), this register is read at the beginning of the interrupt service routine, after the source channel is identified.

NOTE: More than one bit can be high at the same time due to multiple sources for the interrupt.

7	6	5	4	3	2	1	0
—	—	TxDLFEACItr	RxDLItr	RxFEACItrS	AlarmEndItr	AlarmStrtItr	CtrItr

Value after reset: 00

Direction: Read only

Value after enable: Unaffected (affected indirectly by other registers)

TxDLFEACItr Transmit Data Link/FEAC Interrupt Source—Set if one or more of the interrupt-related active status bits in the Transmit Data Link FEAC Status register are high. Cleared when the bits related to interrupt activation in the Transmit Data Link FEAC Status register or their interrupt masks are low.

RxDLItr Receive Data Link Interrupt Source—Set if one or more of the interrupt-related active status bits in the Receive Data Link Status register are high. Cleared when the bits related to interrupt activation in the Receive Data Link Status register or their interrupt masks are low.

RxFEACItrs Receive FEAC Interrupt Source—Set if one or more of the interrupt-related active status bits in the Receive FEAC Status register are high. Cleared when the bits related to interrupt activation in the Receive FEAC Status register or their interrupt masks are low.

AlarmEndItr Alarm End Interrupt Source—Set if one or more of the active status bits in the Alarm End Interrupt Status register are high. Cleared when the bits related to interrupt activation in the Alarm End Interrupt Status register or their interrupt masks are low.

AlarmStrtItr Alarm Start Interrupt Source—Set if one or more of the active status bits in the Alarm Start Interrupt Status register are high. Cleared when the bits related to interrupt activation in the Alarm Start Interrupt Status register or their interrupt masks are low.

CtrItr Counter Interrupt Source—Set if one or more of the active status bits in the Counter Interrupt Status register are high. Cleared when the bits related to interrupt activation in the Counter Interrupt Status register or their interrupt masks are low.

0x42—SR02 (Counter Interrupt Status Register)

The Counter Interrupt Status register contains status information about active interrupts needing service from the controller. This register must be read by the controller upon receiving a counter interrupt to determine the source of the interrupt. The interrupt indications are active high in the register and are available even if they are not enabled to be visible on the MINTR* output pin. Servicing clears this interrupt indication.

The bits in this register are cleared when the register is read.

7	6	5	4	3	2	1	0
EXZCtrItr	XDgrCtrItr	LCVCtrItr	FEBECtrItr	PthCtrItr	FerrCtrItr	PdgrCtrItr	ParCtrItr

Value after reset: 00

Direction: Read only

Value after enable: 00

EXZCtrItr Excessive Zeros Counter Interrupt—Set high on EXZ error counter rollover or saturation. The EXZ Counter Interrupt Enable bit, EXZCtrlE bit in Counter Interrupt Control register, determines the status of the counter (rollover or saturation).

XDgrCtrItr X-Bits Disagreement Counter Interrupt—Set high if the X-Disagreement counter has either rolled over or is saturated. The X-Disagreement Counter Interrupt Enable bit (XDgrCtrIE) determines the status of the counter (rollover or saturation). In E3-G.751 and E3-G.832 modes, this bit is low because there are no X-bits.

LCVCtrItr LCV Counter Interrupt—Set high on an LCV error counter rollover or saturation. The LCV Counter Interrupt Enable bit (LCVCtrIE) determines the status of the counter (rollover or saturation).

FEBECtrItr FEBE Event Counter Interrupt—Set high if the FEBE event counter has either rolled over or is saturated. The FEBE Event Counter Interrupt Enable bit determines the status of the counter (rollover or saturation).

In E3-G.751 and DS3-M13/M23 modes, this bit is low because there is no FEBE/REI event defined.

PthCtrItr Path Parity Error Counter Interrupt—In DS3 mode, set high if the Path Parity Error counter has either rolled over or is saturated. The Path Parity Error Counter Interrupt Enable bit determines the status of the counter (rollover or saturation).

In DS3-M13/M23, E3-G.751, and E3-G.832 modes, this bit is low because there is no path parity check.

FerrCtrItr Frame Error Counter Interrupt—Set high when the frame error counter has either rolled over or is saturated. The Frame Error Counter Interrupt Enable determines the status of the counter (rollover or saturation).

PdgrCtrItr P-Bits Disagreement Counter Interrupt—Set high if the P disagreement counter has either rolled over or is saturated. The Disagreement Counter Interrupt Enable bit determines the status of the counter (rollover or saturation). In E3-G.751 and E3-G832 modes, this bit is low because there is no parity disagreement event defined.

ParCtrItr Parity Error Counter Interrupt—Set high if the parity error counter has either rolled over or is saturated. The Parity Error Counter Interrupt Enable bit determines the status of the counter (rollover or saturation). In E3-G.751 mode, this bit is low because there is no parity/BIP-8 check defined.

3.4.7 Dual-Edge Interrupt Status Registers

The Dual-Edge Interrupt Status registers provide indications for starting and ending points of continuous events, to enable monitoring of the events length. All bits are set due to an event and cleared when the register is read. In addition, every event bit (start or end) is cleared upon setting the channel's enable bit for that event to prevent an immediate interrupt due to an old event.

0x43—SR03 (Alarm Start Interrupt Status Register)

7	6	5	4	3	2	1	0
—	—	SEFStrt	LOSStrt	IdleStrt	YelStrt	AISStrt	OOFStrt

Value after reset: 00

Direction: Read only

Value after enable: 00

SEFStrt Severely Errored Frame Event Start—Set when the receiver detects an SEF condition. This bit is cleared when this register is read. This bit is low in E3 modes since there is no defined SEF alarm in these modes.

LOSStrt Loss of Signal Event Start—Set when the signal received is detected as lost by the receiver prior to B3ZS/HDB3 decoding. This bit is cleared when this register is read.

IdleStrt Idle Event Start—Set when the receiver detects the start of an Idle event in DS3 mode. This bit is cleared when this register is read. This is low in E3 modes, because there is no defined E3 idle signal.

YelStrt Yellow Alarm Start—Set when the receiver detects the start of an RAI/RDI alarm. This bit is cleared when this register is read.

AISStrt AIS Alarm Start—Set when the receiver detects the start of an AIS alarm. This bit is cleared when this register is read.

OOFStrt Out of Frame Event Start—Set when the channel gets into an OOF condition. This bit is cleared when this register is read.

0x44—SR04 (Alarm End Interrupt Status Register)

7	6	5	4	3	2	1	0
—	—	—	LOSEnd	IdleEnd	YelEnd	AISEnd	OOFEnd

Value after reset: 00

Direction: Read only

Value after enable: 00

LOSEnd Loss Of Signal Event End—Set when the received signal satisfies the criteria of correct signal after being in a loss-of-signal state, prior to B3ZS/HDB3 decoding. This bit is cleared when this register is read.

IdleEnd Idle Event End—Set when the receiver detects an end of an Idle event in DS3 mode. This bit is cleared when this register is read. This bit is low in E3 modes, because there is no defined E3 idle signal.

YelEnd Yellow Alarm End—Set when the receiver detects the end of an RAI/RDI alarm. This bit is cleared when this register is read.

AISEnd AIS Alarm End—Set when the receiver detects the end of an AIS alarm. This bit is cleared when this register is read.

OOFEnd Out Of Frame Event End—Set when the channel goes into in-frame state again after being in an OOF state. This bit is cleared when this register is read.

3.4.8 E3-832 MA Fields Registers

The E3-832 MA Fields registers collect data of specific fields from E3-G.832-type frames. In DS3 and E3-G.751 modes, they are ignored.

0x46—SR06 (E3-G.832 MA Fields Status Register)

7	6	5	4	3	2	1	0
—	—	RxMAPT[1]	RxMAPT[2]	RxMAPT[3]	RxMAPD[1]	RxMAPD[2]	RxMATM

Value after reset: Undefined

Direction: Read only

Value after enable: Unaffected

RxMAPT[1:3] Received Payload Type Field—These 3 bits store the pattern of the payload-type field in an MA byte (bits 3–5). No interrupt is issued to report any change in the content of this field. RxMAPT [1] is the first bit received from the line.

RxMAPD[1:2] Received Payload Dependent/Multiframe Indicator Field—These 2 bits store the pattern of the payload-dependent/multiframe indicator in MA byte (bits 6–7). No interrupt is issued to report any change in the content of this field. RxMAPD [1] is the first bit received from the line.

RxMATM Received Timing Marker Bit Field—This bit contains the timing marker bit in an MA byte (bit 8) information. It is valid only when SSM mode is disabled, i.e., when SSMEn bit in Feature4 register is low. No interrupt is issued to report any change in the content of this field.

0x47— SR07 (E3-G.832 SSM Field Status Register)

The E3-G.832 SSM Field Status register (SR07) is valid only when SSM mode is enabled, i.e., when SSMEn bit in Feature Control Register 4 is high.

7	6	5	4	3	2	1	0
—	—	—	—	RxSSM[1]	RxSSM[2]	RxSSM[3]	RxSSM[4]

Value after rest: Undefined

Direction: Read only

Value after enable: Unaffected

RxSSM[1:4] Received SSM Field—These 4 bits store the pattern of SSM field in MA byte (bit 8 collected from 4 frames). The SSM bits are collected from 4 consecutive frames and arranged according to the Multiframe Indicator field. SSM [1] is the MS bit that is received when MI = 00, etc.

0x48—SR08 (Transmit Data Link Status Register)

7	6	5	4	3	2	1	0
—	—	TxFEACItr	TxFull	TxMsg	TxUR	TxNE	TxEmpty

Value after reset: 03

Direction: Read only

Value after enable: 03

TxFEACItr Transmit FEAC Channel Interrupt—In DS3-C-Bit Parity mode, set high indicating that the transmitter is ready for a new byte to be written to the Transmit FEAC Channel Byte register. When FEAC single mode, this happens after every code word transmission start. When in FEAC repetitive mode, this happens after the transmitter has started sending the code word 10 consecutive times for the first time. Cleared when this register is read.

In DS3-M13/M23, E3-G.751, and E3-G.832 modes, this bit should be ignored.

TxFull Transmit Data Link FIFO is Full—Set when the transmit FIFO contains 128 bytes. Cleared when there are less than 128 bytes in the transmit FIFO (i.e., this bit is high and the first byte is read). No interrupt is linked to this bit.

TxMsg Transmit Data Link Message Transmitted Event—Set when the final bit of the closing flag of a message is transmitted. Cleared when this register is read.

TxUR Transmit Data Link Underrun Error—Set when the transmit FIFO buffer is empty and the transmit circuit tries to read another byte from it, i.e., the microprocessor does not meet the requirements and does not fill the FIFO buffer properly. Cleared when this register is read.

TxNE Transmit Data Link Near-Empty Event—Set when TxNEThr bytes or less are left in the FIFO. Cleared when the number of bytes in the FIFO is greater than TxNEThr.

TxEmpty Transmit Data Link FIFO is Empty—Set when the FIFO is empty, i.e., the last byte is read from it. Cleared when set and the first write by the microprocessor (after being empty) is done. No interrupt is linked to this bit.

0x4B—SR11 (Receive Data Link Status Register)

7	6	5	4	3	2	1	0
—	—	RxGoodBlk	RxOVR	RxMsg	RxNF	RxBlk	StatByte

Value after reset: Bit 0, 5: undefined, bits 1–4, 6, 7—00

Direction: Read only

Value after enable: Bit 0, 5: undefined, bits 1–4, 6, 7—00

RxGoodBlk Received Good Block Indication—Defines the type of status byte. Set for status with length type in it (a good block [a1] or [a2] blocks). Cleared for status byte with error type in it (a bad block [b]).

RxOVR Receive Data Link Overrun Error—Set when the receive FIFO is full and another byte was received from the line and should be written into the FIFO (and it is not already set). Cleared if it was set and there are no more unread complete blocks left in the FIFO (this is determined by RxBlk bit in this register).

RxMsg Receive Data Link FIFO Contains a Message—Set when another status byte of a correct-end-of-message or an incorrect-end-of-message (including aborted message) is written into the FIFO. Cleared when this register is read.

RxNF Receive Data Link Near-Full Event—Set when the number of bytes in the receive FIFO equals or exceeds the programmable threshold written in RxNFThr register (and it is not already set). Cleared if was set and there are no more unread complete blocks left in the FIFO (this is determined by RxBlk bit in this register).

RxBlk Receive Data Link FIFO Contains Complete Blocks—Set when there is one or more complete data blocks in the receive FIFO. Cleared when the last data byte of the last complete block is read from the FIFO.

StatByte Byte Type Indication—Set when the next byte to be read from the receive FIFO is a status byte. Clear when the next byte to be read is a data byte. When RxBlk bit in this register is clear, this bit is undefined, i.e., there is no complete block in the FIFO.

0x4C—SR12 (Receive Data Link Message Byte)

7	6	5	4	3	2	1	0
RxDLMsg[7]	RxDLMsg[6]	RxDLMsg[5]	RxDLMsg[4]	RxDLMsg[3]	RxDLMsg[2]	RxDLMsg[1]	RxDLMsg[0]

Value after reset: Undefined

Direction: Read only

Value after enable: Undefined

RxDLMsg[7:0] Receive Data Link Message Byte—This register is used to read the content of the Receive Data Link FIFO. Issuing a receive FIFO read is done by addressing this register, which results in putting the byte read from the FIFO on the microprocessor data bus. The type of this register's content (status or data) is defined by StatByte bit in the Receive Data Link Status register or as described in the Terminal Data Link Reception paragraph.

The receive order of bits from the line is RxDLMsg[0] bit is received first and RxDLMsg[7] bit is received last from the line. When this register contains data it can be any combination of 1s and 0s.

When this register contains a status, it defines the status of the following data block, where the 1 MS bits contain the block's type (correct or partial) for a good block, or undefined for errored block. The other 7 bits are used as length field or error indications.

For RxGoodBlk-set the register contains:

RxDLMsg[7]	RxDLMsg[6]	RxDLMsg[5]	RxDLMsg[4]	RxDLMsg[3]	RxDLMsg[2]	RxDLMsg[1]	RxDLMsg[0]
Type Select	Length[6]	Length[5]	Length[4]	Length[3]	Length[2]	Length[1]	Length[0]

RxDLMsg[7]: set for complete, cleared for partial.

For RxGoodBlk cleared, the register contains the following block, illustrating the content of the status register in incorrect-end-of-message state and details the different error indications that can be set.

NOTE: The length of the following block is always considered as 0, and only one indication can be set at a time.

RxDLMsg[7]	RxDLMsg[6]	RxDLMsg[5]	RxDLMsg[4]	RxDLMsg[3]	RxDLMsg[2]	RxDLMsg[1]	RxDLMsg[0]
—	—	—	—	Abort	OVR	AlignErr	BadFCS

The error indications are as follows:

- Abort—When an abort sequence is detected, the message is terminated and the bit set.
- OVR—When an overrun error happens (FIFO buffer is full and a new byte was received), the message is terminated and the bit set.
- AlignErr—When the number of bits in the message is indivisible by 8 (alignment error), the message is terminated and the bit set.
- BadFCS—When there is a mismatch between the calculated and the received FCS, the message is terminated and the bit set.

Only one error type is set according to this priority: OVR, Abort, AlignErr, BadFCS (highest to lowest).

0x4F—SR15 (Receive FEAC Byte)

7	6	5	4	3	2	1	0
RxFEAC[7]	RxFEAC[6]	RxFEAC[5]	RxFEAC[4]	RxFEAC[3]	RxFEAC[2]	RxFEAC[1]	RxFEAC[0]

Value after reset: Undefined

Direction: Read only

Value after enable: Unaffected

RxFEAC[7:0] Receive FEAC Channel Message Byte—If the incoming format is DS3-C-Bit Parity, this register contains the received byte from the bit-oriented Receive FEAC channel. RxFEAC[0] is the bit received first and RxFEAC[7] is the last bit received from the line. The Receive FEAC channel is only defined in DS3-C-Bit Parity format. This byte is meaningless in DS3-M13/M23, and both E3 modes and should be ignored.

0x50—SR16 (Receive FEAC Stack Byte)

7	6	5	4	3	2	1	0
RxFEACS[5]	RxFEACS[4]	RxFEACS[3]	RxFEACS[2]	RxFEACS[1]	RxFEACS[0]	RxFEACSV	RxFEACSM

Value after reset: Bits 0–1: 0, Bits 2–7: undefined

Direction: Read only

Value after enable: Bits 0–1: 0, Bits 2–7: undefined

RxFEACS[5:0] Receive FEAC Channel Stack Message Byte—If the incoming format is DS3-C-Bit Parity, this register contains the FEAC stack received byte from the bit-oriented Receive FEAC channel. Receive FEAC message reception is described in Far-End Alarm and Control Channel Reception in Section 2.1.2. RxFEACS[0] is the first bit received and RxFEACS[5] is the last bit received from the line. This byte is meaningless in DS3-M13/M23 and both E3 modes and should be ignored.

RxFEACSV Receive FEAC Channel Stack Message Byte is Valid— Set on if RxFEACS [5:0] hold a valid FEAC code word. For a detailed description, refer to Far-End Alarm and Control Channel Reception sections.

RxFEACSM Receive FEAC Channel Stack Has More Data—Set on if the current value of RxFEACS[5:0] is not the last valid code word in the FEAC stack. For a detailed description, refer to Far-End Alarm and Control Channel Reception sections.

0x51—SR17 (Receive FEAC Status Register)

7	6	5	4	3	2	1	0
—	—	—	—	—	RxFEACSNE	RxFEACIdle	RxFEACItr

Value after reset: 00

Direction: Read only

Value after enable: 00

RxFEACSNE Receive FEAC Stack Is Not Empty—Set due to detection of the FEAC stack being not empty (i.e., Receive FEAC Stack byte is holding valid data).

RxFEACIdle Received FEAC Channel Is Idle—In DS3-C-Bit Parity mode, set when the FEAC receiver detects the first appearance of an Idle code, after reception of legal code words. This bit is cleared when this register is read. In DS3-M13/M23 and both E3 modes, this bit should be ignored.

RxFEACItr Receive FEAC Channel Interrupt—In DS3-C-Bit Parity mode, when working in FEAC single mode, set high when an FEAC message byte has been received and placed in the Receive FEAC Channel Byte register. When working in FEAC repetitive mode, set high when the receiver detects an FEAC message byte (see Far-End Alarm and Control Channel Reception paragraph). Reading the Receive FEAC Channel Byte register clears this interrupt. In DS3-M13/M23, E3-G.751 and E3-G.832 modes, this bit should be ignored.

0x52—SR18 (Receive AIC Byte)

7	6	5	4	3	2	1	0
RxAIC[7]	RxAIC[6]	RxAIC[5]	RxAIC[4]	RxAIC[3]	RxAIC[2]	RxAIC[1]	RxAIC[0]

Value after reset: Undefined

Direction: Read only

Value after enable: Unaffected

RxAIC[7:0] Receive AIC Channel Message Byte—If the incoming format is DS3, C-Bit Parity, this register contains 8 AIC (Cb11) bits from 8 consecutive frames. RxAIC[0] is the first bit received and RxAIC[7] is the last bit received from the line. This byte is meaningless in DS3-M13/M23 and both E3 modes and should be ignored.

3.4.9 Counters

There are eight error counters for DS3/E3 errors. All are 16-bit counters except the LCV counter, which is 24 bits long. The counters indicate 0–65,535 (LCV = 16,777,215) counts of a particular error. If the interrupt for a particular counter is not enabled, the counter saturates at 65,535 (LCV = 16,777,215). When more than 65,535 (LCV = 16,777,215) counts of that error are received, the saturation indication appears in the Counter Interrupt Status register. The saturation indication is cleared when the Counter Interrupt Status register is read. The counter is cleared when the counter is read.

If the interrupt for a particular counter is enabled in the Interrupt Control register, the counter does not saturate but rolls over and continue counting from 0. An interrupt is generated on the MINTR* pin and appears in the Counter Interrupt Status register when the counter rolls over to a count of 0. The interrupt is cleared when the Counter Interrupt Status register is read. The counter is cleared when the counter is read. The counters count according to indications set by the receiver circuit.

All counters are cleared when read by the microprocessor. The interrupt indication for a particular counter is cleared when the Counter Interrupt Status register is read. Software should read the low byte first and then the high byte to prevent any missed counts. All counters are designed so that errors occurring during reads by the microprocessor are not missed or double-counted.

0x60—Ctr00 (DS3/E3 Parity Error Counter Low)

7	6	5	4	3	2	1	0
ParCtr[7]	ParCtr[6]	ParCtr[5]	ParCtr[4]	ParCtr[3]	ParCtr[2]	ParCtr[1]	ParCtr[0]

0x61—Ctr00 (DS3/E3 Parity Error Counter High)

15	14	13	12	11	10	9	8
ParCtr[15]	ParCtr[14]	ParCtr[13]	ParCtr[12]	ParCtr[11]	ParCtr[10]	ParCtr[9]	ParCtr[8]

Value after reset: 00

Direction: Read

Value after enable: 0000

ParCtr[15:0] Parity Error Counter—In DS3 mode, increments for each M-frame where the calculated parity of the received data bits of the previous M-frame does not match the received parity bits. If the two parity bits are different, this counter increments. In E3-G.832 mode, it increments for each frame where the calculated BIP-8 pattern of the received data bits of the previous frame do not match the received EM byte. The counter increments are per byte, not bits. In E3-G.751 mode, this counter is not used.

0x62—Ctr01 (DS3 Parity Disagreement Counter Low)

7	6	5	4	3	2	1	0
ParDgrCtr[7]	ParDgrCtr[6]	ParDgrCtr[5]	ParDgrCtr[4]	ParDgrCtr[3]	ParDgrCtr[2]	ParDgrCtr[1]	ParDgrCtr[0]

0x63—Ctr01 (DS3 Parity Disagreement Counter High)

15	14	13	12	11	10	9	8
ParDgrCtr[15]	ParDgrCtr[14]	ParDgrCtr[13]	ParDgrCtr[12]	ParDgrCtr[11]	ParDgrCtr[10]	ParDgrCtr[9]	ParDgrCtr[8]

Value after reset: 0000

Direction: Read

Value after enable: 0000

ParDgrCtr [15:0] Parity-Bit Disagreement Counter—If the two P-bits in an M-frame are in disagreement (e.g., due to line errors), this counter is incremented.

0x64—Ctr02 (DS3 X Disagreement Counter Low)

7	6	5	4	3	2	1	0
XDgrCtr[7]	XDgrCtr[6]	XDgrCtr[5]	XDgrCtr[4]	XDgrCtr[3]	XDgrCtr[2]	XDgrCtr[1]	XDgrCtr[0]

0x65—Ctr02 (DS3 X Disagreement Counter High)

15	14	13	12	11	10	9	8
XDgrCtr[15]	XDgrCtr[14]	XDgrCtr[13]	XDgrCtr[12]	XDgrCtr[11]	XDgrCtr[10]	XDgrCtr[9]	XDgrCtr[8]

Value after reset: 0000

Direction: Read

Value after enable: 0000

XDgrCtr[15:0] X-Bit Disagreement Counter—If the two X-bits in an M-frame are in disagreement (e.g., due to line errors), this counter is incremented.

0x66—Ctr03 (DS3/E3 Frame Error Counter Low)

7	6	5	4	3	2	1	0
FerrCtr[7]	FerrCtr[6]	FerrCtr[5]	FerrCtr[4]	FerrCtr[3]	FerrCtr[2]	FerrCtr[1]	FerrCtr[0]

0x67—Ctr03 (DS3/E3 Frame Error Counter High)

15	14	13	12	11	10	9	8
FerrCtr[15]	FerrCtr[14]	FerrCtr[13]	FerrCtr[12]	FerrCtr[11]	FerrCtr[10]	FerrCtr[9]	FerrCtr[8]

Value after reset: 0000(h)

Direction: Read

Value after enable: 0000(h)

FerrCtr[15:0] Frame Error Counter—The counter increments for each error in the M- or F-bit framing pattern in DS3 mode and for each error in the FAS/FA pattern in E3 mode. Errors are still counted during an OOF condition (OOFAlm = 1).

0x68—Ctr04 (DS3 Path Parity Error Counter Low)

7	6	5	4	3	2	1	0
DS3PthCtr[7]	DS3PthCtr[6]	DS3PthCtr[5]	DS3PthCtr[4]	DS3PthCtr[3]	DS3PthCtr[2]	DS3PthCtr[1]	DS3PthCtr[0]

0x69—Ctr04 (DS3 Path Parity Error Counter High

15	14	13	12	11	10	9	8
DS3PthCtr[15]	DS3PthCtr[14]	DS3PthCtr[13]	DS3PthCtr[12]	DS3PthCtr[11]	DS3PthCtr[10]	DS3PthCtr[9]	DS3PthCt[8]

Value after reset: 0000(h)

Direction: Read

Value after enable: 0000(h)

DS3PthCtr[15:0] DS3 Path Parity Error Counter—Increments the count for each M-frame in which the calculated parity of the received data bits of the previous M-frame do not match a majority vote of the three received CP-bits (C-bits in subframe 3).

0x6A—Ctr05 (DS3/E3 FEBE Event Counter Low)

7	6	5	4	3	2	1	0
FEBE[7]	FEBE[6]	FEBE[5]	FEBE[4]	FEBE[3]	FEBE[2]	FEBE[1]	FEBE[0]

0x6B—Ctr05 (DS3/E3 FEBE Event Counter High)

15	14	13	12	11	10	9	8
FEBE[15]	FEBE[14]	FEBE[13]	FEBE[12]	FEBE[11]	FEBE[10]	FEBE[9]	FEBE[8]

Value after reset: 0000

Direction: Read

Value after enable: 0000

FEBE[15:0] FEBE Event Counter—In DS3-C-Bit Parity mode, increments for each M-frame where any C-bit in subframe 4 is 0. In E3-G.832 mode, increments for each frame where REI bit in MA byte is set. In DS3-M13/M23 and E3-G.751, this counter is not used.

0x6C—Ctr06 (DS3/E3 Excessive Zeros Counter Low)

7	6	5	4	3	2	1	0
EXZCtr[7]	EXZCtr[6]	EXZCtr[5]	EXZCtr[4]	EXZCtr[3]	EXZCtr[2]	EXZCtr[1]	EXZCtr[0]

0x6D—Ctr06 (DS3/E3 Excessive Zeros Counter High)

15	14	13	12	11	10	9	8
EXZCtr[15]	EXZCtr[14]	EXZCtr[13]	EXZCtr[12]	EXZCtr[11]	EXZCtr[10]	EXZCtr[9]	EXZCtr[8]

Value after reset: 0000

Direction: Read

Value after enable: 0000

EXZCtr[15:0] Excessive Zeros Counter—This counter is enabled only when B3ZS/HDB3 encoding or decoding is used. This counter increments upon excessive 0s-event detection by the receiver circuit.

0x6E—Ctr07 (DS3/E3 LCV Counter Low)

7	6	5	4	3	2	1	0
LCVCtr[7]	LCVCtr[6]	LCVCtr[5]	LCVCtr[4]	LCVCtr[3]	LCVCtr[2]	LCVCtr[1]	LCVCtr[0]

0x6F—Ctr07 (DS3/E3 LCV Counter Middle)

15	14	13	12	11	10	9	8
LCVCtr[15]	LCVCtr[14]	LCVCtr[13]	LCVCtr[12]	LCVCtr[11]	LCVCtr[10]	LCVCtr[9]	LCVCtr[8]

0x70—Ctr07 (DS3/E3 LCV Counter High)

23	22	21	20	19	18	17	16
LCVCtr[23]	LCVCtr[22]	LCVCtr[21]	LCVCtr[20]	LCVCtr[19]	LCVCtr[18]	LCVCtr[17]	LCVCtr[16]

Value after reset: 000000

Direction: Read

Value after enable: 000000

LCVCtr[23:0] LCV Counter—This counter is incremented due to LCV events detected by the receiver circuit.

3.5 Common Global Registers (0xE00—0xE7F)

0xE00—GLOB (Global Control Register)

7	6	5	4	3	2	1	0
EnStatLat	EnCntrLat	EnIntPin	OneSecIntEn	—	—	DevLogReset	MasterReset

Value after reset: 00

Direction: Read/Write

EnStatLat When written to 1, One-second status latching is enabled for all status registers. When written to 0, status registers are updated continuously.

EnCntrLat When written to 1, One-second latching is enabled for all error counters. When written to 0, error count information is updated continuously.

EnIntPin When written to 1, the interrupt output pin MINTR* is enabled. When written to 0, the interrupt output is three-stated.

OneSecIntEn When written to 1, the one-second interrupt is enabled to appear on the MINTR* pin.

DevLogReset(1) When written to 1, all cell delineator device logic functions, for all ports, are held in reset mode.

MasterReset(1) When written to 1, all internal state machines are held in reset mode and all control registers are set to their default values (except bit 0 in this register).

NOTE: (1) DevLog Reset and MasterReset should be held active for four 8KHzIn clocks to reset OneSec circuitry. 8KHzIn (pin A5) can be sped up to MCLK (pin E4) rate during reset

0xE01—SYSBUS (System Bus Control Register)

7	6	5	4	3	2	1	0
—	—	—	—	—	UtopMode	Handshake	BusWidth

Value after reset:06

Direction: Read/Write

UtopMode When written to 1, the system bus operates in UTOPIA Level 2 mode and forces the handshake mode to cell handshaking. When written to 0, the system bus operates in UTOPIA Level 1 mode (can be used only for port0 operation).

Handshake When written to 1, cell handshaking is enabled on the UTOPIA bus. When written to 0, octet handshaking is enabled.

BusWidth When written to 0, a 16-bit UTOPIA bus is enabled. When written to 1, an 8-bit UTOPIA bus is enabled.

0xE02—VERSION (Part Number/Version Register)

7	6	5	4	3	2	1	0
Part[3]	Part[2]	Part[1]	Part[0]	Ver[3]	Ver[2]	Ver[1]	Ver[0]

Value after reset: C3

Direction: Read/Write

Part	Part [3:0]
CX28365	0xC
CX28366	0x6
CX28364	0x4

Part[3:0] This is the part number that uniquely identifies the CX2836x.

Ver[3:0] This is the version number that uniquely identifies the specific version of the CX2836x. Version numbers start at 1 for the first version and are incremented for each revision thereafter.

0xE04—GLOBINTL (Global Interrupt Status Register [low byte])

7	6	5	4	3	2	1	0
Port7Int	Port6Int	Port5Int	Port4Int	Port3Int	Port2Int	Port1Int	Port0Int

Direction: Read/Write

Port7Int This bit indicates that an interrupt has occurred in a Port 7 interrupt register.

Port6Int This bit indicates that an interrupt has occurred in a Port 6 interrupt register.

Port5Int This bit indicates that an interrupt has occurred in a Port 5 interrupt register.

Port4Int This bit indicates that an interrupt has occurred in a Port 4 interrupt register.

Port3Int This bit indicates that an interrupt has occurred in a Port 3 interrupt register.

Port2Int This bit indicates that an interrupt has occurred in a Port 2 interrupt register.

Port1Int This bit indicates that an interrupt has occurred in a Port 1 interrupt register.

Port0Int This bit indicates that an interrupt has occurred in a Port 0 interrupt register.

0xE05—GLOBINTH (Global Interrupt Status Register [high byte])

7	6	5	4	3	2	1	0
—	—	—	OneSecInt	Port11Int	Port10Int	Port9Int	Port8Int

Direction: Read/Write

OneSecInt This bit indicates that a one second interrupt has occurred.

Port11Int This bit indicates that an interrupt has occurred in a Port 11 interrupt register.

Port10Int This bit indicates that an interrupt has occurred in a Port 0 interrupt register.

Port9Int This bit indicates that an interrupt has occurred in a Port 9 interrupt register.

Port8Int This bit indicates that an interrupt has occurred in a Port 8 interrupt register.

0xE08—OUT1L (OUTPORT1 Control Register [low byte])

7	6	5	4	3	2	1	0
OutPort1[7]	OutPort1[6]	OutPort1[5]	OutPort1[4]	OutPort1[3]	OutPort1[2]	OutPort1[1]	OutPort1[0]

Value after reset: 00

Direction: Read/Write

OutPort1[7] This bit is output on the OUTPORT1[7] output pin if so selected in the Port7 control register.

OutPort1[6] This bit is output on the OUTPORT1[6] output pin if so selected in the Port6 control register.

OutPort1[5] This bit is output on the OUTPORT1[5] output pin if so selected in the Port5 control register.

OutPort1[4] This bit is output on the OUTPORT1[4] output pin if so selected in the Port4 control register.

OutPort1[3] This bit is output on the OUTPORT1[3] output pin if so selected in the Port3 control register.

OutPort1[2] This bit is output on the OUTPORT1[2] output pin if so selected in the Port2 control register.

OutPort1[1] This bit is output on the OUTPORT1[1] output pin if so selected in the Port1 control register.

OutPort1[0] This bit is output on the OUTPORT1[0] output pin if so selected in the Port0 control register.

0xE09—OUT1H (OUTPORT1 Control Register [high byte])

7	6	5	4	3	2	1	0
—	—	—	—	OutPort1[11]	OutPort1[10]	OutPort1[9]	OutPort1[8]

Value after reset: 00

Direction: Read/Write

OutPort1[11] This bit is output on the OUTPORT1[11] output pin if so selected in the Port11 control register.

OutPort1[10] This bit is output on the OUTPORT1[10] output pin if so selected in the Port10 control register.

OutPort1[9] This bit is output on the OUTPORT1[9] output pin if so selected in the Port9 control register.

OutPort1[8] This bit is output on the OUTPORT1[8] output pin if so selected in the Port8 control register.

0xE0A—OUT2L (OUTPORT2 Control Register [low byte])

7	6	5	4	3	2	1	0
OutPort2[7]	OutPort2[6]	OutPort2[5]	OutPort2[4]	OutPort2[3]	OutPort2[2]	OutPort2[1]	OutPort2[0]

Value after reset: 00

Direction: Read/Write

OutPort2[7] This bit is output on the OUTPORT2[7] output pin if so selected in the Port7 control register.

OutPort2[6] This bit is output on the OUTPORT2[6] output pin if so selected in the Port6 control register

OutPort2[5] This bit is output on the OUTPORT2[5] output pin if so selected in the Port5 control register.

OutPort2[4] This bit is output on the OUTPORT2[4] output pin if so selected in the Port4 control register.

OutPort2[3] This bit is output on the OUTPORT2[3] output pin if so selected in the Port3 control register.

OutPort2[2] This bit is output on the OUTPORT2[2] output pin if so selected in the Port2 control register.

OutPort2[1] This bit is output on the OUTPORT2[1] output pin if so selected in the Port1 control register.

OutPort2[0] This bit is output on the OUTPORT2[0] output pin if so selected in the Port0 control register

0xE0B— (OUT2H) OUTPORT2 Control Register [high byte])

7	6	5	4	3	2	1	0
—	—	—	—	OutPort2[11]	OutPort22[10]	OutPort2[9]	OutPort2[8]

Value after reset: 00

Direction: Read/Write

OutPort2[11] This bit is output on the OUTPORT2[11] output pin if so selected in the Port11 control register.

OutPort2[10] This bit is output on the OUTPORT2[10] output pin if so selected in the Port10 control register.

OutPort2[9] This bit is output on the OUTPORT2[9] output pin if so selected in the Port9 control register.

OutPort2[8] his bit is output on the OUTPORT2[8] output pin if so selected in the Port8 control register.

0xE0C— IN1L (INPORT1 Status Register [low byte])

7	6	5	4	3	2	1	0
InPort1[7]	InPort1[6]	InPort1[5]	InPort1[4]	InPort1[3]	InPort1[2]	InPort1[1]	InPort1[0]

Value after reset: 00

Direction: Read/Write

InPort1[7] This bit reflects the current state of the INPORT1[7] input pin.

InPort1[6] This bit reflects the current state of the INPORT1[6] input pin.

InPort1[5] This bit reflects the current state of the INPORT1[5] input pin.

InPort1[4] This bit reflects the current state of the INPORT1[4] input pin.

InPort1[3] This bit reflects the current state of the INPORT1[3] input pin.

InPort1[2] This bit reflects the current state of the INPORT1[2] input pin.

InPort1[1] This bit reflects the current state of the INPORT1[1] input pin.

InPort1[0] This bit reflects the current state of the INPORT1[0] input pin.

0xE0D—IN1H (INPORT1 Status Register [high byte])

7	6	5	4	3	2	1	0
—	—	—	—	InPort1[11]	InPort1[10]	InPort1[9]	InPort1[8]

Value after reset: 00

Direction: Read/Write

InPort1[11] This bit reflects the current state of the INPORT1[11] input pin.

InPort1[10] This bit reflects the current state of the INPORT1[10] input pin.

InPort1[9] This bit reflects the current state of the INPORT1[9] input pin.

InPort1[8] This bit reflects the current state of the INPORT1[8] input pin.

0xE0E—IN2L (INPORT2 Status Register [low byte])

7	6	5	4	3	2	1	0
InPort2[7]	InPort2[6]	InPort2[5]	InPort2[4]	InPort2[3]	InPort2[2]	InPort2[1]	InPort2[0]

Value after reset: 00

Direction: Read/Write

InPort2[7] This bit reflects the current state of the INPORT2[7] input pin.

InPort2[6] This bit reflects the current state of the INPORT2[6] input pin.

InPort2[5] This bit reflects the current state of the INPORT2[5] input pin.

InPort2[4] This bit reflects the current state of the INPORT2[4] input pin.

InPort2[3] This bit reflects the current state of the INPORT2[3] input pin.

InPort2[2] This bit reflects the current state of the INPORT2[2] input pin.

InPort2[1] This bit reflects the current state of the INPORT2[1] input pin.

InPort2[0] This bit reflects the current state of the INPORT2[0] input pin.

0xE0F—IN2H (INPORT2 Status Register [high byte])

7	6	5	4	3	2	1	0
—	—	—	—	InPort2[11]	InPort2[10]	InPort2[9]	InPort2[8]

Value after reset: 00

Direction: Read/Write

InPort2[11] This bit reflects the current state of the INPORT2[11] input pin.

InPort2[10] This bit reflects the current state of the INPORT2[10] input pin.

InPort2[9] This bit reflects the current state of the INPORT2[9] input pin.

InPort2[8] This bit reflects the current state of the INPORT2[8] input pin.

0xE10—INCL (INPORT2 Control Register [low byte])

7	6	5	4	3	2	1	0
InMode[7]	InMode[6]	InMode[5]	InMode[4]	InMode[3]	InMode[2]	InMode[1]	InMode[0]

Value after reset: 00

Direction: Read/Write

InMode[7] When set to 0, the INPORT2[7] and INPORT1[7] pins function as input pins. When set to 1, the INPORT2[7] and INPORT1[7] pins function as TxSync[7] and RxSync[7], respectively.

InMode[6] When set to 0, the INPORT2[6] and INPORT1[6] pins function as input pins. When set to 1, the INPORT2[6] and INPORT1[7] pins function as TxSync[6] and RxSync[6], respectively.

InMode[5] When set to 0, the INPORT2[5] and INPORT1[5] pins function as input pins. When set to 1, the INPORT2[5] and INPORT1[7] pins function as TxSync[5] and RxSync[5], respectively.

InMode[4] When set to 0, the INPORT2[4] and INPORT1[4] pins function as input pins. When set to 1, the INPORT2[4] and INPORT1[4] pins function as TxSync[4] and RxSync[4], respectively.

InMode[3] When set to 0, the INPORT2[3] and INPORT1[3] pins function as input pins. When set to 1, the INPORT2[3] and INPORT1[3] pins function as TxSync[3] and RxSync[3], respectively.

InMode[2] When set to 0, the INPORT2[2] and INPORT1[2] pins function as input pins. When set to 1, the INPORT2[2] and INPORT1[2] pins function as TxSync[2] and RxSync[2], respectively.

InMode[1] When set to 0, the INPORT2[1] and INPORT1[1] pins function as input pins. When set to 1, the INPORT2[1] and INPORT1[1] pins function as TxSync[1] and RxSync[1], respectively.

InMode[0] When set to 0, the INPORT2[0] and INPORT1[0] pins function as input pins. When set to 1, the INPORT2[0] and INPORT1[0] pins function as TxSync[0] and RxSync[0], respectively.

NOTE: When selected, RxSync[i] is output as described in Section 2.1.2. TxSync[i] is either an output or input, controlled by the bits TxSYOut (bit 3) and TxSYIn (bit 2) in CR05, Feature 2 Control Register. Additional information on the use of the TxSync[i] signal can be found in Section 2.1.1.

0xE11—INCH (INPORT Control Register [high byte])

7	6	5	4	3	2	1	0
—	—	—	—	InMode[11]	InMode[10]	InMode[9]	InMode[8]

Value after reset: 00

Direction: Read/Write

InMode[11] When set to 0, the INPORT2[11] and INPORT1[11] pins function as input pins. When set to 1, the INPORT2[11] and INPORT1[11] pins function as TxSync[11] and RxSync[11], respectively.

InMode[10] When set to 0, the INPORT2[10] and INPORT1[10] pins function as input pins. When set to 1, the INPORT2[10] and INPORT1[10] pins function as TxSync[10] and RxSync[10], respectively.

InMode[9] When set to 0, the INPORT2[9] and INPORT1[9] pins function as input pins. When set to 1, the INPORT2[9] and INPORT1[9] pins function as TxSync[9] and RxSync[9], respectively.

InMode[8] When set to 0, the INPORT2[8] and INPORT1[8] pins function as input pins. When set to 1, the INPORT2[8] and INPORT1[8] pins function as TxSync[8] and RxSync[8], respectively.

NOTE: When selected, RxSync[i] is output as described in Section 2.1.2. TxSync[i] is either an output or input, controlled by the bits TxSYOut (bit 3) and TxSYIn (bit 2) in CR05, Feature 2 Control Register. Additional information on the use of the TxSync[i] signal can be found in Section 2.1.1.

0xE80–0xE8B—PORTn (Port N Mode Control Register)

7	6	5	4	3	2	1	0
FrmBypass	CDBypass	TxTimSel[1:0]	TxTimSel[1:0]	Out1Mode[1:0]	Out1Mode[1:0]	Out2Mode	PortReset

Value after reset: 00

Direction: Read/Write

FrmBypass When set to 1, the framer is bypassed—the data path goes directly between I/O pins and the cell delineation block.

CDBypass When set to 1, the cell delineation block is bypassed—the data path goes directly between I/O pins and the framer block.

TxTimSel[1:0] These bits control the clock source for the transmitter timing.
00 = REFCLK pin (global input)
01 = TxCKI pin (per port transmit clock)
10 = RxCKI pin (per port receive clock) (loop timing)

Out1Mode[1:0] These bits control the OUTPORT1 pin for the slice. The following status is placed on the output pin:
00 = LOCD (or PLCP LOF) from cell delineator
01 = OOF from line framer
10 = Yellow alarm from line framer
11 = Bit ‘n’ from OUTPORT1 control register

Out2Mode This bit controls the OUTPORT2 pin for the slice. When set to 0, the external chip select signal for port ‘n’ is placed on the output pin. When set to 1, bit ‘n’ from the OUTPORT2 control register is placed on the output pin.

PortReset When written to a logical 1, cell delineator device logic functions (for the appropriate port) are held in reset mode.

0xE90–0xE9B—PORTINTn (Port N Interrupt Control/Status Register)

7	6	5	4	3	2	1	0
FrmrIntEn	CDIntEn	LIntEn	FrmChnEn	FrmrInt	CDInt	LInt	—

Value after reset: 0000 xxxx

Direction: Read/Write

FrmrIntEn When set to 1, the interrupts from the framer block for this port are enabled to appear on the MINTR* pin.

CDIntEn When set to 1, the interrupts from the cell delineation block for this port are enabled to appear on the MINTR* pin.

LIntEn When set to 1, the line interrupt from the INPORT1 input for this port is enabled to appear on the MINTR* pin.

FrmChnEn Framer channel enable. Set to 1 for normal operation. Set to 0 to allow programming of framer static controls.

FrmrInt This bit indicates that an interrupt has occurred in the framer block for this port.

CDInt This bit indicates that an interrupt has occurred in the cell delineation block for this port.

LInt This bit indicates that an interrupt has occurred on the LInt* input for this port.

4.0 Specifications

4.1 Absolute Maximum Ratings

Stresses above those listed as absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DDC}	Core Power Supply	–0.25	2.5	V
V_{DDO}	I/O Power Supply	–0.25	4.6	V
V_{GG}	Clamp Voltage Supply	–0.25	6.0	V
Ts	Storage Temperature	–55	125	°C
Tvsol (456-pin PBGA)	Vapor Phase Soldering Temperature (20 seconds)	—	220	°C
—	Static Discharge	–2000	2000	V
—	Latch-up Current	–100	100	mA
Tj	Junction Temperature	—	150	°C
θ_{JA} (456-pin PBGA)	Thermal Resistance, Still Air	—	20	°C/W
$V_{i,hiz}$	Signal Pin Voltage: Input / Hi-Z Output	–0.5	V_{GG}+ 0.5	V
$V_{o,\ loz}$	Signal Pin Voltage: Output Lo-Z	–0.5	V_{DDO} + 0.5	V

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions (Table 4-2 in the Data Sheet)

Symbol	Parameter	Minimum	Maximum	Units
VDDC	Core Power Supply	1.71	1.89	V
VDDO	I/O Power Supply	3.135	3.465	V
VGG	Clamp Voltage Supply	VDDO	5.25	V
Tamb	Ambient Operating Temperature	–40	85	°C
Vh	Input Hysteresis	0.3	—	V
Vih	Input High Voltage, TTL	2.0	VDDO	V
Vth	Input High Threshold Voltage, Hysteresis	0.7 * VDDO	VGG + 0.25	V
Vil	Input Low Voltage, TTL	0	0.8	V
Vtl	Input Low Threshold Voltage, Hysteresis	0	0.3 * VDDO	V
Vih	JTAG TReset	2.6	VDDO	V
Vil	JTAG TCLK	0	0.1 * VDDO	V

4.3 DC Characteristics

All inputs and bidirectional signals have input thresholds compatible with TTL drive levels. All outputs are CMOS drive levels and can be used with CMOS or TTL logic.

Table 4-3. DC Characteristics

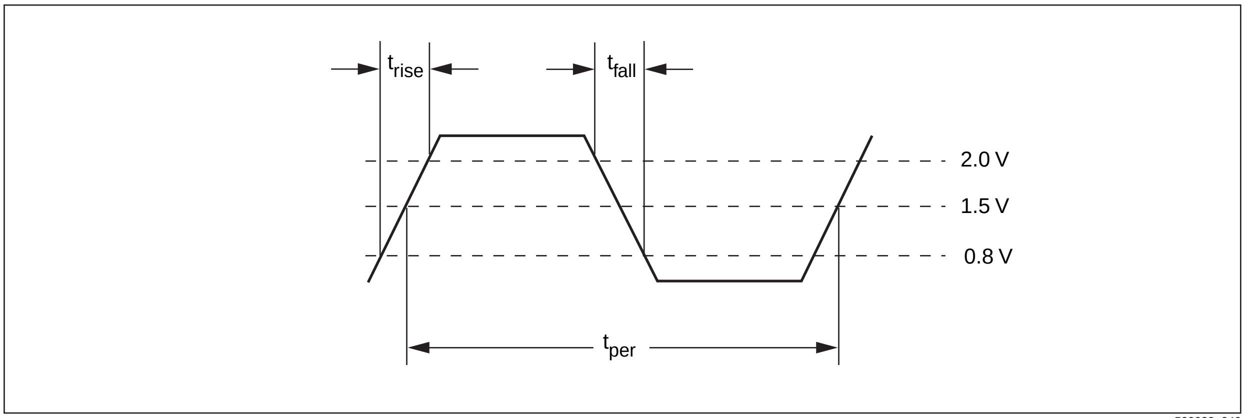
Symbol	Parameter	Minimum	Typical	Maximum	Units
Voh	Output High Voltage (Ioh = –400 μA)	2.4	—	—	V
Vol	Output Low Voltage (Iol = 4 mA)	—	—	0.4	V
Iod	Open Drain Output Current Sink	—	—	3 (TBD)	mA
RPU	Pullup Resistance	50	—	200	kΩ
RPD	Pulldown Resistance	50	—	200	kΩ
Ipr	Resistive Pullup Current	40 (TBD)	100 (TBD)	500 (TBD)	mA
Il	Input Leakage Current	–1 (TBD)	1 (TBD)	1 (TBD)	mA
Ioz	Three-State Leakage Current	–10 (TBD)	1 (TBD)	10 (TBD)	mA
Cin	Input Capacitance (f = 1 MHz, Vin = 2.4 V)	—	2 (TBD)	—	pF
Cio	I/O Capacitance	—	5 (TBD)	—	pF
Cout	Output Capacitance	—	2 (TBD)	—	pF
Cld	Capacitive Loading (test condition)	—	80 (TBD)	—	pF
Iosc	Short Circuit Output Current	40 (TBD)	50 (TBD)	160 (TBD)	mA
IDDC+IDDO	Supply Current (mode: DS3/PLCP) VODC = 1.89 V VODO = 3.465 V, outputs unloaded	—	850 350 600	TBD	mA
IDDC IDDO	Supply Current (mode: E3 direct cell mapping) VODC = 1.89 V VODO = 3.465 V, outputs unloaded	—	TBD	TBD	mA
IDDC IDDO	Supply Current (mode: Framer bypassed) VODC = 1.89 V VODO = 3.465 V, outputs unloaded	—	TBD	TBD	mA
IDDC IDDO	Supply Current (mode: CD bypassed) VODC = 1.89 V VODO = 3.465 V, outputs unloaded	—	TBD	TBD	mA
I_{GG}	Typical Current into V_{GG} (V_{GG} = 5.25V)	—	TBD	TBD	µA

4.4 AC Characteristics

Signals are measured at the 50% point of the changing edge, except for those involving high impedance transitions, which are measured at 10% and 90%.

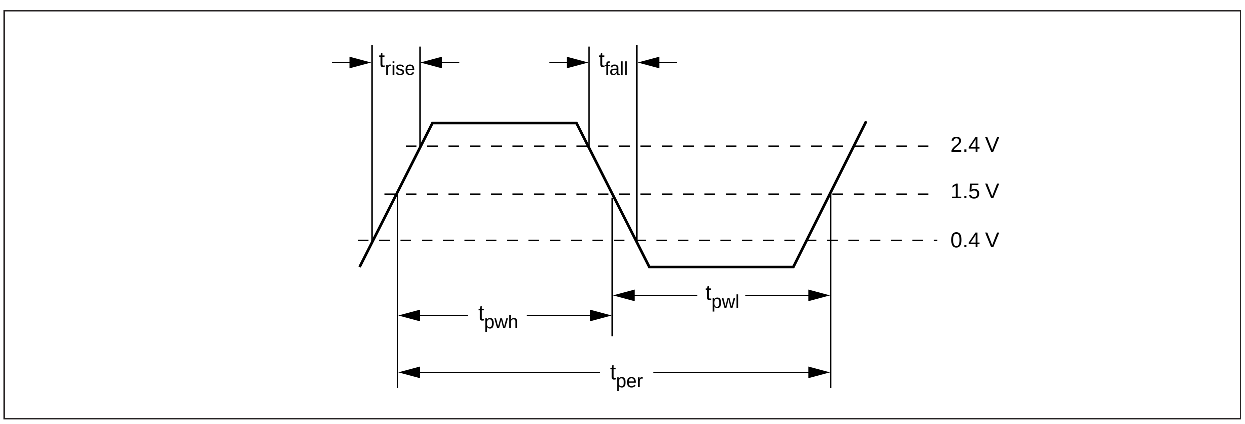
4.4.1 Clock And Signal Timing

Figure 4-1. Input Waveform



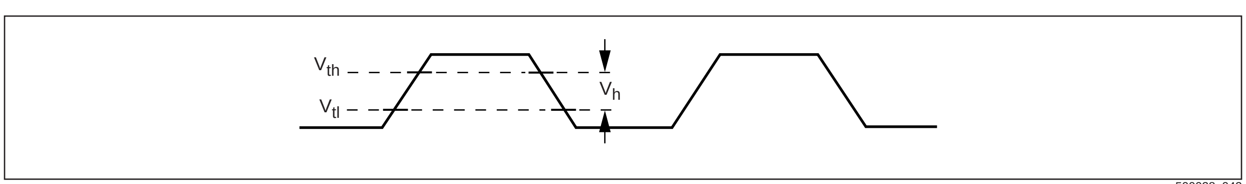
500028_040

Figure 4-2. Output Waveform



500028_041

Figure 4-3. Input Hysteresis (Schmitt Trigger Input)



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4.4.1.1 Input Clock Timing

The following illustrates the various clocks applied to the CX28365 device and associated parameters.

Figure 4-4. Input Clock Timing

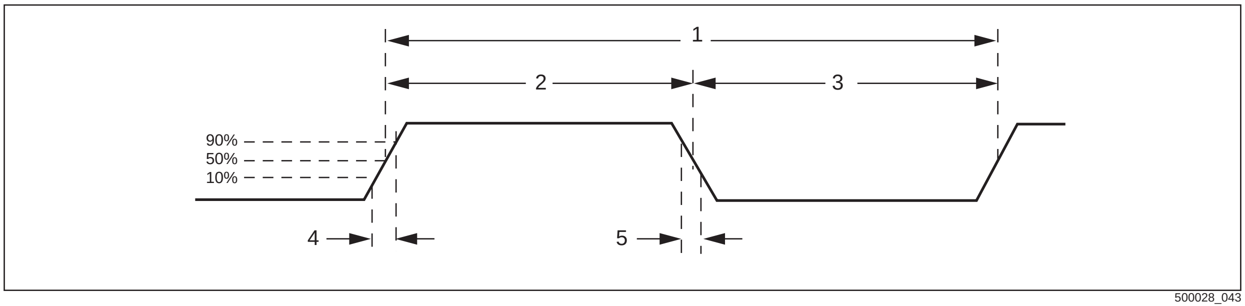

Table 4-4. Input Clock Timing

Symbol	Parameter	Minimum	Maximum	Units
1	TxCKI Frequency	34	52	MHz
1	RxCKI Frequency	34	52	MHz
2	Clock Width High/Low DS3	8.8	13.2	ns
3	Clock Width High/Low E3	11.6	17.4	ns
4	Clock Rise Time	—	3	ns
5	Clock Fall Time	—	3	ns
GENERAL NOTE: There is a limit of 40%–60% duty cycle to all clocks.				

Figure 4-5. Line Side Receiver Input Data Setup/Hold Timing

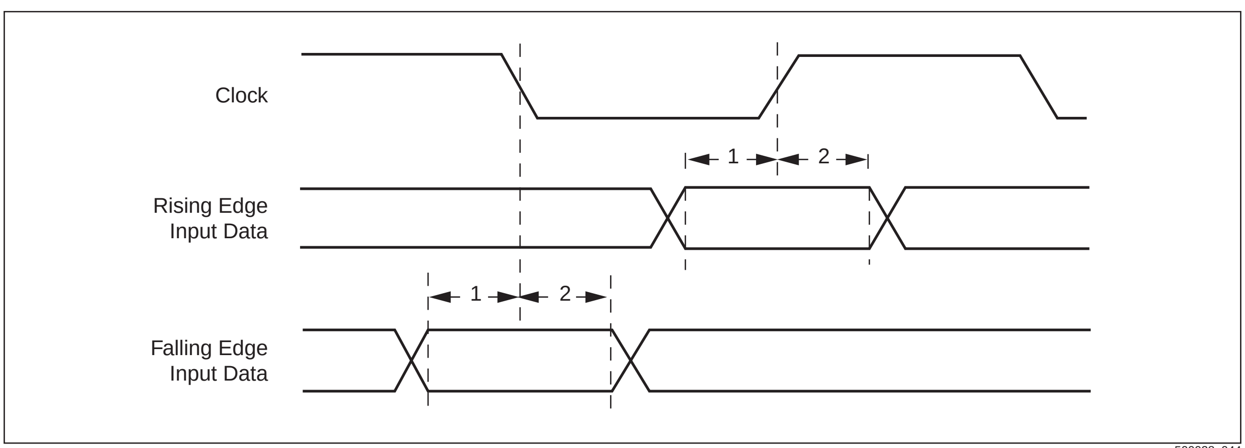

Figure 4-6. Line Side Transmitter Output Data Timing

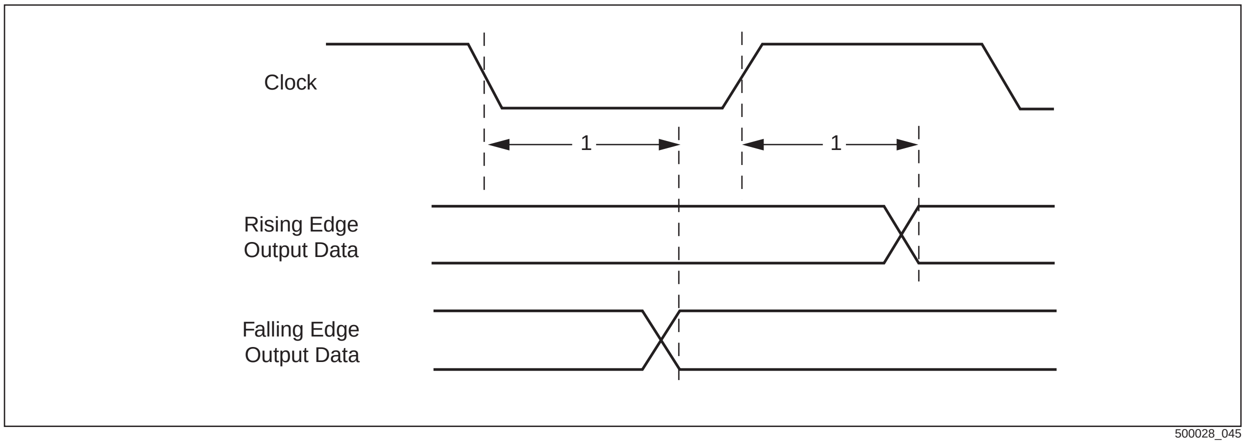

Figure 4-7. System-Side Transmitter Interface Timing

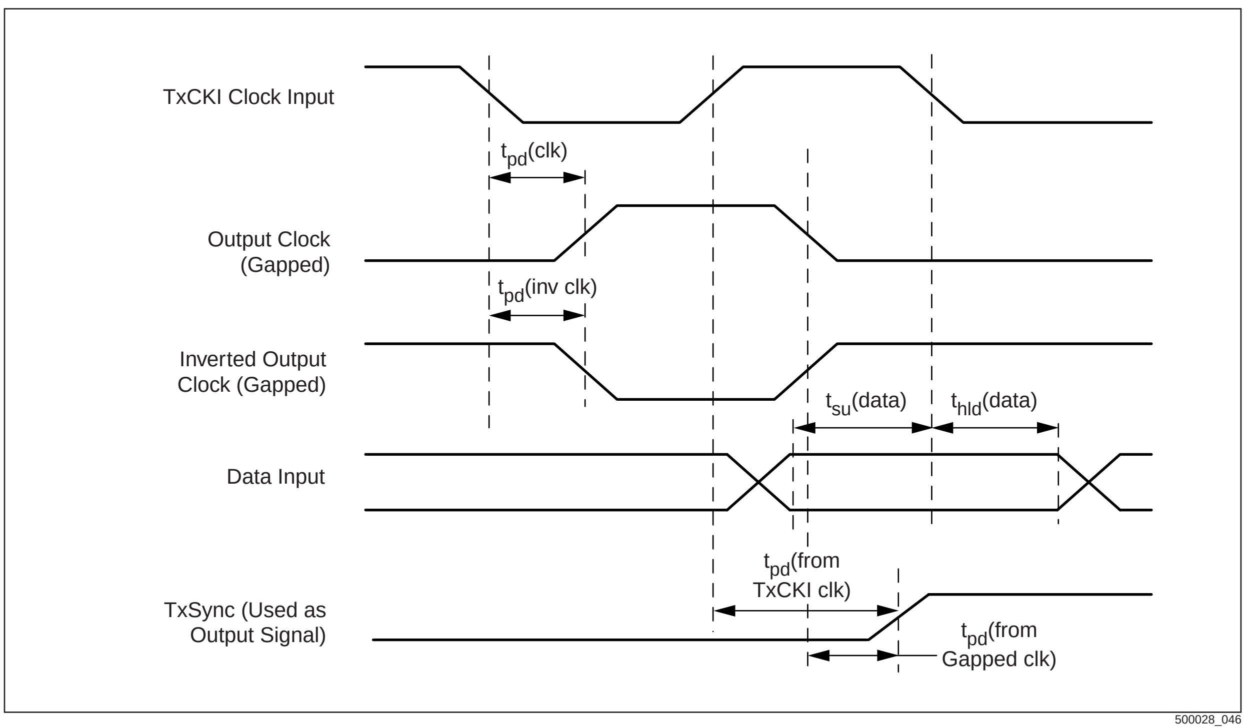

Figure 4-8. System-Side Receiver Interface Timing

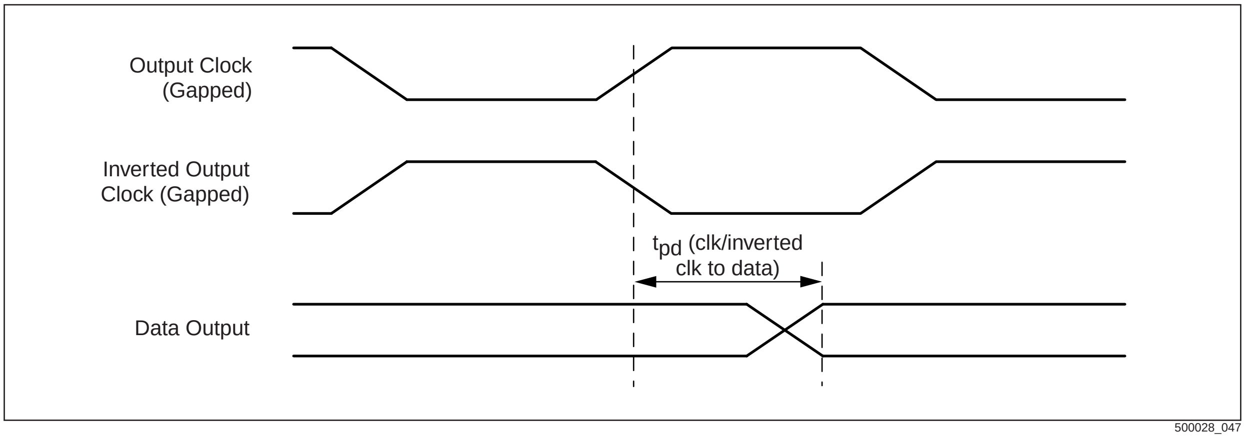

Table 4-5. Output Signal Timing

According To	Output Signal	Clock	tpd Min	tpd Max	Edge	Units
Figure 4-6	TxPOS/TxNRZ/LTxDATA	TxCKO	–3	4	Rising/Falling	ns
Figure 4-6	TxNEGO	TxCKO	–3	4	Rising/Falling	ns
Figure 4-7	TxGCKO (when inverted and not inverted)	TxCKI	1	8	Both	ns
Figure 4-7	TxSync (when set as an output signal)	Relative timing to TxCKI input clock	1	8	Rising	ns
Figure 4-7	TxSync (when set as an output signal)	Relative timing to TxGCKO (both inverted and not inverted)	–3	4	Rising/Falling	ns
Figure 4-7	TEXTCKO (when inverted and not inverted)	TxCKI	1	8	Both	ns
Figure 4-8	RxDATO	REXTCKO	–3	4	Rising/Falling	ns
Figure 4-8	RxDATO	RxGCKO	–3	4	Rising/Falling	ns
Figure 4-8	RxSYNC	RxGCKO	–3	4	Rising/Falling	ns

Table 4-6. Input Signal Timing

According To	Input Signal	Clock	tsu Min	thld Min	Edge	Units
Figure 4-7	TxDATI	TxCKI	2	4	Falling	ns
Figure 4-7	TxSync (when set as input signal)	TxCKI	2	4	Falling	ns
Figure 4-7	TEXTI	TxCKI	2	4	Falling	ns
Figure 4-5	RxPOSI/RxNRZ/LTxDATA	RxCKI	4	5	Rising/Falling	ns
Figure 4-5	RxNEGI/LCVI/LRxMRK	RxCKI	4	5	Rising/Falling	ns

4.4.2 Microprocessor Timing

Figure 4-9. Microprocessor—Read Timing

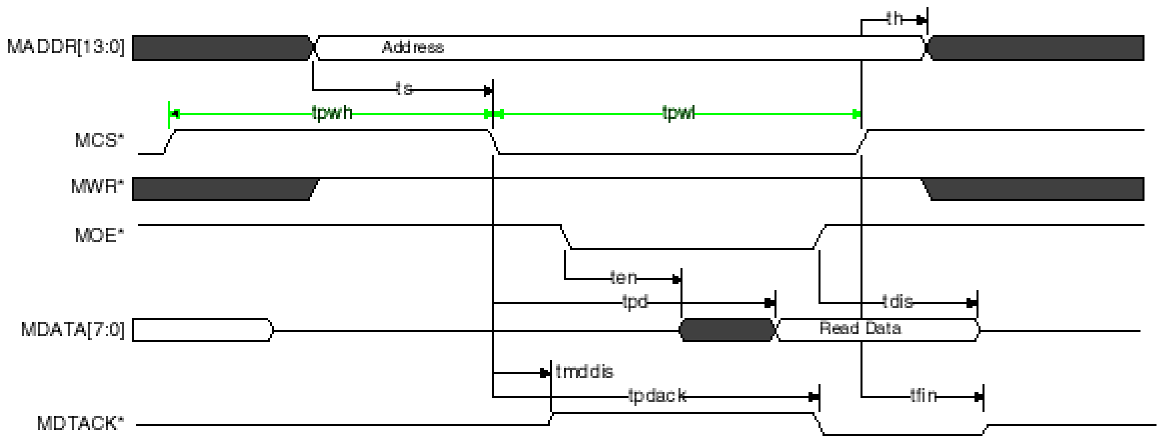

Table 4-7. Microprocessor—Read Timing

Label	Description	Min	Max	Unit
t_{pwl} (1)	Pulse Width Low (MCS*)	(1)	—	ns
t_{pwh} (1)	Pulse Width High (MCS*)	(1)	—	ns
t_s	Setup, MAddr[13:0] to the falling edge of MCS*	10	—	ns
t_h	Hold, MAddr[13:0] from the rising edge of MCS*	7	—	ns
t_{en}	Enable, MData[7:0] when both MCS* and MOE* go active	2	13	ns
t_{pd} (2)	Propagation Delay, Mdata[7:0] from the falling edge of MCS*	—	(2)	ns
t_{dis}	Disable, MData[7:0] when either MCS* or MOE* goes inactive	2	13	ns
t_{mddis}	MDTACK deasserts, from the falling edge of MCS*, data is invalid	2	13	ns
t_{pdack} (3)	MDTACK asserts, data is valid	—	(3)	ns
t_{fin}	Read cycle complete, MDTACK 3-states when MCS* goes inactive	2	13	ns

FOOTNOTE:
(1) 1.5 × MCLK or 35 ns whichever is larger.
(2) $[5 \times t_{RxCKI} + 30]$ or $[2 \times t_{MCLK} + 30]$ whichever is larger. t_{RxCKI} is the period of RxCKI and t_{MCLK} is the period of MCLK.
(3) $[7 \times t_{RxCKI} + 30]$ or $[4 \times t_{MCLK} + 30]$ whichever is larger. t_{RxCKI} is the period of RxCKI and t_{MCLK} is the period of MCLK.

Figure 4-10. Microprocessor—Write Timing

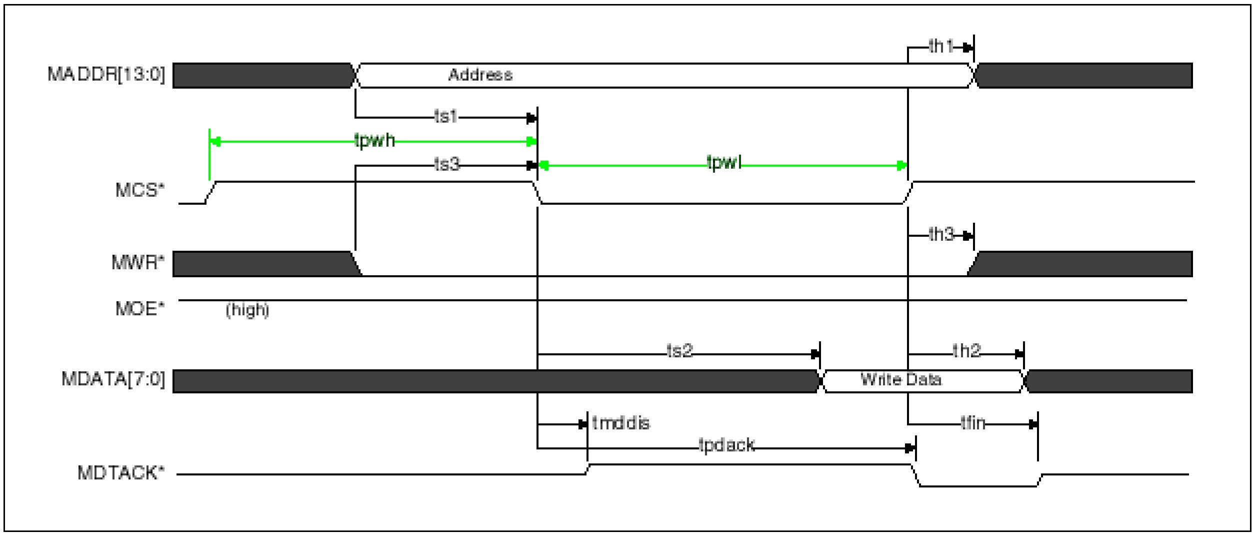

Table 4-8. Microprocessor—Write Timing

Label	Description	Min	Max	Unit
t_{pwl}(1)	Pulse Width Low (MCS*)	(1)	—	ns
t_{pwh}(1)	Pulse Width High (MCS*)	(1)	—	ns
t_{s1}	Setup, MAddr[13:0] to the falling edge of MCS*	10	—	ns
t_{h1}	Hold, MAddr[13:0] from the rising edge of MCS*	7	—	ns
t_{s2}	Setup, MData[7:0] to the falling edge of MCS*	—	t_{ck}(min) – 8	ns
t_{h2}(2)	Hold, MData[7:0] from the rising edge of MCS*	7	—	ns
t_{s3}	Setup, MWR* to the falling edge of MCS*	2	—	ns
t_{h3}	Hold, MWR* from the rising edge of MCS*	2	—	ns
t_{mddis}	MDTACK deasserts, from the falling edge of MCS*, data is invalid	2	13	ns
t_{pdack}(3)	Propagation delay, MDTACK from the falling edge of MCS*	—	(3)	ns
t_{fin}	Write cycle complete, MDTACK 3-states when MCS* goes inactive	2	13	ns

FOOTNOTE: Note(s):
(1) 1.5 × MCLK or 35 ns whichever is larger.
(2) t_{ck} (min) is the period of MCLK or RxCKI, whichever is smaller. (highest frequency)
(3) [7 × t_{RxCKI} + 30] or [4 × t_{MCLK} + 30] whichever is larger. t_{RxCKI} is the period of RxCKI and t_{MCLK} is the period of MCLK.

4.4.2.1 Additional Restrictions

The following restrictions apply:

- When the clock source has been changed due to a setup change (RxFIFEn, LineLp, SourceLp, PayldLp, RlineLp), the CX28365 should not be accessed for 20 of the slowest clock cycles.
- After software reset, the CX28365 should not be accessed for 40 of the slowest clock cycles.
- The OneSec pulse minimal width should be 120 ns.
- When output pin MINTR* is activated, the microprocessor reads the Source Channel Status register and must wait at least one-half cycle of the slowest clock to read the updated information in the Source Channel register.

4.4.3 UTOPIA Interface Timing

Figures 4-11 through 4-12 and Tables 4-9 through 4-10 provide the timing requirements and characteristics of the UTOPIA interface.

Figure 4-11. UTOPIA Transmit Timing

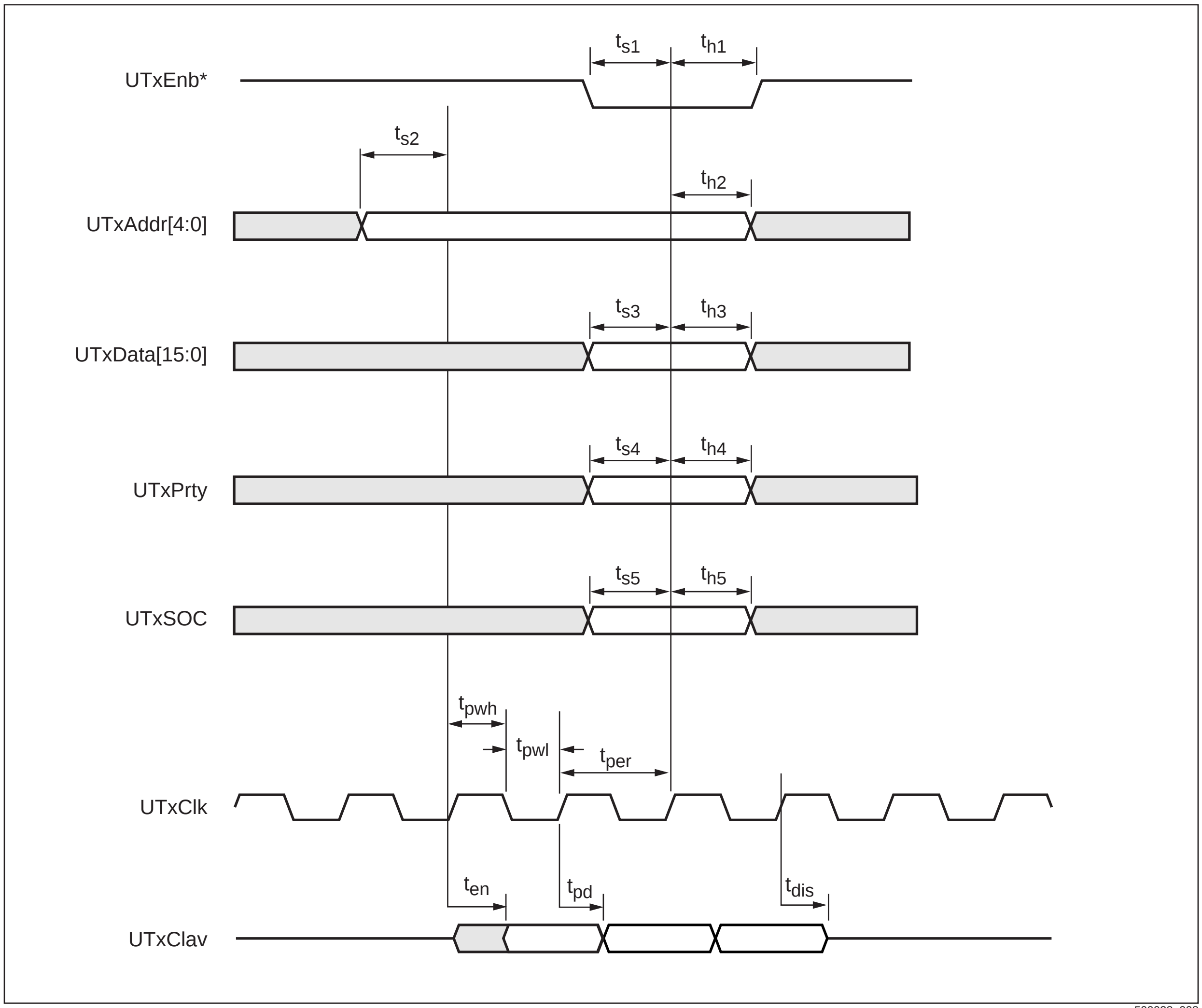

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Table 4-9. UTOPIA Transmit Timing

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, UTxClk	8	—	ns
t_{pwh}	Pulse Width High, UTxClk	8	—	ns
t_{per}	Period, UTxClk	20	—	ns
t_{s1}	Setup, UTxEnb* to the rising edge of UTxClk	4	—	ns
t_{h1}	Hold, UTxEnb* from the rising edge of UTxClk	1	—	ns
t_{s2}	Setup, UTxAddr to the rising edge of UTxClk	4	—	ns
t_{h2}	Hold, UTxAddr from the rising edge of UTxClk	1	—	ns
t_{s3}	Setup, UTxData to the rising edge of UTxClk	4	—	ns
t_{h3}	Hold, UTxData from the rising edge of UTxClk	1	—	ns
t_{s4}	Setup, UTxPrty to the rising edge of UTxClk	4	—	ns
t_{h4}	Hold, UTxPrty from the rising edge of UTxClk	1	—	ns
t_{s5}	Setup, UTxSOC to the rising edge of UTxClk	4	—	ns
t_{h5}	Hold, UTxSOC from the rising edge of UTxClk	1	—	ns
t_{en}	Enable, UTxCLAV from the rising edge of UTxClk	4	13.5	ns
t_{pd}	Propagation Delay, UTxCLAV from the rising edge of UTxClk	4	13.5	ns
t_{dis}	Disable, UTxCLAV from the rising edge of UTxClk	4	13.5	ns

GENERAL NOTE:
1. Measurements made at 30 pF
2. Max column derating 35 ps/pF
3. Min column derating 15 ps/pF

Figure 4-12. UTOPIA Receive Timing

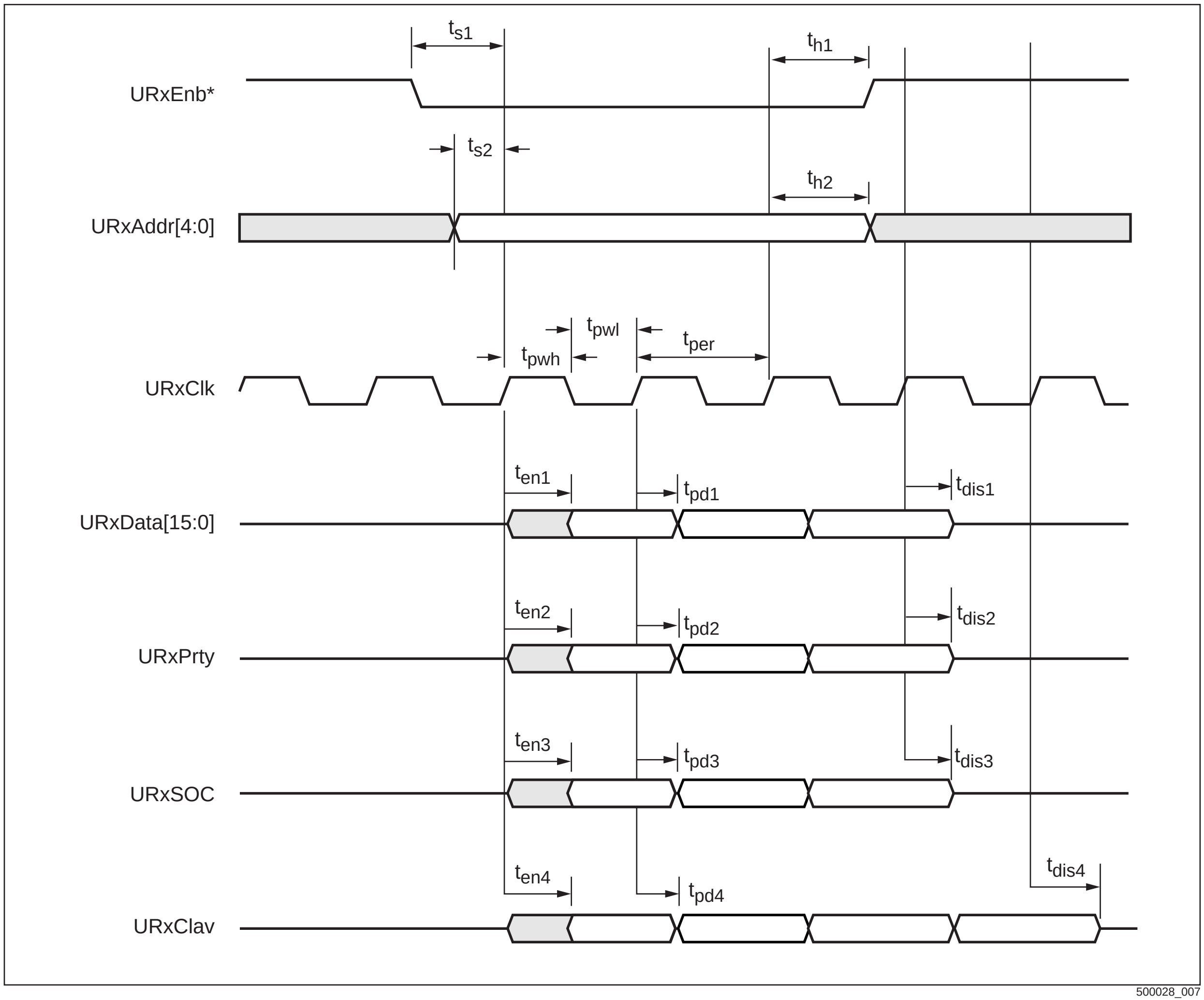


Table 4-10. UTOPIA Receive Timing

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, URxClk	8	—	ns
t_{pwh}	Pulse Width High, URxClk	8	—	ns
t_{per}	Period, URxClk	20	—	ns
t_{s1}	Setup, URxEnb* to the rising edge of URxClk	4	—	ns
t_{h1}	Hold, URxEnb* from the rising edge of URxClk	1	—	ns
t_{s2}	Setup, URxAddr to the rising edge of URxClk	4	—	ns
t_{h2}	Hold, URxAddr from the rising edge of URxClk	1	—	ns
t_{en1}	Enable, URxData[15:0] from the rising edge of URxClk	4	13.5	ns
t_{pd1}	Propagation Delay, URxData[15:0] from the rising edge of URxClk	4	13.5	ns
t_{dis1}	Disable, URxData[15:0] from the rising edge of URxClk	4	13.5	ns
t_{en2}	Enable, URxPrty from the rising edge of URxClk	4	13.5	ns
t_{pd2}	Propagation Delay, URxPrty from the rising edge of URxClk	4	13.5	ns
t_{dis2}	Disable, URxPrty from the rising edge of URxClk	4	13.5	ns
t_{en3}	Enable, URxSOC from the rising edge of URxClk	4	13.5	ns
t_{pd3}	Propagation Delay, URxSOC from the rising edge of URxClk	4	13.5	ns
t_{dis3}	Disable, URxSOC from the rising edge of URxClk	4	13.5	ns
t_{en4}	Enable, URxCLAV from the rising edge of URxClk	4	13.5	ns
t_{pd4}	Propagation Delay, URxCLAV from the rising edge of URxClk	4	13.5	ns
t_{dis4}	Disable, URxCLAV from the rising edge of URxClk	4	13.5	ns

GENERAL NOTE:
1. Measurements made at 30 pF
2. Max column derating 35 ps/pF
3. Min column derating 15 ps/pF

4.4.4 One-Second Interface Timing

Figure 4-13 and Table 4-11 illustrate the timing requirements and characteristics of the one-second interface.

Figure 4-13. One-Second Timing

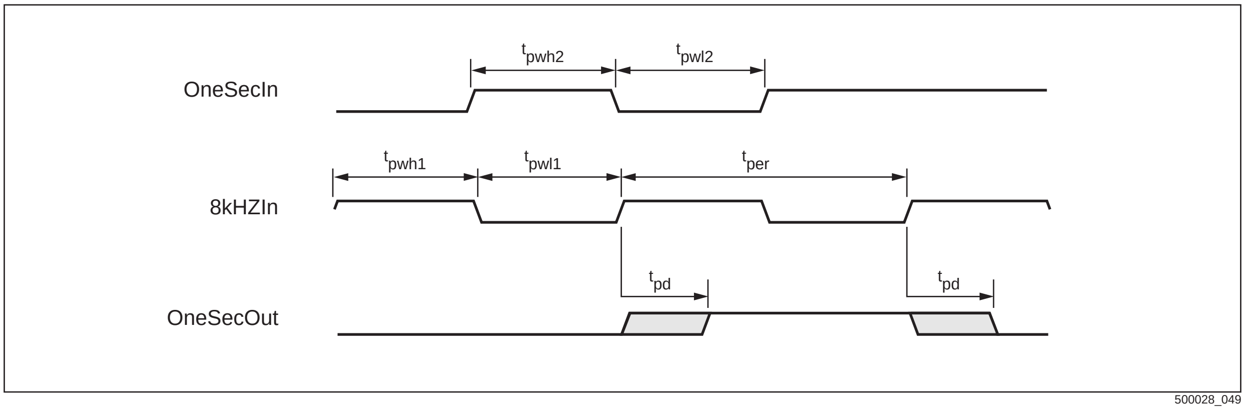


Table 4-11. One-Second Timing[1]

Label	Description	Min	Max	Unit
t_{pwl2}	Pulse Width Low, OneSecIn	125	—	ns
t_{pwh2}	Pulse Width High, OneSecIn	125	—	ns
t_{pwl1}	Pulse Width Low, 8KHzIn	62500	—	ns
t_{pwh1}	Pulse Width High, 8KHzIn	62500	—	ns
t_{per}	Period, 8KHzIn	125000	—	ns
t_{pd}	Propagation Delay, OneSecOut from the rising edge of OneSecClk	1	15	ns

FOOTNOTE:
(1) Assuming MCLK = 50 MHz.

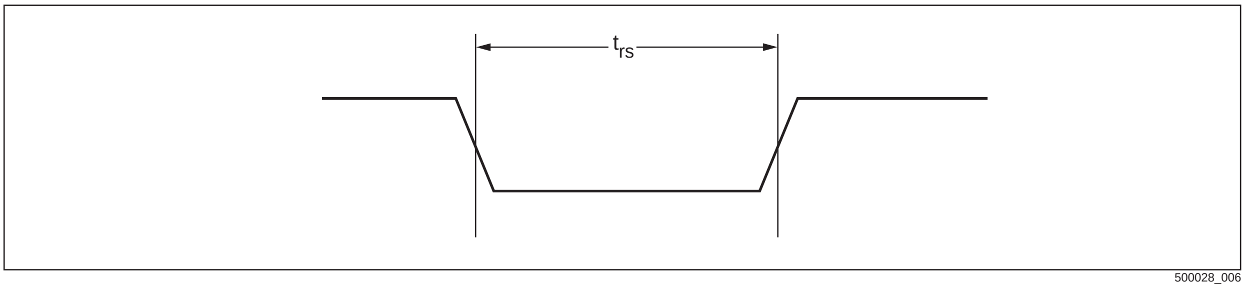
4.4.5 MReset* Timing

Table 4-12. Reset Timing

Label	Description	Min	Max	Unit
t_{RS}	MReset* pulse[(1)]	$30 \times (t_{RxCKI})$ and (t_{TxCKI})	—	cycles

FOOTNOTE:
(1) t_{RxCKI} is the period of the DS3/E3 receive line clock.
t_{TxCKI} is the period of the DS3/E3 transmit line clock.

Figure 4-14. MReset Timing



4.4.6 JTAG Interface Timing

Figure 4-15 and Table 4-13 show the timing requirements and characteristics of the JTAG interface.

Figure 4-15. JTAG Timing

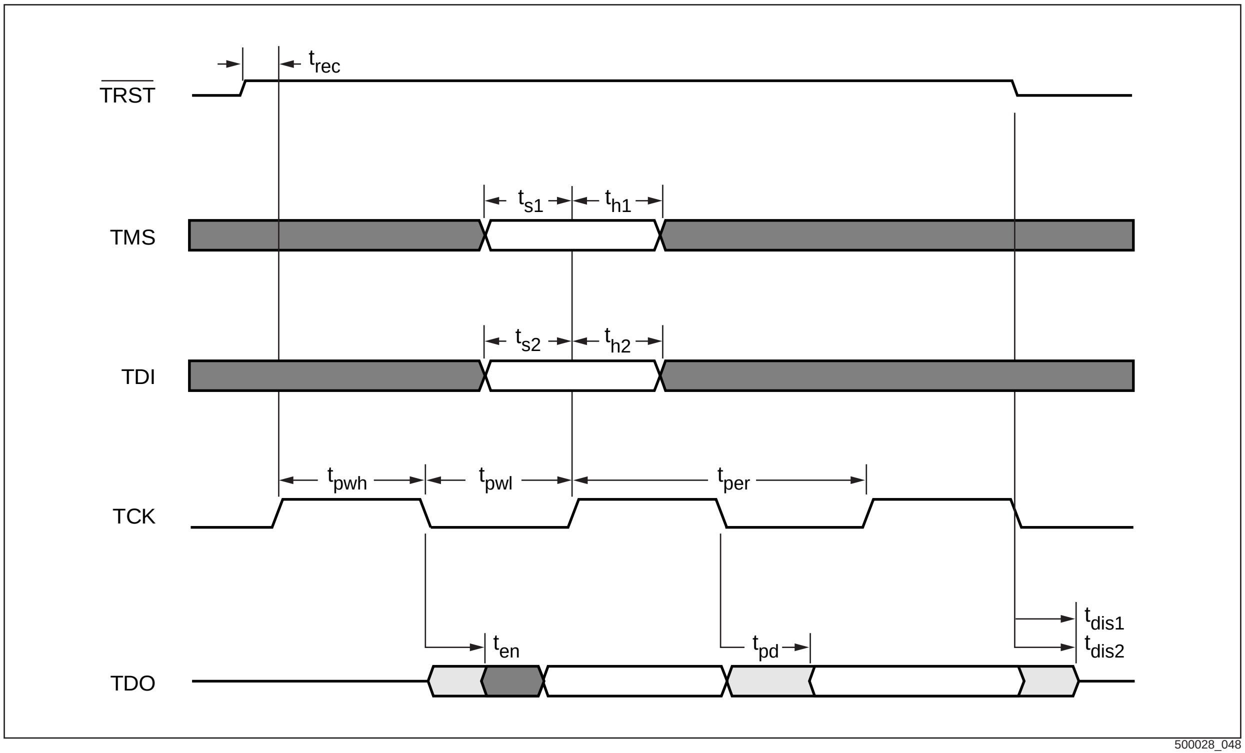
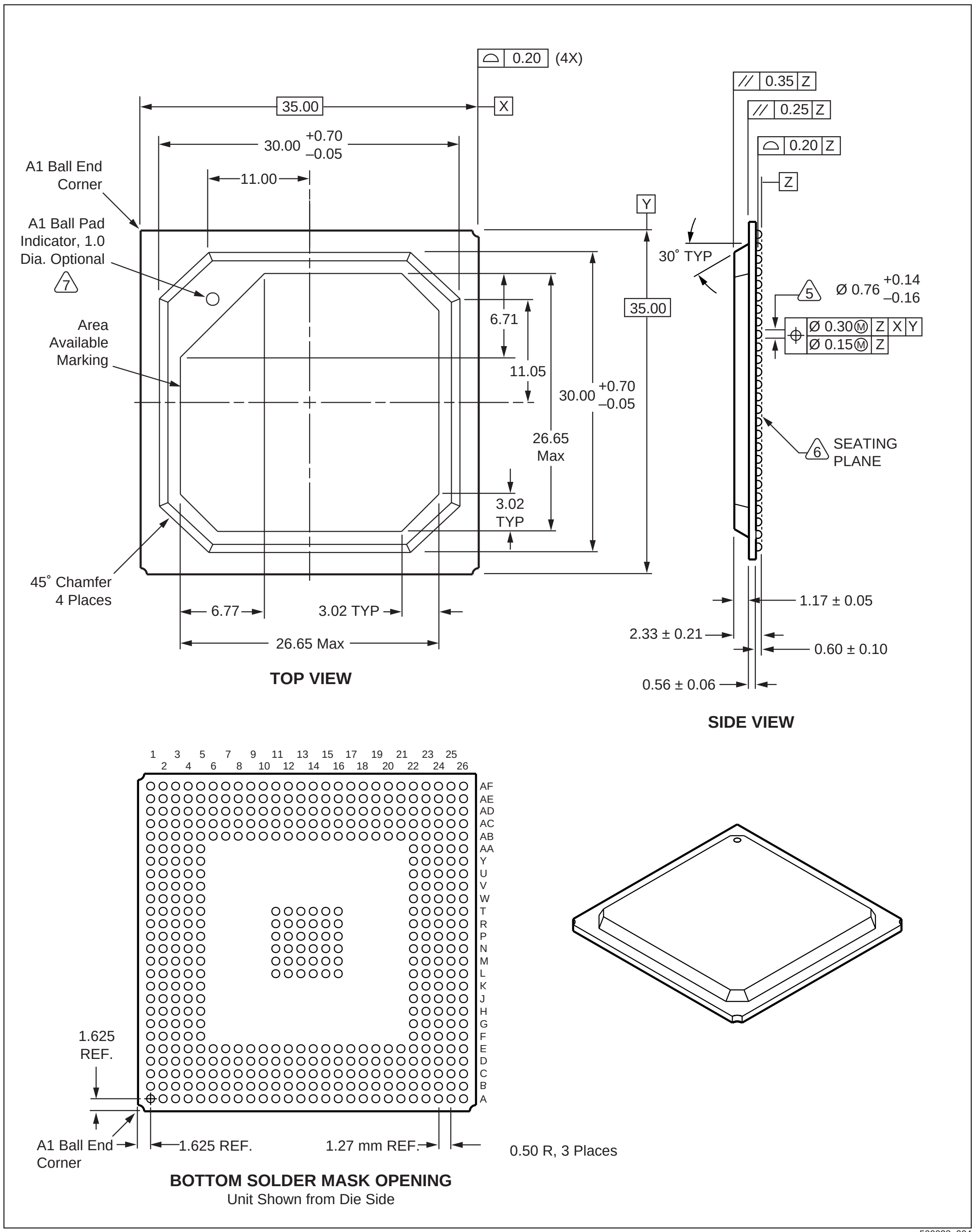


Table 4-13. JTAG Timing

Label	Description	Min	Max	Unit
t_{pwl}	Pulse Width Low, TCK	16	—	ns
t_{pwh}	Pulse Width High, TCK	16	—	ns
t_{per}	Period, TCK	40	—	ns
t_{rec}	Recovery, the rising edge of TCK from the rising edge of TRST*	2.5	—	ns
t_{s1}	Setup, TMS to the rising edge of TCK	2	—	ns
t_{h1}	Hold, TMS from the rising edge of TCK	—	1	ns
t_{s2}	Setup, TDI to the rising edge of TCK	2	—	ns
t_{h2}	Hold, TDI from the rising edge of TCK	—	1	ns
t_{en}	Enable, TDO from the falling edge of TCK	0.8	5	ns
t_{pd}	Propagation Delay, TDO from the falling edge of TCK	0.8	5	ns
t_{dis1}	Disable, TDO from the falling edge of TCK	0.8	5	ns
t_{dis2}	Disable, TDO from the falling edge of TRST*	0.8	5	ns

5.0 Package Specifications

Figure 5-1. Package Drawing



Appendix A: Device Initialization

To reliably initialize the device, use the following initialization routine:

```
1)  device master reset                 0xe00   0x01
                                        0xe00   0x00
2)  assert port logic reset             0xe80   0x01
3)  disable cell receiver               0x00c   0x02
4)  enable framer                       0xe90   0x10
5)  set atm frame type                  0x004   0x*
6)  set framer type                     0x820   0x*
7)  enable plcp                         0x300   0x80
8)  set rx_sync polarity                0x005   0x40
9)  set tx_sync polarity                0x005   0x50
10) set rx_clk polarity                 0x005   0x70
11) set tx sync pin to output           0x825   0x08
12) set rx gap clock to clock all data  0x82c   0x01
```

To enable a port:

```
13) reset tx and rx fifo                0x00d   0xc0
                                        0x00d   0x00
14) disassert port logic reset          0xe80   0x00
15) enable utopia output                0x00e   0x00
16) enable cell receiver                0x00c   0x00
```

* To select the proper configuration, see PMODE, Port Mode Control, in the Cell Delineation register group and CR00, Mode Control, in the Framer register group in this data sheet.

Repeat steps 2–16 with the proper offsets for each port.

Appendix B: Frame Structure Summary

As per ANSI T1.107-1995 and ITU-T G.704-1995, in DS3 mode, a frame is composed of 4760 bits, of which, 4704 (4697 in M13/M23) form the payload, while 56 (63 in M13/M23) are Opportunity bits. The Opportunity bits are divided into several fields, which are described in Table B-1.

Table B-1. Overhead Bits in DS3 Mode

Field	Description
3 M-bits	Bits 2721, 3401 & 4081 for framing, bearing a “010” pattern
28 F-bits	Every 170 bits, from bit 86 to bit 4676 for subframing, bearing a “1001”x7 pattern
2 X-bits	Bits 1 and 681 for remote alarm indication (RAI), bearing a “11” pattern to signal error-free conditions, a “00” pattern to signal RAI
2 P-bits	Bits 1361 and 2041 for parity, bearing a “11” pattern if the digital sum of all the 4704 payload bits of the preceding frame equals 1, a “00” pattern if it equals 0
In DS3 M13/M23 Mode Only	
21 C-bits	Bits 171, 341, 511, 851, 1021, 1191, 1531, 1701, 1871, 2211, 2381, 2551, 2891, 3061, 3231, 3571, 3741, 3911, 4251, 4421, and 4591 for justification control bits of the payload data channels
7 Stuff Opportunity bits	Bits 597, 1278, 1959, 2640, 3321, 4002, and 4683
In DS3 C-bit Parity Mode Only	
1 Cb11 bit	Bit 171 for Application Identification Channel (AIC), set to 1
1 Cb12 bit	Bit 341 reserved, set to 1
1 Cb13 bit	Bit 511 for Far-End Alarm and Control (FEAC), bearing FEAC messages when active, set to 1 when inactive
3 Cb2 bits	Bits 851, 1021, and 1191 reserved, bearing a “111” pattern
3 Cb3 bits	Bits 1531, 1701, and 1871 for path parity, set to equal P-bits by terminating equipment (not to be modified by path equipment)
3 Cb4 bits	Bits 2211, 2381, and 2551 for Far-End Block Error (FEBE), bearing a “111” pattern to signal error-free conditions, any other to signal FEBE
3 Cb5 bits	Bits 2891, 3061, and 3231 for terminal data link (DL), bearing data link messages and flags when active, a “111” pattern when inactive
3 Cb6 bits	Bits 3571, 3741, and 3911 reserved, bearing a “111” pattern
3 Cb7 bits	Bits 4251, 4421, and 4591 reserved, bearing a “111” pattern

As per ITU-T G.751, in E3-G751 mode, a frame is composed of 1536 bits, of which, 1508 form the payload, while 28 are Opportunity bits. The Opportunity bits are divided into several fields, which are described in Table B-2.

Table B-2. Overhead Bits in E3-G751 Mode

Field	Description
10 FAS bits	Bits 1 to 10 for framing, bearing a “1111010000” (left-to-right) pattern
1 A-bit	Bit 11 for remote alarm indication (RAI), set to 0 to signal error-free conditions, to 1 to signal RAI
1 N-bit	Bit 12 for terminal data link (DL), bearing data link messages and flags when active, set to 1 when inactive
12 C_j-bits	Bits 385 to 388, 769 to 772, and 1153 to 1156 for justification control bits of the payload data channels
4 Stuff Opportunity bits	Bits 1157 to 1160

As per ITU-T G.832-1995 and ETS 300 337-1997, in E3-G832 mode, a frame is composed of 537 bytes (octets), of which, 530 form the payload, while 7 are Opportunity bytes. The Opportunity bytes are divided into several fields, which are described in Table B-3.

Table B-3. Overhead Bytes in E3-G832

Field	Description
2 FA bytes	Bytes 1 and 2 for framing, bearing a “1111011000101000” (left-to-right) pattern
1 EM byte	Byte 61 for BIP-8 even parity, each bit set to 1 if the digital sum of the 537 corresponding payload and Opportunity bits of the preceding frame equals 1, to 0 if it equals 0
1 TR byte	Byte 121 for trail trace, bearing 16-byte trail trace messages
1 RDI bit	Bit 1 of byte 181 (MA byte) for Remote Defect Indication (RDI), set to 0 to signal error-free conditions, to 1 to signal RDI
1 REI bit	Bit 2 of byte 181 (MA byte) for Remote Error Indication (REI), set to 0 to signal error-free conditions, to 1 to signal REI
3 PT bits	Bits 3 to 5 of byte 181 (MA byte) for Payload Type (PT) information
2 PD/MI bits	Bit 6 and 7 of byte 181 (MA byte) for Payload-Dependent (PD) information or Multiframe Indication (MI)
1 TM/SSM bit	Bit 8 of byte 181 (MA byte) for Timing Marker (TM) or Synchronization Status Message (SSM)
1 NR byte	Byte 241 for network operator use, optionally carrying a terminal data link (DL)
1 GC byte	Byte 301 for general-purpose communications channel, optionally carrying a terminal data link (DL)

Appendix C: B3ZS/HDB3 Encoding

The definitions of B3ZS and HDB3 encoding, according to the ITUT-G.703 standard, are:

- In DS3 mode of operation, when rail (bipolar) mode is enabled, B3ZS encoding is performed. Each block of three successive zeros is replaced by 00V or B0V. The choice of 00V or B0V is made so that the number of B pulses between consecutive V pulses is odd.
- Both in E3-G.751 and E3-832 modes of operation, when rail mode is enabled, HDB3 encoding is performed. Each block of four successive zeros is replaced by 000V or B00V. The choice of 000V or B00V is made so that the number of B pulses between consecutive V pulses is odd.

NOTE: In the definitions, B represents an inserted pulse conforming to the B3ZS/HDB3 rule, and V represents a violation.

Appendix D: Acronyms

Acronym	Definition
AIC	Application Identification Channel
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
ATM	Asynchronous Transfer Mode
BER	Bit Error Ratio (Rate)
BGA	Ball Grid Array
BIP	Bit Interleaved Parity
BPV	Bipolar Violation
BSDL	Boundary Scan Description Language
CDM	Charged Device Model
DS	Digital Service (Signal)
EM	Error Monitoring
EOM	End of Message
ESD	Electrostatic Discharge
ETS	European Telecommunications Standards
FAS	Frame Alignment Signal
FBE	Framing Bit Error
FCS	Frame Check Sequence
FEAC	Far-End Alarm Control
FEBE	Far-End Block Error
FIFO	First-In First-Out
HBM	Human Body Model
HDLC	High-Level Data Link Control
IEEE	Institute of Electrical and Electronic Engineers

Acronym	Definition
ISO	International Organization for Standardization
ITU	International Telecommunications Union
JTAG	Joint Test Action Group
LAPD	Link Access Procedure Direct (Digital)
LCV	Line Code Violation
LIU	Line (LAN) Interface Unit
LOS	Loss of Signal
LSB	or LSBit—Least Significant Bit [use second form when confusion could result]
MI	Multiframe Indication
MPU	Microprocessor Interface
MSB	or Msbit—Most Significant Bit [use second form when confusion could result]
NRZ	Non-Return to Zero
NR	Network reserved bit
OOF	Out-of-Frame
PBD	P-Bit Disagreement
PBXs	Private Branch Exchanges
PCM	Pulse Code Modulation
PD	Protocol Discriminator/Payload Dependent
PER	Parity Error
PMD	physical media dependant
PPER	Path Parity Error
RAI	Remote Alarm Indication
RDI	Remote Detection Indication or Remote Defect Indicator
RDL	Receive Data Link
REI	Remote Error Indication
RFEAC	Receive FEAC
Rx	or RX—Receiver
SEF	Severely Errored Framing Event
SSM	Synchronization Status Message
TBD	To Be Determined

Acronym	Definition
TDL	Terminal Data Link
TM	Timing Marker
Tx	or TX—Transmitter
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator
XBD	X-Bit Disagreement

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