

# M62398P,FP

8BIT 12CH I<sup>2</sup>C BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

## GENERAL DESCRIPTION

The M62398P,FP is a 12V type CMOS 12-channel D-A converters with output buffer amplifiers.

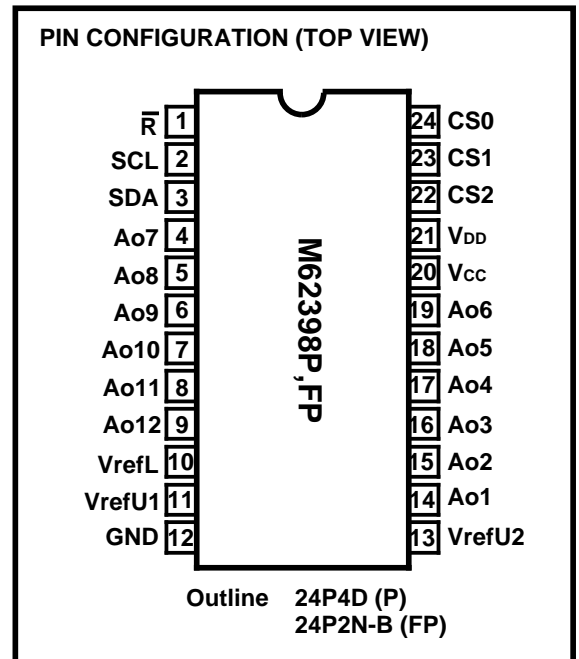
It can communicate with a microcontroller via few wiring thanks to the adoption of the two-line I<sup>2</sup>C BUS.

The output buffer amplifier employs AB class output with sinking and sourcing capability of more than 2.5mA, and an output voltage range is nearly between ground and VrefU.

Maximum 8 ICs can be connected to a bus by using three chip-set pins, so that it is possible to handle up to 96 channels.

## FEATURES

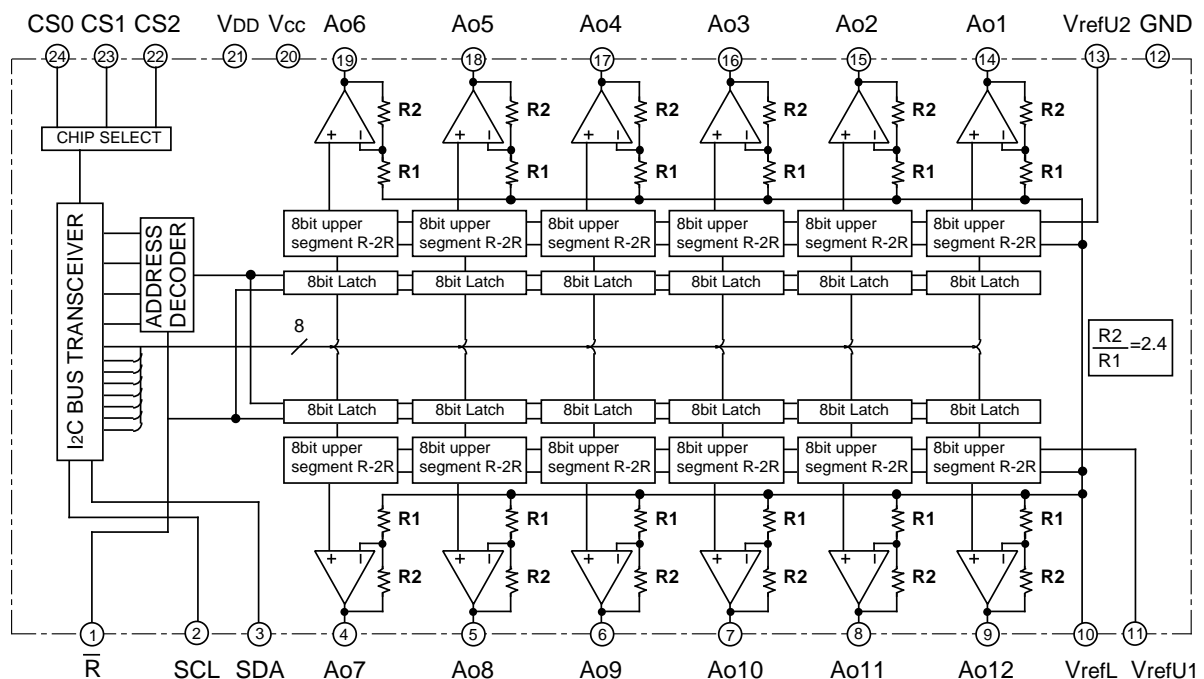
- I<sup>2</sup>C BUS serial data method
- Wide output range  
Nearly between ground and VrefU(0~12V).
- High output current drive capability  
Over ±2.5mA
- 2 setting voltage ranges by dual input pins for upper voltage references (VrefU1,U2)



## APPLICATION

Conversion from digital control data to analog control data for both consumer and industrial equipment. Gain control and automatic adjustment of DISPLAY-MONITOR or CTV.

## BLOCK DIAGRAM



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## EXPLANATION OF TERMINALS

PIN No.	Symbol	Function
③	SDA	Serial data input terminal
①	$\bar{R}$	Reset signal input terminal
②	SCL	Serial clock input terminal
⑭	Ao1	} 8bit D-A converter output terminal
⑮	Ao2	
⑯	Ao3	
⑰	Ao4	
⑱	Ao5	
⑲	Ao6	
④	Ao7	
⑤	Ao8	
⑥	Ao9	
⑦	Ao10	
⑧	Ao11	
⑨	Ao12	
⑳	Vcc	Analog power supply terminal
㉑	VDD	Digital power supply terminal
⑫	GND	Analog and digital common GND
⑩	VrefL	D-A converter low level reference voltage input terminal
⑪	VrefU1	D-A converter high level reference voltage input terminal 1
⑬	VrefU2	D-A converter high level reference voltage input terminal 2
㉒	CS2	Chip select data input terminal 2
㉓	CS1	Chip select data input terminal 1
㉔	CS0	Chip select data input terminal 0

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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.3~13.5	V
V <sub>DD</sub>	Supply voltage		-0.3~7.0	V
V <sub>refU1,2</sub>	D-A converter upper reference voltage		V <sub>DD</sub>	V
V <sub>IND</sub>	Digital input voltage		-0.3~V <sub>DD</sub> +0.3	V
P <sub>d</sub>	Power dissipation		465(DIP) /421(FP)	mW
T <sub>opr</sub>	Operating temperature		-20~85	°C
T <sub>stg</sub>	Storage temperature		-40~125	°C

## ELECTRIC CHARACTERISTICS

< Digital part > (V<sub>CC</sub>=13V, V<sub>DD</sub>=V<sub>ref U1,2</sub>=+5V±10%, GND=V<sub>refL</sub>=0V, T<sub>a</sub>=-20~85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings			Unit
			MIN	TYP	MAX	
V <sub>DD</sub>	Supply voltage		4.5	5.0	5.5	V
I <sub>DD</sub>	Supply current	CLK=1MHz operation I <sub>AO</sub> =0μA			1	mA
I <sub>ILK</sub>	Input leak current	V <sub>IN</sub> =0~V <sub>DD</sub>	-10		10	μA
V <sub>IL</sub>	Input low voltage				0.2V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage		0.8V <sub>DD</sub>			V

< Analog part > (V<sub>CC</sub>=13V, V<sub>DD</sub>=V<sub>refU1,2</sub>=+5V±10%, GND=V<sub>refL</sub>=0V, T<sub>a</sub>=-20~85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings			Unit
			MIN	TYP	MAX	
V <sub>CC</sub>	Supply voltage		2.4V <sub>DD</sub>		13	V
I <sub>CC</sub>	Supply current	CLK=1MHz Operation I <sub>AO</sub> =0μA		2.0	4.0	mA
I <sub>refU</sub>	D-A converter upper reference voltage input current	V <sub>refU</sub> =5V, V <sub>refL</sub> =0V Data condition: at maximum current		1.2	2.5	mA
V <sub>refU</sub>	D-A converter upper reference voltage range	The output dose not necessarily be the values within the reference voltage setting range.	3.5		V <sub>DD</sub>	V
V <sub>refL</sub>	D-A converter lower reference voltage range		GND		1.5	V
V <sub>AO</sub>	Buffer amplifier output voltage range	I <sub>AO</sub> =±500μA	0.1		V <sub>CC</sub> -0.1	V
		I <sub>AO</sub> =±1.0mA	0.2		V <sub>CC</sub> -0.2	V
I <sub>AO</sub>	Buffer amplifier output drive range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	-2.5		2.5	mA
SDL	Differential nonlinearity error	V <sub>refU</sub> =4.79V V <sub>refL</sub> =0.95V V <sub>CC</sub> =13V(36mV/LSB) without load (I <sub>AO</sub> =0)	-1.0		1.0	LSB
SL	Nonlinearity error		-1.5		1.5	LSB
SZERO	Zero code error		-2.0		2.0	LSB
SFULL	Full scale error		-2.0		2.0	LSB
SR	Output slew rate				0.2	V/μs

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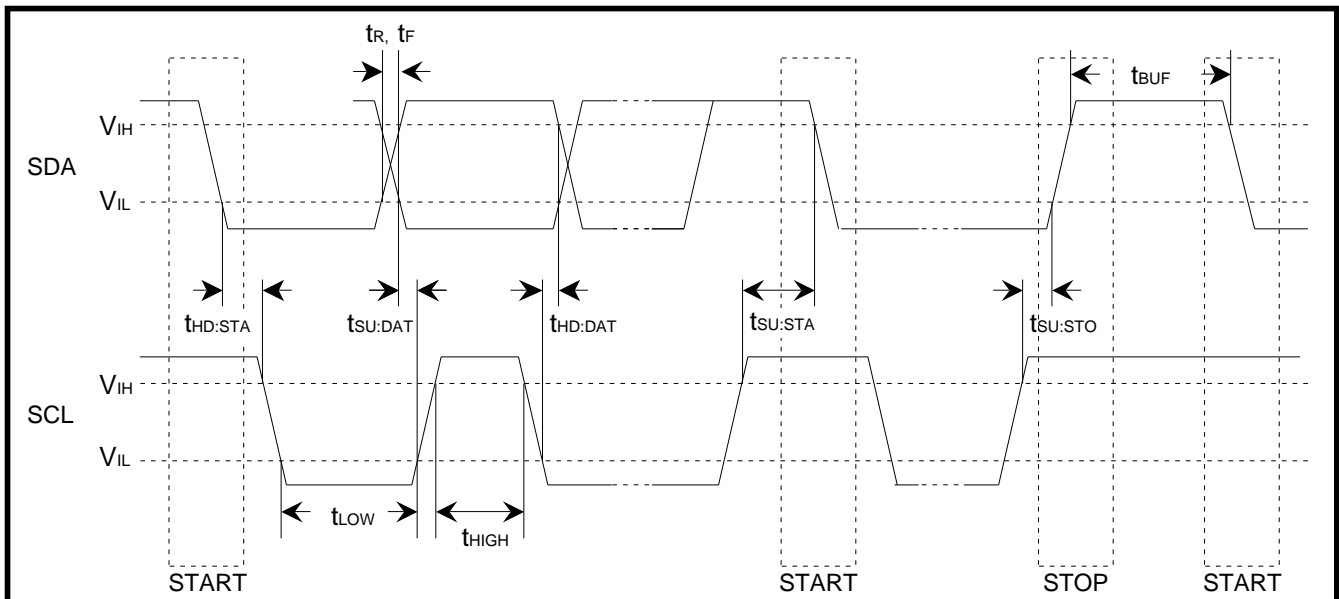
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## I2C BUS LINE CHARACTERISTICS

Symbol	Parameter	Normal mode		High speed mode		units
		Min.	Max.	Min.	Max.	
f <sub>SCL</sub>	SCL clock frequency	0	100	0	400	KHz
t <sub>BUF</sub>	Time the bus must be free before a new transmission can start	4.7	-	1.3	-	μs
t <sub>HD:STA</sub>	Hold time START Condition. After this period, the first clock pulse is generated.	4.0	-	0.6	-	μs
t <sub>LOW</sub>	LOW period of the clock	4.7	-	1.3	-	μs
t <sub>HIGH</sub>	High period of the clock	4.0	-	0.6	-	μs
t <sub>SU:STA</sub>	Set-up time for START condition (Only relevant for a repeated START condition)	4.7	-	4.7	-	μs
t <sub>HD:DAT</sub>	Hold time DATA	0	-	0	0.9	μs
t <sub>SU:DAT</sub>	Set-up time DATA	250	-	100	-	ns
t <sub>R</sub>	Rise time of both SDA and SCL lines	-	1000	20+	300	ns
t <sub>F</sub>	Fall time of both SDA and SCL lines	-	300	20+	300	ns
t <sub>SU:STO</sub>	Set-up time for STOP condition	4.0	-	0.6	-	μs

\*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max.300 ns) of the falling edge of SCL.

## TIMING CHART



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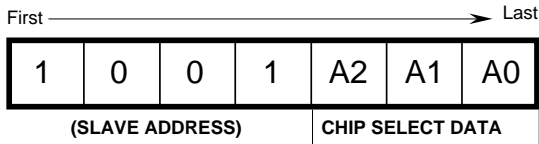
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## I<sup>2</sup>C- BUS FORMAT

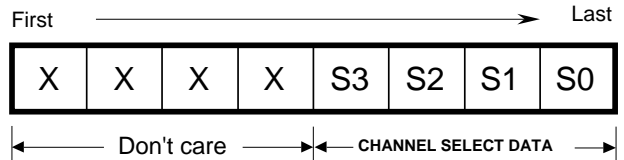


## DIGITAL DATA FORMAT

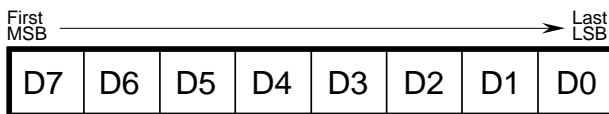
### •SLAVE ADDRESS



### •SUB ADDRESS



### •DAC DATA



### (1)CHIP SELECT DATA

MSB			LSB		
A2	A1	A0	CS2	CS1	CS0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1

Lower 3bits(A0,A1,A2) are a programmable address. This IC is accessed only when the lower 3 bits data of slave address coincide with the data of CS0 to CS2.(refer to the upper table)

### (2)CHANNEL SELECT DATA

MSB				LSB
S3	S2	S1	S0	Channel selection
0	0	0	0	Don't care.
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
⋮	⋮	⋮	⋮	⋮
1	0	1	1	ch11 selection
1	1	0	0	ch12 selection
1	1	0	1	Don't care.
⋮	⋮	⋮	⋮	⋮
1	1	1	1	Don't care.

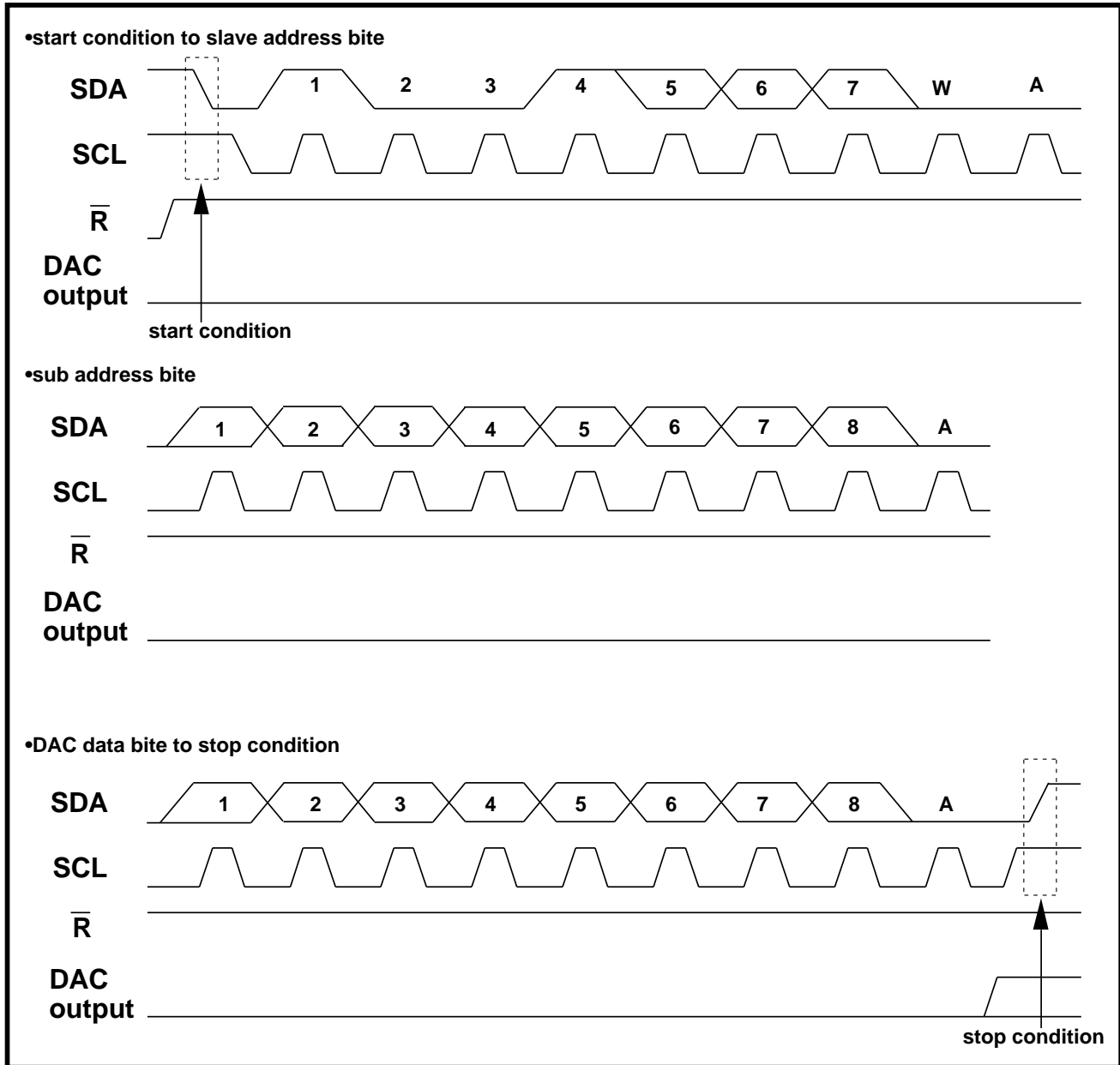
### (3)DAC DATA

First MSB								Last LSB
D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	$(V_{refU}-V_{refL})/256 \times 1 \times 2.4 + V_{refL}$
0	0	0	0	0	0	0	1	$(V_{refU}-V_{refL})/256 \times 2 \times 2.4 + V_{refL}$
0	0	0	0	0	0	1	0	$(V_{refU}-V_{refL})/256 \times 3 \times 2.4 + V_{refL}$
0	0	0	0	0	0	1	1	$(V_{refU}-V_{refL})/256 \times 4 \times 2.4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{refU}-V_{refL})/256 \times 255 \times 2.4 + V_{refL}$
1	1	1	1	1	1	1	1	$(V_{refU}-V_{refL}) \times 2.4 + V_{refL}$

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## TIMING CHART (MODEL)



- Start condition ..... With SCL at HIGH,SDA line goes from HIGH to LOW
- Stop condition ..... With SCL at HIGH,SDA line goes from LOW to HIGH  
(\*Under normal circumstances,SDA is changed when SCL is LOW)
- Acknowledge bit ..... The receiving IC has to pull down SDA line whenever receive slave data.  
(The transmitting IC releases the SDA line just then transmit 8bit data.)

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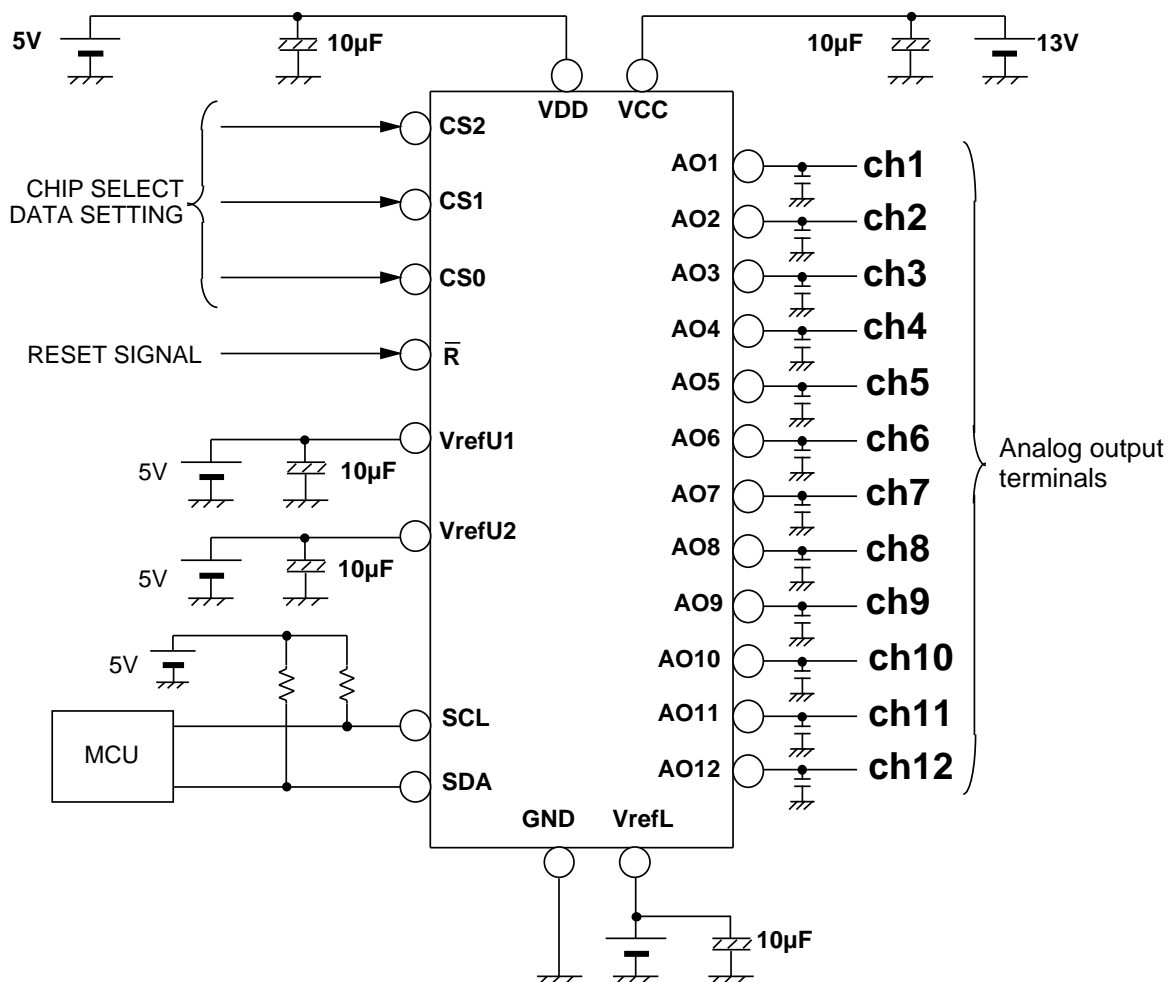
## PRECAUTION FOR USE

M62398 have 5 terminals (VDD,VCC,VrefU1,VrefU2,VrefL) for input constant voltage at use.

IF ripple or spike is input these terminals,accuracy of D-A conversion is down. So,when use this device,please connect capacitor among each terminal to GND for stable D-A conversion.

This IC's output amplifier has an advantage to capacitive load.So it's no problem at device action when connect capacitor (0.1μF MAX) among output to GND for every noise eliminate.

<Standard application circuit>



\*Purchase of MITSUBISHI ELECTRIC CORPORATION'S I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components an I<sup>2</sup>C system,provided that the system conforms to I<sup>2</sup>C Standard Specification as defined by Philips.

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