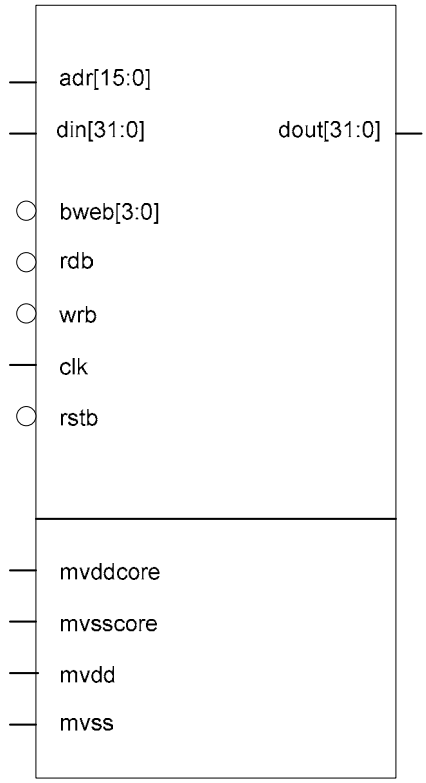
High Speed Pipelined 2-Mbit (64Kx32)
Standard 1T-SRAM® Embedded Memory Macro
M1T2HT18PZ32E

- **High Performance 1T-SRAM Standard Macro**
  - 200 MHz operation
  - 1-Clock cycle time
  - Pipelined read access timing
  - Late-late write mode timing
  - 32-Bit wide data buses
  - Byte Write Enables
  - Simple standard SRAM interface
  - Fast delivery
- **Ultra-Dense Memory**
  - 7.2mm^2 size per macro instance
  - Redundancy & fuses included in macro area
- **Silicon-Proven 1T-SRAM Technology**
  - Qualification programs completed
  - Products in volume production
- **High Yield and Reliability**
  - Built-in redundancy for enhanced yield
- **Standard Logic Process**
  - TSMC 0.18µm CL018G process
  - Logic design rules
  - Uses 4 metal layers
  - Routing over macro possible in layers 5+
- **Power**
  - Single voltage 1.8V Supply
  - Low power consumption



General Description

The M1T2HT18PL32E is a 2Mbit (2,169,152 bits), high speed, embedded 1T-SRAM macro. The M1T2HT18PL32E is organized as 64K(65,536) words of 32 bits. The macro employs a pipelined read timing interface with late-late write timing. Write control over individual bytes in the input data is achieved through the use of the byte write enable (bweb) input signals. The M1T2HT18PL32E macro is implemented using MoSys 1T -SRAM technology, resulting in extremely high density and performance.

Memory Interface Signal List

Signal Name	Valid	Logic	Direction	Description
adr[15:0]	Positive clk edge	Positive	Input	Memory address
bweb[3:0]	Positive clk edge	Negative	Input	Memory byte write enables bweb[n] = 0 enables data write bweb[n] = 1 disables data write bweb[3] controls writing of din[31:24] bweb[2] controls writing of din[23:16] bweb[1] controls writing of din[15:8] bweb[0] controls writing of din[7:0]
rdb	Positive clk edge	Negative	Input	Memory read
wrb	Positive clk edge	Negative	Input	Memory write
din[31:0]	Positive clk edge	Positive	Input	Memory data in bus
dout[31:0]	Positive clk edge	Positive	Output	Memory data out bus
rstb	Positive clk edge	Negative	Input	Memory initialization reset
clk	Clock	Positive	Input	Memory Clock
mvddcore				Memory core supply voltage
mvsscore				Memory core ground
mvdd				Memory interface supply voltage
mvss				Memory interface ground

Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply Voltage Range (1.8V ±10%)	Operating	1.62	1.98	V
T_J	Junction Temperature	Nominal V_{DD}	0	125	°C
tCYC	Cycle Time	Operating	5.0	33*	ns
tCKH	Clock High	Operating	0.45*tCYC	0.55*tCYC	ns
tCKL	Clock Low	Operating	0.45*tCYC	0.55*tCYC	ns

*Note: Minimum clock frequency limit adjustable to meet system timing requirements

Power Requirements

Symbol	Condition	Current per Instance	Units
I_{DD1}	Operating current, V_{DD}=1.8V, clock frequency = 100MHz, output not loaded, memory accessed every clock	0.85	mA/MHz
I_{DD2}	Standby current, V_{DD} =1.8V, clock frequency =100MHz, memory not accessed	0.35	mA/MHz

Input Loading

Symbol	Condition	Load Capacitance	Units
C_{DIN}	din signal input loading	0.1	pF
C_{ADR}	adr signal input loading	0.1	pF
C_{CTL}	rdb, wrb and bweb signal input loading	0.1	pF
C_{CLK}	clk signal input loading	1.0	pF

AC Timing Characteristics at Recommended Operating Conditions

All times in nanoseconds

Bolded numbers reflect worst case design parameters

Parameter	Description	Condition	Slow	Typical	Fast
tAS	Address Setup	Min.	**1.0**	0.8	0.6
tAH	Address Hold	Min.	**0.5**	0.4	0.3
tCS	Control Setup	Min.	**1.0**	0.8	0.6
tCH	Control Hold	Min.	**0.5**	0.4	0.3
tDS	Write Data Setup	Min.	**1.0**	0.8	0.6
tDH	Write Data Hold	Min.	**0.5**	0.4	0.3
tKQ	Clock to Data Valid	Max.	**3.3**	2.9	2.5
tKQE	Data valid extrinsic delay per pF	Max.	**0.8**	0.6	0.4
tKQX	Clock to Data not valid	Min.	0.8	0.6	**0.4**

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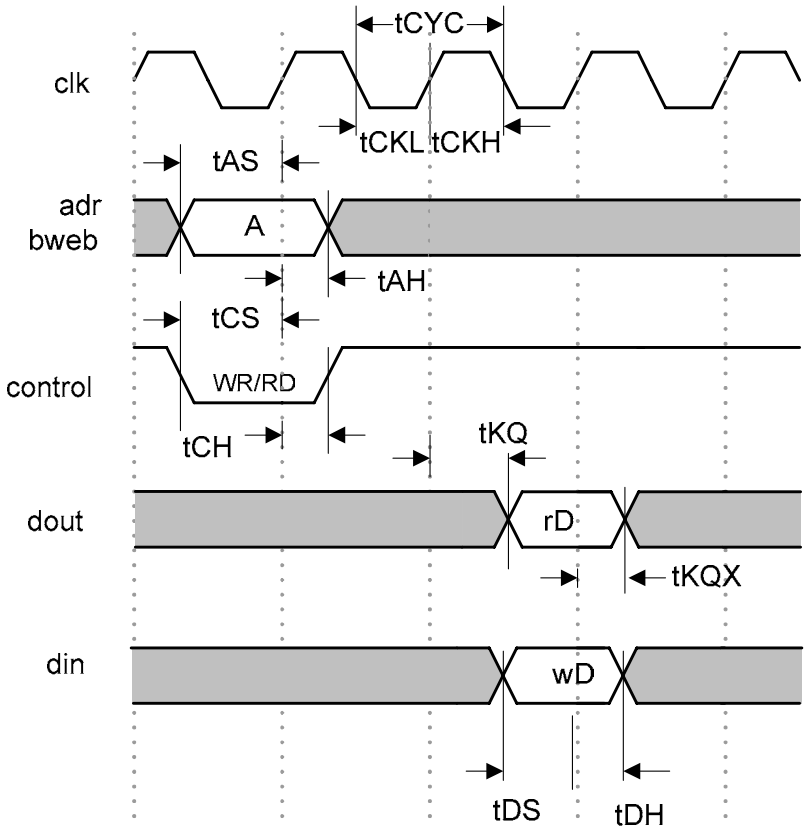
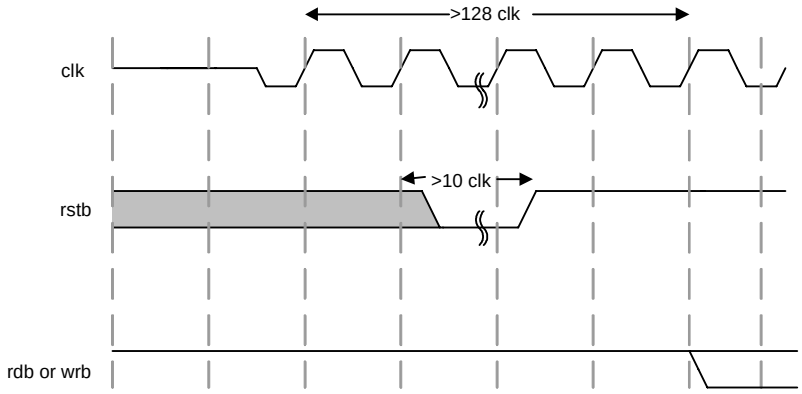


General AC Timing

Memory macro implements a synchronous reset to force state machines into a known state after power-up. This reset does not clear the memory contents. The clock must be running for at least two cycles before the Reset (rstb) signal will be correctly sampled as shown above. The Reset (rstb) signal must be active for at least ten (10) clock periods to initialize all internal circuitry. Independent of the Reset (rstb) signal, after power has stabilized to a voltage within the operating specification and the clock is operating within its timing specifications, there must be at least 128 clock cycles before any read or write access.



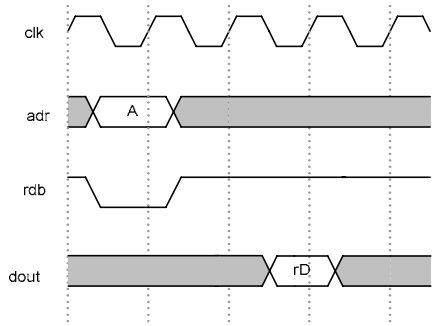
Initialization Timing

OPERATION TRUTH TABLE

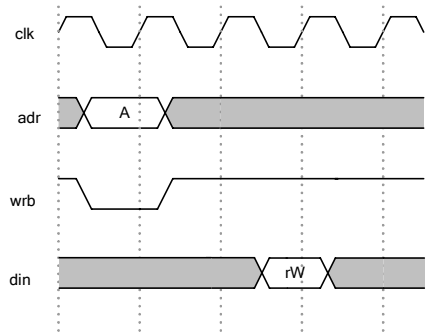
rdb	wrb	Operation
0	0	Illegal
0	1	Read
1	0	Write
1	1	Nop

FUNCTIONAL OPERATION

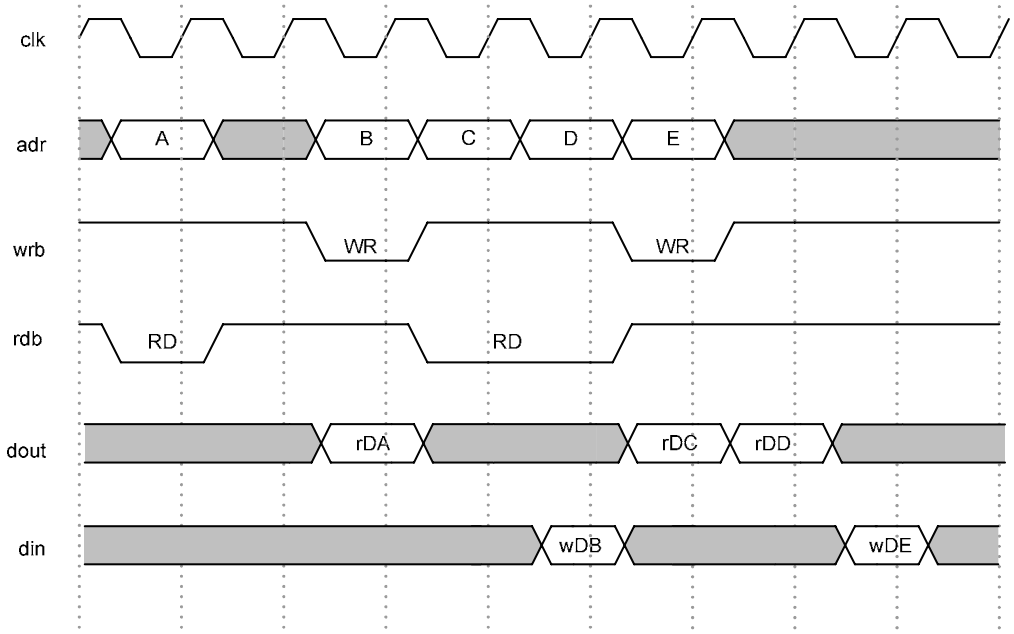
Address and command clocked in by rising clock edge. Read data transfer occurs in the clock cycle following the next clock rising edge. Write data transfer occurs in the following clock cycle. This standard macro uses user-managed refresh hiding. Consult factory for options.



Single Cycle Read Timing

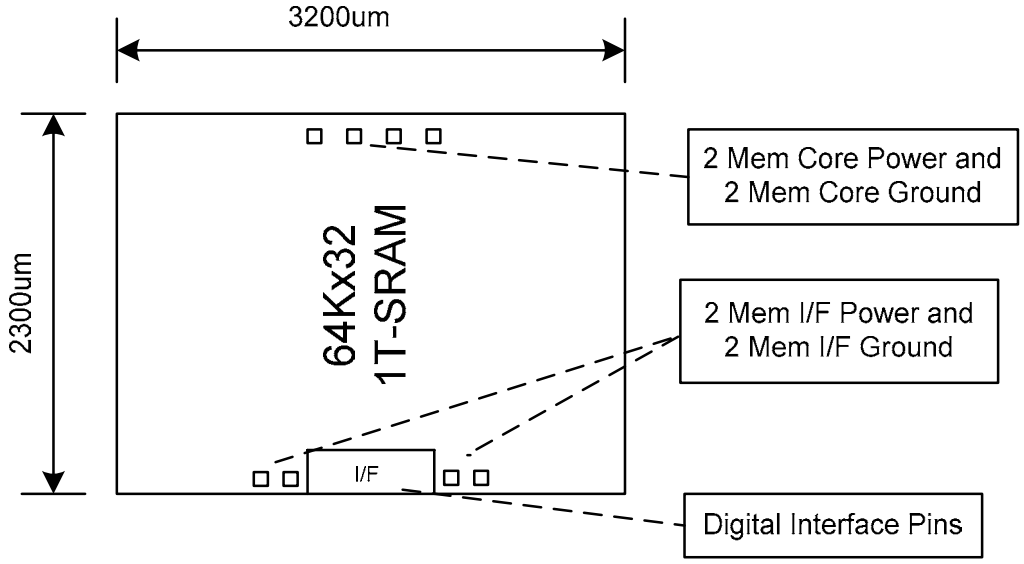


Single Cycle Write Timing



Multiple Cycle Timing

MEMORY BLOCK ESTIMATES*



*Note: Approximate dimensions. Exact dimensions appear on place and route phantom

Physical Layout