

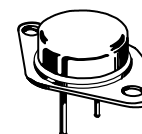
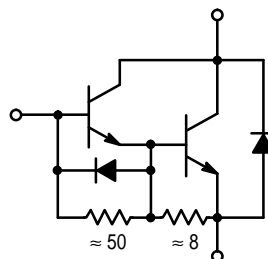
BUT34

Designer's™ Data Sheet
SWITCHMODE Series
NPN Silicon Power Darlington
Transistors with Base-Emitter
Speedup Diode

50 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTOR
850 VOLTS
250 WATTS

The BUT34 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated SWITCHMODE applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 0.7 μ s Inductive Fall Time at 25°C (Typ)
 - 1.8 μ s Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range -65 to 200°C



CASE 197A-05
TO-204AE
(TO-3)

MAXIMUM RATINGS

Rating	Symbol	BUT34	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector-Emitter Voltage	V_{CEV}	850	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous	I_C	50	Adc
— Peak (1)	I_{CM}	75	
Base Current — Continuous	I_B	10	Adc
— Peak (1)	I_{BM}	15	
Free Wheel Diode Forward Current — Continuous	I_F	50	Adc
— Peak	I_{FM}	75	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	250	Watts
@ $T_C = 100^\circ\text{C}$		140	
Derate above 25°C			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

BUT34**ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	—	—	0.2 4.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	350	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 16\text{ A}$, $V_{CE} = 5\text{ V}$) ($I_C = 32\text{ A}$, $V_{CE} = 5\text{ V}$)	h_{FE}	30 15	— —	— —	
Collector–Emitter Saturation Voltage ($I_C = 16\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 32\text{ A}$, $I_B = 3.2\text{ A}$) ($I_C = 40\text{ A}$, $I_B = 4\text{ A}$) ($I_C = 50\text{ A}$, $I_B = 10\text{ A}$)	$V_{CE(sat)}$	— — — —	— — — —	2.0 3.0 3.5 5.0	Vdc
Base–Emitter Saturation Voltage ($I_C = 16\text{ A}$, $I_B = 0.8\text{ A}$) ($I_C = 32\text{ A}$, $I_B = 3.2\text{ A}$) ($I_C = 40\text{ A}$, $I_B = 4\text{ A}$)	$V_{BE(sat)}$	— — —	— — —	2.5 2.9 3.3	Vdc
Diode Forward Voltage ($I_F = 40\text{ A}$)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	$T_C = 25^\circ\text{C}$	See Table 1	t_s	—	1.8	3.0	μs
Fall Time			t_f	—	0.7	1.5	μs
Storage Time	$T_C = 100^\circ\text{C}$	$I_{B1} = 3.2\text{ A}$	t_s	—	2.2	—	μs
Fall Time			t_f	—	0.8	—	μs

(1) Pulse Test: $PW = 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

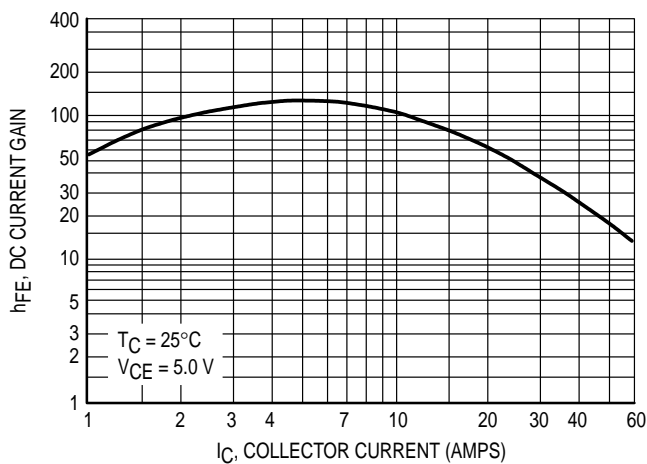


Figure 1. DC Current Gain

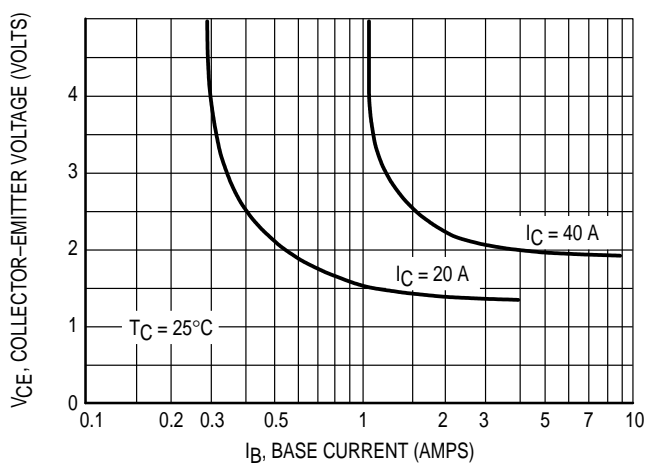


Figure 2. Collector Saturation Region

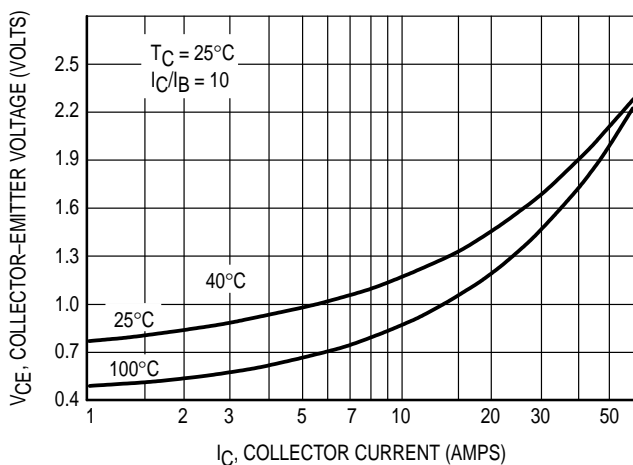


Figure 3. Collector-Emitter Saturation Voltage

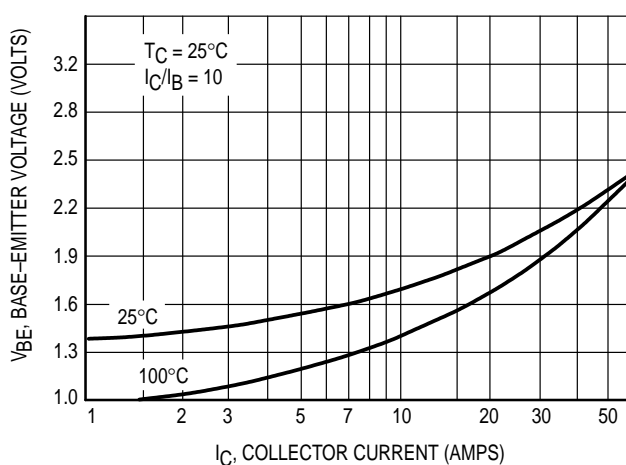


Figure 4. Base-Emitter Voltage

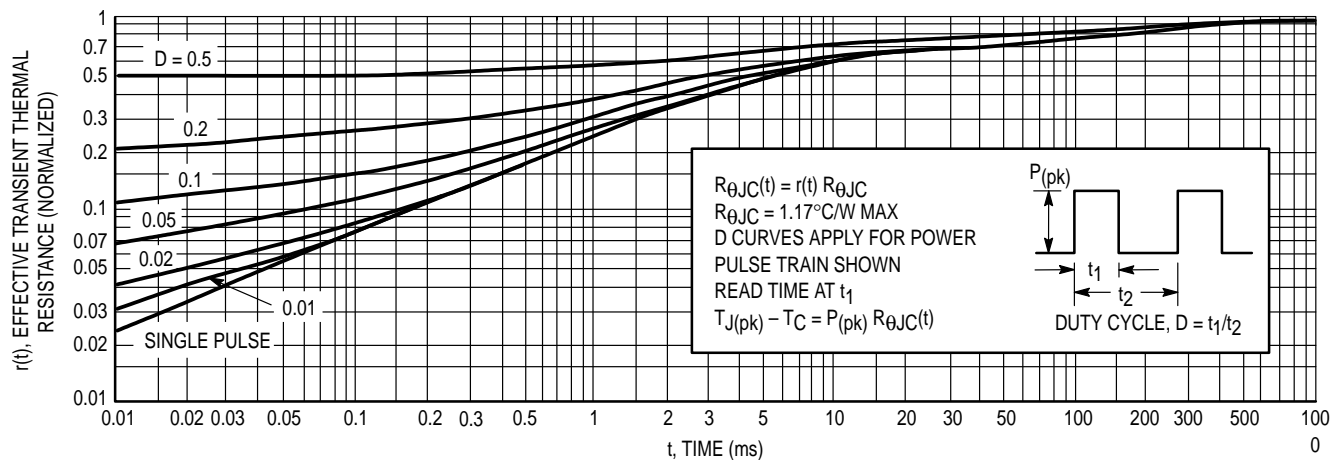
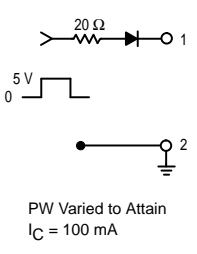
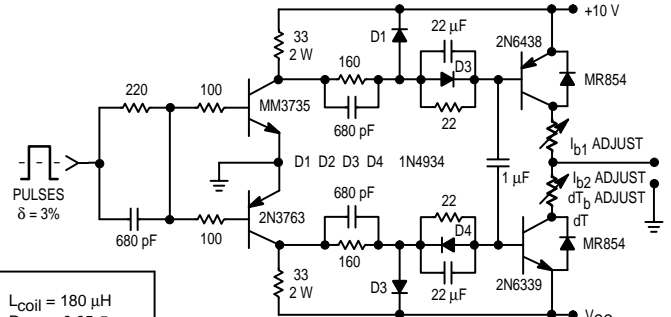
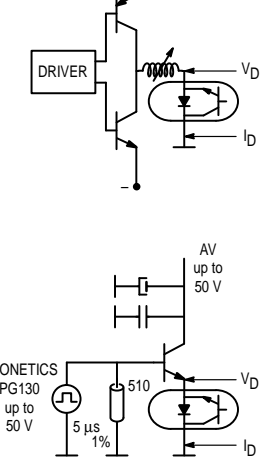
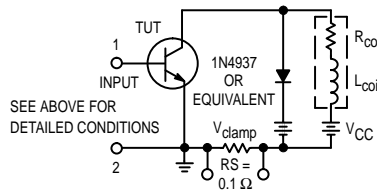
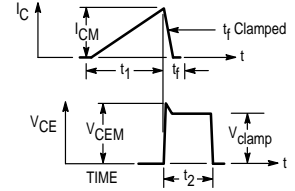


Figure 5. Thermal Response

Table 1. Test Conditions for Dynamic Performance

INPUT CONDITIONS	$V_{CE0}(sus)$	RBSOA AND INDUCTIVE SWITCHING		TEST CIRCUIT for FREE-WHEEL DIODE
 <p>PW Varied to Attain $I_C = 100\text{ mA}$</p>	<p>$L_{coil} = 10\text{ mH}$, $V_{CC} = 10\text{ V}$ $R_{coil} = 0.7\ \Omega$ $V_{clamp} = V_{CE0}(sus)$</p>	<p>$L_{coil} = 180\ \mu\text{H}$ $R_{coil} = 0.05\ \Omega$ $V_{CC} = 10\text{ V}$</p>	 <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{CM})}{V_{clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	 <p>AV up to 50 V CRONETICS PG130 up to 50 V 5 μs 1%</p>
<p>INDUCTIVE TEST CIRCUIT</p>  <p>SEE ABOVE FOR DETAILED CONDITIONS</p>		<p>OUTPUT WAVEFORMS</p> 		

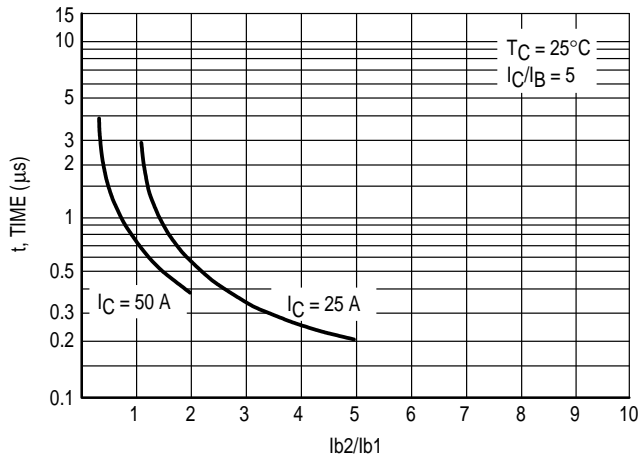


Figure 6. Fall Time versus I_{B2}/I_{B1}

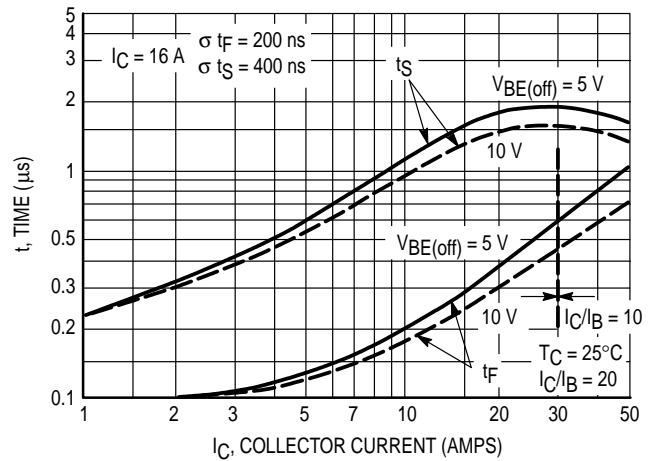


Figure 7. Turn-Off Time versus I_C

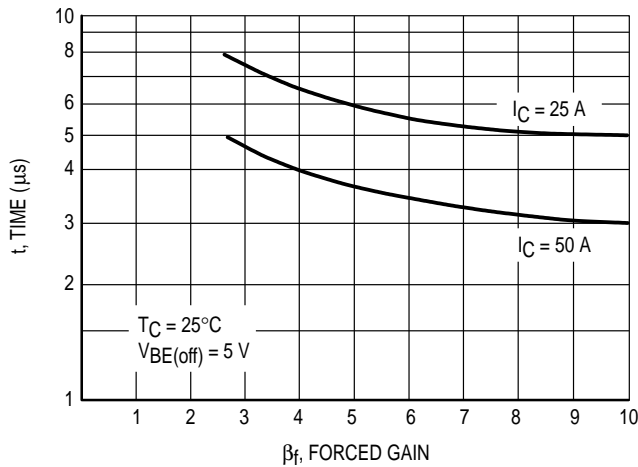


Figure 8. Storage Time versus Forced Gain

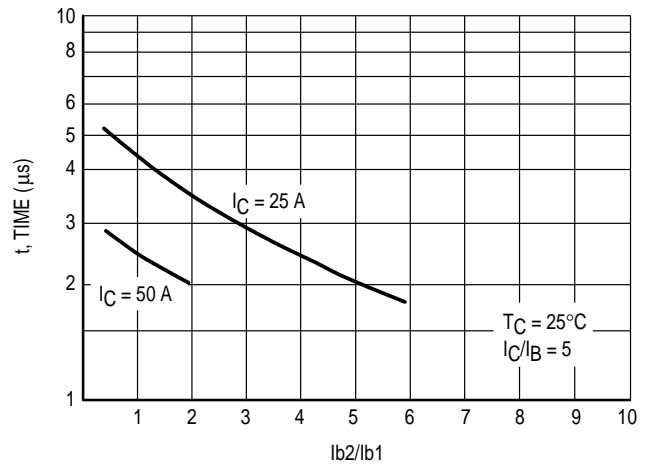


Figure 9. Storage Time versus I_{B2}/I_{B1}

FREE-WHEEL DIODE CHARACTERISTICS

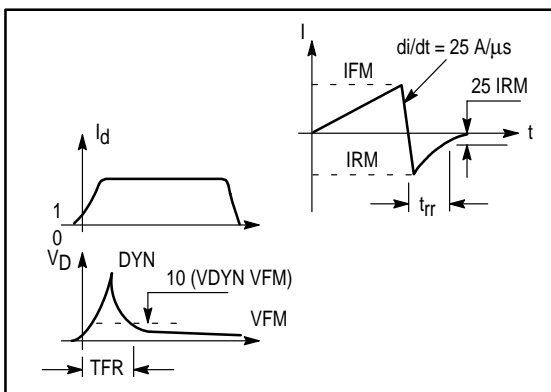


Figure 10. Free Wheel Diode Measurements

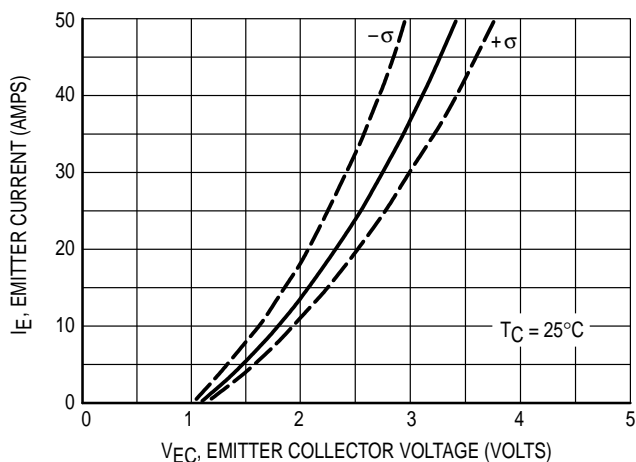


Figure 11. Forward Voltage

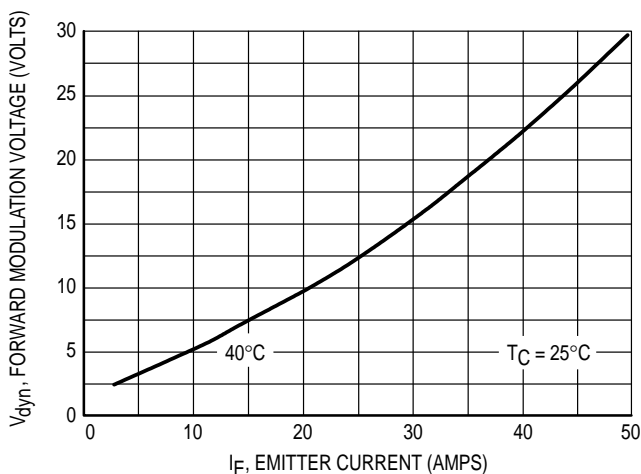


Figure 12. Forward Modulation Voltage

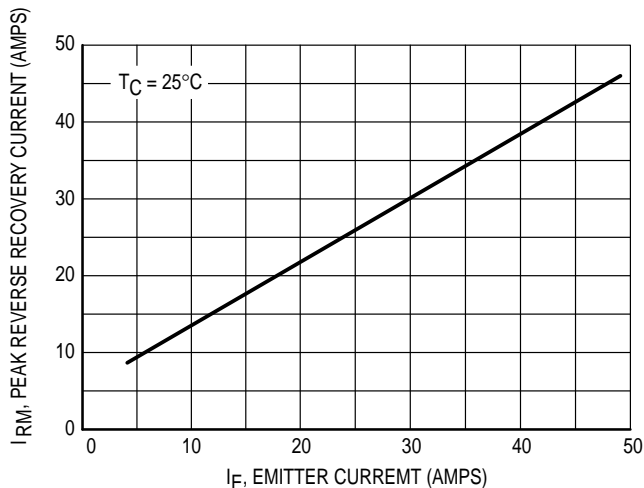


Figure 13. Peak Reverse Recovery Current

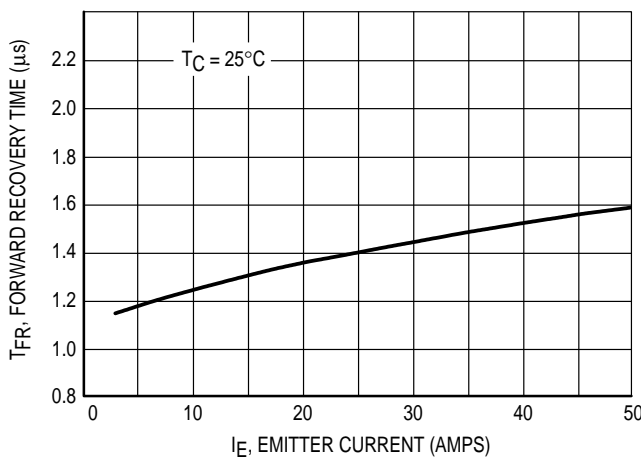


Figure 14. Forward Recovery Time

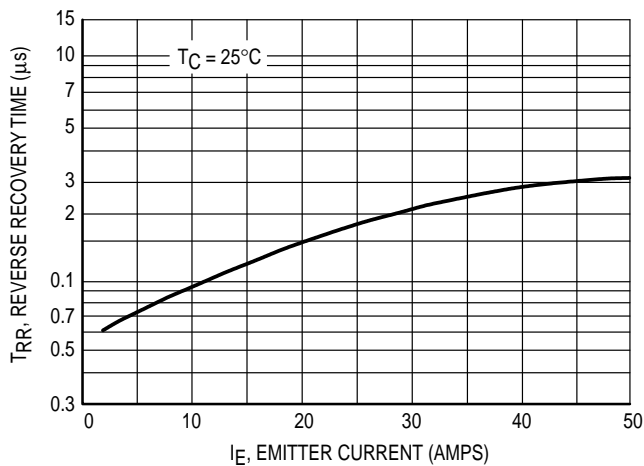


Figure 15. Reverse Recovery Time

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The Safe Operating Area figures shown in Figures 16 and 17 are specified for these devices under the test conditions shown.

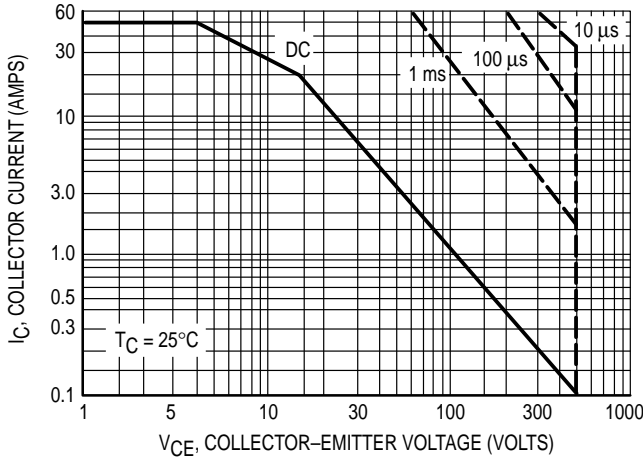


Figure 16. Safe Operating Area

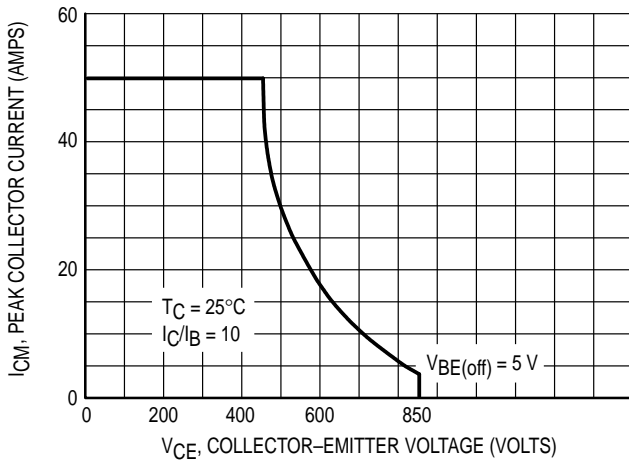


Figure 17. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

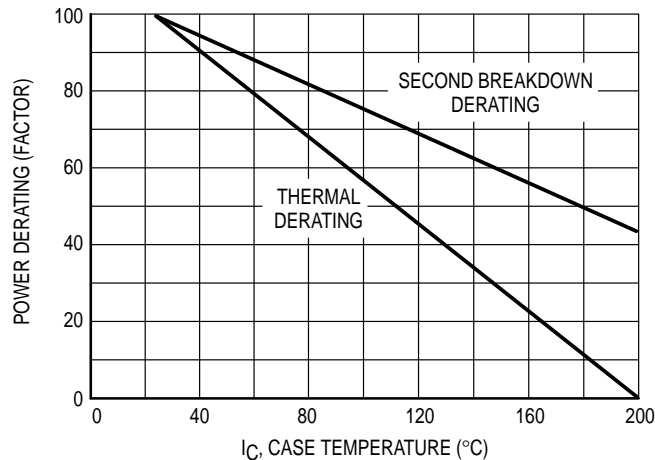
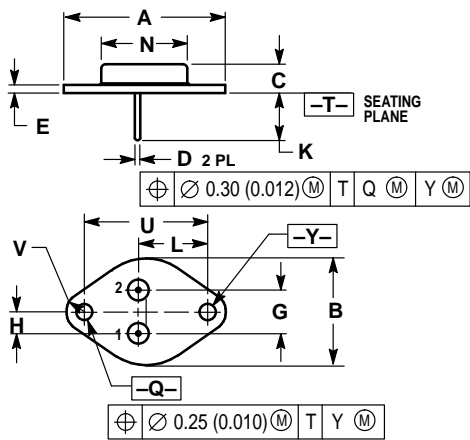


Figure 18. Power Derating

PACKAGE DIMENSIONS




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
 PIN 1. BASE
 2. EMITTER
 CASE: COLLECTOR

**CASE 197A-05
 TO-204AE (TO-3)
 ISSUE J**

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