

Designer's™ Data Sheet

**TMOS V™**

**Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Silicon Gate**

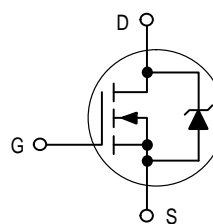
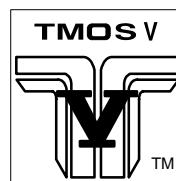
TMOS V is a new technology designed to achieve an on-resistance area product about one-half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E-FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

**New Features of TMOS V**

- On-resistance Area Product about One-half that of Standard MOSFETs with New Low Voltage, Low RDS(on) Technology
- Faster Switching than E-FET Predecessors

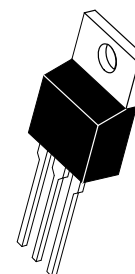
**Features Common to TMOS V and TMOS E-FETS**

- Avalanche Energy Specified
- IDSS and VDS(on) Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET



**MTP20N06V**

**TMOS POWER FET**  
**20 AMPERES**  
**60 VOLTS**  
**RDS(on) = 0.080 OHM**



**CASE 221A-06, Style 5**  
**TO-220AB**

**MAXIMUM RATINGS** (TC = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 1.0 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage — Continuous	V <sub>GS</sub>	± 20	Vdc
— Non-Repetitive (t <sub>p</sub> ≤ 10 ms)	V <sub>GSM</sub>	± 25	Vpk
Drain Current — Continuous	I <sub>D</sub>	20	Adc
— Continuous @ 100°C	I <sub>D</sub>	13	
— Single Pulse (t <sub>p</sub> ≤ 10 μs)	I <sub>DM</sub>	70	Apk
Total Power Dissipation	P <sub>D</sub>	60	Watts
Derate above 25°C		0.40	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C
Single Pulse Drain-to-Source Avalanche Energy — Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 25 Vdc, V <sub>GS</sub> = 10 Vdc, Peak I <sub>L</sub> = 20 Apk, L = 1.0 mH, R <sub>G</sub> = 25 Ω)	E <sub>AS</sub>	200	mJ
Thermal Resistance — Junction to Case	R <sub>θJC</sub>	2.5	°C/W
— Junction to Ambient	R <sub>θJA</sub>	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design. E-FET, Designer's, and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

# MTP20N06V

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 0.25 mAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60	—	—	Vdc
		—	69	—	mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	—	—	10	μAdc
		—	—	100	
Gate-Body Leakage Current (V <sub>GS</sub> = ± 20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	—	—	100	nAdc

## ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0	2.8	4.0	Vdc
		—	5.0	—	mV/°C
Static Drain-to-Source On-Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 10 Adc)	R <sub>DS(on)</sub>	—	0.065	0.080	Ohm
Drain-to-Source On-Voltage (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 20 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 10 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	—	—	2.0	Vdc
		—	—	1.9	
Forward Transconductance (V <sub>DS</sub> = 6.0 Vdc, I <sub>D</sub> = 10 Adc)	g <sub>FS</sub>	6.0	8.0	—	mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	590	830	pF
Output Capacitance		C <sub>oss</sub>	—	180	250	
Reverse Transfer Capacitance		C <sub>rss</sub>	—	40	80	

## SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 20 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	8.7	20	ns
Rise Time		t <sub>r</sub>	—	77	150	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	26	50	
Fall Time		t <sub>f</sub>	—	46	90	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 20 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	—	28	40	nC
		Q <sub>1</sub>	—	4.0	—	
		Q <sub>2</sub>	—	9.0	—	
		Q <sub>3</sub>	—	8.0	—	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (1)	(I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	—	1.05	1.6	Vdc
			—	0.96	—	
Reverse Recovery Time	(I <sub>S</sub> = 20 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	60	—	ns
		t <sub>a</sub>	—	52	—	
		t <sub>b</sub>	—	8.0	—	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	—	0.172	—	μC

## INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>D</sub>	—	3.5	—	nH
		—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	—	7.5	—	nH

- (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.  
 (2) Switching characteristics are independent of operating junction temperature.  
 (3) Reflects typical values.  $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

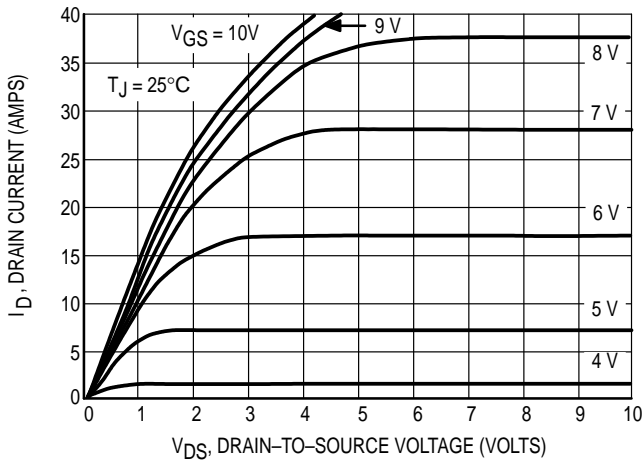


Figure 1. On-Region Characteristics

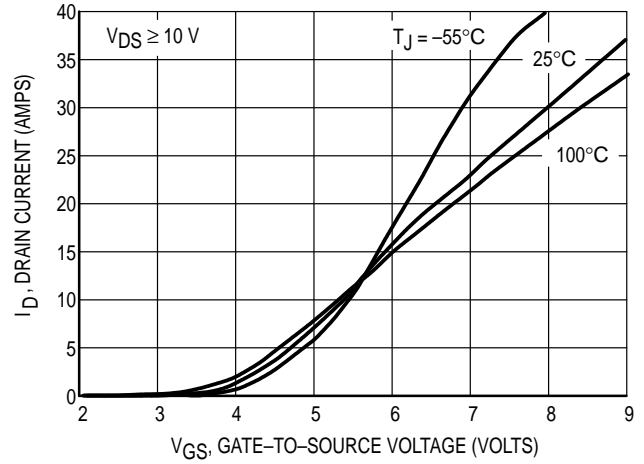


Figure 2. Transfer Characteristics

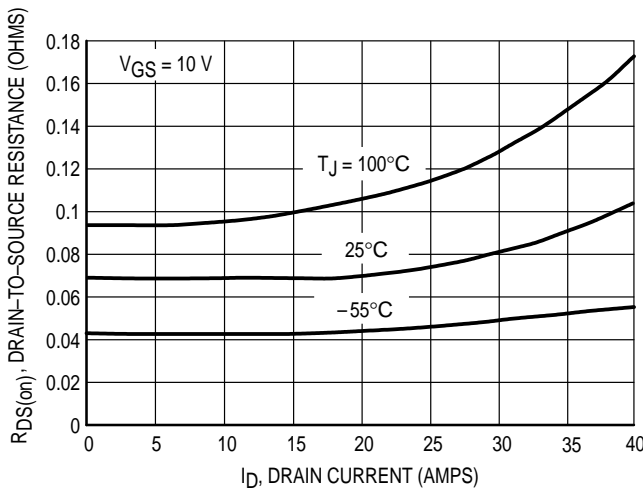


Figure 3. On-Resistance versus Drain Current and Temperature

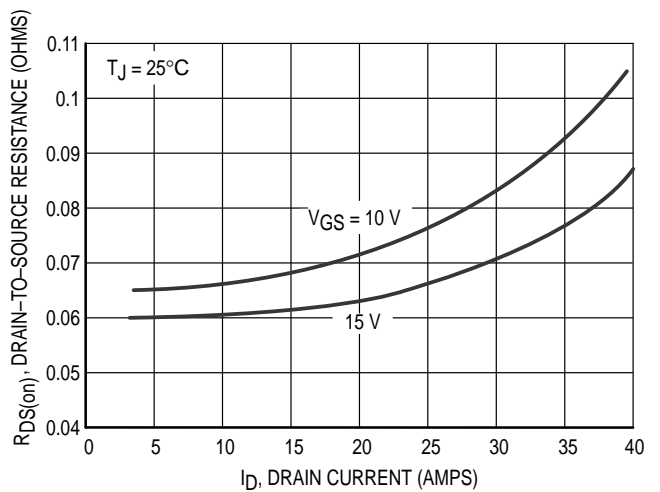


Figure 4. On-Resistance versus Drain Current and Gate Voltage

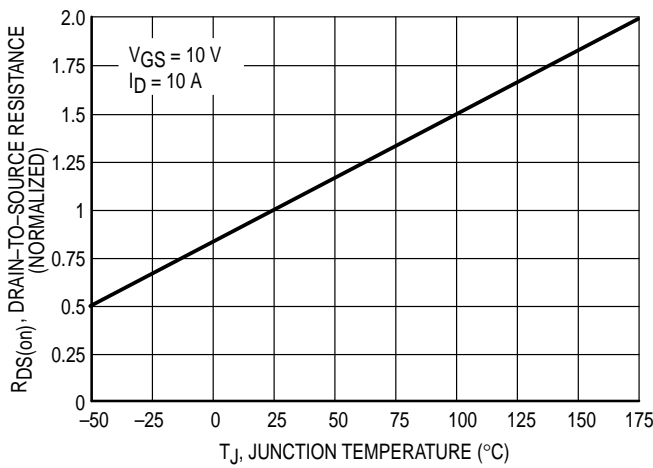


Figure 5. On-Resistance Variation with Temperature

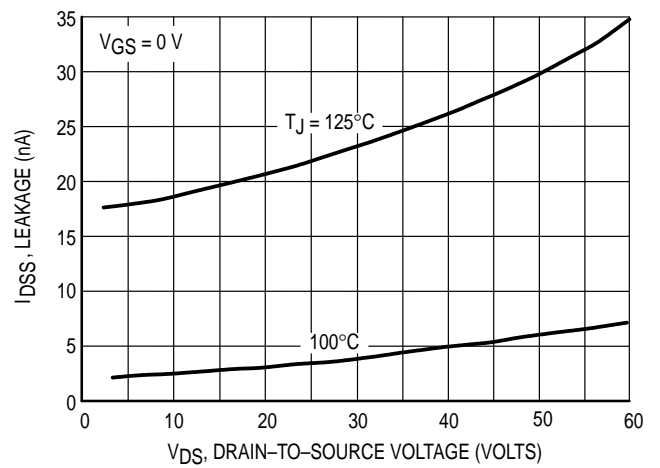


Figure 6. Drain-to-Source Leakage Current versus Voltage

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{SGP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{SGP})$$

$$t_f = Q_2 \times R_G / V_{SGP}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{SGP}$  are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG} / (V_{GG} - V_{SGP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG} / V_{SGP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on–state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $L di/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

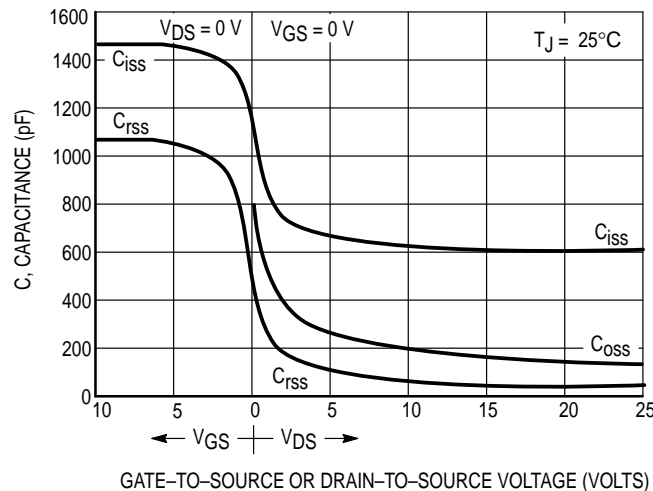


Figure 7. Capacitance Variation

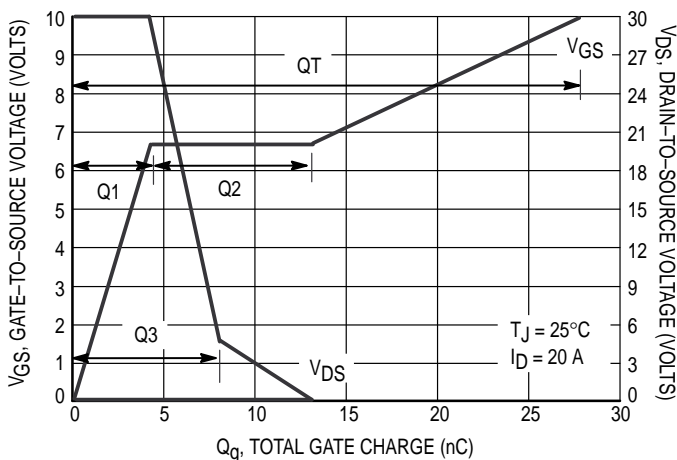


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

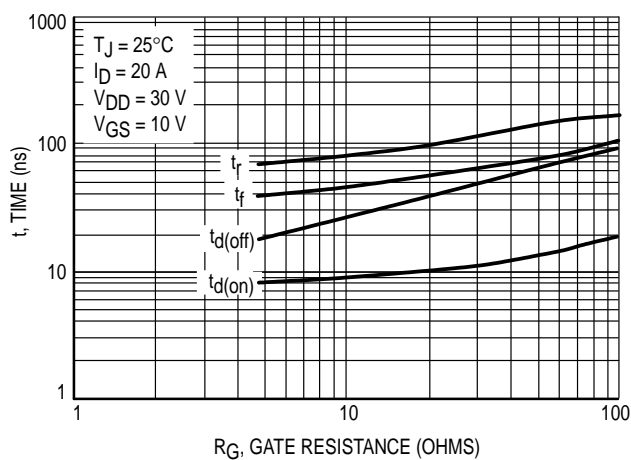


Figure 9. Resistive Switching Time Variation versus Gate Resistance

**DRAIN-TO-SOURCE DIODE CHARACTERISTICS**

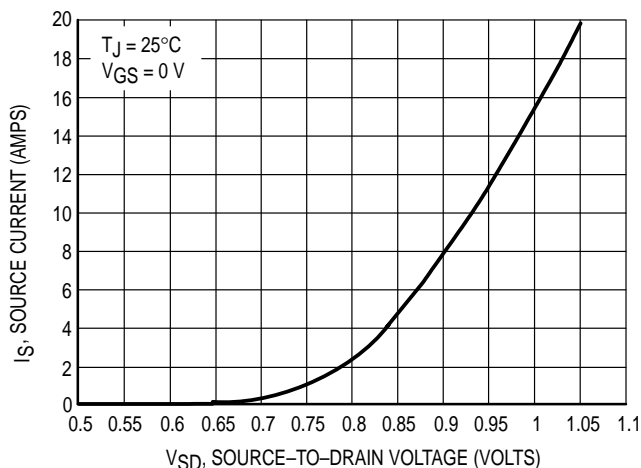


Figure 10. Diode Forward Voltage versus Current

**SAFE OPERATING AREA**

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance—General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded and the transition time ( $t_r, t_f$ ) do not exceed 10  $\mu s$ . In addition the total power averaged over a complete switching cycle must not exceed  $(T_J(MAX) - T_C)/(R_{\theta JC})$ .

A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For reli-

able operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

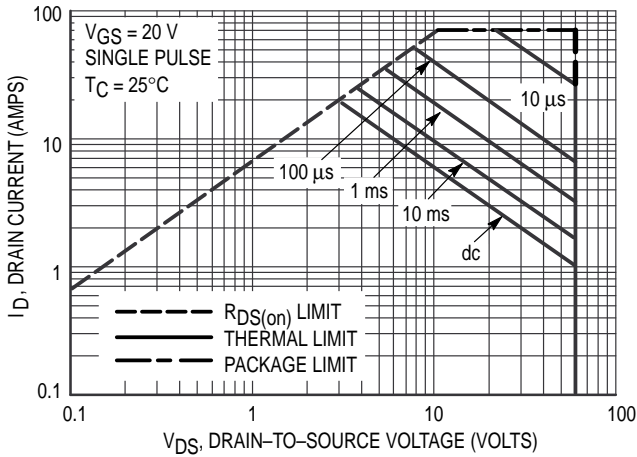


Figure 11. Maximum Rated Forward Biased Safe Operating Area

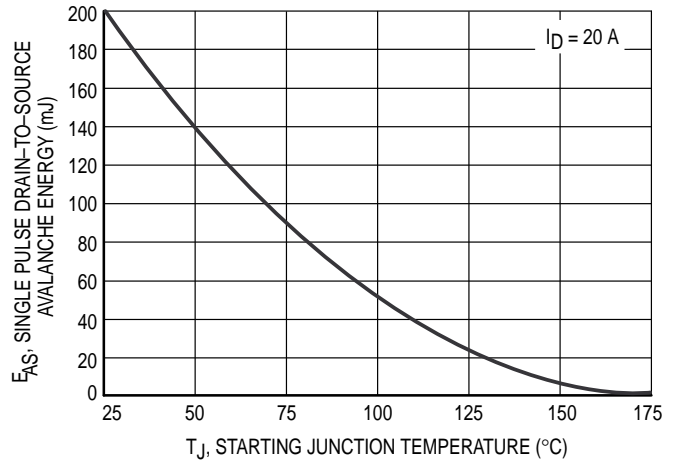


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

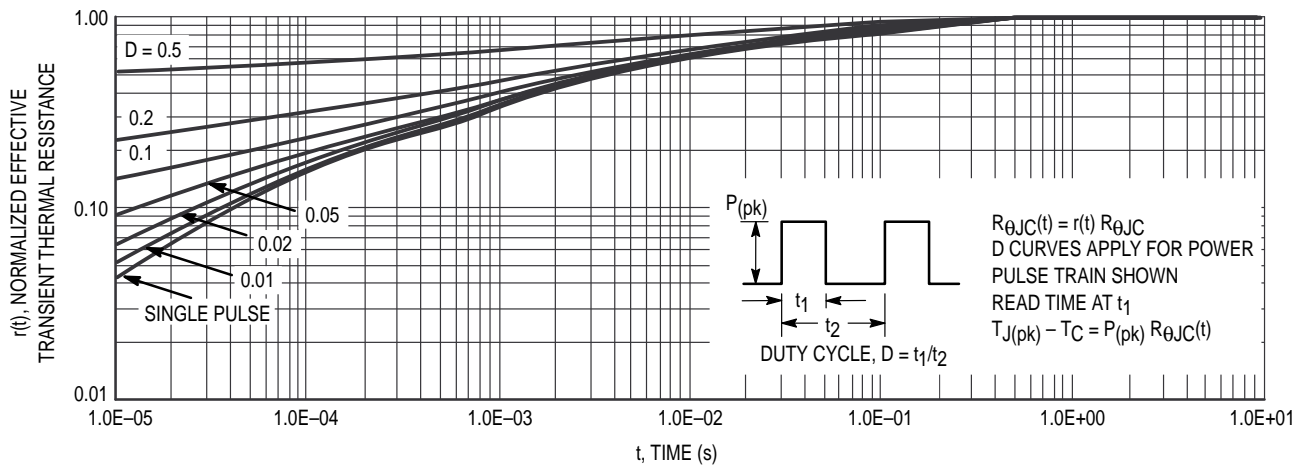


Figure 13. Thermal Response

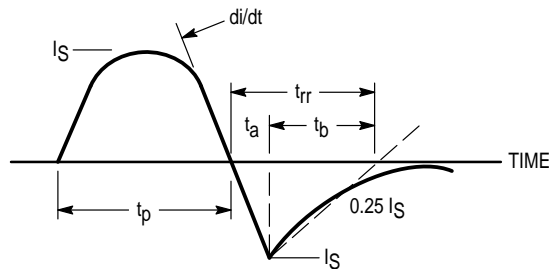
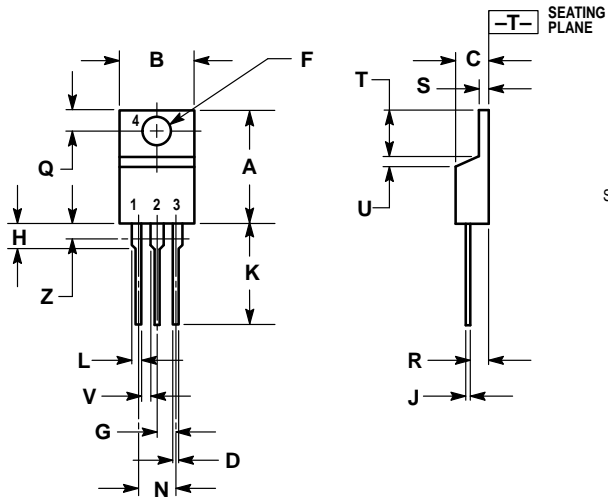


Figure 14. Diode Reverse Recovery Waveform

PACKAGE DIMENSIONS




STYLE 5:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-06  
 ISSUE Y

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