

54ACT563 Octal Latch with TRI-STATE® Outputs

General Description

The 'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

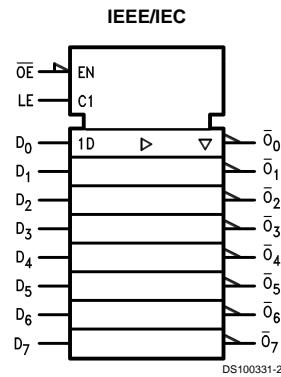
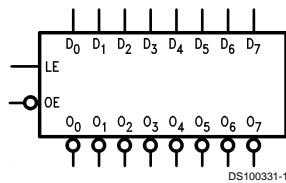
The 'ACT563 device is functionally identical to the 'ACT573, but with inverted outputs.

Features

- I_{CC} and I_{OZ} reduced by 50%

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT573 but with inverted outputs
- Outputs source/sink 24 mA
- 'ACT563 has TTL-compatible inputs
- Standard Military Drawing (SMD)
— 'ACT563: 5962-89556

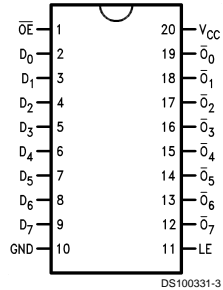
Logic Symbols



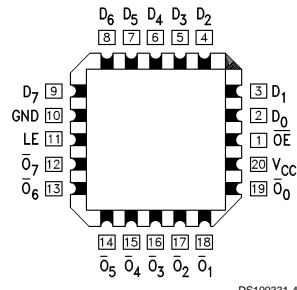
Pin Names	Description
D_0 – D_7	Data Inputs
LE	Latch Enable Input
\overline{OE}	TRI-STATE Output Enable Input
\overline{O}_0 – \overline{O}_7	TRI-STATE Latch Outputs

Connection Diagrams

Pin Assignment
for DIP and Flatpak



Pin Assignment
for LCC



Functional Description

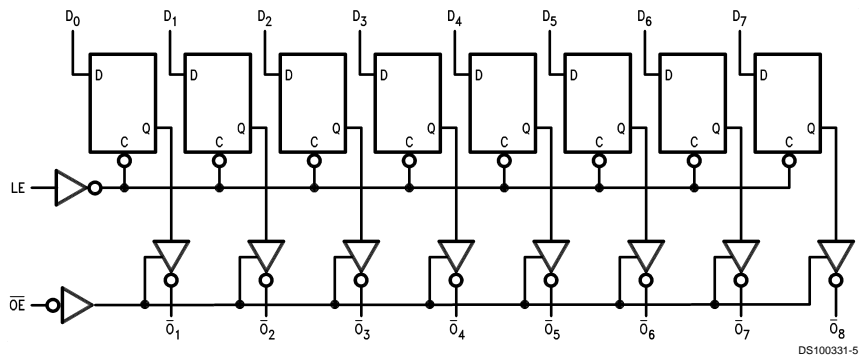
The 'ACT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs		Internal	Outputs	Function
\overline{OE}	LE	Q	O	
H	X	X	Z	High-Z
H	H	L	Z	High-Z
H	H	H	Z	High-Z
H	L	X	Z	Latched
L	H	L	H	Transparent
L	H	H	L	Transparent
L	L	X	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C

Junction Temperature (T_J)

CDIP

175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT	Units	Conditions
			$T_A =$		
			-55°C to +125°C		
			Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 mA$ $I_{OH} = -24 mA$
		5.5	4.70		
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 mA$ $I_{OL} = 24 mA$
		5.5	0.50		
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, GND$
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$
I_{CCT}	Maximum I_{CC} /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	(Note 3) Minimum Dynamic	5.5	50	mA	$V_{OLD} = 1.65V$ Max
	Output Current	5.5	-50	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 5)	54ACT		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
t _{PLH}	Propagation Delay D _n to \bar{O}_n	5.0	1.0	14.5	ns	
t _{PHL}	Propagation Delay D _n to \bar{O}_n	5.0	1.0	12.0	ns	
t _{PLH}	Propagation Delay LE to \bar{O}_n	5.0	1.0	12.5	ns	
t _{PHL}	Propagation Delay LE to \bar{O}_n	5.0	1.0	11.5	ns	
t _{PZH}	Output Enable Time	5.0	1.0	11.5	ns	
t _{PZL}	Output Enable Time	5.0	1.0	11.0	ns	
t _{PHZ}	Output Disable Time	5.0	1.0	12.0	ns	
t _{PLZ}	Output Disable Time	5.0	1.0	9.5	ns	

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

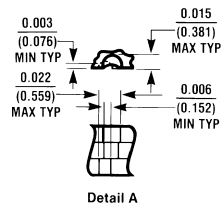
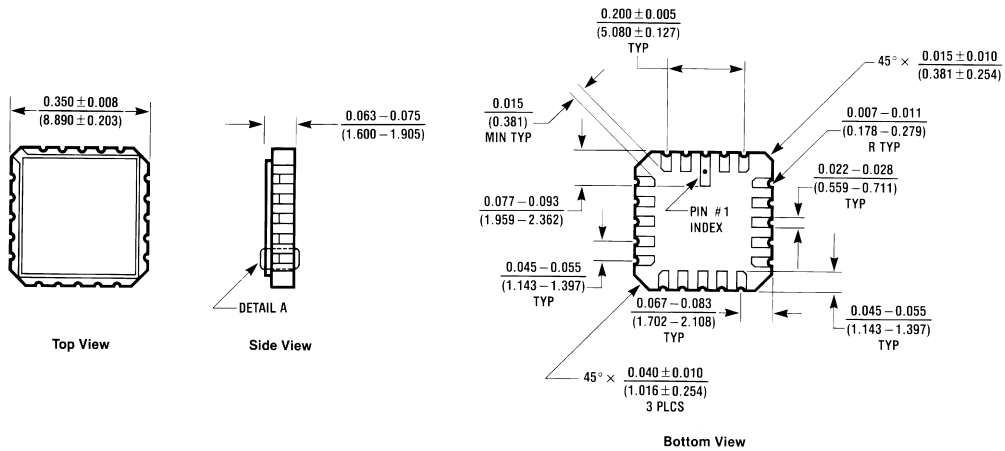
Symbol	Parameter	V _{CC} (V) (Note 6)	54ACT		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	4.5		ns	
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	1.5		ns	
t _w	LE Pulse Width, HIGH	5.0	5.0		ns	

Note 6: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

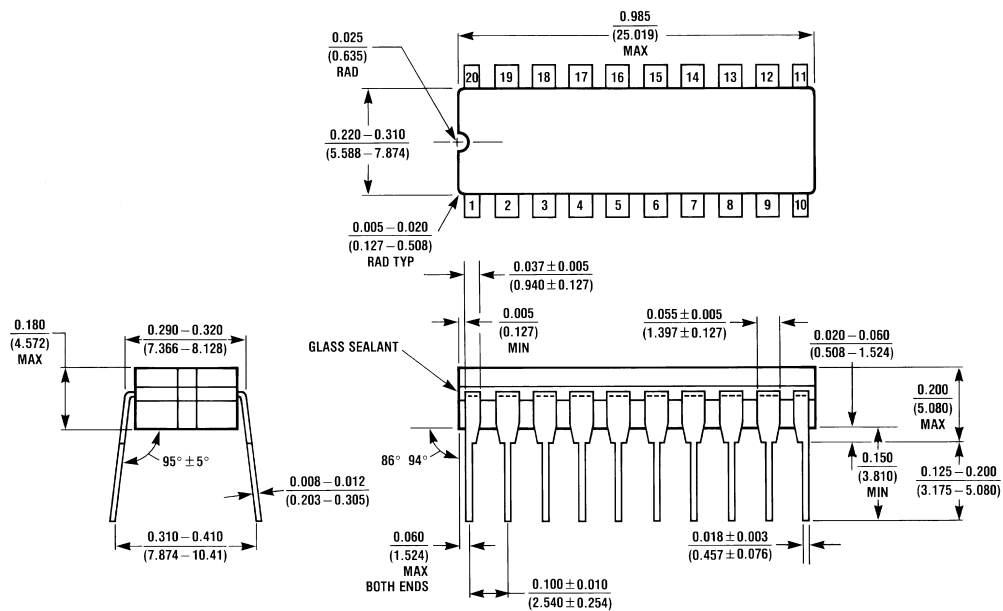
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	50.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



E20A (REV D)

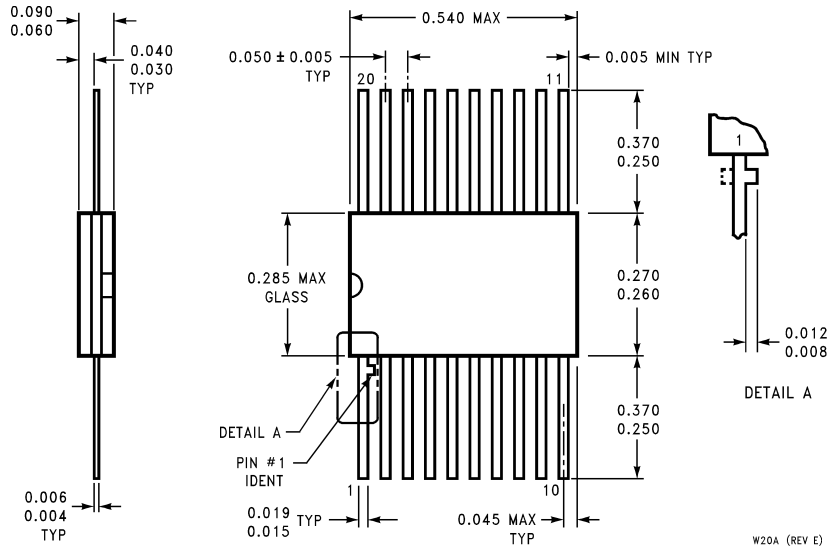
20 Terminal Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A



J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

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