

MAC4DCM, MAC4DCN

Preferred Device

Triacs

Silicon Bidirectional Thyristors

Designed for high volume, low cost, industrial and consumer applications such as motor control; process control; temperature, light and speed control.

Features

- Small Size Surface Mount DPAK Package
- Passivated Die for Reliability and Uniformity
- Blocking Voltage to 800 V
- On-State Current Rating of 4.0 A RMS at 108°C
- High Immunity to dv/dt – 500 V/ μ s at 125°C
- High Immunity to di/dt – 6.0 A/ms at 125°C
- Epoxy Meets UL 94, V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($T_J = -40$ to 125°C , Sine Wave, 50 to 60 Hz, Gate Open)	V_{DRM} , V_{RRM}	600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, $T_C = 108^\circ\text{C}$)	$I_{\text{T(RMS)}}$	4.0	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, $T_J = 125^\circ\text{C}$)	I_{TSM}	40	A
Circuit Fusing Consideration ($t = 8.3$ msec)	I^2t	6.6	A ² sec
Peak Gate Power (Pulse Width ≤ 10 μ sec, $T_C = 108^\circ\text{C}$)	P_{GM}	0.5	W
Average Gate Power ($t = 8.3$ msec, $T_C = 108^\circ\text{C}$)	$P_{\text{G(AV)}}$	0.1	W
Peak Gate Current (Pulse Width ≤ 10 μ sec, $T_C = 108^\circ\text{C}$)	I_{GM}	0.5	A
Peak Gate Voltage (Pulse Width ≤ 10 μ sec, $T_C = 108^\circ\text{C}$)	V_{GM}	5.0	V
Operating Junction Temperature Range	T_J	-40 to 125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to 150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

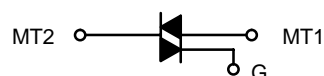
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the device are exceeded.



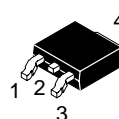
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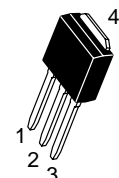
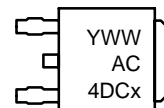
TRIACS
4.0 AMPERES RMS
600 – 800 VOLTS



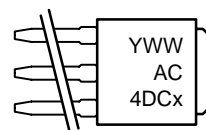
MARKING DIAGRAMS



DPAK
CASE 369C
STYLE 6



DPAK-3
CASE 369D
STYLE 6



Y = Year
WW = Work Week
x = M or N

PIN ASSIGNMENT

1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	3.5	$^{\circ}C/W$
– Junction-to-Ambient	$R_{\theta JA}$	88	
– Junction-to-Ambient (Note 2)	$R_{\theta JA}$	80	
Maximum Lead Temperature for Soldering Purposes (Note 3)	T_L	260	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted; Electricals apply in both directions)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{DRM}, V_{RRM}, \text{ Gate Open}$)	$I_{DRM},$ I_{RRM}	–	–	0.01	mA
		–	–	2.0	

ON CHARACTERISTICS

Peak On-State Voltage (Note 4) ($I_{TM} = \pm 6.0 \text{ A}$)	V_{TM}	–	1.3	1.6	V
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ V}, R_L = 100 \Omega$) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	I_{GT}	8.0 8.0 8.0	12 18 22	35 35 35	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ V}, R_L = 100 \Omega$) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	V_{GT}	0.5 0.5 0.5	0.8 0.8 0.8	1.3 1.3 1.3	V
Gate Non-Trigger Voltage (Continuous dc) ($V_D = 12 \text{ V}, R_L = 100 \Omega$) MT2(+), G(+); MT2(+), G(–); MT2(–), G(–) $T_J = 125^{\circ}C$	V_{GD}	0.2	0.4	–	V
Holding Current ($V_D = 12 \text{ V}, \text{ Gate Open}, \text{ Initiating Current} = \pm 200 \text{ mA}$)	I_H	6.0	22	35	mA
Latching Current ($V_D = 12 \text{ V}, I_G = 35 \text{ mA}$) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	I_L	– – –	30 50 20	60 80 60	mA

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Rate of Change of Commutating Current ($V_D = 400 \text{ V}, I_{TM} = 4.0 \text{ A}, \text{ Commutating } dv/dt = 18 \text{ V}/\mu\text{sec},$ Gate Open, $T_J = 125^{\circ}C, f = 250 \text{ Hz}, CL = 5.0 \mu\text{F}, LL = 20 \text{ mH}, \text{ No Snubber}$) (See Figure 16)	$di/dt(c)$	6.0	8.4	–	A/ms
Critical Rate of Rise of Off-State Voltage ($V_D = 0.67 \times \text{Rated } V_{DRM}, \text{ Exponential Waveform}, \text{ Gate Open}, T_J = 125^{\circ}C$)	dv/dt	500	1700	–	V/ μs

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

3. 1/8" from case for 10 seconds.

4. Pulse Test: Pulse Width $\leq 2.0 \text{ msec}$, Duty Cycle $\leq 2\%$.

ORDERING INFORMATION

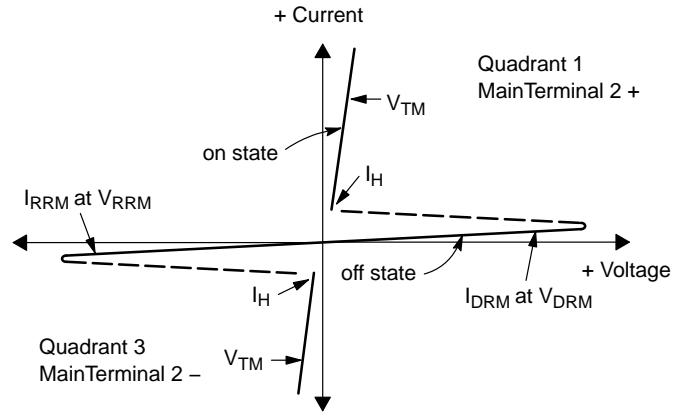
Device	Package Type	Package	Shipping†
MAC4DCM-001	DPAK-3	369D	75 Units / Rail
MAC4DCMT4	DPAK	369C	16 mm Tape & Reel (2.5 k / Reel)
MAC4DCN-001	DPAK-3	369D	75 Units / Rail
MAC4DCNT4	DPAK	369C	16 mm Tape & Reel (2.5 k / Reel)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

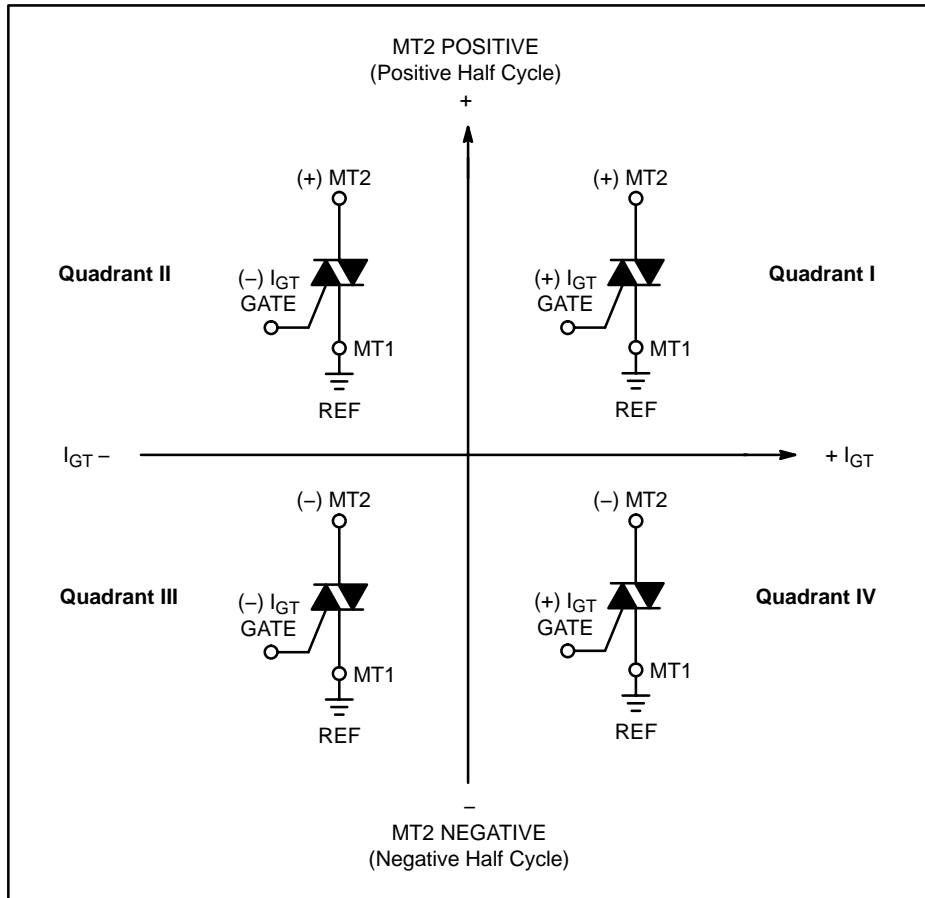
MAC4DCM, MAC4DCN

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off-State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off-State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On-State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.

With in-phase signals (using standard AC lines) quadrants I and III are used.

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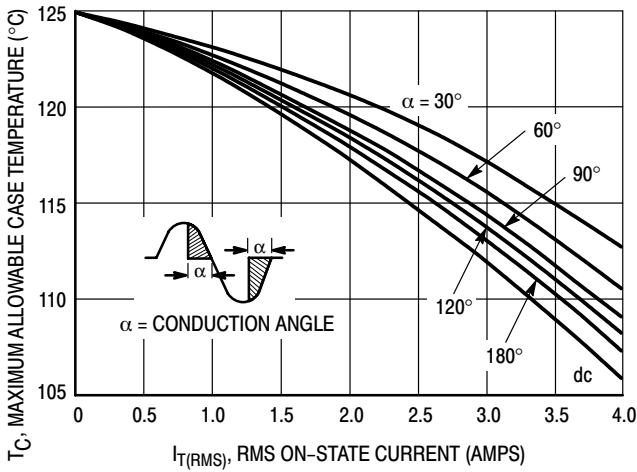


Figure 1. RMS Current Derating

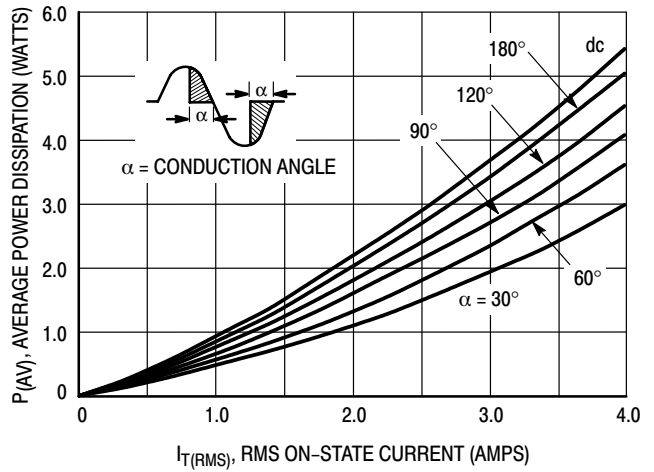


Figure 2. On-State Power Dissipation

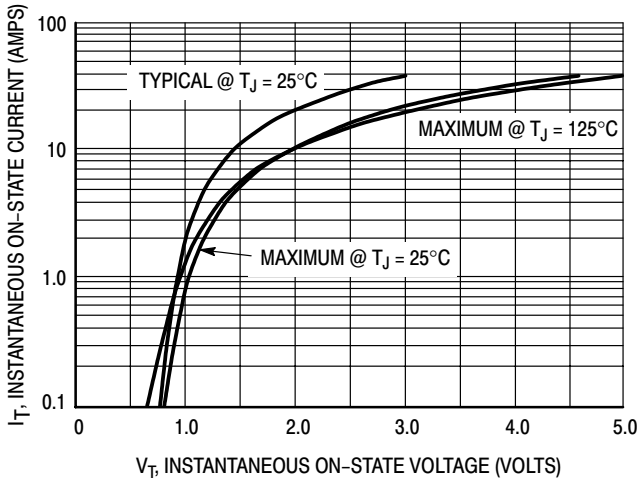


Figure 3. On-State Characteristics

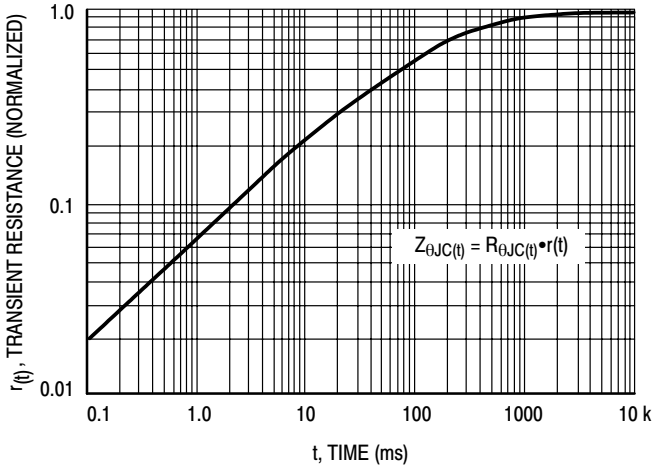


Figure 4. Transient Thermal Response

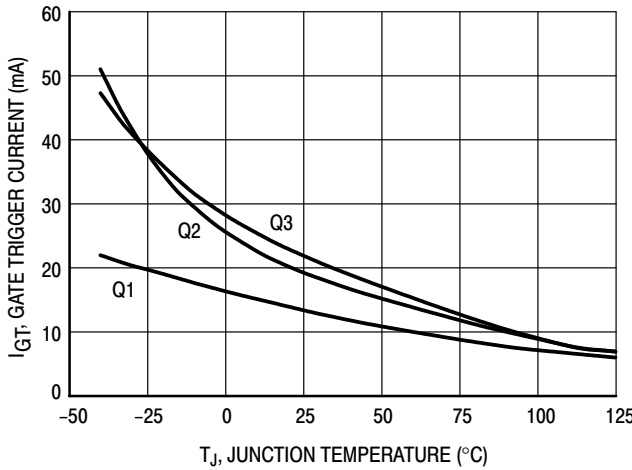


Figure 5. Typical Gate Trigger Current versus Junction Temperature

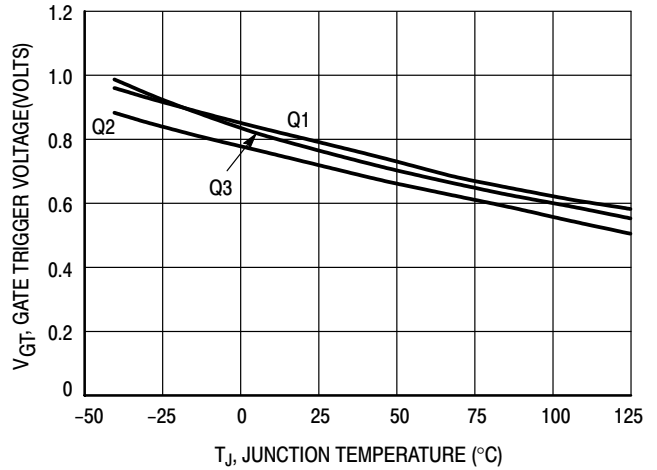


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

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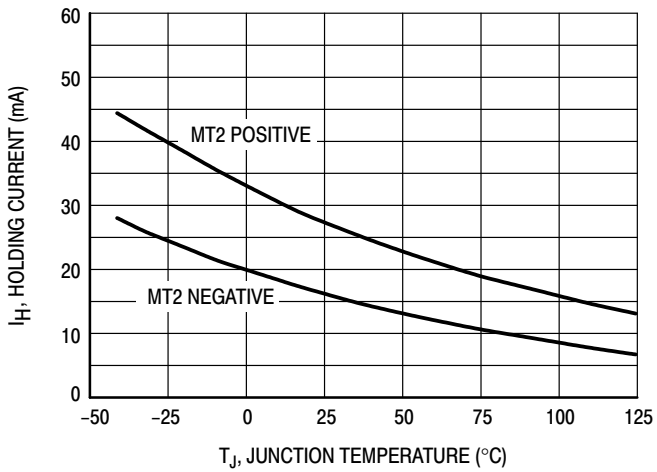


Figure 7. Typical Holding Current versus Junction Temperature

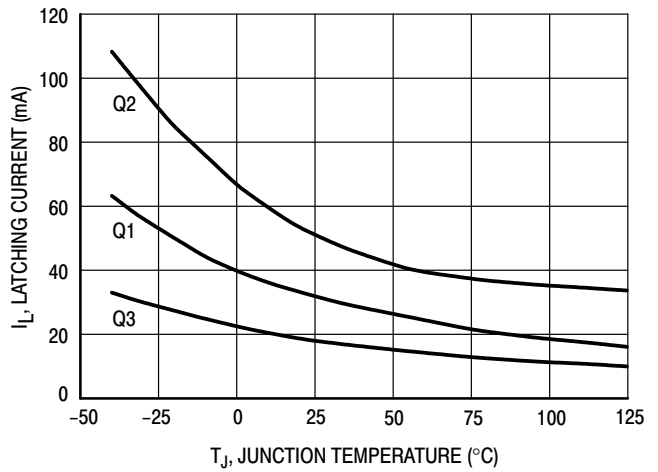


Figure 8. Typical Latching Current versus Junction Temperature

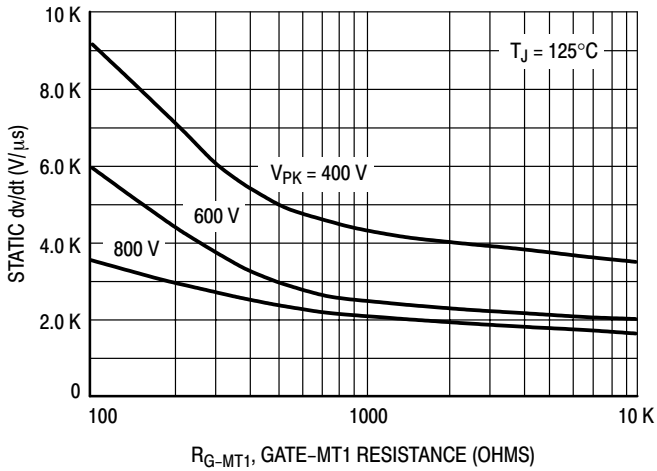


Figure 9. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(+)

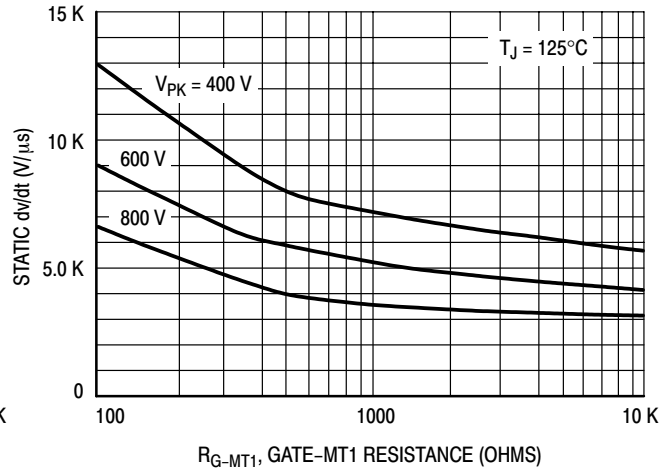


Figure 10. Exponential Static dv/dt versus Gate-MT1 Resistance, MT2(-)

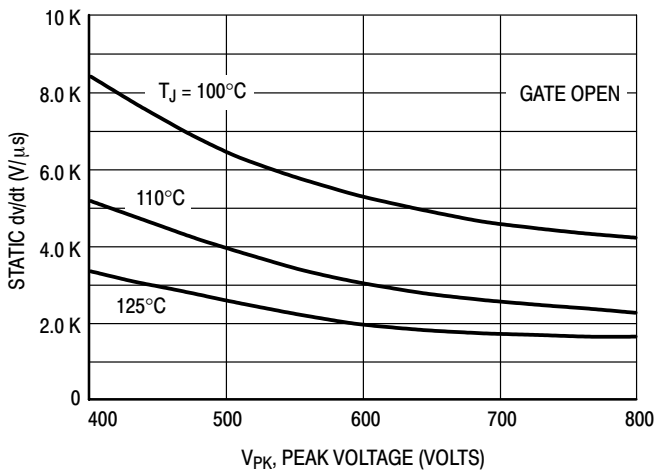


Figure 11. Exponential Static dv/dt versus Peak Voltage, MT2(+)

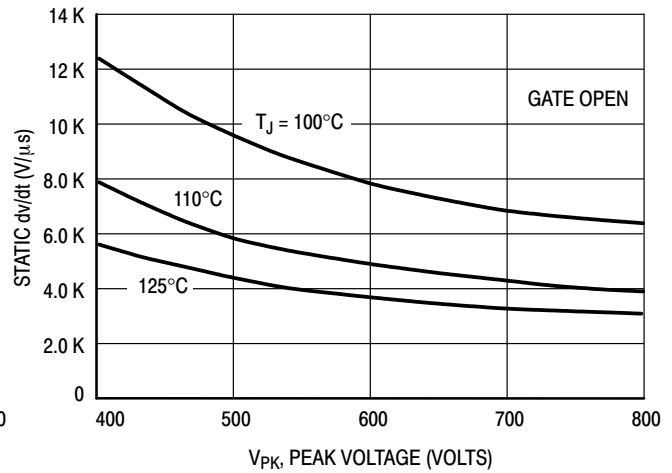


Figure 12. Exponential Static dv/dt versus Peak Voltage, MT2(-)

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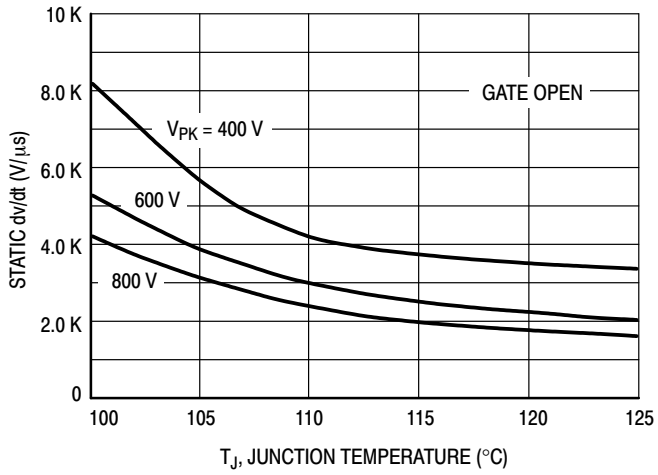


Figure 13. Typical Exponential Static dv/dt versus Junction Temperature, MT2(+)

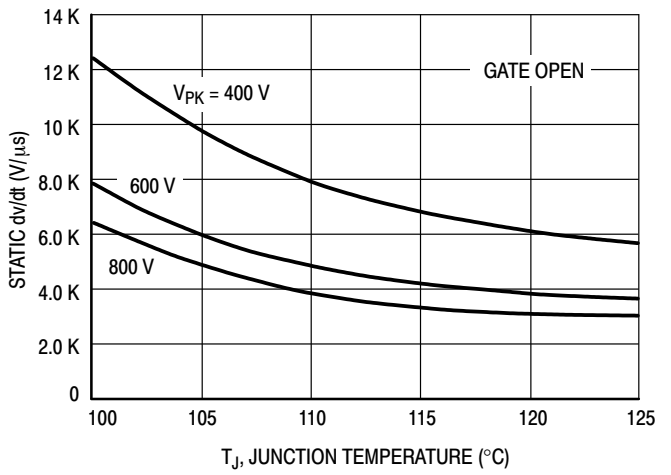


Figure 14. Typical Exponential Static dv/dt versus Junction Temperature, MT2(-)

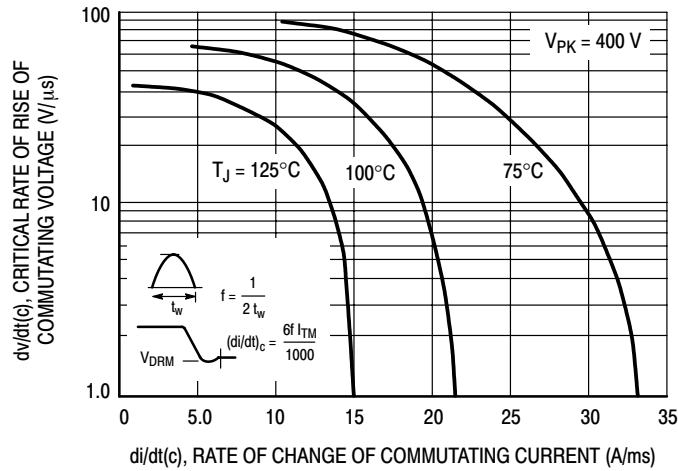
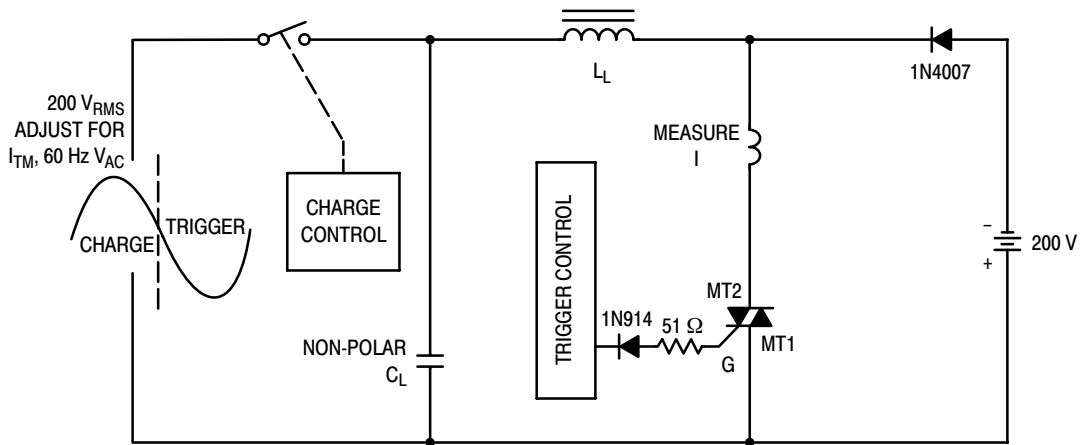


Figure 15. Critical Rate of Rise of Commutating Voltage



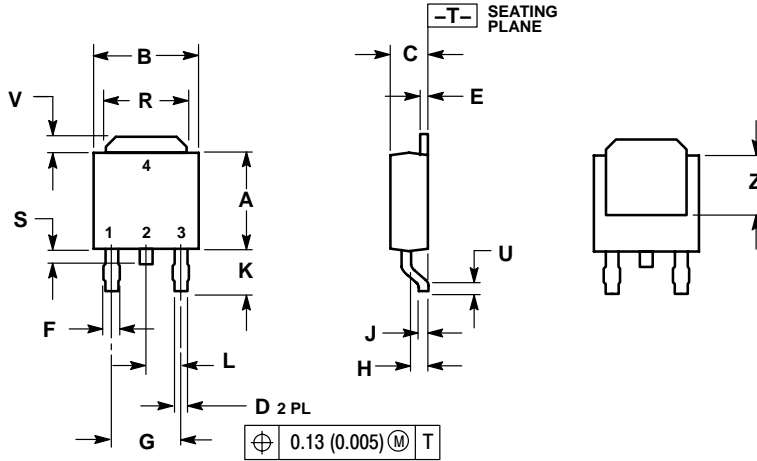
Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current $(di/dt)_c$

MAC4DCM, MAC4DCN

PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

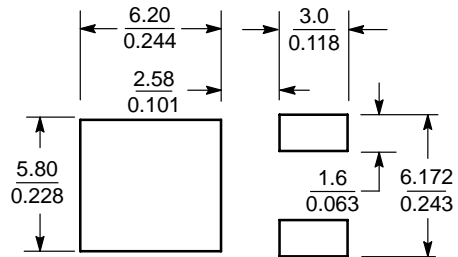


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

SOLDERING FOOTPRINT

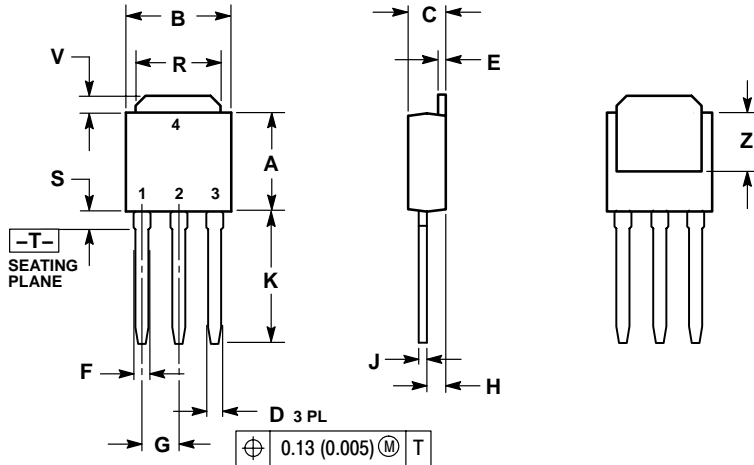


SCALE 3:1 (mm/inches)

MAC4DCM, MAC4DCN

PACKAGE DIMENSIONS

DPAK-3
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 6:

- PIN 1. MT1
- 2. MT2
- 3. GATE
- 4. MT2

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