

SN74LS194A

4-Bit Bidirectional Universal Shift Register

The SN74LS194A is a High Speed 4-Bit Bidirectional Universal Shift Register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The LS194A is similar in operation to the LS195A Universal Shift Register, with added features of shift left without external connections and hold (do nothing) modes of operation. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with all ON Semiconductor TTL families.

- Typical Shift Frequency of 36 MHz
- Asynchronous Master Reset
- Hold (Do Nothing) Mode
- Fully Synchronous Serial or Parallel Data Transfers
- Input Clamp Diodes Limit High Speed Termination Effects

GUARANTEED OPERATING RANGES

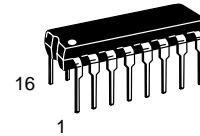
| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|-------------------------------------|------|-----|------|------|
| V _{CC} | Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| T _A | Operating Ambient Temperature Range | 0 | 25 | 70 | °C |
| I _{OH} | Output Current – High | | | –0.4 | mA |
| I _{OL} | Output Current – Low | | | 8.0 | mA |



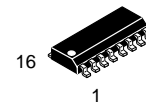
ON Semiconductor™

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**LOW
POWER
SCHOTTKY**



PLASTIC
N SUFFIX
CASE 648



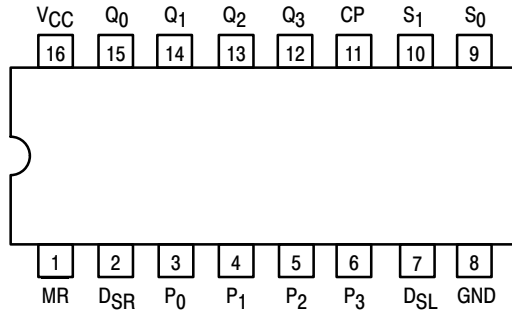
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D SUFFIX
CASE 751B

ORDERING INFORMATION

| Device | Package | Shipping |
|---------------|------------|------------------|
| SN74LS194AN | 16 Pin DIP | 2000 Units/Box |
| SN74LS194AD | SOIC–16 | 38 Units/Rail |
| SN74LS194ADR2 | SOIC–16 | 2500/Tape & Reel |

SN74LS194A

CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES

| | |
|---------------------------------|--------------------------------------|
| S ₀ , S ₁ | Mode Control Inputs |
| P ₀ - P ₃ | Parallel Data Inputs |
| D _{SR} | Serial (Shift Right) Data Input |
| D _{SL} | Serial (Shift Left) Data Input |
| CP | Clock (Active HIGH Going Edge) Input |
| MR | Master Reset (Active LOW) Input |
| Q ₀ - Q ₃ | Parallel Outputs |

LOADING (Note a)

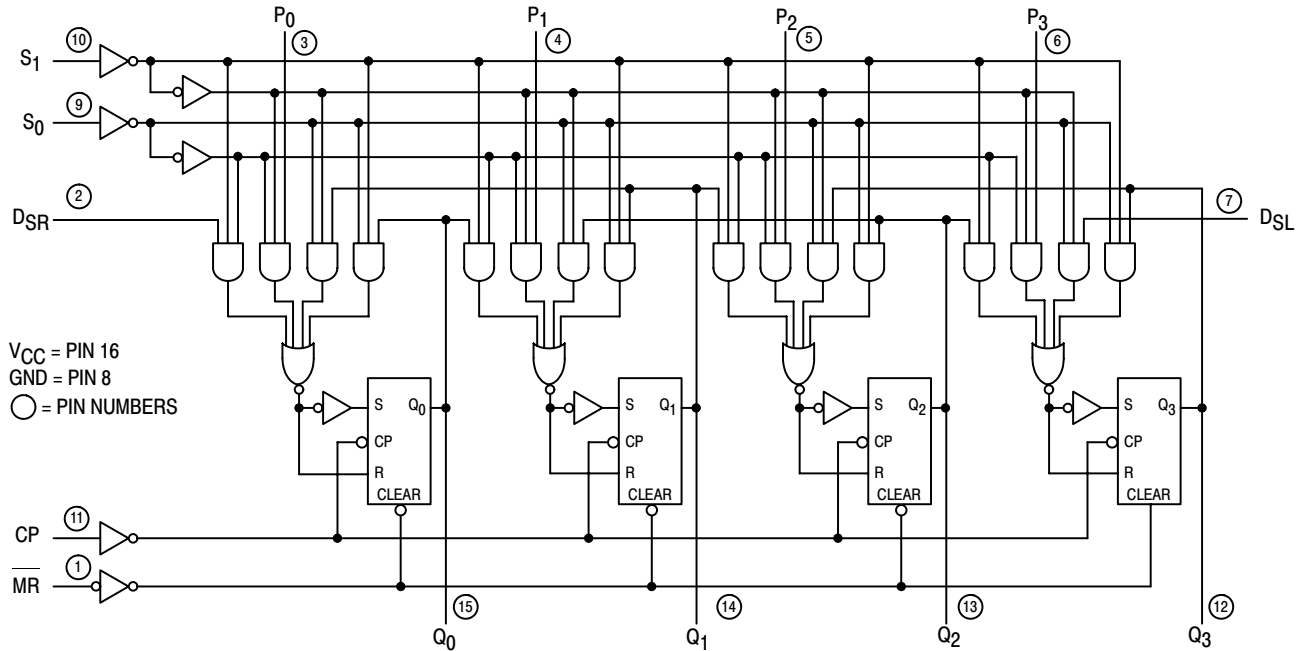
| | HIGH | LOW |
|---------------------------------|----------|-----------|
| S ₀ , S ₁ | 0.5 U.L. | 0.25 U.L. |
| P ₀ - P ₃ | 0.5 U.L. | 0.25 U.L. |
| D _{SR} | 0.5 U.L. | 0.25 U.L. |
| D _{SL} | 0.5 U.L. | 0.25 U.L. |
| CP | 0.5 U.L. | 0.25 U.L. |
| MR | 0.5 U.L. | 0.25 U.L. |
| Q ₀ - Q ₃ | 10 U.L. | 5 U.L. |

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

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LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The Logic Diagram and Truth Table indicate the functional characteristics of the LS194A 4-Bit Bidirectional Shift Register. The LS194A is similar in operation to the ON Semiconductor LS195A Universal Shift Register when used in serial or parallel data register transfers. Some of the common features of the two devices are described below:

All data and mode control inputs are edge-triggered, responding only to the LOW to HIGH transition of the Clock (CP). The only timing restriction, therefore, is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The register is fully synchronous, with all operations taking place in less than 15 ns (typical) making the device especially useful for implementing very high speed CPUs, or the memory buffer registers.

The four parallel data inputs (P_0 , P_1 , P_2 , P_3) are D-type inputs. When both S_0 and S_1 are HIGH, the data appearing on P_0 , P_1 , P_2 , and P_3 inputs is transferred to the Q_0 , Q_1 , Q_2 , and Q_3 outputs respectively following the next LOW to HIGH transition of the clock.

The asynchronous Master Reset (\overline{MR}), when LOW, overrides all other input conditions and forces the Q outputs LOW.

Special logic features of the LS194A design which increase the range of application are described below:

Two mode control inputs (S_0 , S_1) determine the synchronous operation of the device. As shown in the Mode Selection Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered loading all four bits of the register simultaneously. When both S_0 and S_1 are LOW, the existing data is retained in a "do nothing" mode without restricting the HIGH to LOW clock transition.

D-type serial data inputs (D_{SR} , D_{SL}) are provided on both the first and last stages to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

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MODE SELECT — TRUTH TABLE

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | | | |
|----------------|--------|----------------|----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|----------------|
| | MR | S ₁ | S ₀ | D _{SR} | D _{SL} | P _n | Q ₀ | Q ₁ | Q ₂ | Q ₃ |
| Reset | L | X | X | X | X | X | L | L | L | L |
| Hold | H | l | l | X | X | X | q ₀ | q ₁ | q ₂ | q ₃ |
| Shift Left | H | h | l | X | l | X | q ₁ | q ₂ | q ₃ | L |
| | H | h | l | X | h | X | q ₁ | q ₂ | q ₃ | H |
| Shift Right | H | l | h | l | X | X | L | q ₀ | q ₁ | q ₂ |
| | H | l | h | h | X | X | H | q ₀ | q ₁ | q ₂ |
| Parallel Load | H | h | h | X | X | P _n | P ₀ | P ₁ | P ₂ | P ₃ |

L = LOW Voltage Level

H = HIGH Voltage Level

X = Don't Care

l = LOW voltage level one set-up time prior to the LOW to HIGH clock transition

h = HIGH voltage level one set-up time prior to the LOW to HIGH clock transition

P_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|-----------------|--------------------------------|--------|-------|------|------|--|
| | | Min | Typ | Max | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | Guaranteed Input LOW Voltage for All Inputs |
| V _{IK} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V | V _{CC} = MIN, I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 2.7 | 3.5 | | V | V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table |
| V _{OL} | Output LOW Voltage | | 0.25 | 0.4 | V | I _{OL} = 4.0 mA |
| | | | 0.35 | 0.5 | V | I _{OL} = 8.0 mA |
| I _{IH} | Input HIGH Current | | | 20 | μA | V _{CC} = MAX, V _{IN} = 2.7 V |
| | | | | 0.1 | mA | V _{CC} = MAX, V _{IN} = 7.0 V |
| I _{IL} | Input LOW Current | | | -0.4 | mA | V _{CC} = MAX, V _{IN} = 0.4 V |
| I _{OS} | Short Circuit Current (Note 1) | -20 | | -100 | mA | V _{CC} = MAX |
| I _{CC} | Power Supply Current | | | 23 | mA | V _{CC} = MAX |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|--------------------------------------|---------------------------------------|--------|----------|----------|------|---|
| | | Min | Typ | Max | | |
| f _{MAX} | Maximum Clock Frequency | 25 | 36 | | MHz | V _{CC} = 5.0 V C _L = 15 pF |
| t _{PLH} t _{PHL} | Propagation Delay, Clock to Output | | 14 17 | 22 26 | ns | |
| t _{PHL} | Propagation Delay, MR to Output | | 19 | 30 | ns | |

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AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|-----------|-------------------------|--------|-----|-----|------|-------------------------|
| | | Min | Typ | Max | | |
| t_W | Clock or MR Pulse Width | 20 | | | ns | $V_{CC} = 5.0\text{ V}$ |
| t_s | Mode Control Setup Time | 30 | | | ns | |
| t_s | Data Setup Time | 20 | | | ns | |
| t_h | Hold time, Any Input | 0 | | | ns | |
| t_{rec} | Recovery Time | 25 | | | ns | |

DEFINITIONS OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

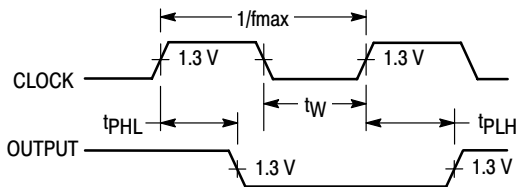
HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure

continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

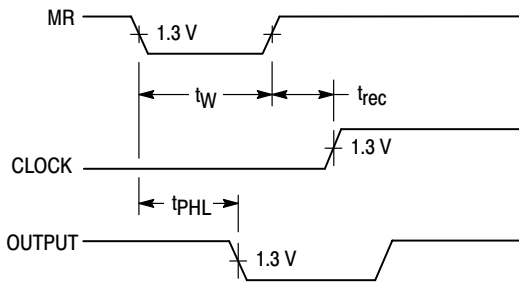
AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



OTHER CONDITIONS: $S_1 = L, \overline{MR} = H, S_0 = H$

Figure 1. Clock to Output Delays Clock Pulse Width and f_{max}



OTHER CONDITIONS: $S_0, S_1 = H$
 $P_0 = P_1 = P_2 = P_3 = H$

Figure 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

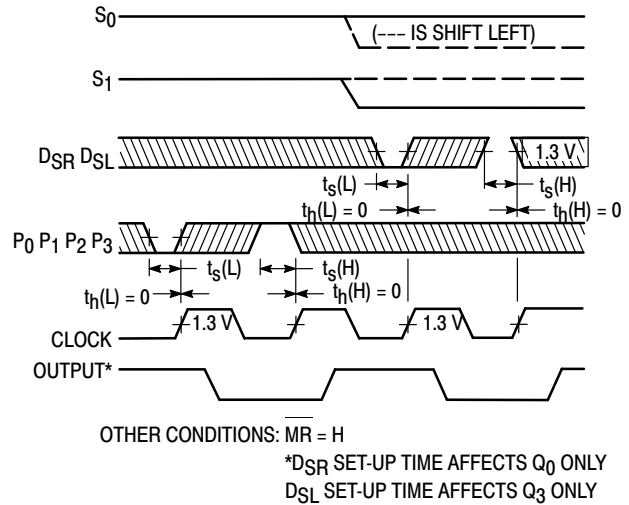


Figure 3. Setup (t_s) and Hold (t_h) Time for Serial Data (D_{SR}, D_{SL}) and Parallel Data (P_0, P_1, P_2, P_3)

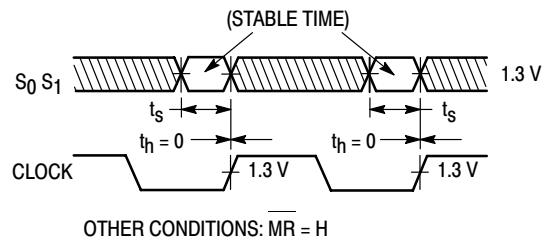
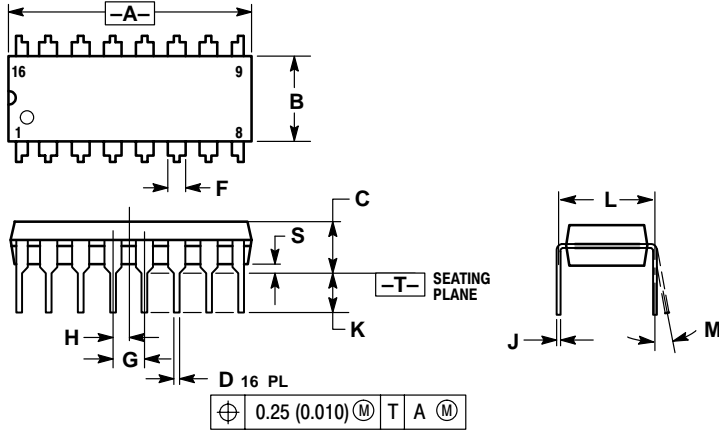


Figure 4. Setup (t_s) and Hold (t_h) Time for S Input

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PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648-08
ISSUE R



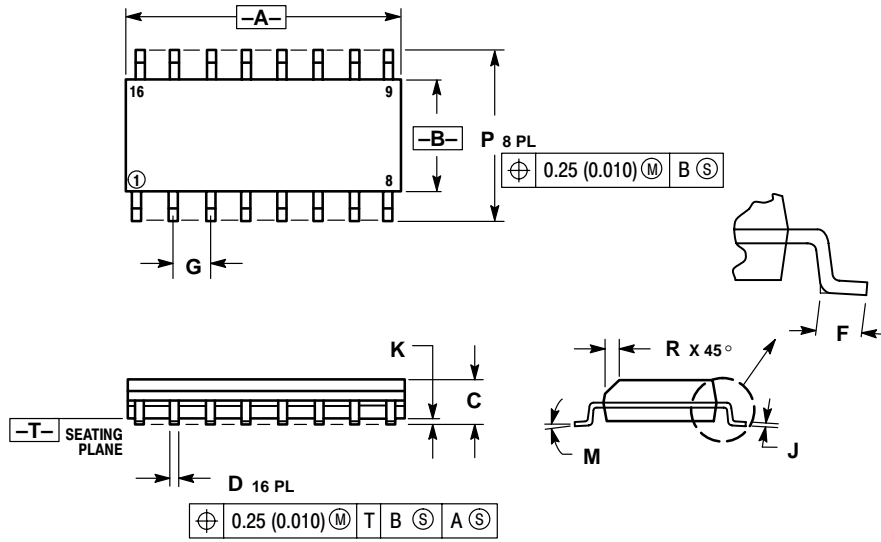
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° 10° | | 0° 10° | |
| S | 0.020 | 0.040 | 0.51 | 1.01 |


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D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| MILLIMETERS | | INCHES | | |
|-------------|----------|--------|-----------|-------|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° 7° | | 0° 7° | |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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