

DATA SHEET

74F378

Hex D flip-flop with enable

Product specification

1989 Oct 05

IC15 Data Handbook

Hex D flip-flop with enable

74F378

FEATURES

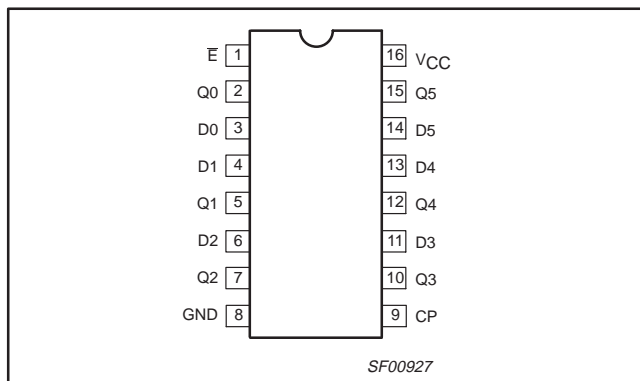
- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common Clock and Enable inputs
- Input clamp diodes limit high speed termination effects
- Fully TTL and CMOS compatible

DESCRIPTION

The 74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable (\bar{E}) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transformed to the corresponding flop-flop's Q output. The \bar{E} input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
16-pin plastic DIP	N74F378N	SOT38-4
16-pin plastic SO	N74F378D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D5	Data inputs	1.0/1.0	20 μ A/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20 μ A/0.6mA
\bar{E}	Enable input (active low)	1.0/1.0	20 μ A/0.6mA
Q0 – Q5	Data outputs	50/33	1.0mA/20mA

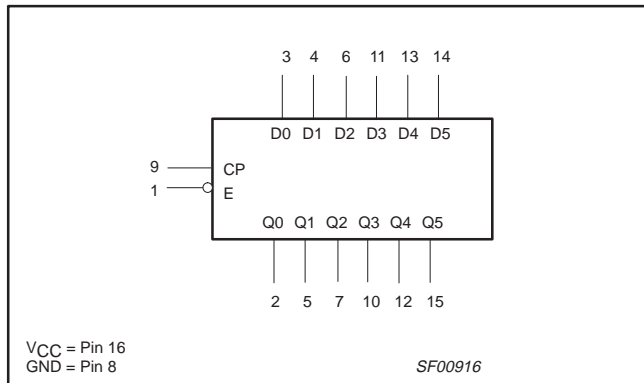
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

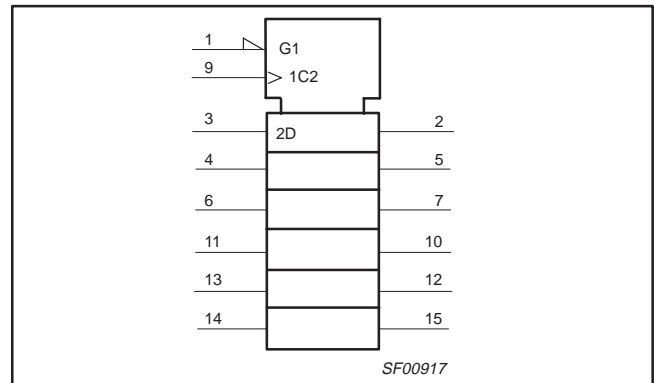
Hex D flip-flop with enable

74F378

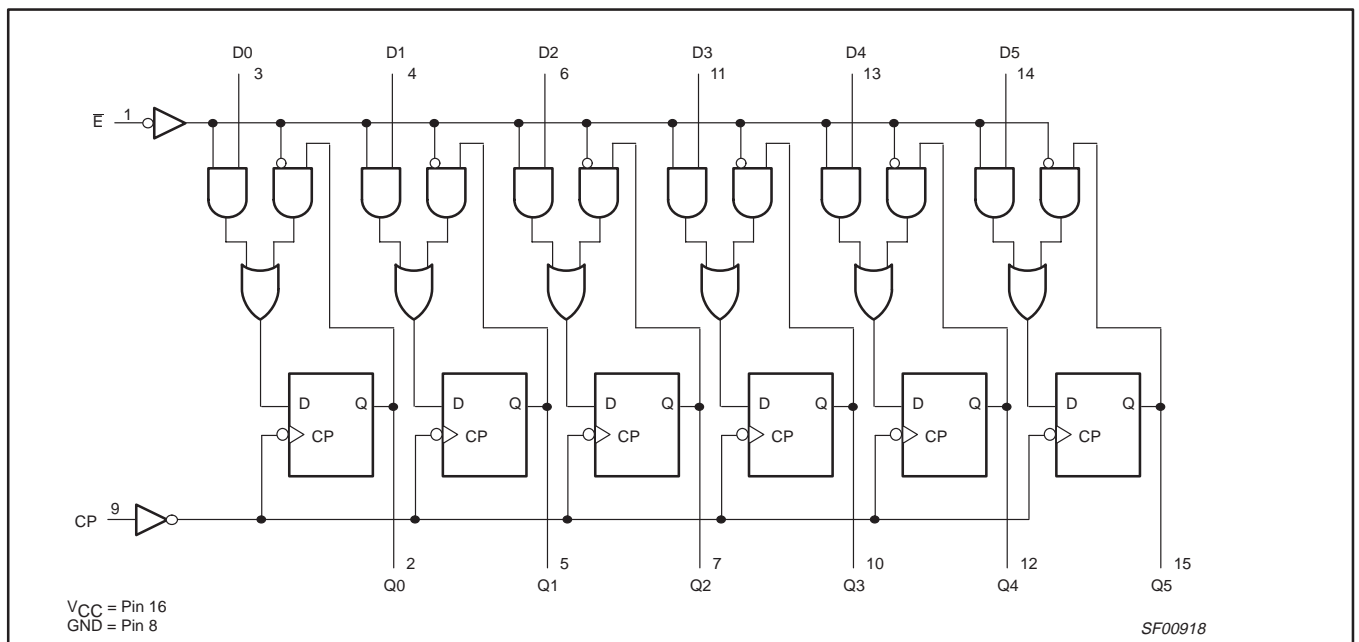
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
\bar{E}	CP	D _n	Q _n	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

- H = High-voltage level
- h = High-voltage level one setup time prior to the Low-to-High clock transition
- L = Low-voltage level
- l = Low-voltage level one setup time prior to the Low-to-High clock transition
- X = Don't care
- ↑ = Low-to-High clock transition

Hex D flip-flop with enable

74F378

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER SYMBOL	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT		
			MIN	TYP ²	MAX			
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$	$\pm 10\%V_{CC}$	2.5		V		
		$V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 5\%V_{CC}$	2.7	3.4	V		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$	$\pm 10\%V_{CC}$		0.30	0.50	V	
		$V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 5\%V_{CC}$		0.30	0.50	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$				100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$				20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$				-0.6	mA	
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$				-60	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$			32	45	mA
		I_{CCL}				35	45	mA

Notes:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ C$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Hex D flip-flop with enable

74F378

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Qn	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns

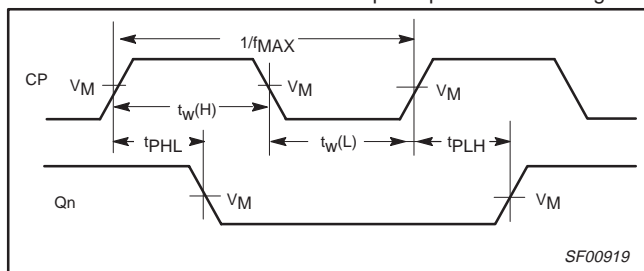
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _s (H) t _s (L)	Setup time, High or Low Dn to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
t _h (H) t _h (L)	Hold time, High or Low Dn to CP	Waveform 2	0 0			0 0		ns
t _s (H) t _s (L)	Setup time, High or Low Ē to CP	Waveform 2	4.0 10.0			4.0 10.0		ns
t _h (H) t _h (L)	Hold time, High or Low Ē to CP	Waveform 2	0 0			0 0		ns
t _w (H) t _w (L)	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

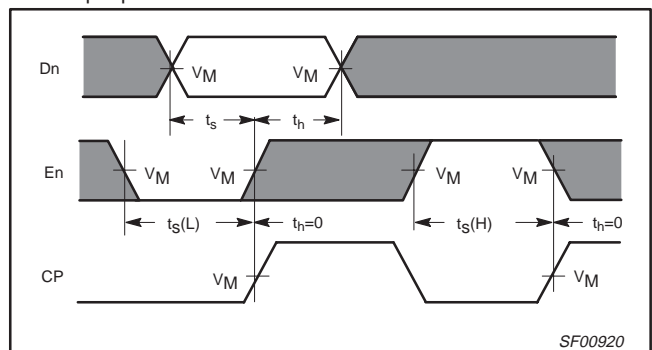
AC WAVEFORMS

For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency

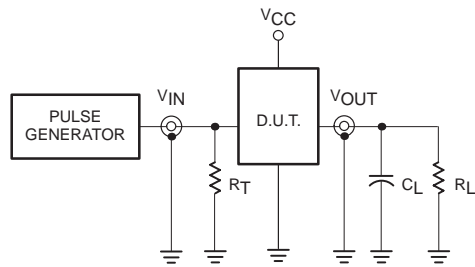


Waveform 2. Data and Enable Setup Time and Hold Times

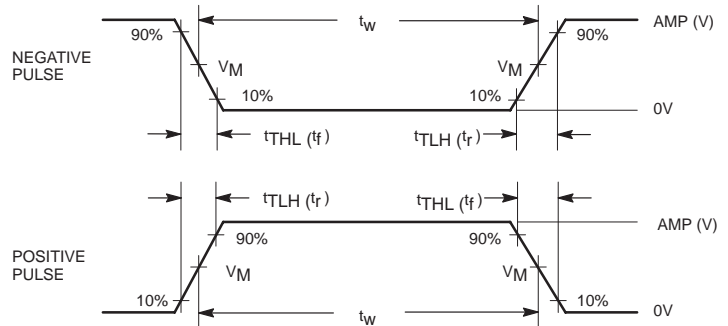
Hex D flip-flop with enable

74F378

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

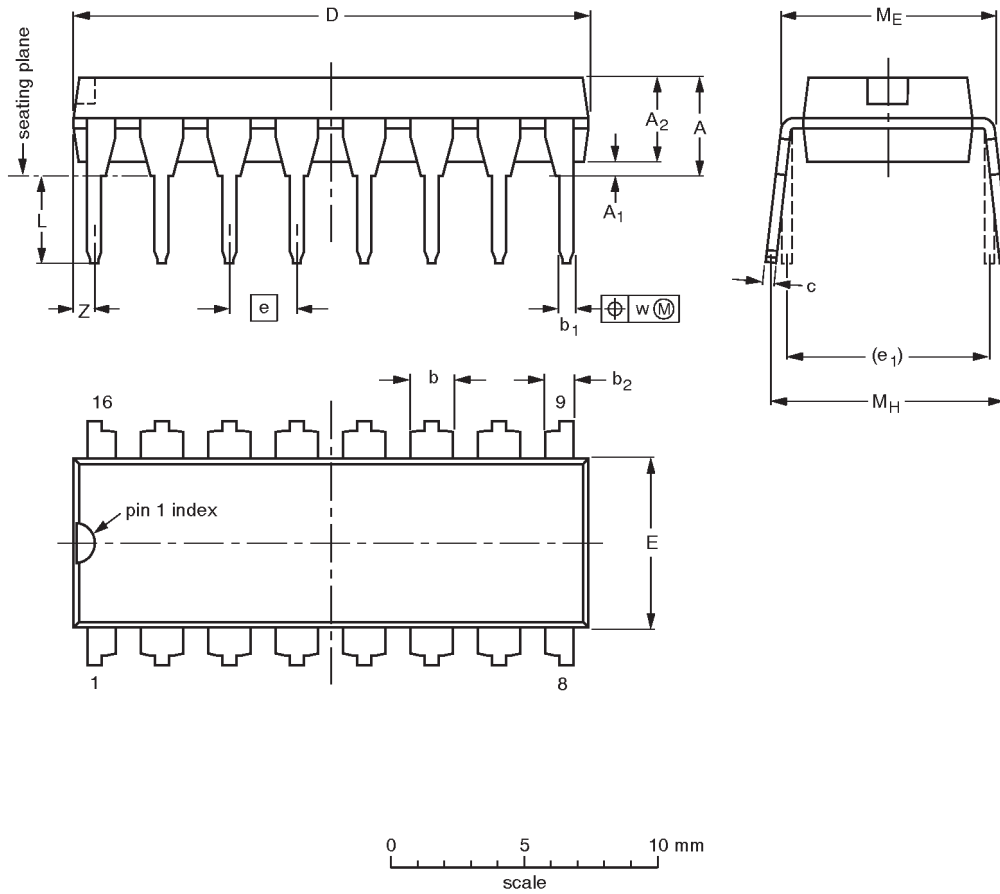
SF00006

Hex D flip-flop with enable

74F378

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

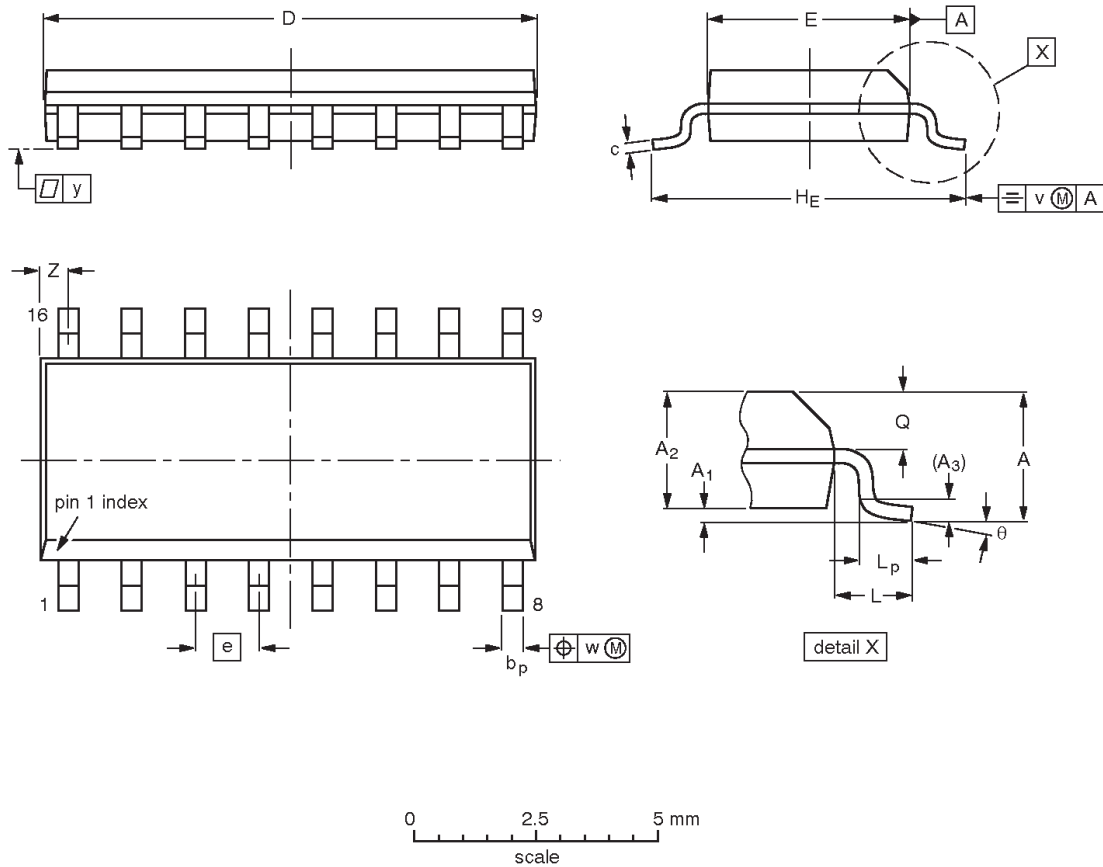
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

Hex D flip-flop with enable

74F378

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75 0.10	0.25 1.25	1.45 0.049	0.25 0.36	0.49 0.19	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01 0.014	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

Hex D flip-flop with enable

74F378

NOTES

Hex D flip-flop with enable

74F378

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998
All rights reserved. Printed in U.S.A.

print code

Date of release: 10-98

Document order number:

9397-750-05122

Let's make things better.