DATA SHEET

CGY2110CU
10 Gbits/s transimpedance amplifier

Preliminary specification
File under Integrated Circuits, IC19

2001 Dec 07

Philips Semiconductors

PHILIPS

FEATURES

- Suitable for 10 Gbits/s optical fibre links
- Transimpedance gain 66 dBΩ (transimpedance 2 kΩ)
- Low noise <9 pA/√Hz
- Differential output
- Single 5.7 V power supply
- Low power consumption of 400 mW
- Supplied in bare die form.

APPLICATIONS

- Digital fibre optic receiver for optical telecommunications (e.g. STM-64 or OC192 systems)
- High sensitivity and high gain amplifier.

GENERAL DESCRIPTION

The CGY2110CU is a 10 Gbits/s transimpedance amplifier. Typical use is as a low noise preamplifier for light wave receiver modules in optical fibre networks.

The CGY2110CU features differential outputs and operates using a single 5.7 V supply voltage with a very low power consumption of 400 mW (typical value).

The RF input and the photodiode biasing pad of the circuit may be directly connected to a low capacitance photodiode using short bond wires. A biasing circuit for the photodiode is integrated on the CGY2110CU.

This GaAs Monolithic Microwave Integrated Circuit (MMIC) was designed in cooperation with France Telecom R&D and is fabricated using one of OMMIC's fully released millimetre-wave GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) processes.

This device is supplied as a RF tested bare die.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2110CU	–	GaAs bare die	–

BLOCK DIAGRAM

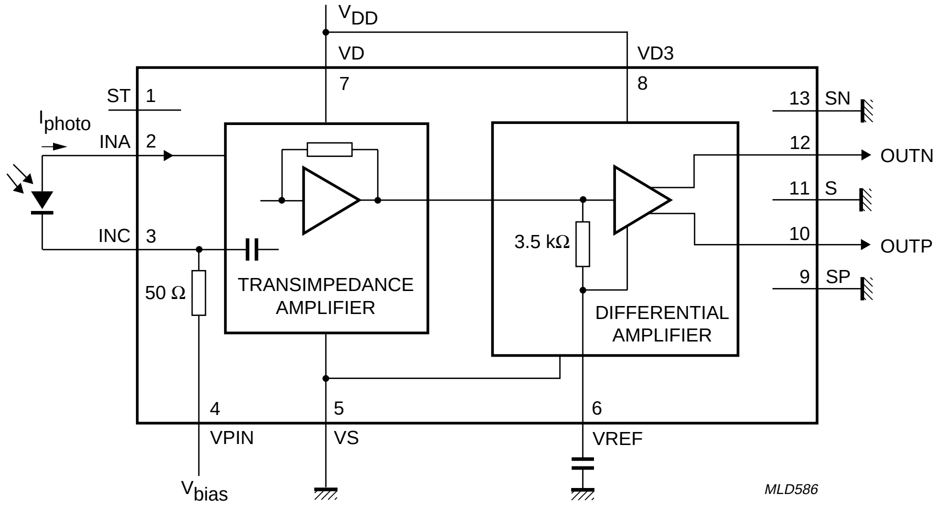


Fig.1 Block diagram.

PINNING

SYMBOL	PAD	DESCRIPTION
ST	1	do not bond
INA	2	photodiode (anode) input
INC	3	photodiode (cathode) biasing pad
VPIN	4	photodiode DC biasing voltage; optional use
VS	5	ground; bond to ground with lowest possible inductance
VREF	6	reference voltage pad; must be decoupled to ground using external capacitor(s)
VD	7	drain supply voltage (V_{DD})
VD3	8	drain supply voltage 3 (V_{DD})
SP	9	ground; bond to ground
OUTP	10	RF output
S	11	ground; bond to ground
OUTN	12	complementary RF output
SN	13	ground; bond to ground

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage on pads VD and VD3	–0.5	+8	V
V_{bias}	photodiode biasing voltage	–15	+15	V
I_{photo}	input photodiode current	–1	+2.5	mA
T_{stg}	storage temperature	–55	+150	°C
$T_{ch(max)}$	maximum operating channel temperature	–	150	°C

ESD WARNING

The CGY2110CU is a very high performance GaAs device and as such care must be taken at all times to avoid damage by electrostatic discharge.

DC CHARACTERISTICS

V_{DD} = 5.7 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage on pads VD and VD3		5.4	5.7	6.0	V
I_{DD}	total supply current		40	70	100	mA
P_{DC}	DC power consumption		228	400	570	mW
$I_{photo(max)}$	maximum photodiode current	before input overload occurs; note 1				
		forward current	–	1.8	–	mA
		reverse current	–	0.3	–	mA
ΔV_O	DC voltage difference between pads OUTP and OUTN		–0.7	–	+0.7	V
T_{amb}	ambient temperature	operating	–10	–	+85	°C

Note

1. As shown in Fig.1, the forward current is assumed to flow from the outside towards the inside of the device, whereas the reverse current is assumed to flow from the inside towards the outside of the device.

AC CHARACTERISTICS

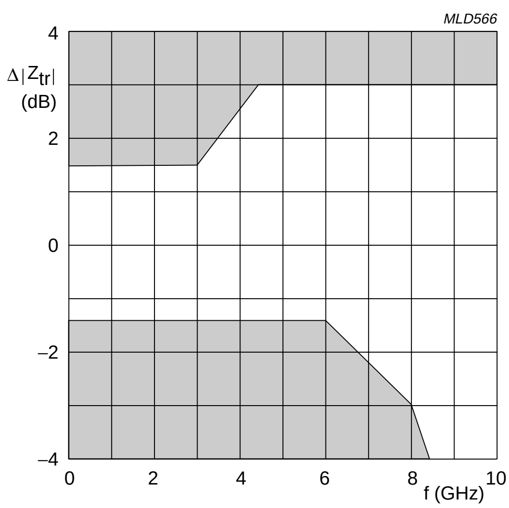
V_{DD} = 5.7 V ±5%; T_{amb} = 25 °C; R_L = 50 Ω; unless otherwise specified; notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\|Z_{tr}\|_{LF}$	low-frequency transimpedance gain	f = 100 MHz				
		single-ended output	62	66	70	dBΩ
		differential output	–	72	–	dBΩ
$\Delta\|Z_{tr}\|$	transimpedance gain ripple	$\Delta\|Z_{tr}\| = \|Z_{tr}\| - \|Z_{tr}\|_{LF}$; see Fig.2				
		f = 1 MHz to 3 GHz	–1.5	0	+1.5	dB
		f = 3 to 6 GHz	–1.5	+1	+3	dB
		f = 6 to 10 GHz	–	–	3	dB
f_{co}	transimpedance cut-off frequency	$\|Z_{tr}\| = \|Z_{tr}\|_{LF} - 3$ dB				
		C_p = 0.22 pF	8	9	–	GHz
		C_p = 0.14 pF	–	10.1	–	GHz
$t_{d(g)}$	group delay	relative to f = 2.5 GHz; see Fig.3				
		f = 1 to 3 GHz	–20	–	+20	ps
		f = 4 GHz	–10	–	+35	ps
		f = 5 GHz	0	–	50	ps
		f = 6.5 to 9 GHz	15	–	75	ps
$\|s_{22}\|$	output reflection coefficient	f = 100 MHz to 10 GHz; note 3	–	–15	–10	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{n(i)(eq)}$	equivalent input noise current density	f = 1 to 4 GHz; C_p = 0.22 pF	–	4.7	7	pA/√Hz
		f = 7 GHz; C_p = 0.22 pF	–	6.5	10	pA/√Hz
		f = 10 GHz; C_p = 0.14 pF	–	8	–	pA/√Hz
$I_{n(i)(tot)(rms)}$	total integrated input noise current (RMS value)	f = 10 MHz to 8 GHz; C_p = 0.22 pF	–	450	650	nA
		f = 10 MHz to 10 GHz; C_p = 0.14 pF	–	500	–	nA
R_L	output load resistance	pads OUTN and OUTP	–	50	–	Ω

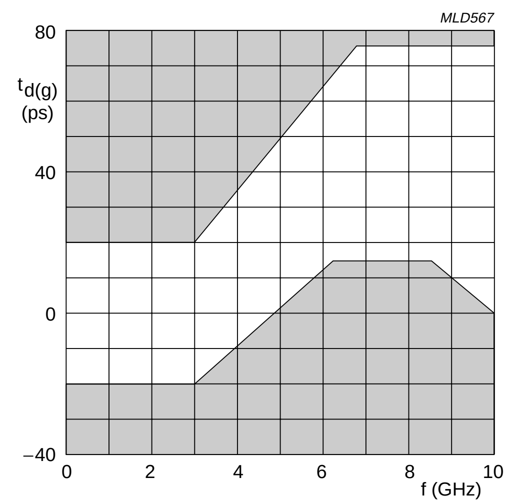
Notes

1. Photodiode and input-parasitics model: C_p = 0.22 pF; R_s = 8 Ω; –3 dB intrinsic optical cut-off frequency = 15 GHz; L_b = 0.6 nH (where $L_b = L_{ba} + L_{bc}$); see Fig.5.
2. AC characteristics are guaranteed for pad OUTP (with pad OUTN loaded by 50 Ω via a DC decoupling capacitor).
3. The $|s_{22}|$ specification given in this table is based on RF on-wafer measurements with low-inductance probes. It is recommended that ground and output bonding wires are kept as short as possible so as not to degrade this parameter (see also “Test and application information”).



Hatched area indicates limit of test specification.

Fig.2 Transimpedance gain ripple as a function of the frequency.



Hatched area indicates limit of test specification.

Fig.3 Group delay as a function of the frequency.

TEST AND APPLICATION INFORMATION

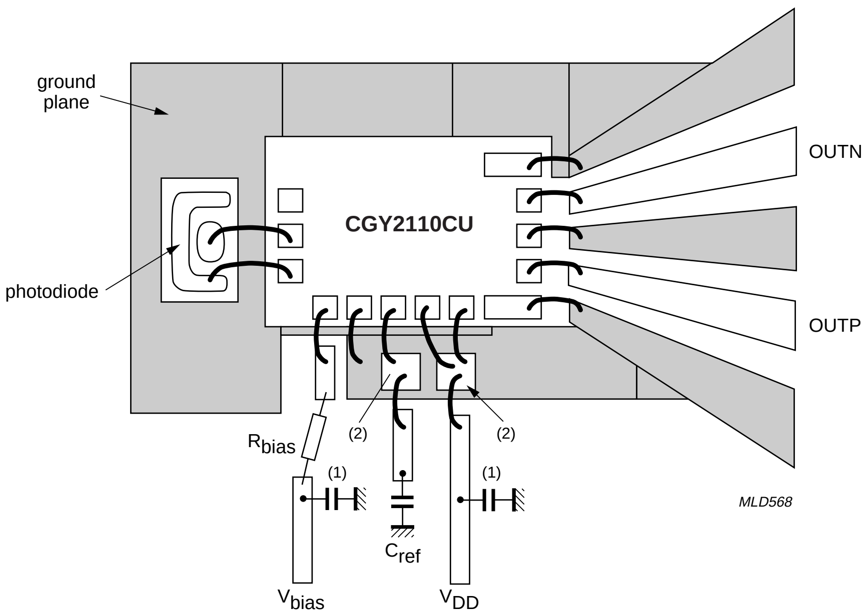
Typical application scheme

A typical receiver module, including a photodiode and a CGY2110CU transimpedance amplifier is shown in Fig.4 and the electrical equivalent model of the module is shown in Fig.5.

To ensure the best performance of the receiver module, the shortest possible connection between photodiode and the IC must be used for both input pads INA and INC. The same precaution applies to the output pads OUTN and OUTP, where the bonding wires should be as short as possible. Pad VS should also be connected to ground with the shortest possible bonding wire.

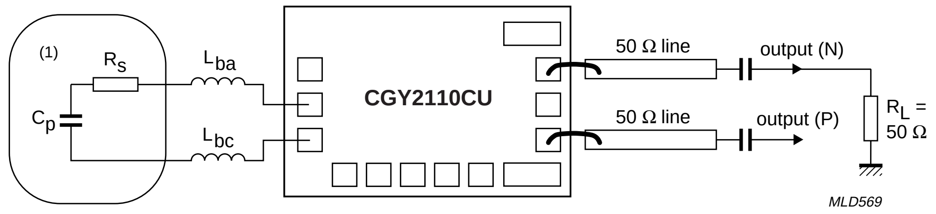
Pad VREF is decoupled directly to ground while pads VD3 and VD are decoupled and connected to the V_{DD} power supply.

A high-value resistor R_{bias} is put in series with pad VPIN to protect the photodiode against high currents in the event of high illumination. The value of R_{bias} is determined by the photodiode characteristics. The recommended decoupling scheme uses a high-frequency ceramic capacitor of 50 pF (typical value) placed close to the IC and a low-frequency multilayer capacitor placed at greater distance. The value of C_{ref} is determined by the required low-frequency cut-off point, given by the time constant of the RC circuit (capacitor C_{ref} and a 3500 Ω on-chip resistor).



(1) Low frequency decoupling capacitor.
(2) High frequency decoupling capacitor.

Fig.4 Module layout for a typical application.



(1) Photodiode equivalent circuit.

Fig.5 Electrical equivalent model of the module.

Operating conditions of photodiode

The performance of the photodiode receiver module is very dependent on both the photodiode capacitance and the interconnection inductance between the photodiode and the CGY2110CU. The circuit was optimized for a photodiode capacitance C_p equal (or lower) than 0.22 pF with a low photodiode series resistance R_s to give the best noise performance from the receiver module.

It is strongly recommended to use short bondings between the photodiode and the CGY2110CU, in order to keep the bonding inductances L_{ba} and L_{bc} to respectively the signal inputs INA and INC as low as possible. A total equivalent inductance L_b of 0.6 nH is recommended while 1.0 nH should be considered a maximum value.

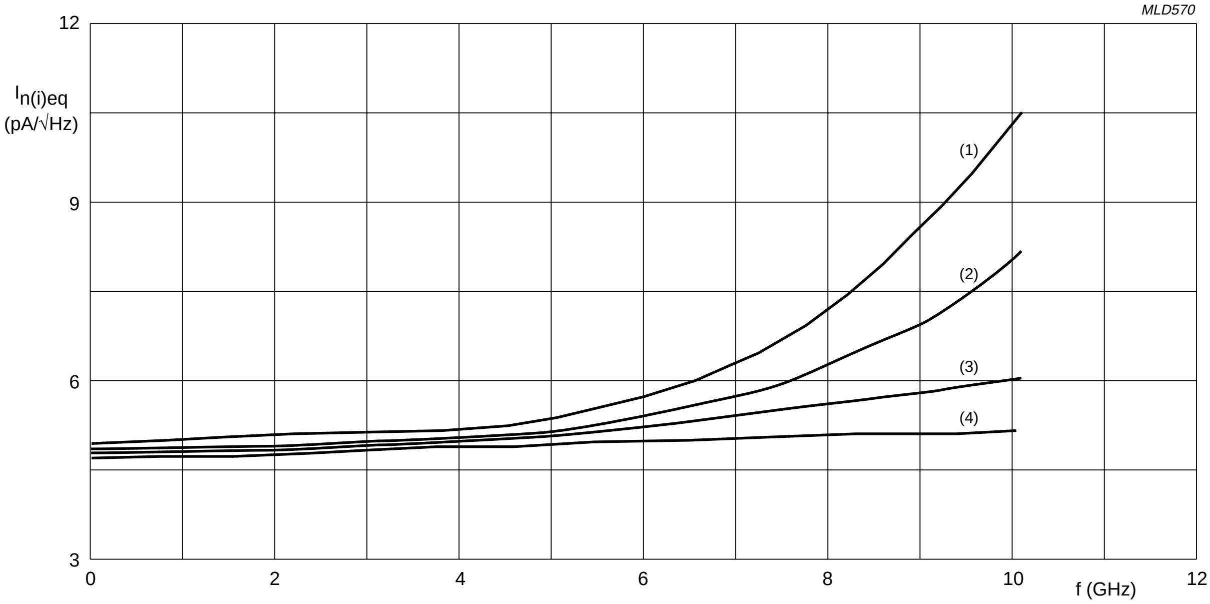
Typical results (computed measurements)

The s-parameters of the CGY2110CU are measured on-wafer under nominal conditions, using 40 GHz bandwidth probes. These s-parameters may then be used with the photodiode parameters in order to simulate the complete 10 Gbits/s receiver module performance (photodiode plus CGY2110CU).

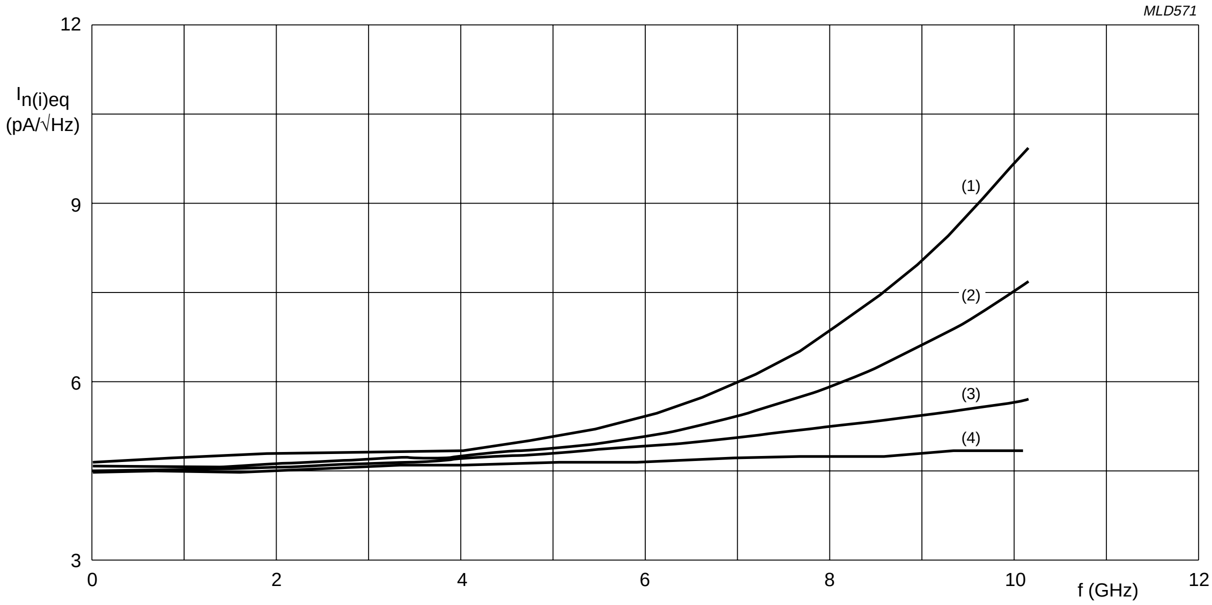
The transimpedance gain and the equivalent input noise current of receiver modules using the CGY2110CU are thus drawn for various photodiode parameter values in Figs 6 to 13. The photodiode –3 dB intrinsinc optical cut-off frequency is always assumed to be 15 GHz. The values of C_p, L_b and R_s are defined as in Fig.5.

From Figs 6 and 7, it is clear that the lowest possible photodiode capacitance C_p will lead to the lowest noise, while Figs 8 and 9 show that the lowest possible bonding inductance value L_b will lead to the flattest gain response. Recommended values are $C_p < 0.25$ pF and $L_b < 0.6$ nH.

Figures 10 to 13 show the variation of the transimpedance gain, equivalent input noise current, group delay and output matching (s_{22}) as a function of the temperature and the supply voltage.



a. V_{DD} = 5.4 V.



b. V_{DD} = 6.0 V.

R_s = 8 Ω; L_b = 0.6 nH.

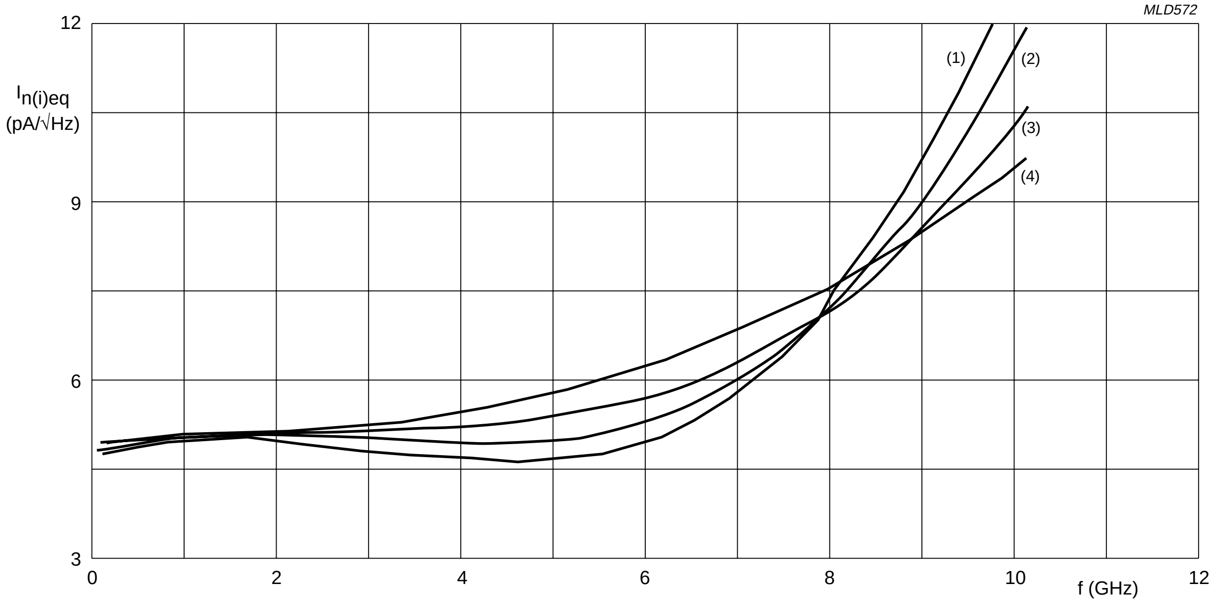
(1) C_p = 0.22 pF.

(2) C_p = 0.18 pF.

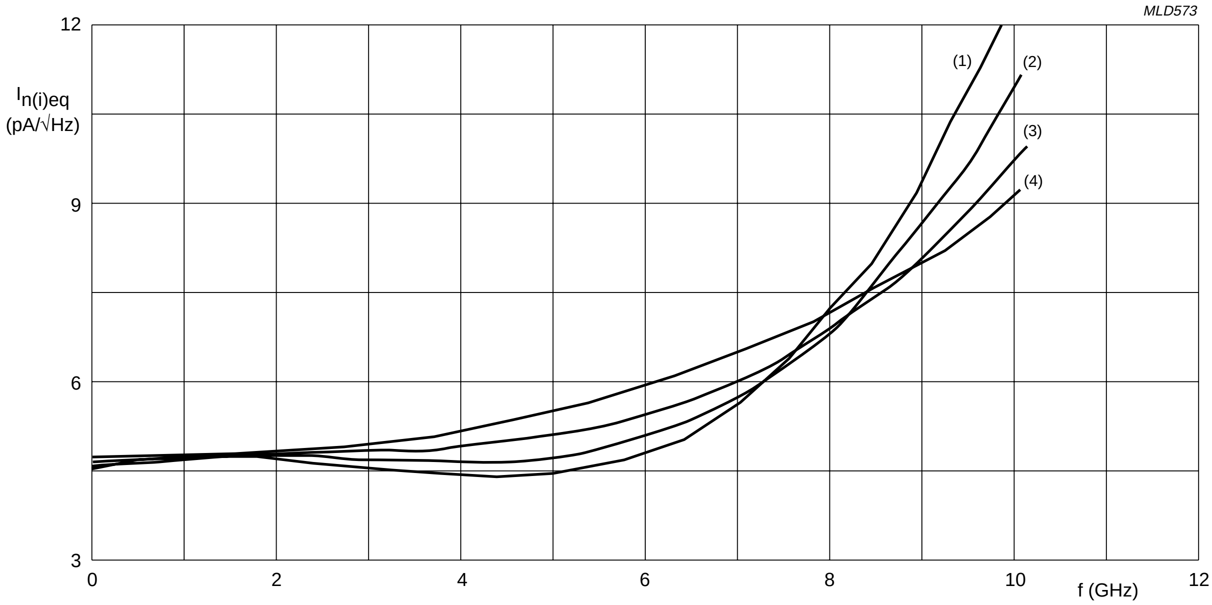
(3) C_p = 0.14 pF.

(4) C_p = 0.10 pF.

Fig.6 Equivalent input noise current density as a function of the frequency with different values of the internal photodiode capacitance.



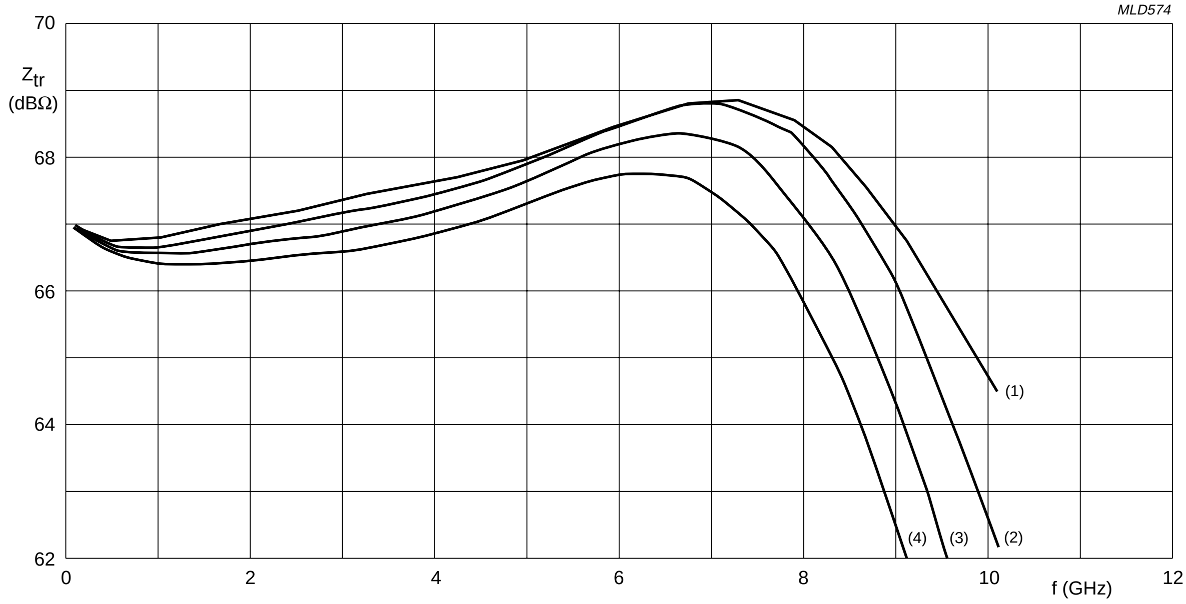
a. V_{DD} = 5.4 V.



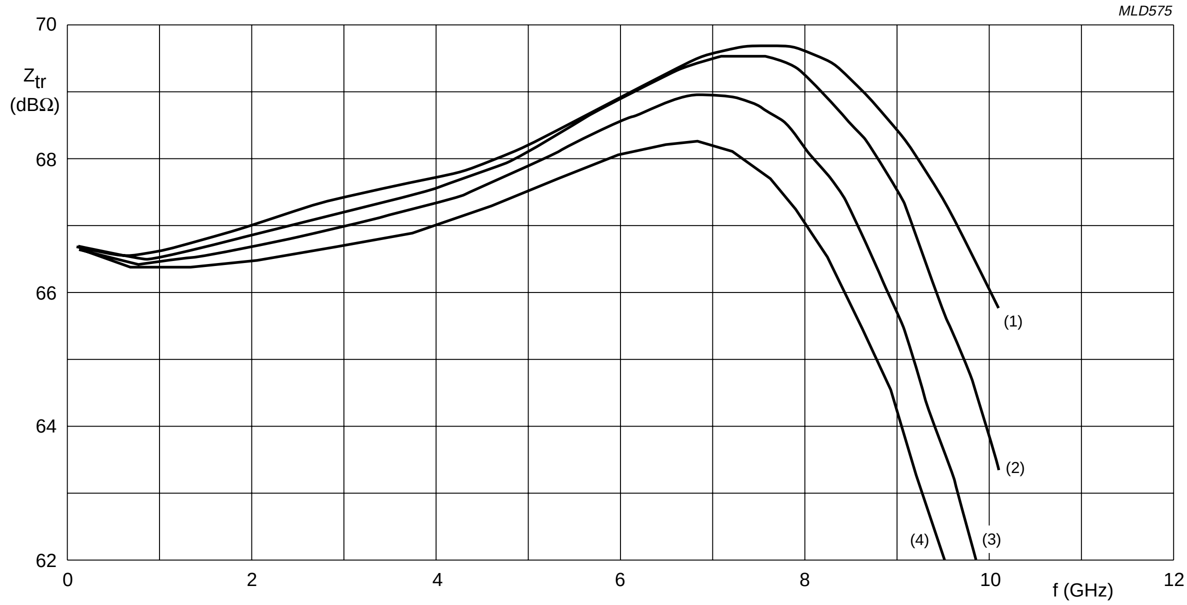
b. V_{DD} = 6.0 V.

R_s = 8 Ω; C_p = 0.22 pF.
(1) $L_b = 2 \times 0.7$ nH.
(2) $L_b = 2 \times 0.5$ nH.
(3) $L_b = 2 \times 0.3$ nH.
(4) $L_b = 2 \times 0.1$ nH.

Fig.7 Equivalent input noise current density as a function of the frequency with different values of the bonding inductance to the photodiode.



a. V_{DD} = 5.4 V.



b. V_{DD} = 6.0 V.

R_s = 8 Ω; L_b = 0.6 nH.

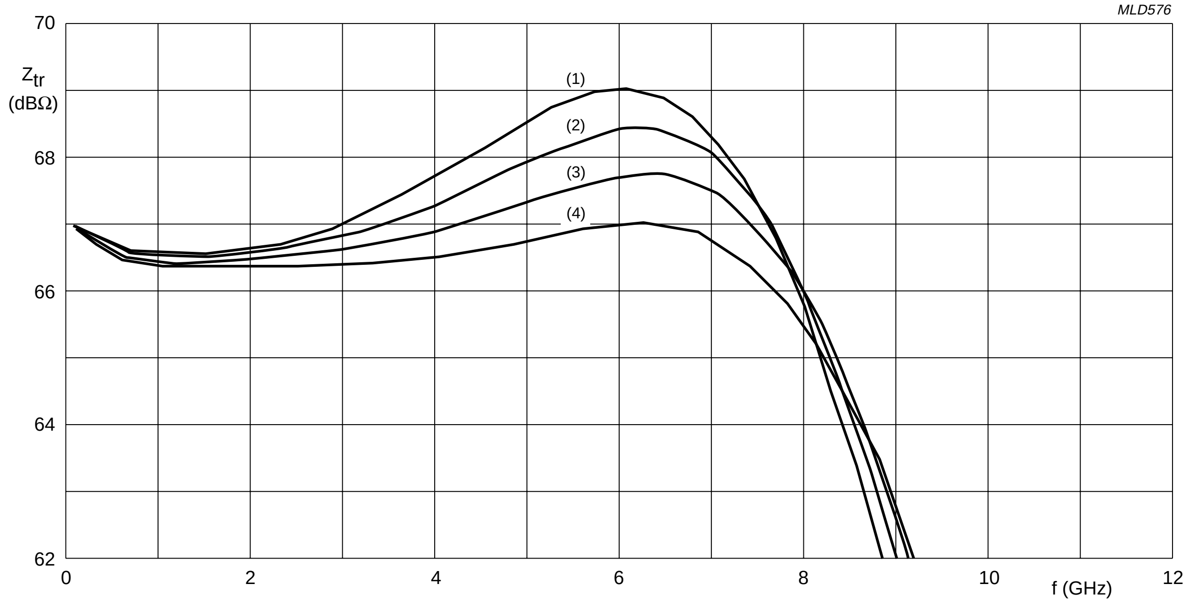
(1) C_p = 0.10 pF.

(2) C_p = 0.14 pF.

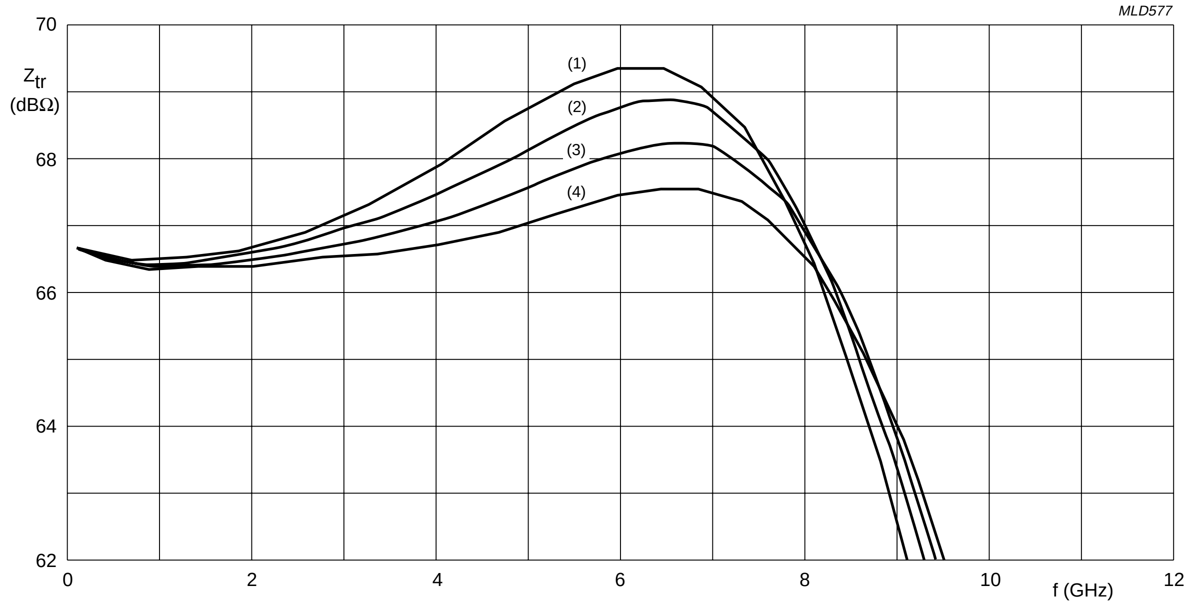
(3) C_p = 0.18 pF.

(4) C_p = 0.22 pF.

Fig.8 Transimpedance gain as a function of the frequency with different values of the internal photodiode capacitance.



a. V_{DD} = 5.4 V.



b. V_{DD} = 6.0 V.

R_s = 8 Ω; C_p = 0.22 pF.

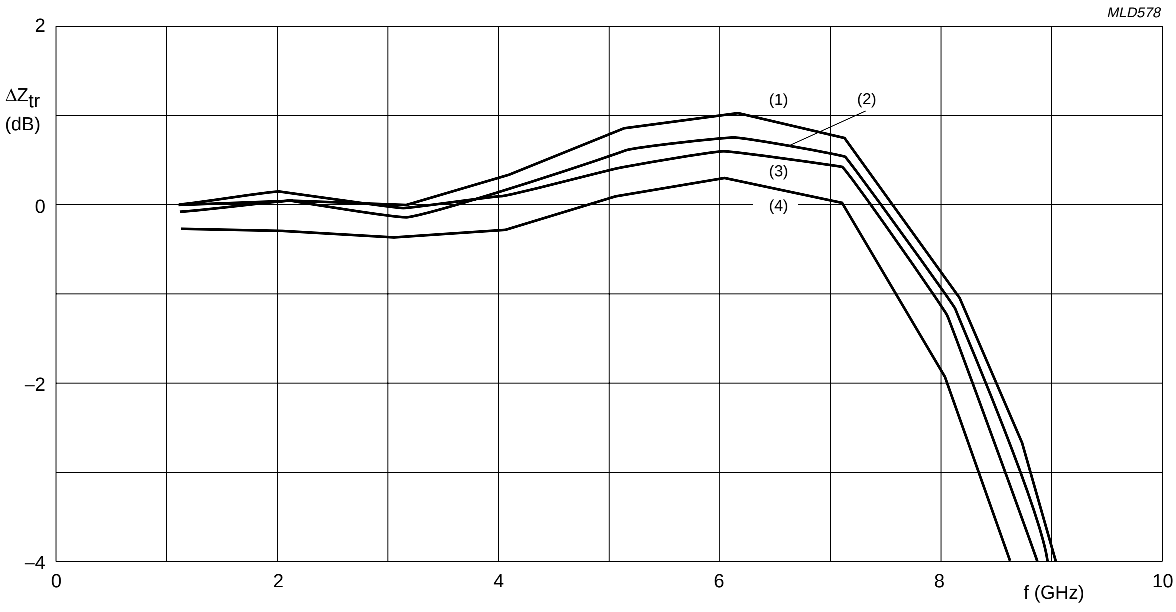
(1) L_b = 2 × 0.7 nH.

(2) L_b = 2 × 0.5 nH.

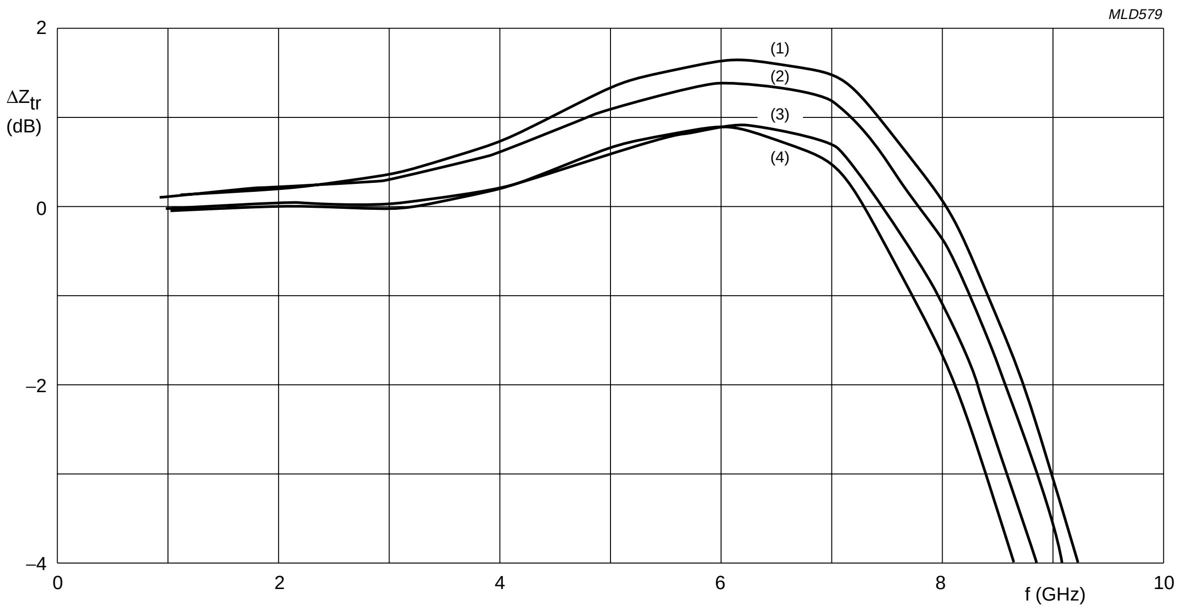
(3) L_b = 2 × 0.3 nH.

(4) L_b = 2 × 0.1 nH.

Fig.9 Transimpedance gain as a function of the frequency with different values of the bonding inductance to the photodiode.



a. V_{DD} = 5.4 V.



b. V_{DD} = 6.0 V.

R_s = 8 Ω; C_p = 0.22 pF; L_b = 0.6 nH.

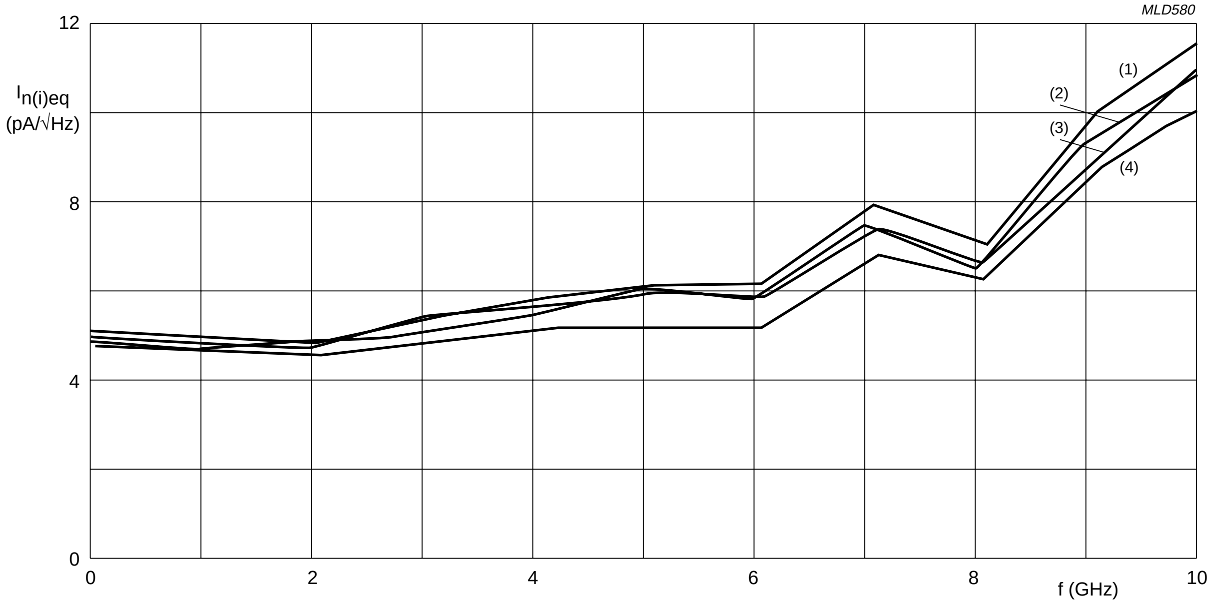
(1) T_{amb} = 25 °C.

(2) T_{amb} = 50 °C.

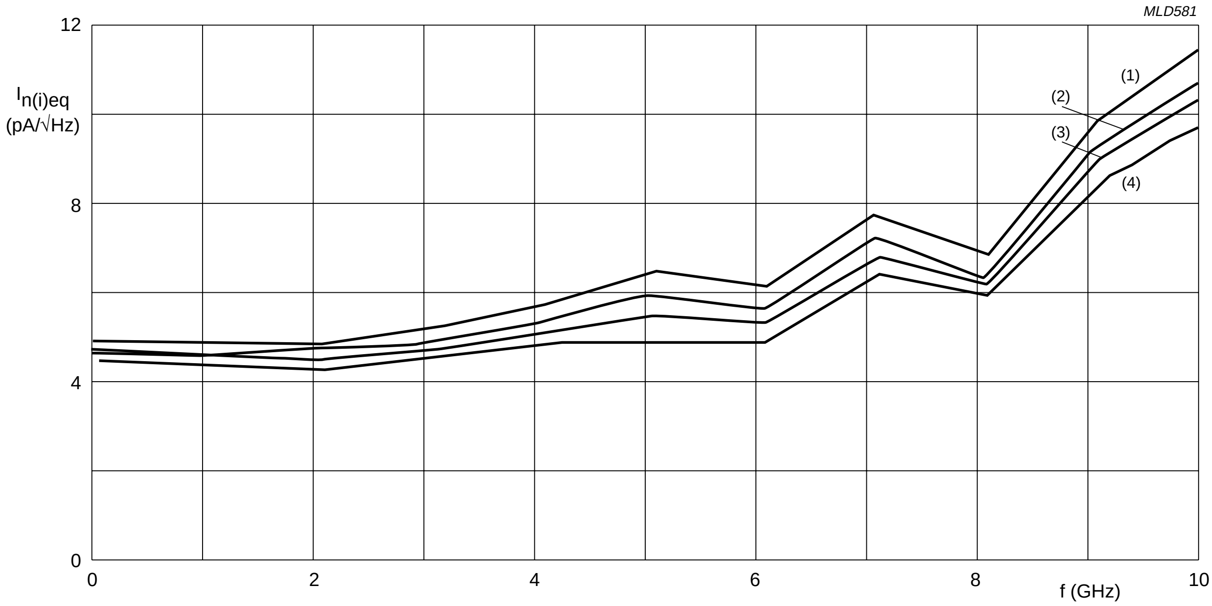
(3) T_{amb} = 75 °C.

(4) T_{amb} = 100 °C.

Fig.10 Transimpedance gain ripple as a function of the frequency with different values of the operating temperature.



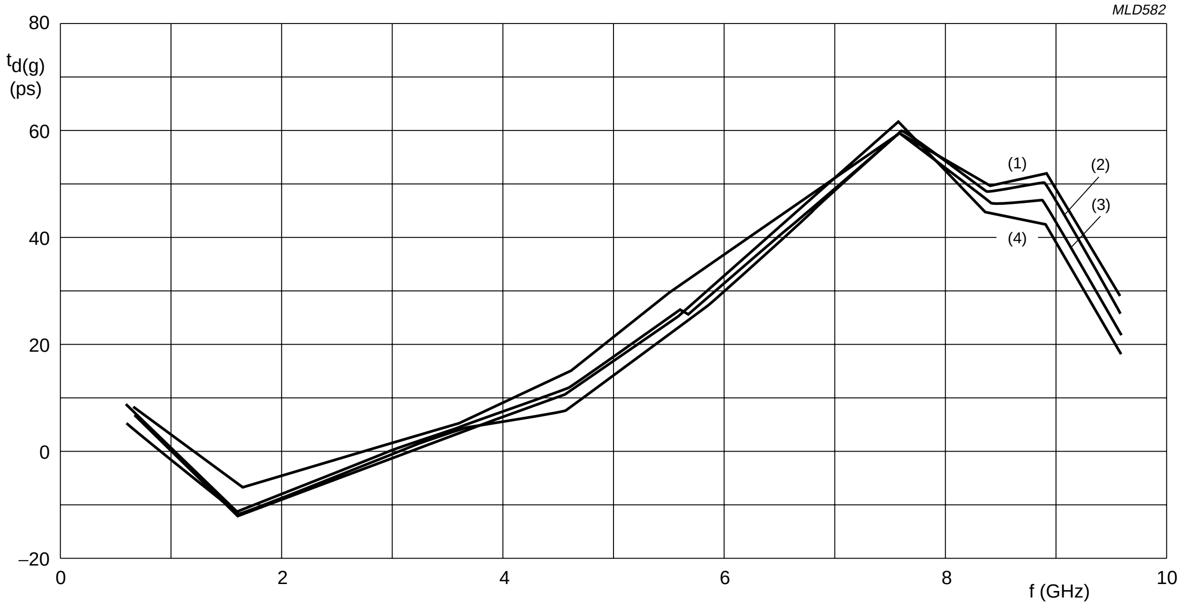
a. V_{DD} = 5.4 V.



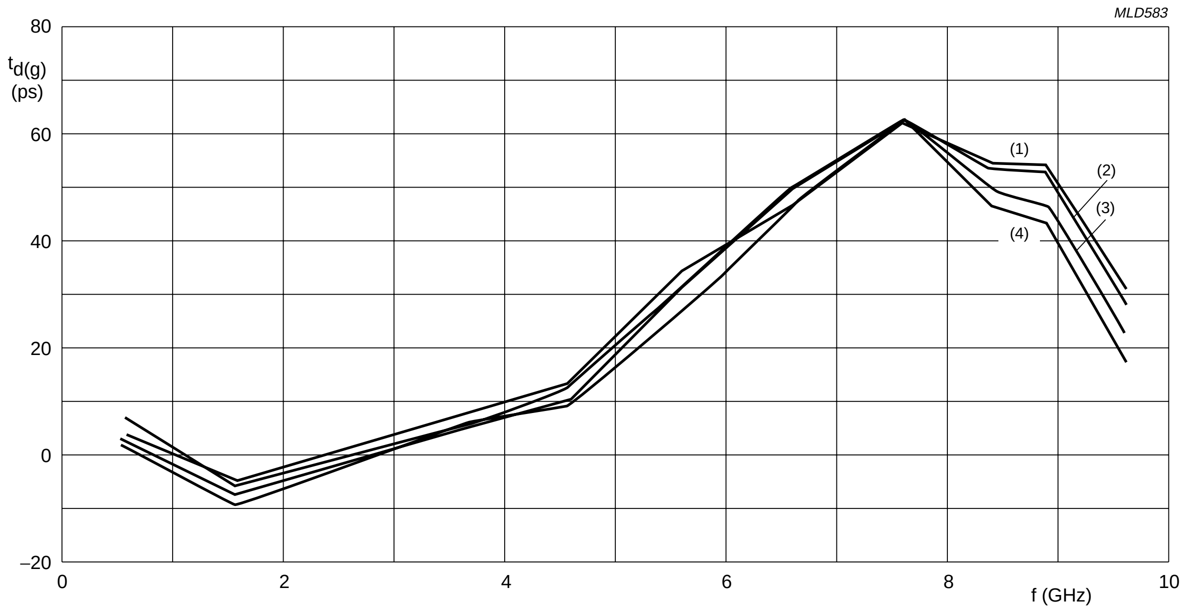
b. V_{DD} = 6.0 V.

R_s = 8 Ω; C_p = 0.22 pF; L_b = 0.6 nH.
(1) T_{amb} = 100 °C.
(2) T_{amb} = 75 °C.
(3) T_{amb} = 50 °C.
(4) T_{amb} = 25 °C.

Fig.11 Equivalent input noise current density as a function of the frequency with different values of the operating temperature.



a. V_{DD} = 5.4 V.



b. V_{DD} = 6.0 V.

R_s = 8 Ω; C_p = 0.22 pF; L_b = 0.6 nH.

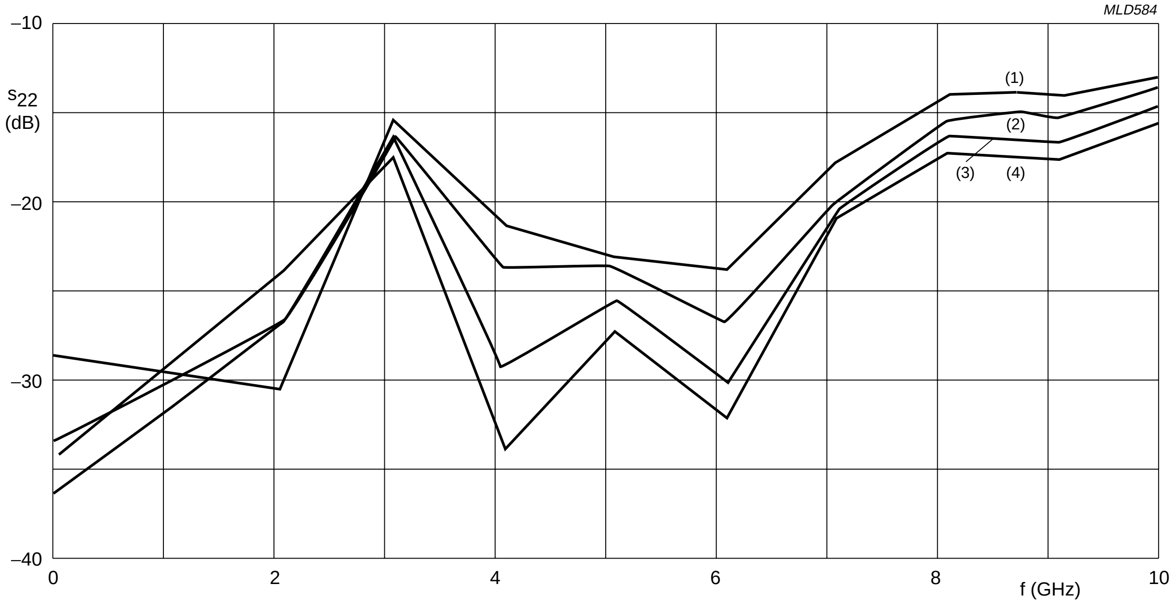
(1) T_{amb} = 25 °C.

(2) T_{amb} = 50 °C.

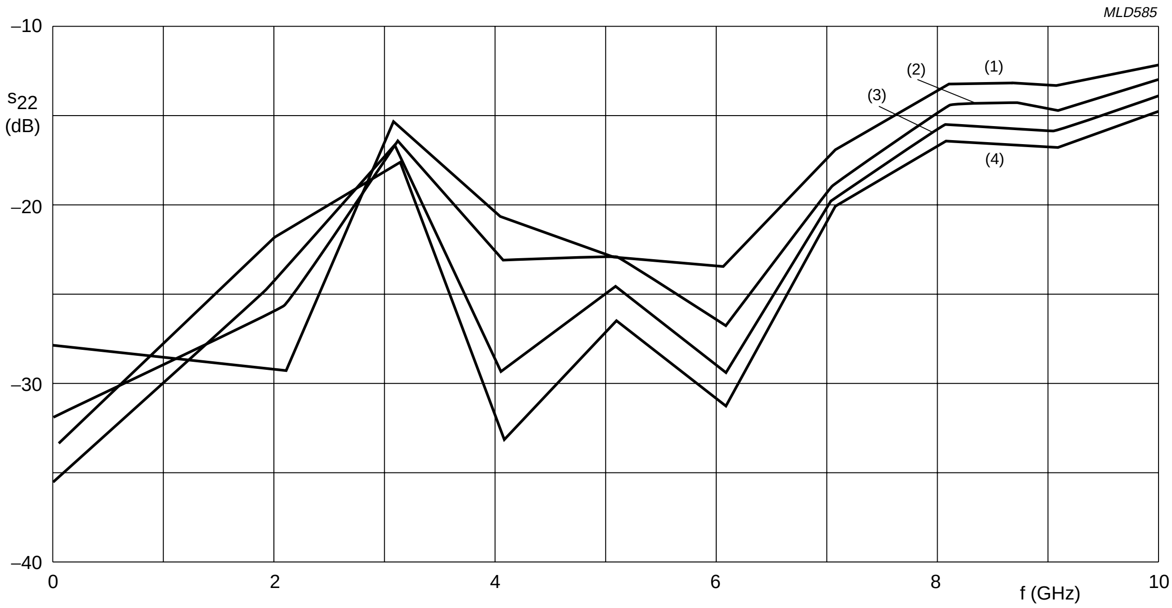
(3) T_{amb} = 75 °C.

(4) T_{amb} = 100 °C.

Fig.12 Group delay (relative to f = 2.5 GHz) as a function of the frequency with different values of the operating temperature.



a. V_{DD} = 5.4 V.



b. V_{DD} = 6.0 V.

R_s = 8 Ω; C_p = 0.22 pF; L_b = 0.6 nH.

(1) T_{amb} = 100 °C.

(2) T_{amb} = 75 °C.

(3) T_{amb} = 50 °C.

(4) T_{amb} = 25 °C.

Fig.13 Output reflection coefficient as a function of the frequency with different values of the operating temperature.

s-parameter data

The s-parameters of the CGY2110CU die are measured on-wafer using 40 GHz bandwidth probes.

Port 1 is the input (INA), while port 2 is the output (OUTP). For these measurements pad OUTN is connected to a 50 Ω load via a DC blocking capacitor.

Measurement data from a typical CGY2110CU chip are shown in Tables 1 and 2.

Table 1 Measured s-parameters of the CGY2110CU at V_{DD} = 5.4 V
Test conditions: R_L = 50 Ω; T_{amb} = 25 °C; magnitude is given in dB and phase is given in degrees.

FREQUENCY (GHz)	$\lvert s_{11}\rvert$	Φs_{11}	$\lvert s_{12}\rvert$	Φs_{12}	$\lvert s_{21}\rvert$	Φs_{21}	$\lvert s_{22}\rvert$	Φs_{22}
0.1	–5.04	–1.17	–72.3	–3	+25.87	–1.5	–53	+152
1.1	–6.02	–11.8	–66.0	–112	+27.44	–19.7	–15.1	+47.2
2.1	–7.38	–15.9	–69.2	+176	+29.21	–49.3	–23.2	–35.6
3.1	–9.32	–16.6	–62.5	–35	+30.48	–84.8	–18.3	–3.37
4.1	–11.1	–7.0	–64.2	–165	+31.29	–124	–22.8	–65
5.1	–12	+9.0	–71.4	+137	+31.77	–164	–27.4	–66.9
6.1	–10.6	+24.7	–82.5	–115	+31.65	+156	–35.4	–178
7.1	–9.19	+31.9	–68.1	–129	+31.32	+112	–21.8	+136
8.1	–7.7	+35.1	–66.8	+179	+30.14	+64.3	–14.4	+72.1
8.7	–6.86	+35.7	–67.0	–158	+28.84	+37.6	–14.7	+44.0
9.1	–6.45	+35.0	–62.8	–162	+27.58	+20.2	–17.0	+31.4
10.1	–5.08	+34.5	–59.4	–173	+24.52	–15.4	–13.4	+40.3

Table 2 Measured s-parameters of the CGY2110CU at V_{DD} = 6.0 V
Test conditions: R_L = 50 Ω; T_{amb} = 25 °C; magnitude is given in dB and phase is given in degrees.

FREQUENCY (GHz)	$\lvert s_{11}\rvert$	Φs_{11}	$\lvert s_{12}\rvert$	Φs_{12}	$\lvert s_{21}\rvert$	Φs_{21}	$\lvert s_{22}\rvert$	Φs_{22}
0.1	–5.57	–0.78	–79.5	+103	+27.17	–1.5	–61.2	+107
1.1	–6.54	–10.5	–65.9	–99	+28.65	–20.1	–14.4	+48.3
2.1	–7.84	–14.1	–69.6	+138	+30.24	–49.4	–24.1	–46.2
3.1	–9.52	–11.9	–62.3	–28	+31.44	–83.6	–17.7	+1.8
4.1	–11	–3.46	–63.8	–167	+32.27	–121	–22.1	–62.7
5.1	–11.7	+13	–69.9	+145	+32.89	–160	–25.6	–65.2
6.1	–10.2	+25.9	–78.7	–154	+32.90	+161	–32.9	–163
7.1	–8.85	+31.2	–70.2	–138	+32.89	+119	–20.9	+145
8.1	–7.51	+33.8	–68.5	–173	+32.23	+70.7	–13.2	+80.3
8.7	–6.77	+34.2	–67.8	–161	+31.08	+42.4	–13.5	+50.4
9.1	–6.29	+34.1	–61.8	–165	+29.82	+24.0	–16.1	+36.7
10.1	–5.01	+33.7	–60.1	–177	+26.71	–13.2	–11.9	+46.2

BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES(1)	
		x	y
ST	1	110	540
INA	2	110	390
INC	3	110	240
VPIN	4	240	110
VS	5	390	110
VREF	6	540	110
VD	7	690	110
VD3	8	840	110
SP	9	1035	110
OUTP	10	1090	265
S	11	1090	390
OUTN	12	1090	515
SN	13	1090	660

Note

1. All x and y coordinates in µm represent the position of the centre of the pad with respect to the left bottom corner (see Fig.14).

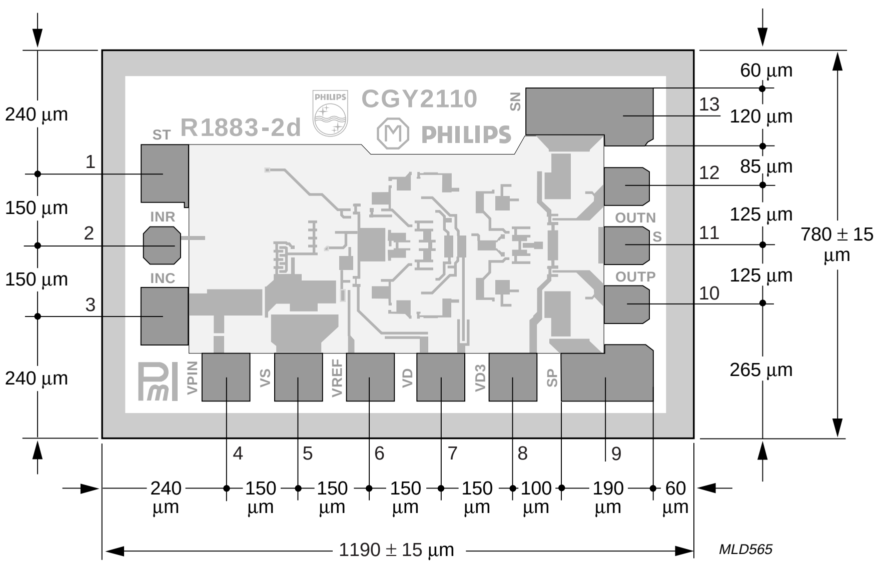


Fig.14 Bonding pad locations.

Table 3 Physical characteristics of bare die

PARAMETER	VALUE
Size	1190 ± 15 µm × 780 ± 15 µm
Thickness	200 µm
Backside material	TiAu
Glass passivation	SiN
Bonding pad dimensions	
VPIN, VS, VREF, VD and VD3	100 × 100 µm
SP	190 × 100 µm
OUTP, OUTN and S	100 × 80 µm
SN	270 × 100 µm
ST and INC	100 × 120 µm
INA	80 × 80 µm
Attach temperature	<135 °C
Attach time	<15 s

DATA SHEET STATUS

DATA SHEET STATUS[(1)]	PRODUCT STATUS[(2)]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Bare die — All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of Philips' delivery. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post packing tests performed on individual die or wafer. Philips Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA73

Printed in The Netherlands 403510/01/pp20 Date of release: 2001 Dec 07 Document order number: 9397 750 07776

Let's make things better.

Philips Semiconductors

PHILIPS