PM4318

OCTLIU

OCTAL E1/T1/J1 LINE INTERFACE DEVICE

DATASHEET

PROPRIETARY AND CONFIDENTIAL

PRELIMINARY

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1 FEATURES

- Monolithic device which integrates eight T1/J1 or E1 short haul and long haul line interface circuits.
- Software switchable between T1/J1 and E1 operation on a per-device basis.
- Meets or exceeds T1/J1 and E1 shorthaul and longhaul network access specifications including ANSI T1.102, T1.403, T1.408, AT&T TR 62411, ITU-T G.703, G.704 as well as ETSI 300-011, CTR-4, CTR-12 and CTR-13.
- Provides encoding and decoding of B8ZS, HDB3 and AMI line codes.
- Provides receive equalization, clock recovery and line performance monitoring.
- Provides transmit and receive jitter attenuation.
- Provides digitally programmable long haul and short haul line build out.
- Provides a selectable, per channel independent de-jittered T1 or E1 recovered clock for system timing and redundancy.
- Provides PRBS generators and detectors on each tributary for error testing at DS1 and E1 rates as recommended in ITU-T O.151.
- Provides either serial clock/data or parallel Scaleable Bandwidth Interconnect (SBI) interfaces on the system side.
- Can be configured to act as a converter between the SBI interfaces and serial clock/data. In this mode, the LIUs are unused.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Provides a hardware-only (no microprocessor) mode in which configuration data is read from an SPI-compatible serial PROM. The PROM interface can be cascaded such that multiple OCTLIU devices can be configured simultaneously from a single PROM.
- Uses line rate system clock.
- Provides an IEEE 1149.1 (JTAG) compliant Test Access Port (TAP) and controller for boundary scan test.
- Implemented in a low power 3.3 V tolerant 1.8/3.3 V CMOS technology.
- Available in a high density 288-pin Tape-SBGA (23 mm by 23 mm) package.
- Provides a –40°C to +85°C Industrial temperature operating range.

1.1 Each Receiver Section:

- Supports T1 signal reception for distances with up to 36 dB of cable attenuation at nominal conditions using PIC 22 gauge cable emulation.
- Supports E1 signal reception for distances with up to 36 dB of cable attenuation at nominal conditions using PIC 22 gauge cable emulation.
- Supports G.772 compliant non-intrusive protected monitoring points.
- Recovers clock and data using a digital phase locked loop for high jitter tolerance.
- Tolerates more than 0.3 UI peak-to-peak; high frequency jitter as required by AT&T TR 62411 and Bellcore TR-TSY-000170.
- Outputs either dual rail recovered line pulses, a single rail DS-1/E1 signal or parallel data in SBI bus format.
- Performs B8ZS or AMI decoding when processing a bipolar DS-1 signal and HDB3 or AMI decoding when processing a bipolar E1 signal.
- Detects line code violations (LCVs), B8ZS/HDB3 line code signatures, and 4 (E1+HDB3), 8 (T1+B8ZS) or 16 (AMI) successive zeros.
- Accumulates up to 8191 line code violations (LCVs), for performance monitoring purposes, over accumulation intervals defined by the period between software write accesses to the LCV register.
- Detects loss of signal (LOS), which is defined as 10, 15, 31, 63, or 175 successive zeros.
- Detects programmable inband loopback activate and deactivate code sequences received in the DS-1 data stream when they are present for 5.1 seconds. Optionally, enters loopback mode automatically on detection of an inband loopback code.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window.
- A pseudo-random sequence user selectable from $2^{11}-1$, $2^{15}-1$ or $2^{20}-1$, may be detected in the T1/E1 stream in either the receive or transmit directions. The detector counts pattern errors using a 24-bit saturating PRBS error counter.

1.2 Each Transmitter Section:

- Supports transfer of transmitted single rail PCM and signaling data from 1.544 Mbit/s and 2.048 Mbit/s backplane buses.
- Generates DSX-1 shorthaul and DS-1 longhaul pulses with programmable pulse shape compatible with AT&T, ANSI and ITU requirements.
- Generates E1 pulses compliant to G.703 recommendations.

- Provides a digitally programmable pulse shape extending up to 5 transmitted bit periods for custom long haul pulse shaping applications.
- Provides line outputs that are current limited and may be tristated for protection or in redundant applications.
- Provides a digital phase locked loop for generation of a low jitter transmit clock complying with all jitter attenuation, jitter transfer and residual jitter specifications of AT&T TR 62411 and ETSI TBR 12 and TBR 13.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.
- Allows bipolar violation (BPV) transparent operation for error restoring regenerator applications.
- Allows bipolar violation (BPV) insertion for diagnostic testing purposes.
- Supports all ones transmission for alarm indication signal (AIS) generation.
- Accepts either dual rail or single rail DS-1/E1 signals or parallel data from the SBI interface.
- Performs B8ZS or AMI encoding when processing a single rail or SBI-sourced DS-1 signal and HDB3 or AMI encoding when processing a single rail or SBI-sourced E1 signal.
- A pseudo-random sequence user selectable from $2^{11}-1$, $2^{15}-1$ or $2^{20}-1$, may be inserted into or detected from the T1 or E1 stream in either the receive or transmit directions.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window and optionally stuffs ones to maintain minimum ones density.
- Supports transmission of a programmable unframed inband loopback code sequence.

2 APPLICATIONS

- Metro Optical Access Equipment
- Edge Router Linecards
- Multiservice ATM Switch Linecards
- 3G Base Station Controllers (BSC)
- 3G Base Transceiver Stations (BTS)
- Digital Private Branch Exchanges (PBX)
- Digital Access Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSX)
- T1/E1 Repeaters
- Test Equipment
- SBI to clk/data converter in multi-service access equipment.

3 REFERENCES

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26. TTC Standard JT-G704 – Frame Structures on Primary and Secondary Hierarchical Digital Interfaces, 1995.
27. TTC Standard JT-I431 – ISDN Primary Rate User-Network Interface Layer 1 – Specification, 1995.
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4 APPLICATION EXAMPLES

Figure 1 – T1/E1 Framer/Transceiver Application

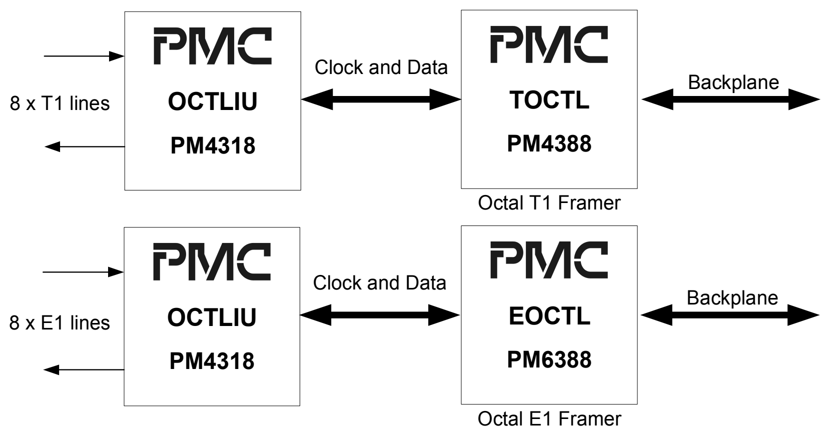


Figure 2 – High Density T1/E1 Framer/Transceiver Application

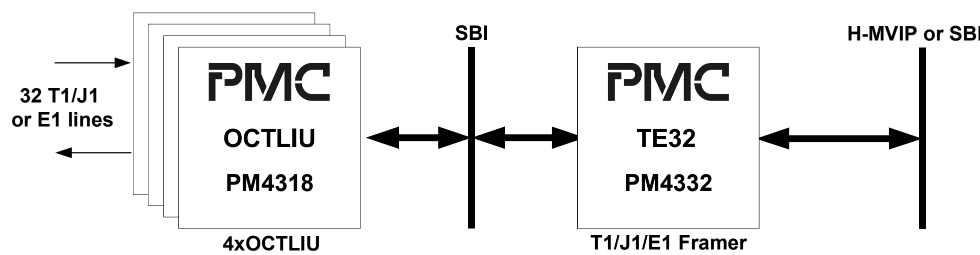


Figure 3 – High Density Leased Line Circuit Emulation Application

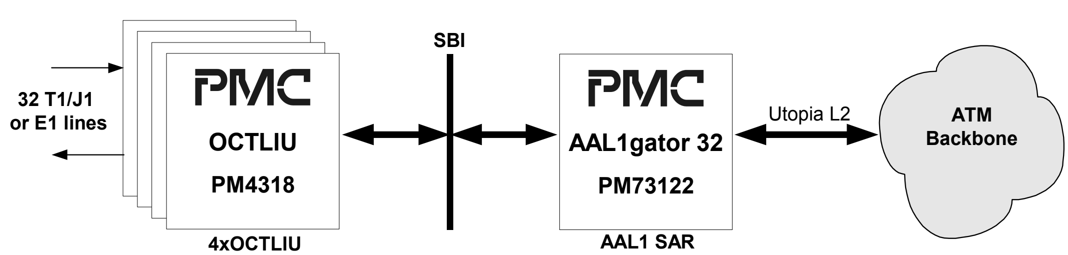
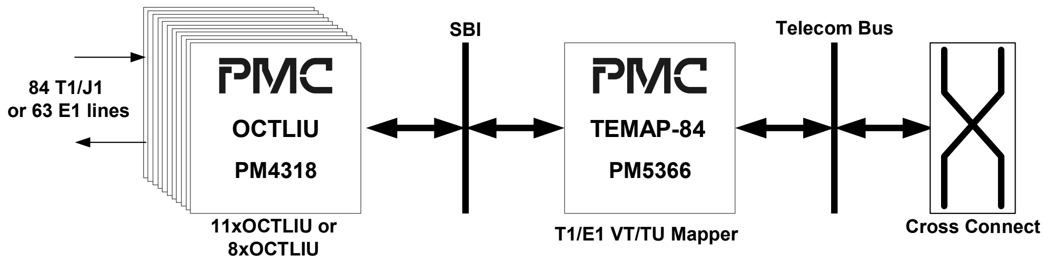


Figure 4 – Metro Optical Access Equipment



5 BLOCK DIAGRAM

Figure 5 – OCTLIU Block Diagram – LIUs Enabled

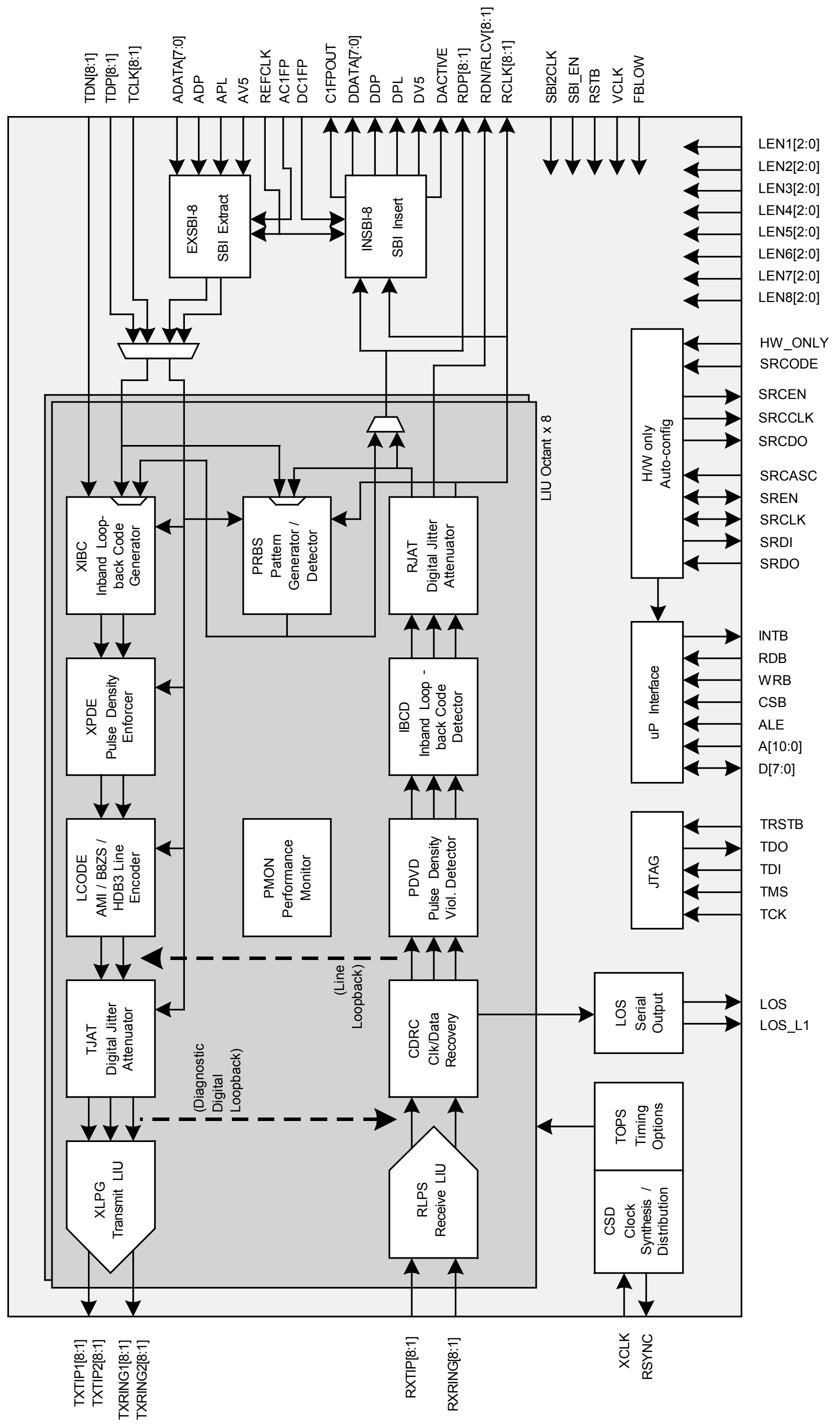
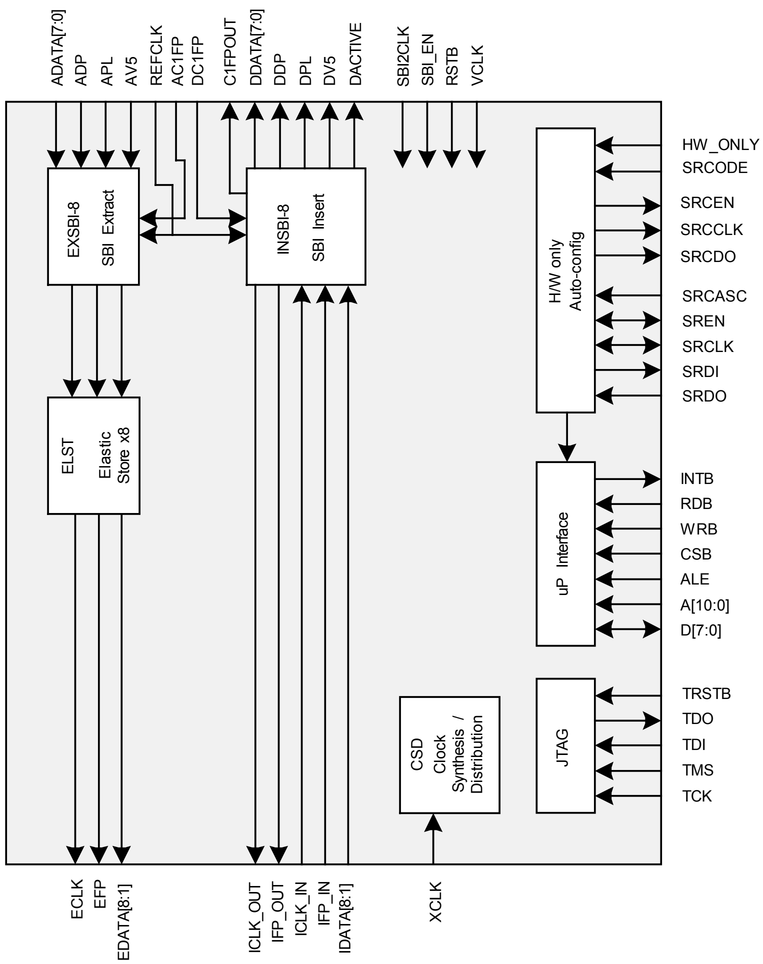


Figure 6 – OCTLIU Block Diagram – SBI to Clk/Data Converter, LIUs Disabled



6 DESCRIPTION

The PM4318 Octal E1/T1/J1 Line Interface Device (OCTLIU) is a monolithic integrated circuit suitable for use in long haul and short haul T1, J1 and E1 systems with a minimum of external circuitry. The OCTLIU is configurable via microprocessor control or SPI-compatible serial PROM interface, allowing feature selection without changes to external wiring.

Analogue circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 36 dB cable loss (at 1.024 MHz) in E1 mode or up to 36 dB cable loss (at 772 kHz) in T1 mode using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required.

The OCTLIU recovers clock and data from the line. Decoding of AMI, HDB3 and B8ZS line codes is supported. In T1 mode, the OCTLIU also detects the presence of in-band loop back codes.

The OCTLIU supports detection of loss of signal, pulse density violation and line code violation alarm conditions. Line code violations are accumulated for performance monitoring purposes.

Internal analogue circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and an optional line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for LBO filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements.

Each channel of the OCTLIU can generate a low jitter transmit clock from the input clock source and also provide jitter attenuation in the receive path. A low jitter recovered T1 clock can be routed outside the OCTLIU for network timing applications.

Serial PCM interfaces to each T1/E1 LIU allow 1.544 Mbit/s or 2.048 Mbit/s backplane receive/backplane transmit system interfaces to be directly supported. Data may be transferred either as dual rail line pulses or single rail DS-1/E1 data. Alternatively, the OCTLIU supports an 8-bit parallel SBI interface for interfacing to high-density framers.

The OCTLIU may be configured to operate in a mode in which the LIUs are disabled and the device acts as a converter between the SBI interface and serial clock and data. Up to 8 serial data streams (sharing a common clock and frame pulse) may be mapped on to the SBI bus in this mode.

The OCTLIU may be configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. Alternatively, the device may be operated in a ‘hardware only’ mode in which no microprocessor is required. In this case, the OCTLIU reads configuration information from an SPI-compatible serial PROM interface on power up. Multiple OCTLIUs can be configured from a single serial PROM via a cascade interface on the OCTLIU.

7 PIN DIAGRAM

The OCTLIU is packaged in a 288-pin Tape-SBGA package having a body size of 23mm by 23mm.

Figure 7 – Pin Diagram

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	ALE/ LEN4[2]	VSS	D[1]/ LEN6[2]	D[2]/ LEN7[0]	D[4]/ LEN7[2]	VSS	VDD1V8	TAVS2[1]	TXRING2 [1]	TXRING1 [1]	TXTIP1[1]	TXTIP2[1]	TXTIP2 [8]	TXTIP1 [8]	TXRING1 [8]	TXRING2 [8]	RSTB	LOS	SRCCLK	SRCLK	VDD3V3	TDI	A
B	VDD3V3	VDD3V3	CSB/ LEN5[2]	D[0]/ LEN6[1]	D[3]/ LEN7[1]	D[6]/ LEN8[1]	SBI_EN	QAVS[4]	RES[5]	TAVD3[1]	TAVS3[8]	TAVD2[8]	QAVD[4]	VDD1V8	VDD3V3	RES[1]	RES[6]	SRCDO	SRDO	SRCASC	TDO	HW_ONLY	B
C	A[8]/ LEN3[2]	A[9]/ LEN4[0]	A[10]/ LEN4[1]	RDB/ LEN5[1]	VDD3V3	VDD3V3	VSS	D[7]/ LEN8[2]	CAVD	TAVD2[1]	TAVS3[1]	TAVD3[8]	TAVS2[8]	VSS	VSS	LOS_L1	SRCODE	SRCEN	SREN	VSS	TCK	SBI2CLK	C
D	A[4]/ LEN2[1]	A[5]/ LEN2[2]	A[6]/ LEN3[0]	VSS	WRB/ LEN5[0]	INTB/ LEN6[0]	VSS	D[5]/ LEN8[0]	CAVS	TAVS1[1]	TAVD1[1]	TAVD1[8]	TAVS1[8]	XCLK	RSYNC/ ICLK_OUT	VDD3V3	SRDI	VSS	NC	TMS	VDD3V3	RAVS1[8]	D
E	A[0]/ LEN1[0]	A[1]/ LEN1[1]	A[2]/ LEN1[2]	A[7]/ LEN3[1]															TRSTB	VSS	RAVD2[8]	RAVD2[7]	E
F	RAVS1[1]	RAVD2[1]	QAVD[1]	A[3]/ LEN2[0]															QAVS[3]	RES[4]	RAVS2[7]	TXRING2 [7]	F
G	RAVD1[1]	RXTIP[1]	RAVS2[1]	VDD3V3															RAVS2[8]	RXTIP[8]	RAVS1[7]	TXRING1 [7]	G
H	TXRING2 [2]	RAVD2[2]	RAVS2[2]	RXRING[1]															RXRING [8]	RAVD1[8]	RAVD1[7]	TXTIP1 [7]	H
J	TXRING1 [2]	RXTIP[2]	RAVS1[2]	RXRING [2]															RXRING [7]	RXTIP[7]	TAVS2[7]	TXTIP2 [7]	J
K	TXTIP1[2]	RAVD1[2]	TAVS2[2]	TAVS1[2]															TAVS1[7]	TAVD2[7]	TAVD3[7]	TXTIP2 [6]	K
L	TXTIP2 [2]	TAVD2[2]	TAVD3[2]	TAVD1[2]						Bottom View									TAVD1[7]	TAVS3[7]	TAVS3[6]	TXTIP1[6]	L
M	TXTIP2 [3]	TAVS3[2]	TAVS3[3]	TAVD1[3]															TAVD1[6]	TAVD3[6]	TAVD2[6]	TXRING1 [6]	M
N	TXTIP1 [3]	TAVD3[3]	TAVD2[3]	TAVS1[3]															TAVS1[6]	TAVS2[6]	RAVD1[6]	TXRING2 [6]	N
P	TXRING1 [3]	TAVS2[3]	RAVD1[3]	RXRING [3]															RXRING [6]	RAVS1[6]	RAVD2[6]	RXTIP[6]	P
R	TXRING2 [3]	RXTIP[3]	RAVD2[3]	RXTIP[4]															RXTIP[5]	RXRING [5]	RAVD1[5]	RAVS2[6]	R
T	RAVS1[3]	RAVS2[3]	RAVD1[4]	RAVS2[4]															QAVD[3]	RAVS2[5]	RAVD2[5]	RAVS1[5]	T
U	RXRING [4]	RAVS1[4]	RAVD2[4]	TCLK[1]/ IDATA[1]															TCLK[7]/ IDATA[7]	TDN[8]/ IFP_IN	TDP[8]/ ADATA[7]	VSS	U
V	RES[1]	QAVS[1]	VSS	TDP[2]/ ADATA[1]															TDN[6]/ AV5	TCLK[6]/ IDATA[6]	TDN[7]/ ICLK_IN	TCLK[8]/ IDATA[8]	V
W	TDP[1]/ ADATA[0]	TDN[1]/ REFCLK	TCLK[2]/ IDATA[2]	VDD3V3	TDN[4]/ ADP	VDD3V3	VDD3V3	RDN[3]/ RLCV[3]/ C1FPOUT	VSS	TAVS1[4]	TAVD1[4]	TAVD1[5]	TAVS1[5]	VDD1V8	RDP[5]/ DDATA[4]	RCLK[6]/ EDATA[6]	RCLK[7]/ EDATA[7]	RDP[8]/ DDATA[7]	NC	VDD3V3	TCLK[5]/ IDATA[5]	TDP[7]/ ADATA[6]	W
Y	TDN[2]/ AC1FP	TDP[3]/ ADATA[2]	VDD3V3	TDP[4]/ ADATA[3]	VSS	RDP[2]/ DDATA[1]	RCLK[3]/ EDATA[3]	VDD3V3	RDN[4]/ RLCV[4]/ DDP	TAVS2[4]	TAVD3[4]	TAVS3[5]	TAVD2[5]	RES[3]	RDN[5]/ RLCV[5]/ DPL	VDD3V3	VSS	RDP[7]/ DDATA[6]	RDN[8]/ RLCV[8]/ DACTIVE	VSS	TDP[5]/ ADATA[4]	TDP[6]/ ADATA[5]	Y
AA	TCLK[3]/ IDATA[3]	TDN[3]/ DC1FP	TCLK[4]/ IDATA[4]	RCLK[1]/ EDATA[1]	RCLK[2]/ EDATA[2]	VSS	VSS	RCLK[4]/ EDATA[4]	VDD1V8	QAVD[2]	TAVD2[4]	TAVS3[4]	TAVD3[5]	TAVS2[5]	QAVS[2]	VSS	VSS	RDP[6]/ DDATA[5]	RDN[7]/ RLCV[7]/ ECLK	VDD3V3	VSS	TDN[5]/ APL	AA
AB	VSS	VSS	VSS	RDP[1]/ DDATA[0]	RDN[1]/ RLCV[1]/ IFP_OUT	RDN[2]/ RLCV[2]/ EFP	RDP[3]/ DDATA[2]	RDP[4]/ DDATA[3]	TXRING2 [4]	TXRING1 [4]	TXTIP1[4]	TXTIP2 [4]	TXTIP2 [5]	TXTIP1[5]	TXRING1 [5]	TXRING2 [5]	RCLK[5]/ EDATA[5]	RDN[6]/ RLCV[6]/ DV5	VDD3V3	VSS	RCLK[8]/ EDATA[8]	VDD3V3	AB
	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

8 PIN DESCRIPTION

By convention, where a bus of eight pins indexed [8:1] is present, the index indicates to which octant the pin applies. With TCLK[8:1], for example, TCLK[1] applies to octant #1, TCLK[2] applies to octant #2, etc.

Pin Name	Type	Pin No.	Function
T1 and E1 System Side Serial Clock and Data Interface			
TCLK[1]/IDATA[1] TCLK[2]/IDATA[2] TCLK[3]/IDATA[3] TCLK[4]/IDATA[4] TCLK[5]/IDATA[5] TCLK[6]/IDATA[6] TCLK[7]/IDATA[7] TCLK[8]/IDATA[8]	Input	U19 W20 AA22 AA20 W2 V3 U4 V1	The Transmit Clock inputs (TCLK[8:1]) should be 1.544 MHz for DS1 or 2.048 MHz for E1 data streams and are used to sample the corresponding TDP[8:1] and TDN[8:1] signals. TCLK[8:1] share the same pins as the IDATA[8:1] inputs. TCLK[8:1] are selected when SBI2CLK is tied low.
TDP[1]/ADATA[0] TDP[2]/ADATA[1] TDP[3]/ADATA[2] TDP[4]/ADATA[3] TDP[5]/ADATA[4] TDP[6]/ADATA[5] TDP[7]/ADATA[6] TDP[8]/ADATA[7]	Input	W22 V19 Y21 Y19 Y2 Y1 W1 U2	Transmit Positive Data (TDP[8:1]). When in single-rail mode, these inputs are the NRZ data signals to be transmitted. These inputs can be configured to be active high or active low. When in dual-rail mode, these inputs are the NRZ positive data signals to be transmitted. TDP[8:1] can be sampled on either the rising or falling edges of the corresponding TCLK[8:1]. TDP[8:1] share the same pins as the ADATA[7:0] inputs. TDP[8:1] are selected when SBI_EN and SBI2CLK are both tied low.
TDN[1]/REFCLK TDN[2]/AC1FP TDN[3]/DC1FP TDN[4]/ADP TDN[5]/APL TDN[6]/AV5 TDN[7]/ICLK_IN TDN[8]/IFP_IN	Input	W21 Y22 AA21 W18 AA1 V4 V2 U3	Transmit Negative Data (TDN[8:1]). When in dual-rail mode, these inputs are the NRZ negative data signals to be transmitted. These inputs can be sampled on either the rising or falling edges of the corresponding TCLK[8:1]. These input pins are ignored if the device is configured for single-rail (unipolar) transmit mode. TDN[8:1] share the same pins as the REFCLK, AC1FP, DC1FP, ADP, APL, AV5, ICLK_IN and IFP_IN inputs. TDN[8:1] are selected when SBI_EN and SBI2CLK are both tied low.

Pin Name	Type	Pin No.	Function
RCLK[1]/EDATA[1] RCLK[2]/EDATA[2] RCLK[3]/EDATA[3] RCLK[4]/EDATA[4] RCLK[5]/EDATA[5] RCLK[6]/EDATA[6] RCLK[7]/EDATA[7] RCLK[8]/EDATA[8]	Output	AA19 AA18 Y16 AA15 AB6 W7 W6 AB2	Recovered Clock Output (RCLK[8:1]). RCLK[8:1] is the clock recovered from the RXTIP[8:1] and RXRING[8:1] input signals. RCLK[8:1] share the same pins as the EDATA[8:1] outputs. RCLK[8:1] are selected when SBI2CLK is tied low.
RDP[1]/DDATA[0] RDP[2]/DDATA[1] RDP[3]/DDATA[2] RDP[4]/DDATA[3] RDP[5]/DDATA[4] RDP[6]/DDATA[5] RDP[7]/DDATA[6] RDP[8]/DDATA[7]	Output	AB19 Y17 AB16 AB15 W8 AA5 Y5 W5	Receive Digital Positive Data (RDP[8:1]). When in single rail mode, RDP[8:1] output NRZ sampled DS-1 or E1 data which has been decoded by AMI, B8ZS, or HDB3 line code rules. When in dual rail mode, RDP[8:1] output NRZ sampled bipolar positive pulses. RDP[8:1] can be updated on either the falling or rising RCLK[8:1] edge. RDP[8:1] share the same pins as the DDATA[7:0] outputs. RDP[8:1] are selected when SBI_EN and SBI2CLK are both tied low.
RDN/RLCV[1]/IFP_OUT RDN/RLCV[2]/EFP RDN/RLCV[3]/C1FPOUT RDN/RLCV[4]/DDP RDN/RLCV[5]/DPL RDN/RLCV[6]/DV5 RDN/RLCV[7]/ECLK RDN/RLCV[8]/DACTIVE	Output	AB18 AB17 W15 Y14 Y8 AB5 AA4 Y4	Receive Digital Negative Data/Line Code Violation Indication (RDN/RLCV[8:1]). When in dual rail mode, RDN/RLCV[8:1] output NRZ sampled bipolar negative pulses. When in single rail mode, RDN/RLCV[8:1] output a NRZ pulse whenever a line code violation or excess zeros condition is detected. RDN/RLCV[8:1] can be updated on either the falling or rising RCLK[8:1] edge. RDN/RLCV[8:1] share the same pins as the IFP_OUT, EFP, C1FPOUT, DDP, DPL, DV5, ECLK and DACTIVE outputs. RDN/RLCV[8:1] are selected when SBI_EN and SBI2CLK are both tied low.
SBI System Side Interface			
REFCLK/TDN[1]	Input	W21	The SBI reference clock signal (REFCLK) provides reference timing for the SBI ADD and DROP busses. REFCLK is nominally a 50% duty cycle clock of frequency 19.44 MHz ±50ppm. REFCLK shares the same pin as the TDN[1] input. REFCLK is selected when SBI_EN or SBI2CLK is tied high.

Pin Name	Type	Pin No.	Function
AC1FP/TDN[2]	Input	Y22	The SBI ADD bus C1 octet frame pulse signal (AC1FP) provides frame synchronisation for devices connected via an SBI interface. AC1FP must be asserted for 1 REFCLK cycle every 500 μs or multiples thereof (i.e. every 9720 n REFCLK cycles, where n is a positive integer). All devices connected to the SBI ADD bus must be synchronised to a AC1FP signal from a single source. AC1FP is sampled on the rising edge of REFCLK. AC1FP shares the same pin as the TDN[2] input. AC1FP is selected when SBI_EN or SBI2CLK is tied high.
DC1FP/TDN[3]	Input	AA21	The SBI DROP bus C1 octet frame pulse signal (DC1FP) provides frame synchronisation for devices connected via an SBI interface. DC1FP must be asserted for 1 REFCLK cycle every 500 μs or multiples thereof (i.e. every 9720 n REFCLK cycles, where n is a positive integer). All devices connected to the SBI DROP bus must be synchronised to a DC1FP signal from a single source. DC1FP is sampled on the rising edge of REFCLK. DC1FP shares the same pin as the TDN[3] input. DC1FP is selected when SBI_EN or SBI2CLK is tied high.
C1FPOUT/RDN/RLCV[3]	Output	W15	The C1 octet frame pulse output signal (C1FPOUT) may be used to provide frame synchronisation for devices interconnected via an SBI interface. C1FPOUT is asserted for 1 REFCLK cycle every 500 μs (i.e. every 9720 REFCLK cycles). If C1FPOUT is used for synchronisation, it must be connected to the A/DC1FP inputs of all the devices connected to the SBI ADD or DROP bus. C1FPOUT is updated on the rising edge of REFCLK. C1FPOUT shares the same pin as the RDN/RLCV[3] output. C1FPOUT is selected when SBI_EN or SBI2CLK is tied high.
ADATA[0]/TDP[1] ADATA[1]/TDP[2] ADATA[2]/TDP[3] ADATA[3]/TDP[4] ADATA[4]/TDP[5] ADATA[5]/TDP[6] ADATA[6]/TDP[7] ADATA[7]/TDP[8]	Input	W22 V19 Y21 Y19 Y2 Y1 W1 U2	The SBI ADD bus data signals (ADATA[7:0]) contain time division multiplexed transmit data from up to 84 independently timed links. Link data is transported as T1 or E1 tributaries within the SBI TDM bus structure. The OCTLIU may be configured to extract data from up to 8 tributaries within the structure. ADATA[7:0] are sampled on the rising edge of REFCLK. ADATA[7:0] share the same pins as the TDP[8:1] inputs. ADATA[7:0] are selected when SBI_EN or SBI2CLK is tied high.

Pin Name	Type	Pin No.	Function
ADP/TDN[4]	Input	W18	The SBI ADD bus parity signal (ADP) carries the even or odd parity for the ADD bus signals. The parity calculation encompasses the ADATA[7:0], APL and AV5 signals. Multiple devices can drive the SBI ADD bus at uniquely assigned tributary column positions. This parity signal is intended to detect accidental driver clashes in the column assignment. ADP is sampled on the rising edge of REFCLK. ADP shares the same pin as the TDN[4] input. ADP is selected when SBI_EN or SBI2CLK is tied high.
APL/TDN[5]	Input	AA1	The SBI ADD bus payload signal (APL) indicates valid data within the SBI TDM bus structure. This signal is asserted during all octets making up a tributary. This signal may be asserted during the V3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed TDM bus structure. This signal may be deasserted during the octet following the V3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed TDM bus structure. APL is sampled on the rising edge of REFCLK. APL shares the same pin as the TDN[5] input. APL is selected when SBI_EN or SBI2CLK is tied high.
AV5/TDN[6]	Input	V4	The SBI ADD bus payload indicator signal (AV5) locates the position of the floating payloads for each tributary within the SBI TDM bus structure. Timing differences between the port timing and the TDM bus timing are indicated by adjustments of this payload indicator relative to the fixed TDM bus structure. All movements indicated by this signal must be accompanied by appropriate adjustments in the APL signal. AV5 is sampled on the rising edge of REFCLK. AV5 shares the same pin as the TDN[6] input. AV5 is selected when SBI_EN or SBI2CLK is tied high.

Pin Name	Type	Pin No.	Function
DDATA[0]/RDP[1] DDATA[1]/RDP[2] DDATA[2]/RDP[3] DDATA[3]/RDP[4] DDATA[4]/RDP[5] DDATA[5]/RDP[6] DDATA[6]/RDP[7] DDATA[7]/RDP[8]	Tristate Output	AB19 Y17 AB16 AB15 W8 AA5 Y5 W5	The SBI DROP bus data signals (DDATA[7:0]) contain time division multiplexed receive data from up to 84 independently timed links. Link data is transported as T1 or E1 tributaries within the SBI TDM bus structure. The OCTLIU may be configured to insert data into up to 8 tributaries within the structure. Multiple LIU devices can drive the SBI DROP bus at uniquely assigned tributary column positions. DDATA[7:0] are tristated when the OCTLIU is not outputting data on a particular tributary column. DDATA[7:0] are updated on the rising edge of REFCLK. DDATA[7:0] share the same pins as the RDP[8:1] outputs. DDATA[7:0] are selected when SBI_EN or SBI2CLK is tied high.
DDP/RDN/RLCV[4]	Tristate Output	Y14	The SBI DROP bus parity signal (DDP) carries the even or odd parity for the DROP bus signals. The parity calculation encompasses the DDATA[7:0], DPL and DV5 signals. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. DDP is tristated when the OCTLIU is not outputting data on a particular tributary column. This parity signal is intended to detect accidental source clashes in the column assignment. DDP is updated on the rising edge of REFCLK. DDP shares the same pin as the RDN/RLCV[4] output. DDP is selected when SBI_EN or SBI2CLK is tied high.
DPL/RDN/RLCV[5]	Tristate Output	Y8	The SBI DROP bus payload signal (DPL) indicates valid data within the SBI TDM bus structure. This signal is asserted during all octets making up a tributary. This signal may be asserted during the V3 octet within a tributary to accommodate negative timing adjustments between the tributary rate and the fixed TDM bus structure. This signal may be deasserted during the octet following the V3 octet within a tributary to accommodate positive timing adjustments between the tributary rate and the fixed TDM bus structure. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. DPL is tristated when the OCTLIU is not outputting data on a particular tributary column. DPL is updated on the rising edge of REFCLK. DPL shares the same pin as the RDN/RLCV[5] output. DPL is selected when SBI_EN or SBI2CLK is tied high.

Pin Name	Type	Pin No.	Function
DV5/RDN/RLCV[6]	Tristate output	AB5	The SBI DROP bus payload indicator signal (DV5) locates the position of the floating payloads for each tributary within the SBI TDM bus structure. Timing differences between the port timing and the TDM bus timing are indicated by adjustments of this payload indicator relative to the fixed TDM bus structure. Multiple LIU devices can drive this signal at uniquely assigned tributary column positions. DV5 is tristated when the OCTLIU is not outputting data on a particular tributary column. DV5 is updated on the rising edge of REFCLK. DV5 shares the same pin as the RDN/RLCV[6] output. DV5 is selected when SBI_EN or SBI2CLK is tied high.
DACTIVE/RDN/RLCV[8]	Output	Y4	The SBI DROP bus active indicator signal (DACTIVE) is asserted whenever the OCTLIU is driving the SBI DROP bus signals, DDATA[7:0], DDP, DPL and DV5. DACTIVE is updated on the rising edge of REFCLK. DACTIVE shares the same pin as the RDN/RLCV[8] output. DACTIVE is selected when SBI_EN or SBI2CLK is tied high.
Transmit Line Interface			
TXTIP1[1] TXTIP1[2] TXTIP1[3] TXTIP1[4] TXTIP1[5] TXTIP1[6] TXTIP1[7] TXTIP1[8] TXTIP2[1] TXTIP2[2] TXTIP2[3] TXTIP2[4] TXTIP2[5] TXTIP2[6] TXTIP2[7] TXTIP2[8]	Analogue Output	A12 K22 N22 AB12 AB9 L1 H1 A9 A11 L22 M22 AB11 AB10 K1 J1 A10	Transmit Analogue Positive Pulse (TXTIP1[8:1] and TXTIP2[8:1]). When the transmit analogue line interface is enabled, the TXTIP1[x] and TXTIP2[x] analogue outputs drive the transmit line pulse signal through an external matching transformer. Both TXTIP1[x] and TXTIP2[x] are normally connected to the positive lead of the transformer primary. Two outputs are provided for better signal integrity and must be shorted together on the board. After a reset, TXTIP1[x] and TXTIP2[x] are high impedance. The HIGHZ bit of the octant's XLPG Line Driver Configuration register must be programmed to logic 0 to remove the high impedance state.

Pin Name	Type	Pin No.	Function
TXRING1[1] TXRING1[2] TXRING1[3] TXRING1[4] TXRING1[5] TXRING1[6] TXRING1[7] TXRING1[8] TXRING2[1] TXRING2[2] TXRING2[3] TXRING2[4] TXRING2[5] TXRING2[6] TXRING2[7] TXRING2[8]	Analogue Output	A13 J22 P22 AB13 AB8 M1 G1 A8 A14 H22 R22 AB14 AB7 N1 F1 A7	Transmit Analogue Negative Pulse (TXRING1[8:1] and TXRING2[8:1]). When the transmit analogue line interface is enabled, the TXRING1[x] and TXRING2[x] analogue outputs drive the transmit line pulse signal through an external matching transformer. Both TXRING1[x] and TXRING2[x] are normally connected to the negative lead of the transformer primary. Two outputs are provided for better signal integrity and must be shorted together on the board. After a reset, TXRING1[x] and TXRING2[x] are high impedance. The HIGHZ bit of the octant's XLPG Line Driver Configuration register must be programmed to logic 0 to remove the high impedance state.
Receive Line Interface			
RXTIP[1] RXTIP[2] RXTIP[3] RXTIP[4] RXTIP[5] RXTIP[6] RXTIP[7] RXTIP[8]	Analogue Input	G21 J21 R21 R19 R4 P1 J3 G3	Receive Analogue Positive Pulse (RXTIP[8:1]). When the analogue receive line interface is enabled, RXTIP[x] samples the received line pulse signal from an external isolation transformer. RXTIP[x] is normally connected directly to the positive lead of the receive transformer secondary.
RXRING[1] RXRING[2] RXRING[3] RXRING[4] RXRING[5] RXRING[6] RXRING[7] RXRING[8]	Analogue Input	H19 J19 P19 U22 R3 P4 J4 H4	Receive Analogue Negative Pulse (RXRING[8:1]). When the analogue receive line interface is enabled, RXRING[x] samples the received line pulse signal from an external isolation transformer. RXRING[x] is normally connected directly to the negative lead of the receive transformer secondary.

Pin Name	Type	Pin No.	Function
SBI to Clk/Data Converter Interface			
SBI_EN SBI2CLK	Input	B16 C1	The SBI interface enable signals (SBI_EN, SBI2CLK) select between the SBI and serial clock/data system side interfaces and allow selection of an operating mode in which the LIUs are disabled and the OCTLIU functions as a converter between the SBI interface and serial clk/data. The signals select the device operating mode as follows: SBI_EN SBI2CLK Mode 0 0 LIUs enabled, clk/data selected on system side. 1 0 LIUs enabled, SBI interface selected on system side. 0 1 LIUs disabled, converter mode. 1 1 Unused
IDATA[1]/TCLK[1] IDATA[2]/TCLK[2] IDATA[3]/TCLK[3] IDATA[4]/TCLK[4] IDATA[5]/TCLK[5] IDATA[6]/TCLK[6] IDATA[7]/TCLK[7] IDATA[8]/TCLK[8]	Input	U19 W20 AA22 AA20 W2 V3 U4 V1	The Ingress Data inputs (IDATA[8:1]) carry eight serial 1.544 Mbps or 2.048 Mbps data streams to be mapped on to the SBI interface when the device is operating as a SBI to clk/data converter. The eight serial data streams are sampled on the rising edge of ICLK_IN. IDATA[8:1] share the same pins as the TCLK[8:1] inputs. IDATA[8:1] are selected when SBI2CLK is tied high.
ICLK_IN/TDN[7]	Input	V2	The Ingress Input Clock (ICLK_IN) should be 1.544 MHz for DS1 or 2.048 MHz for E1 data streams and is used to sample the IDATA[8:1] and IFP_IN signals. ICLK_IN shares the same pin as the TDN[7] input. ICLK_IN is selected when SBI_EN or SBI2CLK is tied high.
IFP_IN/TDN[8]	Input	U3	The Ingress Frame Pulse input (IFP_IN) should be set high during the framing bits of DS1 streams or during the first bit of the framing octet of E1 data streams. IFP_IN is sampled on the rising edge of ICLK_IN. IFP_IN shares the same pin as the TDN[8] input. IFP_IN is selected when SBI_EN or SBI2CLK is tied high.
ICLK_OUT/RSYNC	Output	D8	The Ingress Output Clock (ICLK_OUT) is a nominal 1.544 MHz (for DS1) or 2.048 MHz (for E1) clock and may be used as a source for the ICLK_IN clock if desired. ICLK_OUT shares the same pin as the RSYNC output. ICLK_OUT is selected when SBI2CLK is tied high.

Pin Name	Type	Pin No.	Function
IFP_OUT/RDN/RLCV[1]	Output	AB18	The Ingress Frame Pulse output (IFP_OUT) is pulsed high every 193 ICLK_OUT cycles for DS1 and every 256 ICLK_OUT cycles for E1. It may be used as a framing reference and as a source for IFP_IN if desired. IFP_OUT is updated on the falling edge of ICLK_OUT. IFP_OUT shares the same pin as the RDN/RLCV[1] output. IFP_OUT is selected when SBI_EN or SBI2CLK is tied high.
EDATA[1]/RCLK[1] EDATA[2]/RCLK[2] EDATA[3]/RCLK[3] EDATA[4]/RCLK[4] EDATA[5]/RCLK[5] EDATA[6]/RCLK[6] EDATA[7]/RCLK[7] EDATA[8]/RCLK[8]	Output	AA19 AA18 Y16 AA15 AB6 W7 W6 AB2	The Egress Data outputs (EDATA[8:1]) carry eight serial 1.544 Mbps or 2.048 Mbps data streams de-mapped from the SBI interface when the device is operating as a SBI to clk/data converter. The eight serial data streams are updated on the falling edge of ECLK. EDATA[8:1] share the same pins as the RCLK[8:1] outputs. EDATA[8:1] are selected when SBI2CLK is tied high.
ECLK/RDN/RLCV[7]	Output	AA4	The Egress Clock output (ECLK) is a 1.544 MHz (for DS1) or 2.048 MHz (for E1) clock, recovered from one of the SBI tributaries. The SBI tributary used to recover timing is selectable. ECLK shares the same pin as the RDN/RLCV[7] output. ECLK is selected when SBI_EN or SBI2CLK is tied high.
EFP/RDN/RLCV[2]	Output	AB17	The Egress Frame Pulse output (EFP) is set high during the framing bits of DS1 streams or during the first bit of the framing octet of E1 data streams. EFP is updated on the falling edge of ECLK. EFP shares the same pin as the RDN/RLCV[2] output. EFP is selected when SBI_EN or SBI2CLK is tied high.

Pin Name	Type	Pin No.	Function
Timing Options Control			
XCLK	Input	D9	Crystal Clock Input (XCLK). This signal provides a stable, global timing reference for the OCTLIU internal circuitry via an internal clock synthesizer. XCLK is a nominally jitter free clock at 1.544 MHz in T1 mode and 2.048 MHz in E1 mode. In T1 mode, a 2.048 MHz clock may be used as a reference. When used in this way, however, the intrinsic jitter specifications in AT&T TR62411 may not be met.
RSYNC/ICLK_OUT	Output	D8	Recovered Clock Synchronization Signal (RSYNC). This output signal is the recovered, jitter attenuated, receiver line rate clock (1.544 or 2.048 MHz) of one of the eight T1 or E1 channels or, optionally, the recovered, jitter attenuated clock synchronously divided by 193 (T1 mode) or 256 (E1 mode) to create a 8 kHz timing reference signal. The default is to source RSYNC from octant #1. When the OCTLIU is in a loss of signal state, RSYNC is derived from the XCLK input or, optionally, is held high. RSYNC shares the same pin as the ICLK_OUT output. RSYNC is selected when SBI2CLK is tied low.
Alarm Interface			
LOS	Output	A5	Loss of Signal Alarm (LOS). This signal outputs the LOS status of the 8 LIU octants in a serial format which repeats every 8 XCLK cycles. The presence of the LOS status for LIU #1 on this output is indicated by the LOS_L1 output pulsing high. On the following XCLK cycle, the LOS status for LIU #2 is output, then LIU #3, and so on. This signal is intended for use in Hardware Only mode. When the microprocessor interface is enabled, the status of the LOS alarm can also be determined by reading the LOSV bit in the CDRC Interrupt Status register. LOS is updated on the falling edge of XCLK.
LOS_L1	Output	C7	Loss of Signal LIU #1 indicator (LOS_L1). This signal is pulsed high for one XCLK cycle every 8 XCLK cycles and indicates that the LOS status for LIU #1 is being output on LOS. LOS_L1 is updated on the falling edge of XCLK.

Pin Name	Type	Pin No.	Function
Misc. Control Signals			
RSTB	Input	A6	Active Low Reset (RSTB). This signal provides an asynchronous OCTLIU reset. RSTB is a Schmidt triggered input with an internal pull up resistor.
RES[1]	Input	B7	This pin must be tied low for normal operation.
RES[2] RES[3] RES[4] RES[5]	Analogue I/O	V22 Y9 F3 B14	These pins must be connected to an analogue ground for normal operation.
RES[6]	Input	B6	This pin must be tied to ground for normal operation.

Pin Name	Type	Pin No.	Function
Microprocessor Interface			
A[0]/LEN1[0] A[1]/LEN1[1] A[2]/LEN1[2] A[3]/LEN2[0] A[4]/LEN2[1] A[5]/LEN2[2] A[6]/LEN3[0] A[7]/LEN3[1] A[8]/LEN3[2] A[9]/LEN4[0] A[10]/LEN4[1]	Input	E22 E21 E20 F19 D22 D21 D20 E19 C22 C21 C20	Address Bus (A[10:0]). This bus selects specific registers during OCTLIU register accesses. Signal A[10] selects between normal mode and test mode register access. A[10] has an internal pull down resistor. A[10:0] share the same pins as some of the LENx[2:0] inputs. A[10:0] are selected when HW_ONLY is tied low.
ALE/LEN4[2]	Input	A22	Address Latch Enable (ALE). This signal is active high and latches the address bus contents, A[10:0], when low. When ALE is high, the internal address latches are transparent. ALE allows the OCTLIU to interface to a multiplexed address/data bus. The ALE input has an internal pull up resistor. ALE shares the same pin as the LEN4[2] input. ALE is selected when HW_ONLY is tied low.
WRB/LEN5[0]	Input	D18	Active Low Write Strobe (WRB). This signal is low during a OCTLIU register write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low. WRB shares the same pin as the LEN5[0] input. WRB is selected when HW_ONLY is tied low.
RDB/LEN5[1]	Input	C19	Active Low Read Enable (RDB). This signal is low during OCTLIU register read accesses. The OCTLIU drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low. RDB shares the same pin as the LEN5[1] input. RDB is selected when HW_ONLY is tied low.
CSB/LEN5[2]	Input	B20	Active Low Chip Select (CSB). CSB must be low to enable OCTLIU register accesses. CSB must go high at least once after power up to clear internal test modes. If CSB is not used, it should be tied to an inverted version of RSTB, in which case, RDB and WRB determine register accesses. CSB shares the same pin as the LEN5[2] input. CSB is selected when HW_ONLY is tied low.

Pin Name	Type	Pin No.	Function
INTB/LEN6[0]	Open-drain Output	D17	Active low Open-Drain Interrupt (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source at which time, INTB will tristate. INTB shares the same pin as the LEN6[0] input. INTB is selected when HW_ONLY is tied low.
D[0]/LEN6[1] D[1]/LEN6[2] D[2]/LEN7[0] D[3]/LEN7[1] D[4]/LEN7[2] D[5]/LEN8[0] D[6]/LEN8[1] D[7]/LEN8[2]	I/O	B19 A20 A19 B18 A18 D15 B17 C15	Bidirectional Data Bus (D[7:0]). This bus provides OCTLIU register read and write accesses. D[7:0] share the same pins as some of the LENx[2:0] inputs. D[7:0] are selected when HW_ONLY is tied low.
Hardware-Only Control Interface			
HW_ONLY	Input	B1	The Hardware Only mode enable signal (HW_ONLY) selects between the microprocessor-controlled and hardware-only modes of operation. When HW_ONLY is tied low, the microprocessor interface is enabled. When HW_ONLY is tied high, the hardware-only control interface is enabled and the microprocessor interface is unused.
SRCASC	Input	B3	Serial PROM Cascade Control (SRCASC). When SRCASC is tied low, the OCTLIU acts as the Serial PROM master controller and the SREN, SRCLK, SRDI and SRDO pins should be connected to the serial PROM. When SRCASC is tied high, the OCTLIU acts as a Serial PROM cascade slave and the SREN, SRCLK and SRDO pins should be connected to the SRCEN, SRCCLK and SRCDO pins of another OCTLIU device upstream in the cascade.
SREN	I/O	C4	Serial PROM Enable (SREN). When operating as a Serial PROM master (SRCASC tied low), the SREN pin functions as an output and generates an active low chip select signal for the serial PROM. When operating as a Serial PROM slave (SRCASC tied high), the SREN pin functions as an input and indicates the validity of cascade data on the SRDO input. When configured as an output, SREN is updated on the falling edge of SRCLK. When configured as an input, SREN is sampled on the rising edge of SRCLK.

Pin Name	Type	Pin No.	Function
SRCLK	I/O	A3	Serial PROM Clock (SRCLK). When operating as a Serial PROM master (SRCASC tied low), the SRCLK pin functions as an output and generates a clock for the serial PROM. When operating as a Serial PROM slave (SRCASC tied high), the SRCLK pin functions as an input and is connected to the SRCCLK output of an OCTLIU device upstream in the serial PROM cascade.
SRDI	Output	D6	Serial PROM Data In (SRDI). When operating as a Serial PROM master (SRCASC tied low), the SRDI output is used to send read commands to the serial PROM. When operating as a Serial PROM slave (SRCASC tied high), SRDI is unused. SRDI is updated on the falling edge of SRCLK.
SRDO	Input	B4	Serial PROM Data Out (SRDO). When operating as a Serial PROM master (SRCASC tied low), the SRDO input receives data from the serial PROM. When operating as a Serial PROM slave (SRCASC tied high), the SRDO input receives data from the SRCDO output of an OCTLIU device upstream in the serial PROM cascade. SRDO is sampled on the rising edge of SRCLK.
SRCEN	Output	C5	Serial PROM Cascade Enable (SRCEN). The SRCEN output is asserted when valid data is being output on SRCDO. SRCEN is updated on the falling edge of SRCCLK.
SRCCLK	Output	A4	Serial PROM Cascade Clock (SRCCLK). When operating as a Serial PROM master (SRCASC tied low), the SRCCLK output is a copy of the SRCLK output. When operating as a Serial PROM slave (SRCASC tied high), the SRCCLK output is a copy of the SRCLK input.
SRCDO	Output	B5	Serial PROM Cascade Data Out (SRCDO). The SRCDO output is a buffered, retimed copy of the SRDO input. SRCDO is updated on the falling edge of SRCCLK.
SRCODE	Input	C6	Serial PROM Code (SRCODE). The SRCODE input provides a means for controlling the execution of configuration instructions stored in the serial PROM. Instructions can be coded to execute only if SRCODE is logic 0, only if SRCODE is logic 1 or unconditionally. The SRCODE input thus allows the selection of two different configuration sequences within a single PROM load. This could be used, for example, to store two configurations for T1 and E1 operation within one serial PROM.

Pin Name	Type	Pin No.	Function
LEN1[0]/A[0] LEN1[1]/A[1] LEN1[2]/A[2] LEN2[0]/A[3] LEN2[1]/A[4] LEN2[2]/A[5] LEN3[0]/A[6] LEN3[1]/A[7] LEN3[2]/A[8] LEN4[0]/A[9] LEN4[1]/A[10] LEN4[2]/ALE LEN5[0]/WRB LEN5[1]/RDB LEN5[2]/CSB LEN6[0]/INTB LEN6[1]/D[0] LEN6[2]/D[1] LEN7[0]/D[2] LEN7[1]/D[3] LEN7[2]/D[4] LEN8[0]/D[5] LEN8[1]/D[6] LEN8[2]/D[7]	Input	E22 E21 E20 F19 D22 D21 D20 E19 C22 C21 C20 A22 D18 C19 B20 D17 B19 A20 A19 B18 A18 D15 B17 C15	Line Length Build-out Select (LENn[2:0]). These signals can be preset to select one of eight different pulse templates to be used by the line transmitters, depending on line length, etc. LENn[2:0] selects the pulse template for the line transmitter of octant #n. LENn[2:0] share the same pins as the microprocessor interface signals. LENn[2:0] are selected when HW_ONLY is tied high. The LENn[2:0] inputs are latched following reset of the OCTLIU and any changes to their value will have no effect on the operation of OCTLIU until a subsequent reset.

Pin Name	Type	Pin No.	Function
JTAG Interface			
TDO	Tristate Output	B2	Test Data Output (TDO). This signal carries test data out of the OCTLIU via the IEEE 1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is tri-stated except when scanning of data is in progress.
TDI	Input	A1	Test Data Input (TDI). This signal carries test data into the OCTLIU via the IEEE 1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull up resistor.
TCK	Input	C2	Test Clock (TCK). This signal provides timing for test operations that can be carried out using the IEEE 1149.1 test access port.
TMS	Input	D3	Test Mode Select (TMS). This signal controls the test operations that can be carried out using the IEEE 1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull up resistor.
TRSTB	Input	E4	Active low Test Reset (TRSTB). This signal provides an asynchronous OCTLIU test access port reset via the IEEE 1149.1 test access port. TRSTB is a Schmidt triggered input with an internal pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB should be connected to the RSTB input.
Analogue Power and Ground Pins			
TAVD1[1] TAVD1[2] TAVD1[3] TAVD1[4] TAVD1[5] TAVD1[6] TAVD1[7] TAVD1[8]	Analogue Power	D12 L19 M19 W12 W11 M4 L4 D11	Transmit Analogue Power (TAVD1[8:1]). TAVD1[8:1] provide power for the transmit LIU analogue circuitry. TAVD1[8:1] should be connected to analogue +3.3 V.

Pin Name	Type	Pin No.	Function
TAVD2[1] TAVD2[2] TAVD2[3] TAVD2[4] TAVD2[5] TAVD2[6] TAVD2[7] TAVD2[8] TAVD3[1] TAVD3[2] TAVD3[3] TAVD3[4] TAVD3[5] TAVD3[6] TAVD3[7] TAVD3[8]	Analogue Power	C13 L21 N20 AA12 Y10 M2 K3 B11 B13 L20 N21 Y12 AA10 M3 K2 C11	Transmit Analogue Power (TAVD2[8:1], TAVD3[8:1]). TAVD2[8:1] and TAVD3[8:1] supply power for the transmit LIU current DACs. They should be connected to analogue +3.3 V.
CAVD	Analogue Power	C14	Clock Synthesis Unit Analogue Power (CAVD). CAVD supplies power for the transmit clock synthesis unit. CAVD should be connected to analogue +3.3 V.
TAVS1[1] TAVS1[2] TAVS1[3] TAVS1[4] TAVS1[5] TAVS1[6] TAVS1[7] TAVS1[8]	Analogue Ground	D13 K19 N19 W13 W10 N4 K4 D10	Transmit Analogue Ground (TAVS1[8:1]). TAVS1[8:1] provide ground for the transmit LIU analogue circuitry. TAVS1[8:1] should be connected to analogue GND.

Pin Name	Type	Pin No.	Function
TAVS2[1] TAVS2[2] TAVS2[3] TAVS2[4] TAVS2[5] TAVS2[6] TAVS2[7] TAVS2[8] TAVS3[1] TAVS3[2] TAVS3[3] TAVS3[4] TAVS3[5] TAVS3[6] TAVS3[7] TAVS3[8]	Analogue Ground	A15 K20 P21 Y13 AA9 N3 J2 C10 C12 M21 M20 AA11 Y11 L2 L3 B12	Transmit Analogue Ground (TAVS2[8:1], TAVS3[8:1]). TAVS2[8:1] and TAVS3[8:1] supply ground for the transmit LIU current DACs. They should be connected to analogue GND.
CAVS	Analogue Ground	D14	Clock Synthesis Unit Analogue Ground (CAVS). CAVS supplies ground for the transmit clock synthesis unit. CAVS should be connected to analogue GND.
RAVD1[1] RAVD1[2] RAVD1[3] RAVD1[4] RAVD1[5] RAVD1[6] RAVD1[7] RAVD1[8]	Analogue Power	G22 K21 P20 T20 R2 N2 H2 H3	Receive Analogue Power (RAVD1[8:1]). RAVD1[8:1] supplies power for the receive LIU input equalizer. RAVD1[8:1] should be connected to analogue +3.3 V.
RAVD2[1] RAVD2[2] RAVD2[3] RAVD2[4] RAVD2[5] RAVD2[6] RAVD2[7] RAVD2[8]	Analogue Power	F21 H21 R20 U20 T2 P2 E1 E2	Receive Analogue Power (RAVD2[8:1]). RAVD2[8:1] supplies power for the receive LIU peak detect and slicer. RAVD2[8:1] should be connected to analogue +3.3 V.

Pin Name	Type	Pin No.	Function
RAVS1[1] RAVS1[2] RAVS1[3] RAVS1[4] RAVS1[5] RAVS1[6] RAVS1[7] RAVS1[8]	Analogue Ground	F22 J20 T22 U21 T1 P3 G2 D1	Receive Analogue Ground (RAVS1[8:1]). RAVS1[8:1] supplies ground for the receive LIU input equalizer. RAVS1[8:1] should be connected to analogue GND.
RAVS2[1] RAVS2[2] RAVS2[3] RAVS2[4] RAVS2[5] RAVS2[6] RAVS2[7] RAVS2[8]	Analogue Ground	G20 H20 T21 T19 T3 R1 F2 G4	Receive Analogue Ground (RAVS2[8:1]). RAVS2[8:1] supplies ground for the receive LIU peak detect and slicer. RAVS2[8:1] should be connected to analogue GND.
QAVD[1] QAVD[2] QAVD[3] QAVD[4]	Analogue Power	F20 AA13 T4 B10	Quiet Analogue Power (QAVD[4:1]). QAVD[4:1] supplies power for the core analogue circuitry. QAVD[4:1] should be connected to analogue +3.3 V.
QAVS[1] QAVS[2] QAVS[3] QAVS[4]	Analogue Ground	V21 AA8 F4 B15	Quiet Analogue Ground (QAVS[4:1]). QAVS[4:1] supplies ground for the core analogue circuitry. QAVS[4:1] should be connected to analogue GND.
Digital Power and Ground Pins			
VDD1V8[1] VDD1V8[2] VDD1V8[3] VDD1V8[4]	Power	A16 B9 W9 AA14	Core Power (VDD1V8[4:1]). The VDD1V8[4:1] pins should be connected to a well decoupled +1.8V DC power supply.

Pin Name	Type	Pin No.	Function
VDD3V3[1] VDD3V3[2] VDD3V3[3] VDD3V3[4] VDD3V3[5] VDD3V3[6] VDD3V3[7] VDD3V3[8] VDD3V3[9] VDD3V3[10] VDD3V3[11] VDD3V3[12] VDD3V3[13] VDD3V3[14] VDD3V3[15] VDD3V3[16] VDD3V3[17] VDD3V3[18] VDD3V3[19]	Power	A2 B8 B21 B22 C17 C18 D2 D7 G19 W3 W16 W17 W19 Y7 Y15 Y20 AA3 AB1 AB4	I/O Power (VDD3V3[19:1]). The VDD3V3[19:1] pins should be connected to a well decoupled +3.3V DC power supply.

Pin Name	Type	Pin No.	Function
VSS[1] VSS[2] VSS[3] VSS[4] VSS[5] VSS[6] VSS[7] VSS[8] VSS[9] VSS[10] VSS[11] VSS[12] VSS[13] VSS[14] VSS[15] VSS[16] VSS[17] VSS[18] VSS[19] VSS[20] VSS[21] VSS[22] VSS[23] VSS[24] VSS[25]	Ground	A17 A21 C3 C8 C9 C16 D5 D16 D19 E3 U1 V20 W14 Y3 Y6 Y18 AA2 AA6 AA7 AA16 AA17 AB3 AB20 AB21 AB22	Ground (VSS [25:1]). The VSS[25:1] pins should be connected to Ground.
NC1 NC2	Open	D4 W4	These pins must be left unconnected.

NOTES ON PIN DESCRIPTIONS:

1. All OCTLIU inputs and bi-directionals present minimum capacitive loading.
2. All OCTLIU inputs and bi-directionals, when configured as inputs, tolerate TTL logic levels.
3. All OCTLIU outputs and bi-directionals have at least 8 mA drive capability, except the LOS, LOS_L1, TDO and serial PROM interface outputs, which have at least 6 mA drive capability. The transmit analogue outputs (TXTIP and TXRING) have built-in short circuit current limiting.
4. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
5. Inputs A[10], RES[1], and RES[6] have internal pull-down resistors.
6. All unused inputs should be connected to GROUND.

7. The 3.3 Volt power pins (i.e., TAVD1, TAVD2, TAVD3, CAVD, RAVD1, RAVD2, QAVD, and VDD3V3) will be collectively referred to as $V_{DDall33}$ in this document.

8. Power to $V_{DDall33}$ should be applied *before* power to the VDD1V8 pins is applied. Similarly, power to the VDD1V8 pins should be removed *before* power to $V_{DDall33}$ is removed.

9. The $V_{DDall33}$ voltage level should not be allowed to drop below the VDD1V8 voltage level except when VDD1V8 is not powered.

9 FUNCTIONAL DESCRIPTION

9.1 Octants

The OCTLIU's eight E1/T1 line interface units operate independently and can be configured to operate uniquely. The octants do share a common XCLK clock input and internal clock synthesizer; hence only a single CSU Configuration register is present. Additionally, all octants share a common E1/T1B mode register bit to select between T1 and E1 operation.

9.2 Receive Interface

The analogue receive interface is configurable to operate in both E1 and T1 short-haul and long-haul applications. Short-haul T1 is defined as transmission over less than 655 ft of cable. Short-haul E1 is defined as transmission on any cable that attenuates the signal by less than 6 dB.

For long-haul signals, unequalized long- or short-haul bipolar alternate mark inversion (AMI) signals are received as the differential voltage between the RXTIP and RXRING inputs. The OCTLIU typically accepts unequalized signals that are attenuated for both T1 and E1 signals and are non-linearly distorted by typical cables.

For short-haul, the slicing threshold is set to a fraction of the input signal's peak amplitude, and adapts to changes in this amplitude. The slicing threshold is programmable, but is typically 67% and 50% for DSX-1 and E1 applications, respectively. Abnormally low input signals are detected when the input level is below a programmable threshold, which is typically 140 mV for E1 and 105 mV for T1.

Figure 8 – External Analogue Interface Circuits

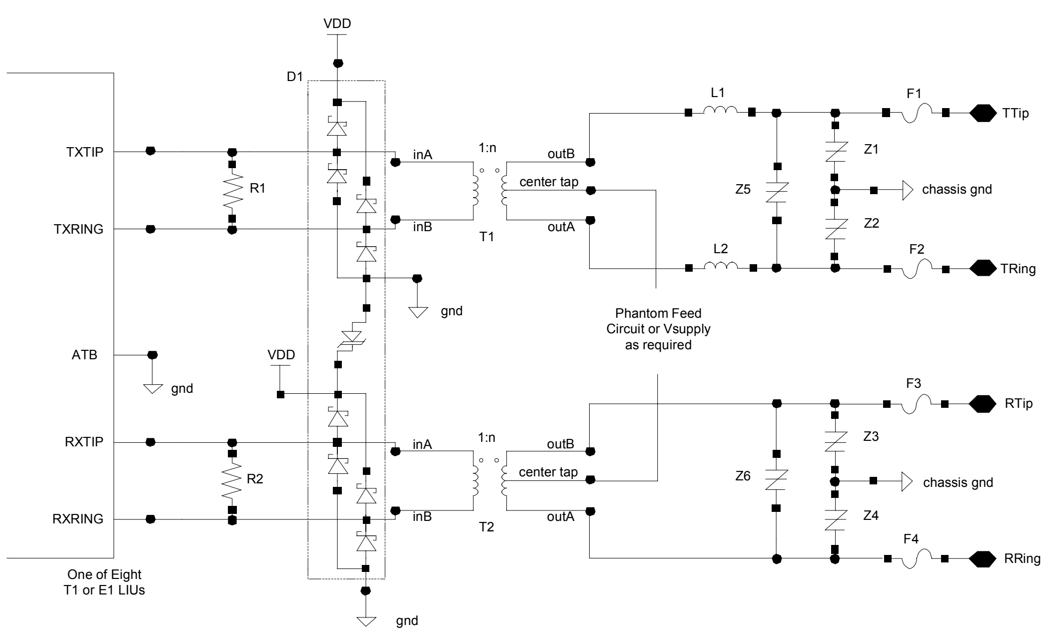


Figure 8 gives the recommended external protection circuitry for designs required to meet the major surge immunity and electrical safety standards including FCC Part 68, UL1950, and Bellcore TR-NWT-001089. This circuit has not been tested as of December, 1999. Please refer to an upcoming PMC application note for more details.

For systems not requiring phantom feed or inter-building line protection, the Bi-directional Transient Surge Suppressors (Z1-Z4), their associated ground connection and the center tap of the transformer can be removed from the circuit.

See Table 1 for the descriptions of components for Figure 8.

Note that the crowbar devices (Z1 – Z4) are not required if the transformer's isolation rating is not exceeded.

Table 1 – External Component Descriptions

Component	Description	Part #	Source
R1	36.0Ω ±1%, 0.25W Resistor		
R2	27.0Ω ±1%, 0.25W Resistor		
D1	Surge Protector Diode Array	SRDA3.3-4	Semtech
T1 & T2	1:1.58 CT Transformers (E1 75Ω cable) 1:2 CT Transformers (otherwise)		Pulse
Z1 – Z4	Bi-directional Transient Surge Suppressors	P1800SC	Teccor
Z5 – Z6	Bi-directional Transient Surge Suppressors	P0720SC	Teccor
L1 & L2	Dual Choke, 27µH	PE-68624	Pulse
F1 – F4	Telecom/Time Lag Fuses	F1250T	Teccor

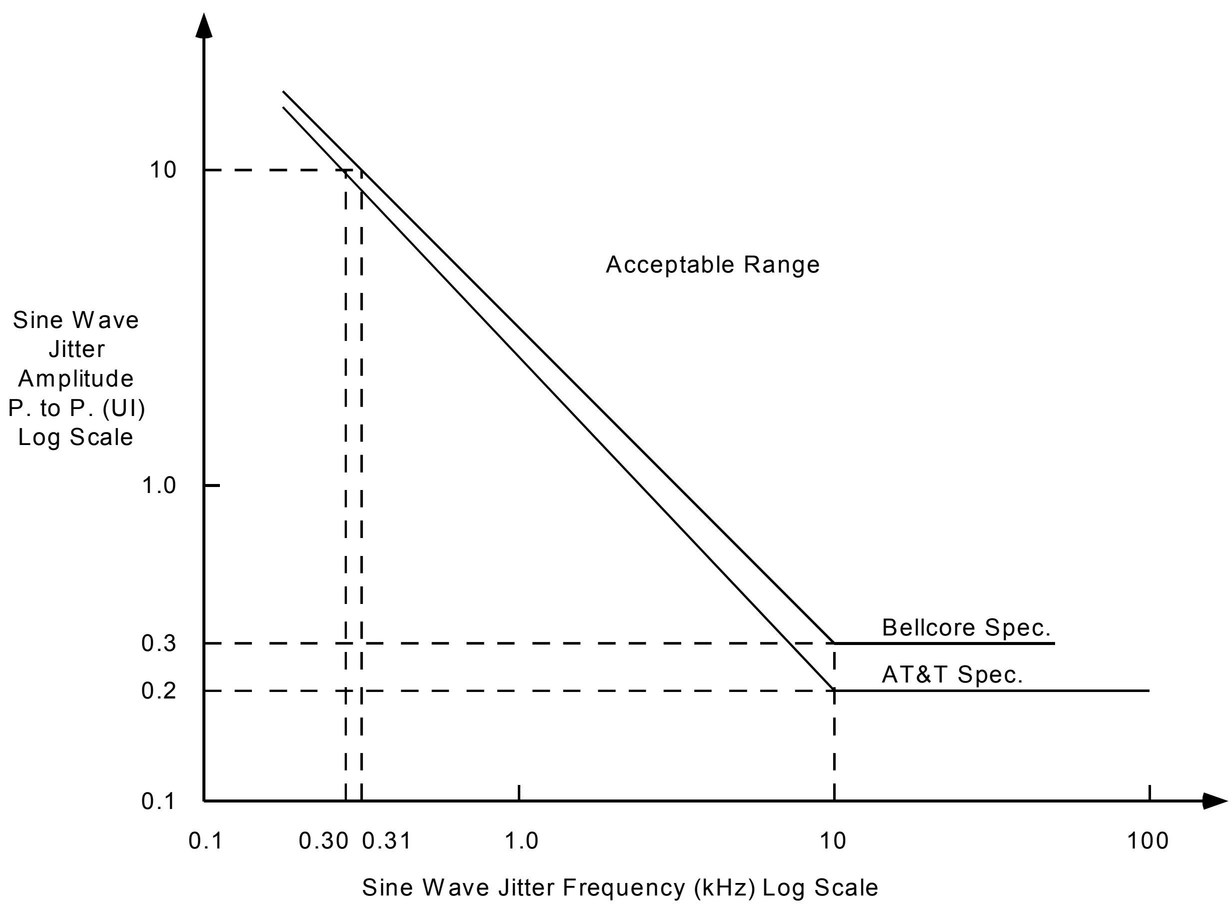
When operating in E1 mode with 75Ω cable, a 1:1.58 turns ratio transformer is specified in the above table. It is in fact also possible to use a 1:2 turns ratio transformer, in which case the value of R1 must be changed to 22.0Ω ±1% and the value of R2 must be changed to 18.0Ω ±1%.

9.3 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by the Clock and Data Recovery (CDRC) block. The CDRC provides clock and PCM data recovery, B8ZS and HDB3 decoding, line code violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and reconstructs the NRZ data. Loss of signal is indicated after a programmable threshold of consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared upon meeting an 1-in-8 pulse density criteria for T1 and a 1-in-4 pulse density criteria for E1. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. A line code violation is defined as a bipolar violation (BPV) for AMI-coded signals, is defined as a BPV that is not part of a zero substitution code for B8ZS-coded signals, and is defined as a bipolar violation of the same polarity as the last bipolar violation for HDB3-coded signals.

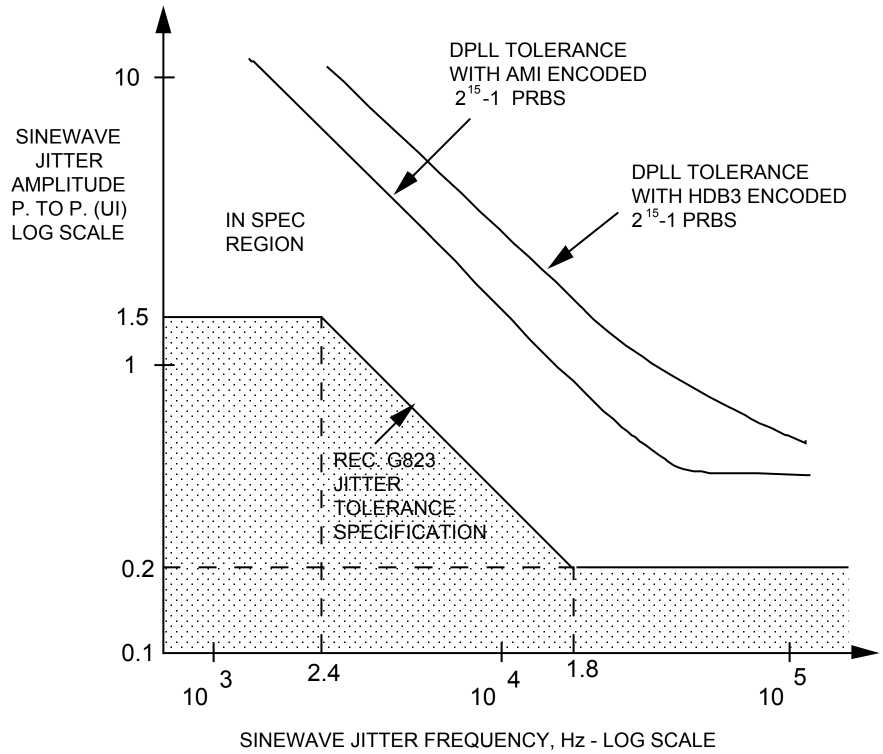
In T1 mode, the input jitter tolerance of the OCTLIU complies with the Bellcore Document TA-TSY-000170 and with the AT&T specification TR62411, as shown in Figure 9. The tolerance is measured with a QRSS sequence (2^{20}-1 with 14 zero restriction). The CDRC block provides two algorithms for clock recovery that result in differing jitter tolerance characteristics. The first algorithm (when the ALGSEL register bit is logic 0) provides good low frequency jitter tolerance, but the high frequency tolerance is close to the TR62411 limit. The second algorithm (when ALGSEL is logic 1) provides much better high frequency jitter tolerance at the expense of the low frequency tolerance; the low frequency tolerance of the second algorithm is approximately 80% that of the first algorithm.

Figure 9 – T1 Jitter Tolerance



For E1 applications, the input jitter tolerance complies with the ITU-T Recommendation G.823 “The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy.” Figure 10 illustrates this specification and the performance of the phase-locked loop when the ALGSEL register bit is logic 0.

Figure 10 – Compliance with ITU-T Specification G.823 for E1 Input Jitter



9.4 Receive Jitter Attenuator (RJAT)

The Receive Jitter Attenuator (RJAT) digital PLL attenuates the jitter present on the RXTIP/RXRING inputs. The attenuation is only performed when the RJATBYP register bit is a logic 0.

The jitter characteristics of the Receive Jitter Attenuator (RJAT) are the same as the Transmit Jitter Attenuator (TJAT).

9.5 T1 Inband Loopback Code Detector (IBCD)

The T1 Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and DEACTIVATE code sequences in the receive data stream. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403-1993, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

9.6 T1 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. The block detects pulse density violations of the requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event, and/or a change of state on the pulse density violation indication.

9.7 Performance Monitor Counters (PMON)

The Performance Monitor block accumulates line code violation events with a saturating counter over consecutive intervals as defined by the period between writes to trigger registers (typically 1 second). When the trigger is applied, the PMON transfers the counter value into holding registers and resets the counter to begin accumulating events for the interval. The counter is reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive triggers, an overrun register bit is asserted.

Triggering a counter transfer within an octant is performed by writing to any counter register location within the octant or by writing to the “Line Interface Interrupt Source #1 / PMON Update” register.

9.8 Pseudo Random Binary Sequence Generation and Detection (PRBS)

The Pseudo Random Binary Sequence Generator/Detector (PRBS) block is a software selectable PRBS generator and checker for 2^{11}-1, 2^{15}-1 or 2^{20}-1 PRBS polynomials for use in the T1 and E1 links. PRBS patterns may be generated and detected in either the transmit or receive directions.

The PRBS block can perform an auto synchronization to the expected PRBS pattern and accumulates the total number of bit errors in two 24-bit counters. The error count accumulates over the interval defined by successive writes to the Line Interface Interrupt Source #1 / PMON Update register. When an accumulation is forced, the holding register is updated, and the counter reset to begin accumulating for the next interval. The counter is reset in such a way that no events are missed. The data is then available in the Error Count registers until the next accumulation.

9.9 T1 Inband Loopback Code Generator (XIBC)

The T1 Inband Loopback Code Generator (XIBC) block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code. The contents of the code and its length are programmable from 3 to 8 bits.

9.10 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. Pulse density enforcement is enabled by a register bit within the XPDE.

This block monitors the digital output of the transmitter and detects when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the block can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the digital stream from the transmitter is passed through unaltered.

9.11 Transmit Jitter Attenuator (TJAT)

The Transmit Jitter Attenuation function is provided by a digital phase lock loop and 80-bit deep FIFO. The TJAT receives jittery, dual-rail data in NRZ format on two separate inputs, which allows bipolar violations to pass through the block uncorrected. The incoming data streams are stored in a FIFO timed to the transmit clock. The respective input data emerges from the FIFO timed to the jitter attenuated clock.

The jitter attenuator generates the jitter-free 1.544 MHz or 2.048 MHz Transmit clock output by adjusting the Transmit clock's phase in 1/96 UI increments to minimize the phase difference between the generated Transmit clock and input data clock to TJAT. Jitter fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within TJAT so that the frequency of Transmit clock is equal to the average frequency of the input data clock. For T1 applications, to best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 5.7 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 5.7 Hz are tracked by the generated Transmit clock. In E1 applications, the corner frequency is 7.6 Hz. To provide a smooth flow of data out of TJAT, the Transmit clock is used to read data out of the FIFO.

If the FIFO read pointer (timed to the Transmit clock) comes within one bit of the write pointer (timed to the input data clock), TJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

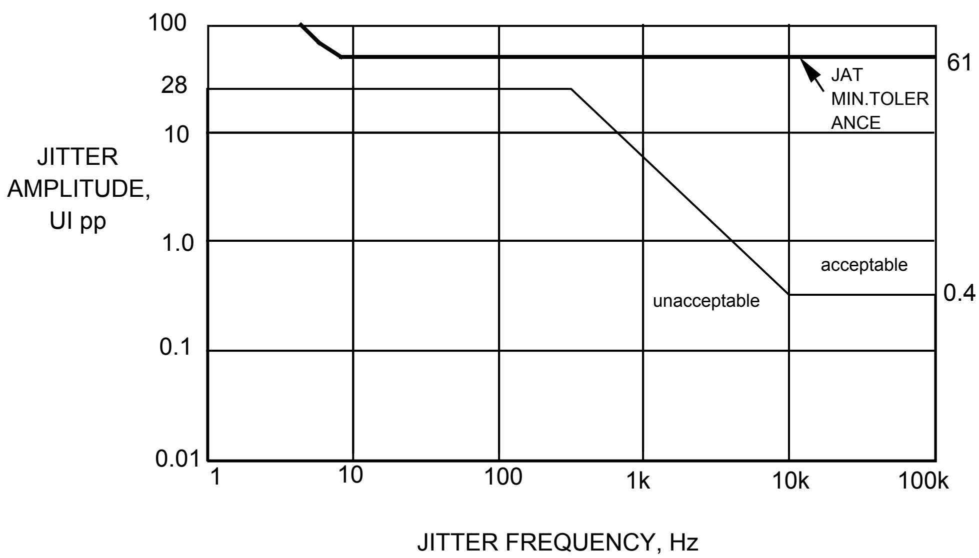
The TJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 61 Uipp of input jitter at jitter frequencies above 5.7 Hz (7.6 Hz for E1). For jitter frequencies below 5.7 Hz (7.6 Hz for E1), more correctly called wander, the tolerance increases 20 dB per decade. In most applications the TJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The TJAT block meets the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and thus allows compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

TJAT exhibits negligible jitter gain for jitter frequencies below 5.7 Hz (7.6 Hz for E1), and attenuates jitter at frequencies above 5.7 Hz (7.6 Hz for E1) by 20 dB per decade. In most applications, the TJAT block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through TJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of a 1/96 UI phase adjustment quantum. TJAT meets the jitter attenuation requirements of AT&T TR 62411. The block allows the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.

Jitter Tolerance

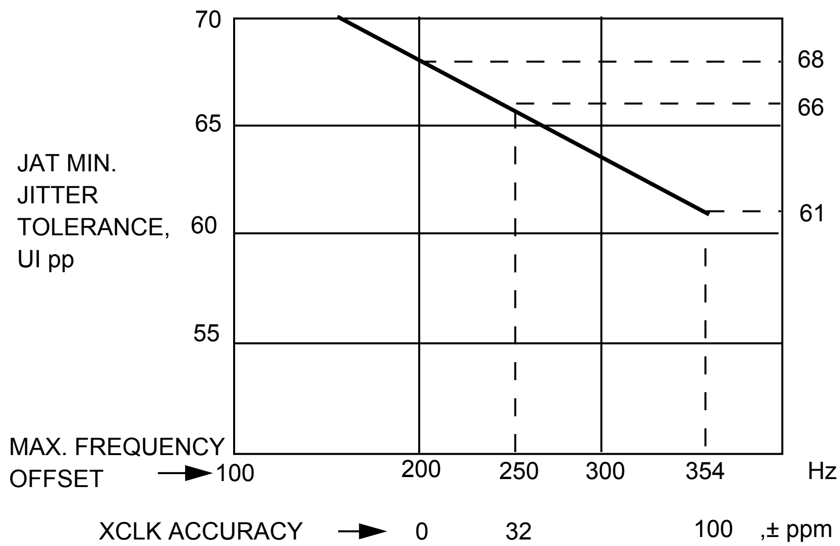
Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For TJAT, the input jitter tolerance is 61 Unit Intervals peak-to-peak (Uipp) with a worst case frequency offset of 354 Hz. It is 80 Uipp with no frequency offset. The frequency offset is the difference between the frequency of XCLK and that of the input data clock.

Figure 11 – TJAT Jitter Tolerance



The accuracy of the XCLK frequency and that of the TJAT PLL reference input clock used to generate the jitter-free Transmit clock output have an effect on the minimum jitter tolerance. Given that the TJAT PLL reference clock accuracy can be ±200 Hz and that the XCLK input accuracy can be ±100 ppm, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK are shown in Figure 12.

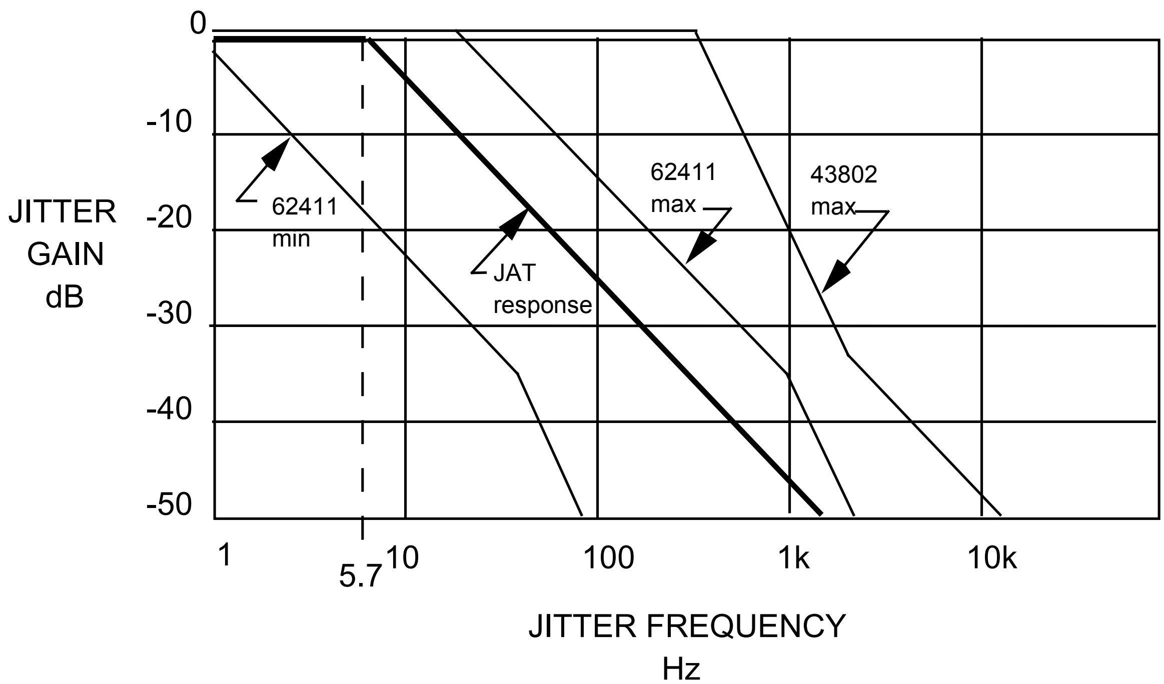
Figure 12 – TJAT Minimum Jitter Tolerance vs. XCLK Accuracy



Jitter Transfer

For T1 applications, the output jitter for jitter frequencies from 0 to 5.7 Hz (7.6 Hz for E1) is no more than 0.1 dB greater than the input jitter, excluding residual jitter. Jitter frequencies above 5.7 Hz (7.6 Hz for E1) are attenuated at a level of 6 dB per octave, as shown in Figure 13. The figure is valid for the case where the N1 = 2FH in the TJAT Jitter Attenuator Divider N1 Control register and N2 = 2FH in the TJAT Divider N2 Control register.

Figure 13 – TJAT Jitter Transfer



T1

In the non-attenuating mode, when the FIFO is within one UI of overrunning or underrunning, the tracking range is 1.48 MHz to 1.608 MHz.

The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (61 Uipp), and maximum system clock frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or system clock frequency offset.

E1

In the non-attenuating mode, when the FIFO is within one UI of overrunning or underrunning, the tracking range is 2.13 MHz to 1.97 MHz.

The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 300 Hz with worst case jitter (61 Uipp), and maximum system clock frequency offset (± 100 ppm). The nominal range is 2.048 MHz ± 1277 Hz with no jitter or system clock frequency offset.

Jitter Generation

In the absence of input jitter, the output jitter shall be less than 0.025 Uipp. This complies with the AT&T TR 62411 requirement of less than 0.025 Uipp of jitter generation.

9.12 Line Transmitter

The line transmitter generates Alternate Mark Inversion (AMI) transmit pulses suitable for use in the DSX-1 (short haul T1), short haul E1, long haul T1 and long haul E1 environments. The voltage pulses are produced by applying a current to a known termination (termination resistor plus line impedance). The use of current (instead of a voltage driver) simplifies transmit Input Return Loss (IRL), transmit short circuit protection (none needed) and transmit tri-stating.

The output pulse shape is synthesized digitally with current digital-to-analogue (DAC) converters, which produce 24 samples per symbol. The current DAC's produce differential bipolar outputs that directly drive the TXTIP1[x], TXTIP2[x], TXRING1[x] and TXRING2[x] pins. The current output is applied to a terminating resistor and line-coupling transformer in a differential manner, which when viewed from the line side of the transformer produce the output pulses at the required levels and ensures a small positive to negative pulse imbalance.

The pulse shape is user programmable. For T1 short haul, the cable length between the OCTLIU and the cross-connect (where the pulse template specifications are given) greatly affects the resulting pulse shapes. Hence, the data applied to the converter must account for different cable lengths. For CEPT E1 applications the pulse template is specified at the transmitter, thus only one setting is required. For T1 long haul with a LBO of 7.5 dB the previous bits effect what the transmitter must drive to compensate for inter-symbol interference; for LBO's of 15 dB or 22.5 dB the previous 3 or 4 bits effect what the transmitter must send out.

Refer to the Operation section for details on creating the synthesized pulse shape.

9.13 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the TJAT block, and the reference clock for the TJAT digital PLL.

9.14 Scaleable Bandwidth Interconnect (SBI) Interface

The Scaleable Bandwidth Interconnect is a synchronous, time-division multiplexed bus designed to transfer, in a pin-efficient manner, data belonging to a number of independently timed links of varying bandwidth. The bus is timed to a reference 19.44MHz clock and a 2 kHz (or fraction thereof) frame pulse. All sources and sinks of data on the bus are timed to the reference clock and frame pulse.

Timing is communicated across the Scaleable Bandwidth Interconnect by floating data structures. Payload indicator signals in the SBI control the position of the floating data structure and therefore the timing. When sources are running faster than the SBI the floating payload structure is advanced by an octet by passing an extra octet in the V3 octet locations (H3 octet for DS3 mappings which are not used by the OCTLIU). When the source is slower than the SBI the floating payload is retarded by leaving the octet after the V3 or H3 octet unused. Both these rate adjustments are indicated by the SBI control signals.

The SBI multiplexing structure is modeled on the SONET/SDH standards. The SONET/SDH virtual tributary structure is used to carry T1/J1 and E1 links. Unchannelized DS3 payloads (not used by OCTLIU) follow a byte synchronous structure modeled on the SONET/SDH format.

The SBI structure uses a locked SONET/SDH structure fixing the position of the TUG-3/TU-3 relative to the STS-3/STM-1 transport frame. The SBI is also of fixed frequency and alignment as determined by the reference clock (REFCLK) and frame indicator signal (C1FP). Frequency deviations are compensated by adjusting the location of the T1/J1/E1/DS3 channels using floating tributaries as determined by the V5 indicator and payload signals (DV5, AV5, DPL and APL). Note that the OCTLIU always operates as a clock slave on the SBI ADD bus and as a clock master on the SBI DROP bus, i.e. it does not support the AJUST_REQ and DJUST_REQ timing adjustment request signals defined in the SBI bus specification.

The multiplexed links are separated into three Synchronous Payload Envelopes (SPE). Each envelope may be configured independently to carry up to 28 T1/J1s, 21 E1s or a DS3. The OCTLIU may be configured to use any eight T1/J1 tributaries or any eight E1 tributaries from any of the three SPE's. The eight tributaries need not all be selected from the same SPE. A single OCTLIU device cannot, however, use T1/J1 and E1 tributaries simultaneously.

9.14.1 Interfacing OCTLIUs to a High Density Framer

Figure 14 – SBI to Framer Line Side Interface

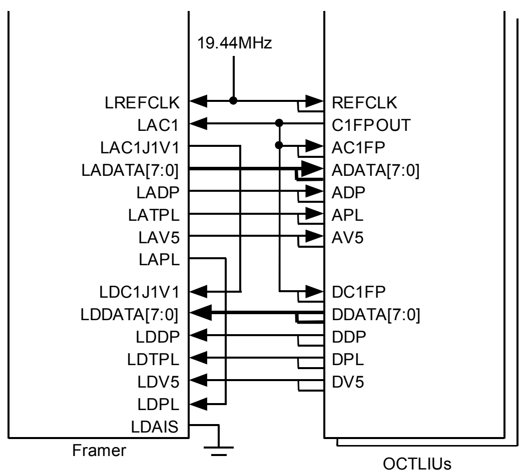


Figure 14 shows how the SBI interfaces of multiple OCTLIU's may be connected to the line side interface of a high density framer. With the exception of C1FPOUT, all signals on the OCTLIU side are simply bussed in parallel to the multiple devices. The C1FPOUT port of a single OCTLIU is used to provide a frame reference for all the devices. Alternatively, the C1 frame pulse can be generated by external circuitry if desired. The framer's interface must be configured such that VT pointer processors are bypassed, VT's are byte synchronously mapped, and that the STS-1 SPE's are locked to the STS-3 transport envelope with a fixed pointer offset of 522.

9.15 SBI Extracter and PISO

The SBI Extract block receives data from the SBI ADD BUS and converts it to serial bit streams for transmission. The SBI Extract block may be configured to enable or disable extraction of individual tributaries within the SBI ADD bus. It may also be configured to generate an all-1s output to the transmit LIU when an alarm indication is signalled for a particular tributary via the SBI bus.

9.16 SBI Inserter and SIPO

The SBI Insert block receives serial data from the LIU octants and inserts it on the SBI DROP BUS. The SBI Insert block may be configured to enable or disable transmission of individual tributaries on to the SBI DROP bus.

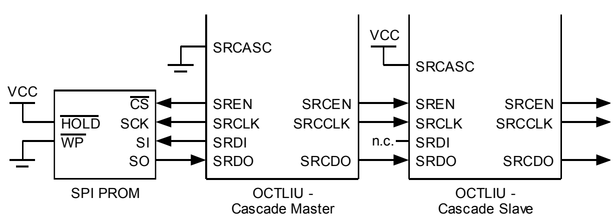
9.17 SBI to Clk/Data Converter

The OCTLIU may be configured (by setting the SBI_EN and SBI2CLK inputs) to operate in a mode in which the LIUs are disabled and the device performs conversion between the SBI interface and serial clock and data (see Figure 6). Up to eight tributaries may be converted to serial format. The serial data streams are required to share a common clock and frame pulse. In the egress direction (from SBI ADD BUS to egress clk/data), elastic stores are provided to align the tributary outputs to a common clock and frame alignment.

9.18 Serial PROM Interface

The serial PROM interface is used to configure the OCTLIU in the absence of a microprocessor. A single SPI-compatible serial PROM can be used to configure a number of OCTLIU devices simultaneously (provided all such devices are intended to be configured identically) by connecting the devices in a cascade as shown in Figure 15.

Figure 15 – Serial PROM Cascade Interface



SPI-compatible PROMs are organised as n x 8-bit words. The contents of the PROM are read sequentially starting at address 0 and continuing until a specially coded stop command is encountered. Each configuration command is coded in 3-bytes as follows:

Figure 16 – Serial PROM Command Format

Code1	Code0	Reg[13:8]
Reg[7:0]		
Data[7:0]		

Reg[13:0] specifies one of the OCTLIU registers defined in Table 4. Data[7:0] is the value to be written to the specified register. Commands are interpreted depending on the Code1 and Code0 bits as follows:

Table 2 – Serial PROM Commands – Code Bits

Code1	Code0	Action
0	0	Special Command
0	1	Write Data[7:0] to Reg[13:0] only if SRCODE = 0
1	0	Write Data[7:0] to Reg[13:0] only if SRCODE = 1
1	1	Write Data[7:0] to Reg[13:0] regardless of value of SRCODE

The SRCODE input to OCTLIU provides a means to execute configuration instructions conditionally. Two different configuration sequences can be stored in a single PROM (for T1 or E1 operation, for example) and the SRCODE input used to select which one will be applied. Different OCTLIU devices in a cascade can have their SRCODE inputs set to different values.

When Code1 = Code0 = ‘0’, the Reg[13:0] and Data[7:0] fields are interpreted as a special command, not as a register/data pair. The following special commands are defined:

Table 3 – Serial PROM Special Commands

Reg[13:0]	Action
3FFB	Resume acting upon register write commands. Only meaningfull if a 3FFD command (see below) has previously been received.
3FFC	No-op.
3FFD	Ignore subsequent register write commands. This command is only acted upon by the first OCTLIU in the cascade which receives it and which is not already ignoring register write commands. The OCTLIU which acts upon this command does not propagate the command down the cascade, but instead substitutes the 3FFC special command.

Reg[13:0]	Action
3FFE	Pause for Data[7:0] x 4096 XCLK periods before reading next PROM command.
3FFF	Stop, i.e. configuration of OCTLIU has finished.

The ‘ignore subsequent register write commands’ command can be used to configure multiple OCTLIU’s in a cascade individually (for example, to allocate different SBI tributaries to different OCTLIU devices). It provides a means to progressively ‘switch off’ each device in the cascade once it has been configured. Consider for example the following sequence of configuration commands:

Command (hex)	Explanation
C00102	Write 02 to register 01 of all devices in the cascade, regardless of SRCODE.
: :	(Subsequent configuration commands are acted upon by all devices in the cascade.)
3FFD00	First device in cascade ignores all further register writes.
C00103 :	Write 03 to register 01 of all devices in the cascade except the first, regardless of SRCODE.
: :	(Subsequent configuration commands are acted upon by all devices in the cascade except the first.)
3FFD00	Second device in cascade ignores all further register writes.
C00104 :	Write 04 to register 01 of all devices in the cascade except the first two, regardless of SRCODE.
: :	(Subsequent configuration commands are acted upon by all devices in the cascade except the first and second.)

The pause command can be used, for example, to allow the clock synthesis circuitry within the CSD block time to stablise before configuring the rest of the device.

9.19 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported.

9.20 Microprocessor Interface

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Microprocessor Interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the OCTLIU.

10 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the OCTLIU. Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

The Register Memory Map in Table 4 below shows where the normal mode registers are accessed. The OCTLIU contains 1 set of master configuration, SBI, and CSU registers and 8 sets of T1/E1 LIU registers. Where only 1 set is present, the registers apply to the entire device. Where 8 sets are present, each set of registers apply to a single octant of the OCTLIU. By convention, where 8 sets of registers are present, address space 000H – 07FH applies to octant #1, 080H – 0FFH applies to octant #2, etc, up to 380H – 3FFH for octant #8.

On reset the OCTLIU defaults to T1 mode. For proper operation some register configuration is expected. By default interrupts will not be enabled, and automatic alarm generation is disabled.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the OCTLIU to determine the programming state of the chip.
3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect OCTLIU operation unless otherwise noted.
5. Certain register bits are reserved. These bits are associated with functions that are unused in this application. To ensure that the OCTLIU operates as intended, reserved register bits must only be written with their default values unless otherwise stated. Similarly, writing to reserved registers should be avoided unless otherwise stated.

10.1 Normal Mode Register Memory Map

Table 4 – Normal Mode Register Memory Map

Addr	Register
000H	Reset / Revision ID / Device ID
080H, 100H, 180H, 200H, 280H, 300H, 380H	Reserved
001H	Global Configuration / Clock Monitor
081H, 101H, 181H, 201H, 281H, 301H, 381H	Reserved
002H	Master Interrupt Source #1
082H, 102H, 182H, 202H, 282H, 302H, 382H	Reserved
003H	Master Interrupt Source #2
083H, 103H, 183H, 203H, 283H, 303H, 383H	Reserved
004H	Master Test Control #1
084H, 104H, 184H, 204H, 284H, 304H, 384H	Reserved
005H	Master Test Control #2
085H, 105H, 185H, 205H, 285H, 305H, 385H	Reserved
006H	CSU Configuration
086H, 106H, 186H, 206H, 286H, 306H, 386H	Reserved
007H	CSU Reserved
087H, 107H, 187H, 207H, 287H, 307H, 387H	Reserved
008H, 088H, 108H, 188H, 208H, 288H, 308H, 388H	Receive Line Interface Configuration #1
009H, 089H, 109H, 189H, 209H, 289H, 309H, 389H	Receive Line Interface Configuration #2
00AH, 08AH, 10AH, 18AH, 20AH, 28AH, 30AH, 38AH	Transmit Line Interface Configuration
00BH, 08BH, 10BH, 18BH, 20BH, 28BH, 30BH, 38BH	Transmit Line Interface Timing Options / Clock Monitor / Pulse Template Selection

Addr	Register
00CH, 08CH, 10CH, 18CH, 20CH, 28CH, 30CH, 38CH	Line Interface Interrupt Source #1 / PMON Update
00DH, 08DH, 10DH, 18DH, 20DH, 28DH, 30DH, 38DH	Line Interface Interrupt Source #2
00EH, 08EH, 10EH, 18EH, 20EH, 28EH, 30EH, 38EH	Line Interface Diagnostics
00FH, 08FH, 10FH, 18FH, 20FH, 28FH, 30FH, 38FH	Line Interface PRBS Position
010H – 03FH	Reserved
090H – 0BFH	Reserved
110H – 13FH	Reserved
190H – 1BFH	Reserved
210H – 23FH	Reserved
290H – 2BFH	Reserved
310H	INSBI Control
311H	INSBI FIFO Underrun Interrupt Status
312H	INSBI FIFO Overrun Interrupt Status
313H	INSBI Page A Octant to Tributary Mapping #1
314H	INSBI Page A Octant to Tributary Mapping #2
315H	INSBI Page A Octant to Tributary Mapping #3
316H	INSBI Page A Octant to Tributary Mapping #4
317H	INSBI Page A Octant to Tributary Mapping #5
318H	INSBI Page A Octant to Tributary Mapping #6
319H	INSBI Page A Octant to Tributary Mapping #7
31AH	INSBI Page A Octant to Tributary Mapping #8
31BH	INSBI Page B Octant to Tributary Mapping #1
31CH	INSBI Page B Octant to Tributary Mapping #2
31DH	INSBI Page B Octant to Tributary Mapping #3
31EH	INSBI Page B Octant to Tributary Mapping #4
31FH	INSBI Page B Octant to Tributary Mapping #5
320H	INSBI Page B Octant to Tributary Mapping #6
321H	INSBI Page B Octant to Tributary Mapping #7

Addr	Register
322H	INSBI Page B Octant to Tributary Mapping #8
323H	INSBI Link Enable
324H	INSBI Link Enable Busy
325H	INSBI Tributary Control #1
326H	INSBI Tributary Control #2
327H	INSBI Tributary Control #3
328H	INSBI Tributary Control #4
329H	INSBI Tributary Control #5
32AH	INSBI Tributary Control #6
32BH	INSBI Tributary Control #7
32CH	INSBI Tributary Control #8
32DH	INSBI Minimum Depth
32EH	INSBI FIFO Thresholds
32FH – 330H	INSBI Reserved
331H	INSBI Depth Check Interrupt Status
332H	INSBI Master Interrupt Status
333H – 33FH	INSBI Reserved
390H	EXSBI Control
391H	EXSBI FIFO Underrun Interrupt Status
392H	EXSBI FIFO Overrun Interrupt Status
393H	EXSBI Parity Error Interrupt Reason
394H	EXSBI Depth Check Interrupt Status
395H	EXSBI Master Interrupt Status
396H	EXSBI Minimum Depth
397H	EXSBI FIFO Thresholds
398H	EXSBI Link Enable
399H	EXSBI Link Enable Busy
39AH – 39FH	EXSBI Reserved
3A0H	EXSBI Tributary Control #1
3A1H	EXSBI Tributary Control #2

Addr	Register
3A2H	EXSBI Tributary Control #3
3A3H	EXSBI Tributary Control #4
3A4H	EXSBI Tributary Control #5
3A5H	EXSBI Tributary Control #6
3A6H	EXSBI Tributary Control #7
3A7H	EXSBI Tributary Control #8
3A8H	EXSBI Page A Octant to Tributary Mapping #1
3A9H	EXSBI Page A Octant to Tributary Mapping #2
3AAH	EXSBI Page A Octant to Tributary Mapping #3
3ABH	EXSBI Page A Octant to Tributary Mapping #4
3ACH	EXSBI Page A Octant to Tributary Mapping #5
3ADH	EXSBI Page A Octant to Tributary Mapping #6
3AEH	EXSBI Page A Octant to Tributary Mapping #7
3AFH	EXSBI Page A Octant to Tributary Mapping #8
3B0H	EXSBI Page B Octant to Tributary Mapping #1
3B1H	EXSBI Page B Octant to Tributary Mapping #2
3B2H	EXSBI Page B Octant to Tributary Mapping #3
3B3H	EXSBI Page B Octant to Tributary Mapping #4
3B4H	EXSBI Page B Octant to Tributary Mapping #5
3B5H	EXSBI Page B Octant to Tributary Mapping #6
3B6H	EXSBI Page B Octant to Tributary Mapping #7
3B7H	EXSBI Page B Octant to Tributary Mapping #8
3B8H – 3BFH	EXSBI Reserved
040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H	ELST Configuration
041H, 0C1H, 141H, 1C1H, 241H, 2C1H, 341H, 3C1H	ELST Interrupt Enable/Status
042H, 0C2H, 142H, 1C2H, 242H, 2C2H, 342H, 3C2H	T1 PDVD Reserved
043H, 0C3H, 143H, 1C3H, 243H, 2C3H, 343H, 3C3H	T1 PDVD Interrupt Enable/Status

Addr	Register
044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H	T1 XPDE Reserved
045H, 0C5H, 145H, 1C5H, 245H, 2C5H, 345H, 3C5H	T1 XPDE Interrupt Enable/Status
046H, 0C6H, 146H, 1C6H, 246H, 2C6H, 346H, 3C6H	T1 XIBC Control
047H, 0C7H, 147H, 1C7H, 247H, 2C7H, 347H, 3C7H	T1 XIBC Loopback Code
048H, 0C8H, 148H, 1C8H, 248H, 2C8H, 348H, 3C8H	RJAT Interrupt Status
049H, 0C9H, 149H, 1C9H, 249H, 2C9H, 349H, 3C9H	RJAT Reference Clock Divisor (N1) Control
04AH, 0CAH, 14AH, 1CAH, 24AH, 2CAH, 34AH, 3CAH	RJAT Output Clock Divisor (N2) Control
04BH, 0CBH, 14BH, 1CBH, 24BH, 2CBH, 34BH, 3CBH	RJAT Configuration
04CH, 0CCH, 14CH, 1CCH, 24CH, 2CCH, 34CH, 3CCH	TJAT Interrupt Status
04DH, 0CDH, 14DH, 1CDH, 24DH, 2CDH, 34DH, 3CDH	TJAT Reference Clock Divisor (N1) Control
04EH, 0CEH, 14EH, 1CEH, 24EH, 2CEH, 34EH, 3CEH	TJAT Output Clock Divisor (N2) Control
04FH, 0CFH, 14FH, 1CFH, 24FH, 2CFH, 34FH, 3CFH	TJAT Configuration
050H, 0D0H, 150H, 1D0H, 250H, 2D0H, 350H, 3D0H	IBCD Configuration
051H, 0D1H, 151H, 1D1H, 251H, 2D1H, 351H, 3D1H	IBCD Interrupt Enable/Status
052H, 0D2H, 152H, 1D2H, 252H, 2D2H, 352H, 3D2H	IBCD Activate Code
053H, 0D3H, 153H, 1D3H, 253H, 2D3H, 353H, 3D3H	IBCD Deactivate Code
054H, 0D4H, 154H, 1D4H, 254H, 2D4H, 354H, 3D4H	CDRC Configuration
055H, 0D5H, 155H, 1D5H, 255H, 2D5H, 355H, 3D5H	CDRC Interrupt Control

Addr	Register
056H, 0D6H, 156H, 1D6H, 256H, 2D6H, 356H, 3D6H	CDRC Interrupt Status
057H, 0D7H, 157H, 1D7H, 257H, 2D7H, 357H, 3D7H	CDRC Alternate Loss of Signal
058H, 0D8H, 158H, 1D8H, 258H, 2D8H, 358H, 3D8H	PMON Interrupt Enable/Status
059H, 0D9H, 159H, 1D9H, 259H, 2D9H, 359H, 3D9H	PMON Reserved
05AH, 0DAH, 15AH, 1DAH, 25AH, 2DAH, 35AH, 3DAH	PMON Reserved
05BH, 0DBH, 15BH, 1DBH, 25BH, 2DBH, 35BH, 3DBH	PMON Reserved
05CH, 0DCH, 15CH, 1DCH, 25CH, 2DCH, 35CH, 3DCH	PMON Reserved
05DH, 0DDH, 15DH, 1DDH, 25DH, 2DDH, 35DH, 3DDH	PMON Reserved
05EH, 0DEH, 15EH, 1DEH, 25EH, 2DEH, 35EH, 3DEH	PMON LCV Count (LSB)
05FH, 0DFH, 15FH, 1DFH, 25FH, 2DFH, 35FH, 3DFH	PMON LCV Count (MSB)
060H, 0E0H, 160H, 1E0H, 260H, 2E0H, 360H, 3E0H	PRBS Generator/Checker Control
061H, 0E1H, 161H, 1E1H, 261H, 2E1H, 361H, 3E1H	PRBS Checker Interrupt Enable/Status
062H, 0E2H, 162H, 1E2H, 262H, 2E2H, 362H, 3E2H	PRBS Pattern Select
063H, 0E3H, 163H, 1E3H, 263H, 2E3H, 363H, 3E3H	PRBS Reserved
064H, 0E4H, 164H, 1E4H, 264H, 2E4H, 364H, 3E4H	PRBS Error Count #1
065H, 0E5H, 165H, 1E5H, 265H, 2E5H, 365H, 3E5H	PRBS Error Count #2
066H, 0E6H, 166H, 1E6H, 266H, 2E6H, 366H, 3E6H	PRBS Error Count #3
067H, 0E7H, 167H, 1E7H, 267H, 2E7H, 367H, 3E7H	PRBS Reserved

Addr	Register
068H, 0E8H, 168H, 1E8H, 268H, 2E8H, 368H, 3E8H	XLPG Control/Status
069H, 0E9H, 169H, 1E9H, 269H, 2E9H, 369H, 3E9H	XLPG Pulse Waveform Scale
06AH, 0EAH, 16AH, 1EAH, 26AH, 2EAH, 36AH, 3EAH	XLPG Pulse Waveform Storage Write Address #1
06BH, 0EBH, 16BH, 1EBH, 26BH, 2EBH, 36BH, 3EBH	XLPG Pulse Waveform Storage Write Address #2
06CH, 0ECH, 16CH, 1ECH, 26CH, 2ECH, 36CH, 3ECH	XLPG Pulse Waveform Storage Data
06DH, 0EDH, 16DH, 1EDH, 26DH, 2EDH, 36DH, 3EDH	XLPG Reserved
06EH, 0EEH, 16EH, 1EEH, 26EH, 2EEH, 36EH, 3EEH	XLPG Reserved
06FH, 0EFH, 16FH, 1EFH, 26FH, 2EFH, 36FH, 3EFH	XLPG Reserved
070H, 0F0H, 170H, 1F0H, 270H, 2F0H, 370H, 3F0H	RLPS Configuration and Status
071H, 0F1H, 171H, 1F1H, 271H, 2F1H, 371H, 3F1H	RLPS ALOS Detection/Clearance Threshold
072H, 0F2H, 172H, 1F2H, 272H, 2F2H, 372H, 3F2H	RLPS ALOS Detection Period
073H, 0F3H, 173H, 1F3H, 273H, 2F3H, 373H, 3F3H	RLPS ALOS Clearance Period
074H, 0F4H, 174H, 1F4H, 274H, 2F4H, 374H, 3F4H	RLPS Equalization Indirect Address
075H, 0F5H, 175H, 1F5H, 275H, 2F5H, 375H, 3F5H	RLPS Equalization Read/WriteB Select
076H, 0F6H, 176H, 1F6H, 276H, 2F6H, 376H, 3F6H	RLPS Equalizer Loop Status and Control
077H, 0F7H, 177H, 1F7H, 277H, 2F7H, 377H, 3F7H	RLPS Equalizer Configuration
078H, 0F8H, 178H, 1F8H, 278H, 2F8H, 378H, 3F8H	RLPS Equalization Indirect Data Register
079H, 0F9H, 179H, 1F9H, 279H, 2F9H, 379H, 3F9H	RLPS Equalization Indirect Data Register

Addr	Register
07AH, 0FAH, 17AH, 1FAH, 27AH, 2FAH, 37AH, 3FAH	RLPS Indirect Data Register
07BH, 0FBH, 17BH, 1FBH, 27BH, 2FBH, 37BH, 3FBH	RLPS Indirect Data Register
07CH, 0FCH, 17CH, 1FCH, 27CH, 2FCH, 37CH, 3FCH	RLPS Voltage Thresholds #1
07DH, 0FDH, 17DH, 1FDH, 27DH, 2FDH, 37DH, 3FDH	RLPS Voltage Thresholds #2
07EH, 0FEH, 17EH, 1FEH, 27EH, 2FEH, 37EH, 3FEH	RLPSReserved
07FH, 0FFH, 17FH, 1FFH, 27FH, 2FFH, 37FH, 3FFH	RLPS Reserved
400H – 7FFH	Reserved for Test

Register 000H: Reset / Revision ID / Device ID

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[2]	1
Bit 5	R	TYPE[1]	0
Bit 4	R	TYPE[0]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

RESET:

The RESET bit implements a software reset. If the RESET bit is a logic 1, the OCTLIU is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the OCTLIU out of reset. Holding the OCTLIU in a reset state effectively puts it into a low-power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

TYPE:

The device identification bits, TYPE[2:0], are set to a fixed value of “100”

ID:

The version identification bits, ID[3:0], are set to a fixed value representing the version number of the OCTLIU.

Register 001H: Global Configuration / Clock Monitor

Bit	Type	Function	Default
Bit 7	R	XCLKA	X
Bit 6	R	REFCLKA	X
Bit 5	R/W	SIMUL_REGWR	0
Bit 4	R/W	SBI_SYNCH	0
Bit 3	R/W	RSYNC_SEL[2] / ELST_SEL[2]	0
Bit 2	R/W	RSYNC_SEL[1] / ELST_SEL[1]	0
Bit 1	R/W	RSYNC_SEL[0] / ELST_SEL[0]	0
Bit 0	R/W	E1/T1B	0

XCLKA:

The XCLK active (XCLKA) bit detects low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read. A lack of transitions is indicated by the register bit reading low. This register bit may be read at periodic intervals to detect clock failures.

REFCLKA:

The REFCLK active (REFCLKA) bit detects low to high transitions on the REFCLK input. REFCLKA is set high on a rising edge of REFCLK, and is set low when this register is read. A lack of transitions is indicated by the register bit reading low. This register bit may be read at periodic intervals to detect clock failures.

SIMUL_REGWR:

The Simultaneous Register Write (SIMUL_REGWR) bit enables registers for all 8 octants to be written simultaneously. When SIMUL_REGWR is set high, a write to an octant register will result in the same data also being written simultaneously to the corresponding registers belonging to the other 7 octants. When SIMUL_REGWR is set low, a write to a register will result in the addressed register, and that register only, being written.

Note – SIMUL_REGWR must be set low prior to reading any OCTLIU register.

SBI_SYNCH:

The SBI Synchronous Mode (SBI_SYNCH) bit configures the INSBI to operate in SBI Synchronous mode when set to 1. Synchronous mode should only be selected when the device is operating as a SBI to clk/data converter (SBI2CLK input tied high). When operating in synchronous mode, the ICLK_OUT and IFP_OUT outputs **must** be used as clock and frame pulse references, but need not be looped back to the ICLK_IN and IFP_IN inputs. (In synchronous mode, the loopback is done internally and the ICLK_IN and IFP_IN inputs are ignored.)

RSYNC_SEL[2:0]:

When the SBI2CLK input is tied low, the RSYNC Select register bits, RSYNC_SEL[2:0], select the source of the RSYNC OCTLIU output.

When RSYNC_SEL[2:0] = “000”, octant #1 is selected as the source.
When RSYNC_SEL[2:0] = “001”, octant #2 is selected as the source.
When RSYNC_SEL[2:0] = “010”, octant #3 is selected as the source.
When RSYNC_SEL[2:0] = “011”, octant #4 is selected as the source.
When RSYNC_SEL[2:0] = “100”, octant #5 is selected as the source.
When RSYNC_SEL[2:0] = “101”, octant #6 is selected as the source.
When RSYNC_SEL[2:0] = “110”, octant #7 is selected as the source.
When RSYNC_SEL[2:0] = “111”, octant #8 is selected as the source.

ELST_SEL[2:0]:

When the SBI2CLK input is tied high, the Elastic Store Select register bits, ELST_SEL[2:0], select the source of the clock and frame pulse used to read data from the Elastic Stores. The clock and frame pulse are derived from one of the SBI tributaries de-mapped from the SBI BUS and are output on ECLK and EFP respectively.

When ELST_SEL[2:0] = “000”, EXSBI link #1 is selected as the source.
When ELST_SEL[2:0] = “001”, EXSBI link #2 is selected as the source.
When ELST_SEL[2:0] = “010”, EXSBI link #3 is selected as the source.
When ELST_SEL[2:0] = “011”, EXSBI link #4 is selected as the source.
When ELST_SEL[2:0] = “100”, EXSBI link #5 is selected as the source.
When ELST_SEL[2:0] = “101”, EXSBI link #6 is selected as the source.
When ELST_SEL[2:0] = “110”, EXSBI link #7 is selected as the source.
When ELST_SEL[2:0] = “111”, EXSBI link #8 is selected as the source.

E1/T1B:

The global E1/T1B bit selects the operating mode of all eight of the OCTLIU octants. If E1/T1B is logic 1, the 2.048 Mbit/s E1 mode is selected for all eight octants. If E1/T1B is logic 0, the 1.544 Mbit/s T1 mode is selected for all eight octants.

Register 002H: Master Interrupt Source #1

Bit	Type	Function	Default
Bit 7	R	LIU[8]	X
Bit 6	R	LIU[7]	X
Bit 5	R	LIU[6]	X
Bit 4	R	LIU[5]	X
Bit 3	R	LIU[4]	X
Bit 2	R	LIU[3]	X
Bit 1	R	LIU[2]	X
Bit 0	R	LIU[1]	X

<u>LIU[8:1]:</u>

The LIU[8:1] register bits allow software to determine which octant's LIU(s) is/are producing an interrupt on the INTB output pin. A logic 1 indicates an interrupt is being produced from the corresponding octant.

Reading this register does not remove the interrupt indication; within the corresponding octant, the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 003H: Master Interrupt Source #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	EXSBI	X
Bit 0	R	INSBI	X

INSBI, EXSBI:

The INSBI and EXSBI register bits allow software to determine whether the INSBI and/or EXSBI blocks are producing an interrupt on the INTB output pin. A logic 1 indicates an interrupt is being produced from the corresponding block.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 004H: Master Test Control #1

Bit	Type	Function	Default
Bit 7	W	Reserved	X
Bit 6	W	Reserved	X
Bit 5	W	Reserved	X
Bit 4	W	Reserved	X
Bit 3	W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select OCTLIU test features. All bits, except for 7,6,5 and 4 are reset to zero by a hardware reset of the OCTLIU, a software reset of the OCTLIU does not affect the state of the bits in this register.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the OCTLIU. While the HIZIO bit is a logic 1, all output pins of the OCTLIU except TDO and the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is held in a high-impedance state which inhibits microprocessor read cycles.

Register 005H: Master Test Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

Reserved:

These bits must be 0 for correct operation.

Register 006H: CSU Configuration

Bit	Type	Function	Default
Bit 7	R/W	CSU_RESET	0
Bit 6	R/W	IDDQ_EN	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	CSU_LOCK	X
Bit 2	R/W	MODE[2]	0
Bit 1	R/W	MODE[1]	0
Bit 0	R/W	MODE[0]	0

MODE[2:0]:

The MODE[2:0] selects the mode of the CSU. Table 5 indicates the required XCLK frequency, and output frequencies for each mode.

Table 5 – Clock Synthesis Mode

MODE[2:0]	XCLK frequency	Transmit clock frequency
000	2.048 MHz	2.048 MHz
001	1.544 MHz	1.544 MHz
01X	Reserved	Reserved
10X	Reserved	Reserved
110	Reserved	Reserved
111	2.048 MHz	1.544 MHz

CSU_LOCK:

The CSU_LOCK bit can be used to determine whether or not the embedded clock synthesis unit (CSU) has achieved phase and frequency lock to XCLK. If the CSU_LOCK bit is polled repetitively and is persistently a logic 1, then the divided down synthesized clock frequency is within 244 ppm of the XCLK frequency. A persistent logic 0 may indicate a mismatch between the actual and expected XCLK frequency or a problem with the analogue supplies (CAVS and CAVD).

IDDQ_EN:

The IDDQ enable bit (IDDQ_EN) is used to configure the embedded CSU for IDDQ tests. When IDDQ_EN is a logic 1, or the IDDQEN bit in the Master Test Control #1 register is a logic 1, the digital outputs of the CSU are pulled to ground. When either the IDDQ_EN bit or IDDQEN bit is set to logic 1, the HIGHZ bit in the XLPG Line Driver Configuration register must also be set to logic 1.

CSU_RESET:

Setting the CSU_RESET bit to logic 1 causes the embedded CSU to be forced to a frequency much lower than normal operation.

Register 008H, 088H, 108H, 188H, 208H, 288H, 308H, 388H: Receive Line Interface Configuration #1

Bit	Type	Function	Default
Bit 7	R/W	LLB_AIS	0
Bit 6	R/W	AUTO_LLB	0
Bit 5	R/W	LOS_SBI	0
Bit 4	R/W	LOS_AIS	0
Bit 3	R/W	RDUAL	0
Bit 2	R/W	BPV	0
Bit 1	R/W	RINV	0
Bit 0	R/W	RFALL	1

<u>LLB_AIS:</u>

When the LLB_AIS bit is set to logic 1, the LIU will generate AIS on the receive data output whenever line loopback is active. When the LLB_AIS bit is set to logic 0, the LIU receive path will operate normally, regardless of whether or not line loopback is active. If LLB_AIS is logic 0, AIS may be inserted manually via the RAIS register bit.

<u>AUTO_LLB:</u>

When the AUTO_LLB bit is set to logic 1, the LIU will activate and deactivate line loopback automatically upon detection of the line loopback activate/deactivate codes by the IBCD. The AUTO_LLB bit is only valid in T1 mode and must be set to logic 0 in E1 mode.

<u>LOS_SBI:</u>

The LOS_SBI bit enables the indication of loss of signal over the SBI interface. When LOS_SBI is set to logic 1, loss of signal will result in the ALM (alarm) bit of the affected tributary being asserted on the SBI interface. When LOS_SBI is set to logic 0, the tributary's ALM bit will be set to 0.

<u>LOS_AIS:</u>

If the LOS_AIS bit is logic 1, AIS is inserted in the receive path for the duration of a loss of signal condition. [ref: T1.403-1995 Annex H]. If LOS_AIS is logic 0, AIS may be inserted manually via the RAIS register bit.

<u>RDUAL:</u>

The RDUAL bit configures the LIU receive path for dual-rail (bipolar) operation. When RDUAL is set to logic 1, NRZ sampled bipolar positive and negative pulses are output on RDP[n] and RDN[n] respectively. When RDUAL is set to logic 0, NRZ sampled unipolar data is output on RDP[n] (decoded according to AMI, B8ZS or HDB3) and line code violations / excessive zeros are signalled on RLCV[n].

If RDUAL is set to logic 1, the PDVD, IBCD and PRBS blocks, and also the ability to generate AIS, are disabled in the LIU receive path.

BPV:

In T1 mode, the BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPV is set to logic 1, BPVs (provided they are not part of a valid B8ZS signature if B8ZS line coding is used) generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (provided they are not part of a valid B8ZS signature if B8ZS line coding is used) and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than fifteen bits long for an AMI-coded signal and greater than seven bits long for a B8ZS-coded signal.

In E1 mode, the BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. (The O162 bit in the CDRC Configuration register provides two E1 LCV definitions.) When BPV is set to logic 1, BPVs (provided they are not part of a valid HDB3 signature if HDB3 line coding is used) generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (provided they are not part of a valid HDB3 signature if HDB3 line coding is used) and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than fifteen bits long for an AMI-coded signal and greater than four bits long for an HDB3-coded signal.

RINV:

When RINV is set to logic 1, the receive digital outputs RDP[n] and RDN/RLCV[n] are assumed to be active low and all output data and LCV indications are inverted. When RINV is set to logic 0, the receive digital outputs RDP[n] and RDN/RLCV[n] are assumed to be active high. RINV must be set to 0 when the SBI interface is enabled (SBI_EN = 1).

RFALL:

When RFALL is set to logic 1, the RDP[n] and RDN/RLCV[n] outputs are updated on falling edges of RCLK[n]. When RFALL is set to logic 0, the outputs are updated on rising edges of RCLK[n]. RFALL must be set to 1 when the SBI interface is enabled (SBI_EN = 1).

Register 009H, 089H, 109H, 189H, 209H, 289H, 309H, 389H: Receive Line Interface Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	RJATBYP	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	RSYNC_ALOSB	0
Bit 1	R/W	RSYNC_MEM	0
Bit 0	R/W	RSYNCSEL	0

RJATBYP:

The RJATBYP bit disables jitter attenuation in the receive direction. When receive jitter attenuation is not being used, setting RJATBYP to logic 1 will reduce the latency through the receiver section by typically 40 bits. When RJATBYP is set to logic 0, the LIU's RSYNC output is jitter attenuated. When the RJAT is bypassed, the octant's RSYNC is not jitter attenuated.

RSYNC_ALOSB:

The RSYNC_ALOSB bit controls the source of the loss of signal condition used to control the behaviour of the receive reference presented on the RSYNC output. If RSYNC_ALOSB is a logic 0, analogue loss of signal is used. If RSYNC_ALOSB is a logic 1, digital loss of signal is used. When the LIU is in a loss of signal state, the RSYNC output is derived from XCLK or held high, as determined by the RSYNC_MEM bit. When the LIU is not in a loss of signal state, the RSYNC output is derived from the receive recovered clock of the selected octant.

The octant to be used as the source of RSYNC is determined by the RSYNC_SEL[2:0] bits.

RSYNC_MEM:

The RSYNC_MEM bit controls the octant's RSYNC output under a loss of signal condition (as determined by the RSYNC_ALOSB register bit). When RSYNC_MEM is a logic 1, the octant's RSYNC output is held high during a loss of signal condition. When RSYNC_MEM is a logic 0, the octant's RSYNC output is derived from the CSU 1x line rate clock during a loss of signal condition.

RSYNCSEL:

The RSYNCSEL bit selects the frequency of the receive reference presented on the octant's RSYNC output. If RSYNCSEL is a logic 1, the octant's RSYNC will be an 8 kHz clock. If

RSYNCSEL is a logic 0, the octant's RSYNC will be an 1.544 MHz (T1) or 2.048 MHz (E1) clock.

Register 00AH, 08AH, 10AH, 18AH, 20AH, 28AH, 30AH, 38AH: Transmit Line Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	TJATBYP	0
Bit 6	R/W	TAISEN	0
Bit 5	R/W	TAUXP	0
Bit 4	R/W	SBI_AIS	1
Bit 3	R/W	TDUAL	0
Bit 2	R/W	AMI	0
Bit 1	R/W	TINV	0
Bit 0	R/W	TRISE	1

TJATBYP:

The TJATBYP bit enables the transmit jitter attenuator to be removed from the transmit data path. When the transmit jitter attenuator is bypassed, the latency through the transmitter section is reduced by typically 40 bits.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TXTIP[n] and TXRING[n]. When TAISEN is set to logic 1, the bipolar TXTIP[n] and TXRING[n] outputs are forced to pulse alternately, creating an all-ones signal. The transition to transmitting AIS on the TXTIP[n] and TXRING[n] outputs is done in such a way as to avoid introducing any bipolar violations.

The diagnostic digital loopback point is prior to the AIS insertion point.

(Implementation note. TAISEN has priority over TAUXP, which in turn has priority over TDATINV.).

TAUXP:

The TAUXP bit enables the interface to generate an unframed alternating zeros and ones (i.e. 010101…) auxiliary pattern (AUXP) on the TXTIP[n] and TXRING[n]. When TAUXP is set to logic 1, the bipolar TXTIP[n] and TXRING[n] outputs are forced to pulse alternately every other cycle. The transition to transmitting AUXP on the TXTIP[n] and TXRING[n] outputs is done in such a way as to avoid introducing any bipolar violations.

The diagnostic digital loopback point is prior to the AUXP insertion point.

SBI_AIS:

The SBI_AIS bit enables the insertion of AIS in the transmit path in response to an alarm indication from the SBI interface. When SBI_AIS is set to logic 1, setting the ALM (alarm) bit of a tributary on the SBI interface causes the bipolar TXTIP[n] and TXRING[n] outputs to be forced to pulse alternately, creating an all-ones signal. The transition to transmitting AIS on the TXTIP[n] and TXRING[n] outputs is done in such a way as to avoid introducing any bipolar violations.

The diagnostic digital loopback point is prior to the AIS insertion point.

TDUAL:

The TDUAL bit configures the LIU transmit path for dual-rail (bipolar) operation. When TDUAL is set to logic 1, NRZ bipolar positive and negative data is input on TDP[n] and TDN[n] respectively. When TDUAL is set to logic 0, NRZ unipolar data is input on TDP[n] and TDN[n] is ignored. TDUAL must be set to logic 0 when operating in SBI mode (i.e. when the SBI_EN input is logic 1).

If TDUAL is set to logic 1, the XIBC, XPDE, LCODE and PRBS blocks are disabled in the LIU transmit path.

AMI:

The AMI bit enables AMI line coding. If AMI is set to a logic 1, the LIU will perform AMI line encoding on the TDP[n] single-rail input data stream. If AMI is set to a logic 0, the LIU will perform B8ZS (if operating in T1 mode) or HDB3 (if operating in E1 mode) line encoding on the TDP[n] data stream. The AMI bit is ignored if the TDUAL bit is set to logic 1.

TINV:

When TINV is set to logic 1, the transmit digital inputs TDP[n] and TDN[n] are assumed to be active low and all input data is inverted. When TINV is set to logic 0, the transmit digital inputs TDP[n] and TDN[n] are assumed to be active high.

TRISE:

When TRISE is set to logic 1, the TDP[n] and TDN[n] inputs are sampled on rising edges of TCLK[n]. When TRISE is set to logic 0, the inputs are sampled on falling edges of TCLK[n].

**Register 00BH, 08BH, 10BH, 18BH, 20BH, 28BH, 30BH, 38BH:
Transmit Timing Options / Clock Monitor / Pulse Template Selection**

Bit	Type	Function	Default
Bit 7	R/W	PT_SEL[3]	0
Bit 6	R/W	PT_SEL[2]	0
Bit 5	R/W	PT_SEL[1]	0
Bit 4	R/W	PT_SEL[0]	0
Bit 3	R	TCLKA	X
Bit 2	R/W	OCLKSEL	0
Bit 1	R/W	PLLREF[1]	0
Bit 0	R/W	PLLREF[0]	0

PT_SEL[3:0]:

The Pulse Template Selection (PT_SEL[3:0]) bits determine which of the twelve pulse template waveforms stored in the XLPG is used to generate transmit data pulses on the TXTIP[n] and TXRING[n] outputs. PT_SEL[3:0] must be set to a value between 0 and 11.

PT_SEL[3:0] are not used when operating in hardware-only mode (HW_ONLY input = 1). In hardware-only mode, the LENx[2:0] inputs select which pulse template is to be used and only pulse templates 0 to 7 may be selected.

TCLKA:

The TCLK[n] active (TCLKA) bit detects low to high transitions on the TCLK[n] input. TCLKA is set high on a rising edge of TCLK[n], and is set low when this register is read. A lack of transitions is indicated by the register bit reading low. This register bit may be read at periodic intervals to detect clock failures.

OCLKSEL:

The OCLKSEL bit selects the source of the Transmit Jitter Attenuator FIFO output clock signal.

Table 6 – TJAT FIFO Output Clock Source

OCLKSEL	Source of FIFO Output Clock
0	The TJAT FIFO output clock is connected to the internal jitter-attenuated 1.544 MHz or 2.048 MHz clock.
1	The TJAT FIFO output clock is connected to the FIFO input clock. In this mode the jitter attenuation is disabled and the input clock must be jitter-free. PLLREF[1:0] must be set to “00” in this mode.

<u>PLLREF:</u>

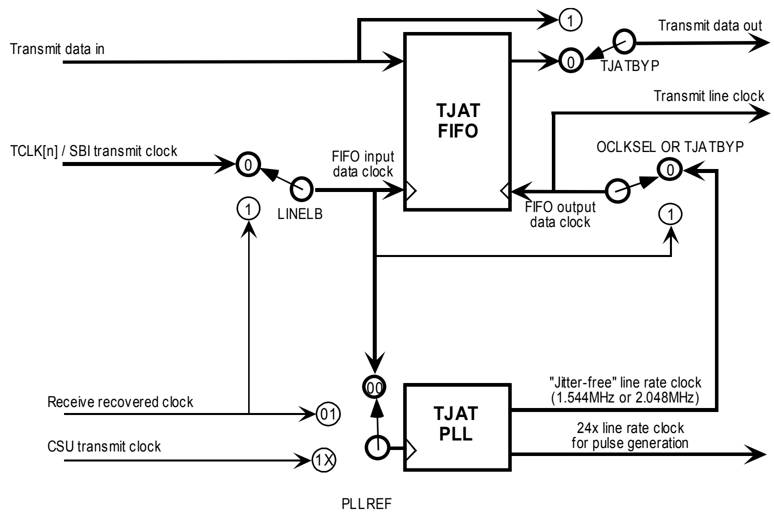
The PLLREF bit selects the source of the Transmit Jitter Attenuator phase locked loop reference signal as follows:

Table 7 – TJAT PLL Source

PLLREF[1:0]	Source of PLL Reference
00	TJAT FIFO input clock (either the transmit clock or the receive recovered clock, as selected by LINELB)
01	Receive recovered clock
1X	CSU transmit clock (see Table 5)

Upon reset of the OCTLIU, the OCLKSEL and PLLREF bits are cleared to zero, selecting jitter attenuation with transmit line clock referenced to the transmit clock, TCLK[n] (or the SBI tributary clock). Figure 17 illustrates the various bit setting options, with the reset condition highlighted.

Figure 17 – Transmit Timing Options



**Register 00CH, 08CH, 10CH, 18CH, 20CH, 28CH, 30CH, 38CH:
Line Interface Interrupt Source #1 / PMON Update**

Bit	Type	Function	Default
Bit 7	R	PMON	X
Bit 6	R	PRBS	X
Bit 5	R	IBCD	X
Bit 4	R	PDVD	X
Bit 3	R	XPDE	X
Bit 2	R	TJAT	X
Bit 1	R	RJAT	X
Bit 0	R	CDRC	X

This register allows software to determine the block which produced the interrupt on the INTB output pin. A logic 1 indicates an interrupt was produced from the block.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Writing any value to this register causes the octant's performance monitor LCV counter and PRBS error counter to be updated.

Register 00DH, 08DH, 10DH, 18DH, 20DH, 28DH, 30DH, 38DH:
Line Interface Interrupt Source #2

Bit	Type	Function	Default
Bit 7	R	ELST	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	RLPS	X

This register allows software to determine the block that produced the interrupt on the INTB output pin. A logic 1 indicates an interrupt was produced from the block.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 00EH, 08EH, 10EH, 18EH, 20EH, 28EH, 30EH, 38EH: Line Interface Diagnostics

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	LCVINS	0
Bit 4	R/W	LINELB	0
Bit 3	R/W	RAIS	0
Bit 2	R/W	DDLB	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

LCVINS:

The LCVINS bit introduces a single line code violation on the transmitted data stream. In B8ZS, the violation is generated by masking the first violation pulse of a B8ZS signature. In AMI, one pulse is sent with the same polarity as the previous pulse. In HDB3, the violation is generated by causing the next HDB3-code generated bipolar violation pulse to be of the same polarity as the previous bipolar violation. To generate another violation, this bit must first be written to 0 and then to logic 1 again. At least one bit period should elapse between writing LCVINS 0 and writing it 1 again, or vice versa, if an error is to be successfully inserted. LCVINS has no effect when TDUAL is set to logic 1.

LINELB:

The LINELB bit selects the line loopback mode, where the recovered data are internally directed to the digital inputs of the transmit jitter attenuator. The data sent to the TJAT is the recovered data from the output of the CDRC block. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. Note that when line loopback is enabled, to correctly attenuate the jitter on the receive clock, the contents of the TJAT Reference Clock Divisor and Output Clock Divisor registers should be programmed to 2FH in T1 mode / FFH in E1 mode and the Transmit Timing Options register should be cleared to all zeros. Only one of LINELB and DDLB can be enabled at any one time.

RAIS:

When the RAIS bit is set to logic 1, the receive output data stream of the octant is forced to all ones.

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the octant is configured to internally direct the output of the TJAT to the inputs of the receiver section. The dual-rail RZ outputs of the TJAT are directed to the dual-rail inputs of the CDRC. When DDLB is set to logic 1, the diagnostic digital loopback mode is enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled. Only one of LINELB and DDLB can be enabled at any one time.

Reserved:

These bits must be a logic 0 for correct operation.

Register 00FH, 08FH, 10FH, 18FH, 20FH, 28FH, 30FH, 38FH: Line Interface PRBS Position

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	TX_GEN	0
Bit 1	R/W	RX_GEN	0
Bit 0	R/W	TX_DET	0

TX_GEN:

The Transmit Path Generate, TX_GEN, bit controls the output of the PRBS generator. When TX_GEN is set to logic 1, the PRBS generator output is inserted into the transmit path. When TX_GEN is set to logic 0, the transmit path functions normally.

RX_GEN:

The Receive Path Generate, RX_GEN, bit controls the output of the PRBS generator. When RX_GEN is set to logic 1, the PRBS generator output is inserted into the receive path. When RX_GEN is set to logic 0, the receive path functions normally.

TX_DET:

The Transmit Path Detect, TX_DET, bit controls the input of the PRBS checker. When TX_DET is set to logic 1, the PRBS checker monitors the transmit path. When TX_DET is set to logic 0, the PRBS detector monitors the receive path.

Register 310H: INSBI Control

Bit	Type	Function	Default
Bit 7	R/W	APAGE	0
Bit 6	R/W	DC_ENBL	1
Bit 5	R/W	DC_INT_EN	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	TS_EN	0
Bit 1		Unused	X
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for generation of the SBI data parity signal, DDP as follows:

- When SBI_PAR_CTL is a ‘0’ parity will be even.
- When SBI_PAR_CTL is a ‘1’ parity will be odd.

TS_EN:

The TS_EN bit is used to enable the SBI tributary to LIU octant data stream mapping capability.

- When TS_EN is a ‘0’, the mapping is fixed to a one to one mapping and is not programmable. The 8 LIU data streams are mapped to tributaries 1 to 8 of SPE #1 within the SBI structure.
- When TS_EN is a ‘1’, SBI tributary to LIU octant data stream mapping is enabled and is specified by the contents of the INSBI Tributary Mapping registers.

FIFO_UDRE:

The FIFO_UDRE bit is used to enable/disable the generation of an interrupt when a FIFO underrun is detected.

- When FIFO_UDRE is a ‘0’ underrun interrupt generation is disabled.
- When FIFO_UDRE is a ‘1’ underrun interrupt generation is enabled.

FIFO_OVRE:

The FIFO_OVRE bit is used to enable/disable the generation of an interrupt when a FIFO overrun is detected.

- When FIFO_OVRE is a ‘0’ overrun interrupt generation is disabled.

- When FIFO_OVRE is a ‘1’ overrun interrupt generation is enabled.

DC_INT_EN:

This bit is set to enable the generation of an interrupt when either of the following events occurs:

- A Depth Check error
- An external resynchronization event occurs on the DC1FP signal

DC_ENBL:

This bit enables depth check resets. The depth checker periodically monitors the link FIFO depths and compares them against the read and write pointers. Discrepancies are reported in the Depth Checker Interrupt Status Register. If DC_ENBL is ‘1’, the affected link is automatically reset. If DC_ENBL is ‘0’, the link is not reset.

APAGE:

The tributary mapping register active page select bit (APAGE) controls the selection of one of two pages of tributary mapping registers. When APAGE is set low, the configuration in page A of the tributary mapping registers is used to associate SBI tributaries to LIU octant data streams. When APAGE is set high, the configuration in page B of the tributary mapping registers is used to associate SBI tributaries to LIU octant data streams. When APAGE changes state, any data streams where the mapping registers do not match are automatically reset.

Register 311H: INSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	FIFO_UDRI	0

FIFO_UDRI:

This bit is set when a FIFO underrun is detected. It is cleared when the register is read (but may be set again immediately thereafter if a further underrun report is pending).

LINK[3:0]:

The LINK[3:0] field is used to specify the LIU octant data stream associated with the FIFO buffer in which the underrun was detected. LINK[3:0] should only be looked at when FIFO_UDRI is a ‘1’. Valid values of LINK[3:0] are from 1 to 8.

This register will contain the interrupt status even if the corresponding interrupt enable is not set.

Register 312H: INSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	FIFO_OVRI	0

FIFO_OVRI:

This bit is set when a FIFO overrun is detected. It is cleared when the register is read (but may be set again immediately thereafter if a further overrun report is pending).

LINK[3:0]:

The LINK[3:0] field is used to specify the LIU octant data stream associated with the FIFO buffer in which the overrun was detected. LINK[3:0] should only be looked at when FIFO_OVRI is a ‘1’. Valid values of LINK[3:0] are from 1 to 8.

This register will contain the interrupt status even if the corresponding interrupt enable is not set.

Register 313H – 31AH: INSBI Page A Octant to Tributary Mapping #1 - #8

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

SPE[1:0] and TRIB[4:0]:

The SPE[1:0] and TRIB[4:0] fields are used to specify the LIU octant data stream to SBI tributary mapping when APAGE is set to 0. The output of the octant corresponding to the register (1-8) is mapped to the SPE and tributary specified by the value of SPE[1:0] and TRIB[4:0]. Valid values of SPE[1:0] are from 1 to 3. Valid values of TRIB[4:0] are from 1 to 28 in T1 mode and from 1 to 21 in E1 mode.

Note: The mapping of more than one tributary to the same LIU octant data stream or more than one LIU octant data stream to the same tributary is not allowed. Special care must be taken to ensure that all LIU octants and tributaries are uniquely mapped when using multiple OCTLIU's on the same SBI bus. Failure to do so will result in bus contention.

Register 31BH – 322H: INSBI Page B Octant to Tributary Mapping #1 - #8

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

SPE[1:0] and TRIB[4:0]:

The SPE[1:0] and TRIB[4:0] fields are used to specify the LIU octant data stream to SBI tributary mapping when APAGE is set to 1. The output of the octant corresponding to the register (1-8) is mapped to the SPE and tributary specified by the value of SPE[1:0] and TRIB[4:0]. Valid values of SPE[1:0] are from 1 to 3. Valid values of TRIB[4:0] are from 1 to 28 in T1 mode and from 1 to 21 in E1 mode.

Note: The mapping of more than one tributary to the same LIU octant data stream or more than one LIU octant data stream to the same tributary is not allowed. Special care must be taken to ensure that all LIU octants and tributaries are uniquely mapped when using multiple OCTLIU's on the same SBI bus. Failure to do so will result in bus contention.

Register 323H: INSBI Link Enable

Bit	Type	Function	Default
Bit 7	R/W	ENBL8	0
Bit 6	R/W	ENBL7	0
Bit 5	R/W	ENBL6	0
Bit 4	R/W	ENBL5	0
Bit 3	R/W	ENBL4	0
Bit 2	R/W	ENBL3	0
Bit 1	R/W	ENBL2	0
Bit 0	R/W	ENBL1	0

<u>ENBL1 – ENBL8:</u>

The ENBLx bits are used to enable the LIU octant data streams. Setting the ENBL bit for a particular LIU octant data stream enables the INSBI8 to take data from the octant and transmit that data to the SBI tributary mapped to that stream.

Register 324H: INSBI Link Enable Busy

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	BUSY	0

BUSY:

A write to the INSBI Link Enable Register sets BUSY to ‘1’. BUSY is cleared to ‘0’ approximately three REFCLK cycles later after the register contents have been synchronized to REFCLK.

The user must check that BUSY is ‘0’ before writing to the INSBI Link Enable Register.

Following a reset, BUSY will be ‘1’ until startup circuitry has finished automatically initializing certain RAMs within INSBI.

Register 325H – 32CH: INSBI Tributary Control #1 – #8

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	TRIB_TYP[1]	1
Bit 1	R/W	TRIB_TYP[0]	0
Bit 0	R/W	Reserved	0

A tributary control register should only be written when the associated ENBLx bit is ‘0’.

Reserved:

The reserved bits must be set to 0 for correct operation of the OCTLIU device.

TRIB_TYP[1:0]:

The TRIB_TYP[1:0] field specifies the characteristics of the SBI tributary, as shown in Table 8.

Table 8 – INSBI Tributary Characteristics

TRIB_TYP[1:0]	Description
00	Reserved.
01	Framed (IFP_IN determines frame alignment).
10	Unframed (IFP_IN ignored).
11	Reserved.

The TRIB_TYP[1:0] bits must be set to “10” whenever the LIUs are enabled (SBI2CLK tied low).

Register 32DH: INSBI Minimum Depth

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MIN_DEP[3]	0
Bit 2	R/W	MIN_DEP[2]	1
Bit 1	R/W	MIN_DEP[1]	1
Bit 0	R/W	MIN_DEP[0]	1

MIN_DEP [3:0]:

The MIN_DEPTH[3:0] bits specify the tributary FIFO Minimum Depth, i.e. the depth that must be reached before the FIFO reader starts to take data from the FIFO.

Register 32EH: INSBI FIFO Thresholds

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR[3]	0
Bit 6	R/W	MIN_THR[2]	1
Bit 5	R/W	MIN_THR[1]	1
Bit 4	R/W	MIN_THR[0]	0
Bit 3	R/W	MAX_THR[3]	1
Bit 2	R/W	MAX_THR[2]	1
Bit 1	R/W	MAX_THR[1]	1
Bit 0	R/W	MAX_THR[0]	0

<u>MIN_THR[3:0]:</u>

The MIN_THR[3:0] bits specify the tributary FIFO minimum threshold, i.e. the FIFO depth below which a positive justification is performed.

Note – The default value of this register is the recommended value when operating in T1 mode. When operating in E1 mode, it is recommended that MIN_THR[3:0] be set to “0010”.

<u>MAX_THR[3:0]:</u>

The MAX_THR[3:0] bits specify the tributary FIFO maximum threshold, i.e. the FIFO depth which when exceeded will cause a negative justification.

Register 331H: INSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	DCR_INTI	0

DCR_INTI:

This bit is set when a depth check error is detected. It is cleared when the register is read (but may be set again immediately thereafter if a further depth check error report is pending).

LINK[3:0]:

The LINK[3:0] field is used to specify the LIU octant data stream associated with the FIFO buffer in which the depth check error was detected. LINK[3:0] should only be looked at when DCR_INTI is a '1'. Valid values for LINK[3:0] are from 1 to 8.

This register will contain the interrupt status even if the corresponding interrupt enable is not set.

Register 332H: INSBI Master Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	DCR_INTI_SHDW	0
Bit 4		Unused	X
Bit 3	R	FIFO_UDRI_SHDW	0
Bit 2	R	FIFO_OVRI_SHDW	0
Bit 1		Unused	X
Bit 0	R	C1FP_SYNC_INTI	0

C1FP_SYNC_INTI:

This bit is set when a DC1FP realignment has been detected. It is cleared when the register is read.

FIFO_OVRI_SHDW:

This bit is a shadow of the FIFO_OVRI bit in the INSBI FIFO Over Run Interrupt Status Register. It is set when the FIFO_OVRI bit is set and the interrupt enable FIFO_OVRE is set. Reading this register has no affect on the interrupt status.

FIFO_UDRI_SHDW:

This bit is a shadow of the FIFO_UDRI bit in the INSBI FIFO Under Run Interrupt Status Register. It is set when the FIFO_UDRI bit is set and the interrupt enable FIFO_UDRE is set. Reading this register has no affect on the interrupt status.

DCR_INTI_SHDW:

This bit is a shadow of the DCR_INTI bit in the INSBI Depth Check Interrupt Status Register. It is set when the DCR_INTI bit is set and the interrupt enable DCR_INT_EN is set. Reading this register has no affect on the interrupt status.

Register 390H: EXSBI Control

Bit	Type	Function	Default
Bit 7	R/W	APAGE	0
Bit 6	R/W	DC_ENBL	1
Bit 5	R/W	DC_INT_EN	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	TS_EN	0
Bit 1	R/W	SBI_PERR_EN	0
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for checking of the SBI data parity signal, ADP as follows:

- When SBI_PAR_CTL is a ‘0’ parity will be even.
- When SBI_PAR_CTL is a ‘1’ parity will be odd.

SBI_PERR_EN:

The SBI_PERR_EN bit is used to enable the SBI Parity Error interrupt generation

- When SBI_PERR_EN is ‘0’ SBI Parity Error Interrupts will be disabled
- When SBI_PERR_EN is ‘1’ SBI Parity Error Interrupts will be enabled

In both cases the SBI Parity checker logic will update the SBI Parity Error Interrupt Reason Register.

TS_EN:

The TS_EN bit is used to enable the SBI tributary to LIU octant data stream mapping capability.

- When TS_EN is a ‘0’, the mapping is fixed to a one to one mapping and is not programmable. The 8 LIU data streams are mapped to tributaries 1 to 8 of SPE #1 within the SBI structure.
- When TS_EN is a ‘1’, SBI tributary to LIU octant data stream mapping is enabled and is specified by the contents of the EXSBI Tributary Mapping registers.

FIFO_UDRE:

The FIFO_UDRE bit is used to enable/disable the generation of an interrupt when a FIFO underrun is detected.

- When FIFO_UDRE is a '0' underrun interrupt generation is disabled.
- When FIFO_UDRE is a '1' underrun interrupt generation is enabled.

FIFO_OVRE:

The FIFO_OVRE bit is used to enable/disable the generation of an interrupt when a FIFO overrun is detected.

- When FIFO_OVRE is a '0' overrun interrupt generation is disabled.
- When FIFO_OVRE is a '1' overrun interrupt generation is enabled.

DC_INT_EN:

This bit is set to enable the generation of an interrupt when either of the following events occurs:

- A Depth Check error
- An external resynchronization event occurs on the AC1FP signal

DC_ENBL:

This bit enables depth check resets. The depth checker periodically monitors the link FIFO depths and compares them against the read and write pointers. Discrepancies are reported in the Depth Checker Interrupt Status Register. If DC_ENBL is '1', the affected link is automatically reset. If DC_ENBL is '0', the link is not reset.

APAGE:

The tributary mapping active page select bit (APAGE) controls the group of mapping registers used to associate SBI tributaries and LIU octant data streams. When mapping is enabled and APAGE is low, the A set of mapping registers (0x3A8 to 0x3AF) is used. When mapping is enabled and APAGE is high, the B set of mapping registers (0x3B0 to 0x3B7) is used. When APAGE changes state, any data streams where the mapping registers do not match are automatically reset.

Register 391H: EXSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	FIFO_UDRI	0

FIFO_UDRI:

This bit is set when a FIFO underrun is detected. It is cleared when the register is read.

LINK[3:0]:

The LINK[3:0] field is used to specify the LIU octant data stream associated with the FIFO buffer in which the underrun was detected. LINK[3:0] should only be looked at when FIFO_UDRI is a ‘1’. Valid values of LINK[3:0] are from 1 to 8.

This register will contain the interrupt status even if the corresponding interrupt enable is not set.

Register 392H: EXSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	FIFO_OVRI	0

FIFO_OVRI:

This bit is set when a FIFO overrun is detected. It is cleared when the register is read.

LINK[3:0]:

The LINK[3:0] field is used to specify the LIU octant data stream associated with the FIFO buffer in which the over-run was detected. LINK[3:0] should only be looked at when FIFO_OVRI is a ‘1’. Valid values of LINK[3:0] are from 1 to 8.

This register will contain the interrupt status even if the corresponding interrupt enable is not set.

Register 393H: EXSBI Parity Error Interrupt Reason

Bit	Type	Function	Default
Bit 7	R	SPE[1]	0
Bit 6	R	SPE[0]	0
Bit 5	R	TRIB[4]	0
Bit 4	R	TRIB[3]	0
Bit 3	R	TRIB[2]	0
Bit 2	R	TRIB[1]	0
Bit 1	R	TRIB[0]	0
Bit 0	R	PERRI	0

PERRI:

When set PERRI indicates that an SBI parity error has been detected. It is cleared when the register is read.

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] field are used to specify the SBI tributary for which a parity error was detected. These fields are only valid only when PERRI is set. When a parity error has not been detected the TRIB[4:0] field may contain an out of range tributary value.

If the type of the SPE where the parity error occurred does not correspond to the operating mode of the OCTLIU (e.g. a parity error in a SPE containing E1s when the OCTLIU is operating in T1 mode), SPE[1:0] will be valid but TRIB[4:0] will be invalid.

Values in these fields should only be looked at when PERRI is a ‘1’.

Register 394H: EXSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	DCRI	0

DCRI:

This bit is set when a Depth Check error is detected. It is cleared when the register is read.

LINK[3:0]:

The LINK[3:0] field is used to specify the LIU octant data stream associated with the FIFO buffer in which the depth check error was detected. LINK[3:0] should only be looked at when DCRI is a ‘1’. Valid values for LINK[3:0] are from 1 to 8.

This register will contain the interrupt status even if the corresponding interrupt enable is not set.

Register 395H: EXSBI Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	DCRI_SHDW	0
Bit 4	R	PERRI_SHDW	0
Bit 3	R	FIFO_UDRI_SHDW	0
Bit 2	R	FIFO_OVRI_SHDW	0
Bit 1		Unused	X
Bit 0	R	C1FP_SYNCI	0

C1FP_SYNCI:

This bit is set when a AC1FP realignment has been detected. Reading this register clears this interrupt source.

FIFO_OVRI_SHDW:

This bit is a shadow of the FIFO_OVRI bit in the EXSBI FIFO Overrun Interrupt Status Register. It is set when the FIFO_OVRI bit is set and the interrupt enable FIFO_OVRE is set. Reading this register has no affect on this interrupt source.

FIFO_UDRI_SHDW:

This bit is a shadow of the FIFO_UDRI bit in the EXSBI FIFO Underrun Interrupt Status Register. It is set when the FIFO_UDRI bit is set and the interrupt enable FIFO_UDRE is set. Reading this register has no affect on this interrupt source.

PERRI_SHDW:

This bit is a shadow of the PERRI bit in the EXSBI Parity Error Interrupt Reason Register. It is set when the PERRI bit is set and the interrupt enable SBI_PERR_EN is set. Reading this register has no affect on this interrupt source.

DCRI_SHDW:

This bit is a shadow of the DCRI bit in the EXSBI Depth Check Interrupt Status Register. It is set when the DCRI bit is set and the interrupt enable DCR_INT_EN is set. Reading this register has no affect on this interrupt source.

Reserved:

The reserved bit must be set to 0 for correct operation of the OCTLIU device.

Register 396H: EXSBI Minimum Depth

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	MIN_DEP[3]	0
Bit 2	R/W	MIN_DEP[2]	1
Bit 1	R/W	MIN_DEP[1]	1
Bit 0	R/W	MIN_DEP[0]	1

MIN_DEP[3:0]:

The MIN_DEPTH[3:0] bits specify the tributary FIFO Minimum Depth, i.e. the depth that must be reached before the FIFO reader starts to take data from the FIFO.

Register 397H: EXSBI FIFO Thresholds

Bit	Type	Function	Default
Bit 7	R/W	MIN_THR[3]	0
Bit 6	R/W	MIN_THR[2]	0
Bit 5	R/W	MIN_THR[1]	1
Bit 4	R/W	MIN_THR[0]	0
Bit 3	R/W	MAX_THR[3]	1
Bit 2	R/W	MAX_THR[2]	1
Bit 1	R/W	MAX_THR[1]	0
Bit 0	R/W	MAX_THR[0]	1

MIN_THR[3:0]:

The MIN_THR[3:0] bits specify the tributary FIFO minimum threshold, i.e. the FIFO depth below which the serial data stream to the LIU octant is slowed down (when CLK_MODE[1:0] = “00” in the EXSBI Tributary Control Register for the octant).

MAX_THR[3:0]:

The MAX_THR[3:0] bits specify the tributary FIFO maximum threshold, i.e. the FIFO depth above which the serial data stream to the LIU octant is sped up (when CLK_MODE[1:0] = “00” in the EXSBI Tributary Control Register for the octant).

Register 398H: EXSBI Link Enable

Bit	Type	Function	Default
Bit 7	R/W	LINK_ENBL[8]	0
Bit 6	R/W	LINK_ENBL[7]	0
Bit 5	R/W	LINK_ENBL[6]	0
Bit 4	R/W	LINK_ENBL[5]	0
Bit 3	R/W	LINK_ENBL[4]	0
Bit 2	R/W	LINK_ENBL[3]	0
Bit 1	R/W	LINK_ENBL[2]	0
Bit 0	R/W	LINK_ENBL[1]	0

LINK_ENBL[8:1]:

The LINK_ENBL[8:1] bits enable the operation of the corresponding LIU octant data streams. When LINK_ENBL is ‘1’ for a stream, the EXSBI8 will take data from an SBI tributary and transmit that data to the LIU octant. The tributary to octant mapping is determined by the Octant to Tributary Mapping Registers and APAGE.

Register 399H: EXSBI Link Enable Busy

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	BUSY	0

BUSY:

A write to the EXSBI Link Enable Register sets BUSY to ‘1’. BUSY is cleared to ‘0’ approximately three REFCLK cycles later after the register contents have been synchronized to REFCLK.

The user must check that BUSY is ‘0’ before writing to the EXSBI Link Enable Register.

Following a reset, BUSY will be ‘1’ until startup circuitry has finished automatically initializing certain RAMs within EXSBI.

Register 3A0H – 3A7H: EXSBI Tributary Control #1 – #8

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CLK_MODE[1]	0
Bit 5	R/W	CLK_MODE[0]	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TRIB_TYP[1]	1
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

A tributary control register should only be written when the associated LINK_ENBL bit is ‘0’.

Reserved:

The reserved bits must be set to 0 for correct operation of the OCTLIU device.

TRIB_TYP[1:0]:

The TRIB_TYP[1:0] field specifies the characteristics of the SBI tributary, as shown in Table 9.

Table 9 – EXSBI Tributary Characteristics

TRIB_TYP[1:0]	Description
00	Reserved.
01	Framed (EFP indicates frame alignment).
10	Unframed (EFP remains low).
11	Reserved.

The TRIB_TYP[1:0] bits must be set to “10” whenever the LIUs are enabled (SBI2CLK tied low).

CLK_MODE[1:0]:

The CLK_MODE[1:0] field selects one of three different methods whereby the frequency of the serial data stream output to the LIU octant is determined, as shown in Table 10.

Table 10 – EXSBI Clock Generation Options

CLK_MODE[1:0]	Description
00	Speed up and slow down the output serial clock depending on the FIFO fill level and the thresholds specified in the EXSBI Thresholds Register.
01	Speed up and slow down the output serial clock depending on the 'ClkRate' field of the tributary's Link Rate Octet on the SBI bus.
10	Speed up and slow down the output serial clock depending on the 'Phase' field of the tributary's Link Rate Octet on the SBI bus.
11	Reserved.

Register 3A8H – 3AFH: EXSBI Page A Octant to Tributary Mapping #1 - #8

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

SPE[1:0] and TRIB[4:0]:

The SPE[1:0] and TRIB[4:0] fields are used to specify the LIU octant data stream to SBI tributary mapping when APAGE is set to 0. The input of the octant corresponding to the register (1-8) is sourced from the SPE and tributary specified by the value of SPE[1:0] and TRIB[4:0]. Valid values of SPE[1:0] are from 1 to 3. Valid values of TRIB[4:0] are from 1 to 28 in T1 mode and from 1 to 21 in E1 mode.

Register 3B0H to 3B7H: EXSBI Page B Octant to Tributary Mapping #1 - #8

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

SPE[1:0] and TRIB[4:0]:

The SPE[1:0] and TRIB[4:0] fields are used to specify the LIU octant data stream to SBI tributary mapping when APAGE is set to 1. The input of the octant corresponding to the register (1-8) is sourced from the SPE and tributary specified by the value of SPE[1:0] and TRIB[4:0]. Valid values of SPE[1:0] are from 1 to 3. Valid values of TRIB[4:0] are from 1 to 28 in T1 mode and from 1 to 21 in E1 mode.

Note: The mapping of more than one tributary to the same LIU octant data stream or more than one LIU octant data stream to the same tributary is not allowed. Special care must be taken to ensure that all LIU octants and tributaries are uniquely mapped when using multiple OCTLIU's on the same SBI bus. Failure to do so will result in bus contention.

Register 040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H: ELST Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	1
Bit 0	R/W	OR	1

IR:

The IR bit selects the data rate to be used at the input of the Elastic Store. This bit should be set to 0 for T1/J1 operation and to 1 for E1 operation.

OR:

The OR bit selects the data rate to be used at the output of the Elastic Store. This bit should be set to 0 for T1/J1 operation and to 1 for E1 operation.

Register 041H, 0C1H, 141H, 1C1H, 241H, 2C1H, 341H, 3C1H: ELST Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPEE	0
Bit 1	R	SLIPD	X
Bit 0	R	SLIPI	X

SLIPE:

The SLIPE bit enables an interrupt to be generated on the microprocessor INTB pin when a frame slip occurs in the Elastic Store. When SLIPE is set to logic 1, interrupt generation is enabled. When SLIPE is set to logic 0, interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last frame slip. When SLIPD is set to logic 1, the last frame slip was a write slip (frame skipped due to buffer becoming full). When SLIPE is set to logic 0, the last frame slip was a read slip (frame repeated due to buffer becoming empty).

SLIPI:

The SLIPI bit indicates the occurrence of a frame slip when set to 1. SLIPI is cleared to 0 when this register is read. Note that the SLIPI interrupt indication operates regardless of whether interrupts are enabled or disabled.

Register 043H, 0C3H, 143H, 1C3H, 243H, 2C3H, 343H, 3C3H: T1 PDVD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	PDV	X
Bit 3	R	Z16DI	X
Bit 2	R	PDVI	X
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether interrupts are enabled or disabled.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist. When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Register 045H, 0C5H, 145H, 1C5H, 245H, 2C5H, 345H, 3C5H: T1 XPDE Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	STUFE	0
Bit 6	R/W	STUFF	0
Bit 5	R	STUFI	X
Bit 4	R	PDV	X
Bit 3	R	Z16DI	X
Bit 2	R	PDVI	X
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

STUFE:

The STUFE bit enables the occurrence of pulse stuffing to generate an interrupt on INTB. When STUFE is set to logic 1, an interrupt is generated on the occurrence of a bit stuff. When STUFE is a logic 0, bit stuffing occurrences do not generate an interrupt on INTB.

STUFF:

The STUFF bit enables pulse stuffing to occur upon detection of a violation of the pulse density rule. Bit stuffing is performed in such a way that the resulting data stream no longer violates the pulse density rule. When STUFF is set to logic 1, bit stuffing is enabled and the STUFI bit indicates the occurrence of bit stuffs. When STUFF is a logic 0, bit stuffing is disabled and the PDVI bit indicates occurrences of pulse density violation. Also, when STUFF is a logic 0, PCM data passes through XPDE unaltered.

STUFI:

The STUFI bit is valid when pulse stuffing is active. This bit indicates when a bit stuff occurred to eliminate a pulse density violation and that an interrupt was generated due to the bit stuff (if STUFE is logic 1). When pulse stuffing is active, PDVI remains logic 0, indicating that the stuffing has removed the density violation. The STUFI bit is reset to logic 0 once this register is read. If the STUFE bit is also logic 1, the interrupt is also cleared once this register is read.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether the corresponding interrupt enables are enabled or disabled. When STUFF is set to logic 1, the PDVI and Z16DI bits are forced to logic 0.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist (if STUFE is logic 0). When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Register 046H, 0C6H, 146H, 1C6H, 246H, 2C6H, 346H, 3C6H: T1 XIBC Control

Bit	Type	Function	Default
Bit 7	R/W	EN	0
Bit 6	R/W	Reserved	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	CL1	0
Bit 0	R/W	CL0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

EN:

The EN bit controls whether the Inband Code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

Reserved:

The reserved bit must be set to 0 for correct operation of the OCTLIU device.

CL1, CL0:

The bit positions CL1 and CL0 of this register indicate the length of the inband loopback code sequence, as follows:

Table 11 – Transmit In-band Code Length

CL1	CL0	Code Length
0	0	5
0	1	6
1	0	7
1	1	8

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e., a 3-bit code would use the 6-bit code length setting).

Register 047H, 0C7H, 147H, 1C7H, 247H, 2C7H, 347H, 3C7H: T1 XIBC Loopback Code

Bit	Type	Function	Default
Bit 7	R/W	IBC7	X
Bit 6	R/W	IBC6	X
Bit 5	R/W	IBC5	X
Bit 4	R/W	IBC4	X
Bit 3	R/W	IBC3	X
Bit 2	R/W	IBC2	X
Bit 1	R/W	IBC1	X
Bit 0	R/W	IBC0	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register contains the inband loopback code pattern to be transmitted. The code is transmitted most significant bit (IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (e.g., a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (i.e., the 3-bit code ‘011’ would be written as the 6-bit code ‘011011’).

When the OCTLIU is reset, the contents of this register are not affected.

Register 048H, 0C8H, 148H, 1C8H, 248H, 2C8H, 348H, 3C8H: RJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the receive FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the receive FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

Register 049H, 0C9H, 149H, 1C9H, 249H, 2C9H, 349H, 3C9H: RJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the recovered clock (or the transmit clock if a diagnostic loopback is enabled) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL. If the FIFORST bit of the RJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N1 after a device reset is 47 = 2FH.

Register 04AH, 0CAH, 14AH, 1CAH, 24AH, 2CAH, 34AH, 3CAH: RJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock, RCLK[n], and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL. If the FIFORST bit of the RJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N2 after a device reset is 47 = 2FH.

Recommendations

In general, the relationship N1 = N2 must always be true in order for the PLL to operate correctly.

In order to meet jitter transfer specifications for some modes, such as basic E1 operation, N1 and N2 must be large in order to reduce the PLL transfer cutoff frequency. In general, for E1 operation, N2 is set to FFH to meet ETSI jitter transfer specifications.

For T1 mode, the recommended values are N1 = N2 = 2FH. For E1 mode, the recommended values are N1 = N2 = FFH.

Register 04BH, 0CBH, 14BH, 1CBH, 24BH, 2CBH, 34BH, 3CBH: RJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	FIFORST	0
Bit 0	R/W	LIMIT	1

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions.

The recommended value of CENT is logic 1.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INTB output low.

FIFORST:

Setting the FIFORST bit allows the FIFO to reset when the PLL is reset by software. When FIFORST is logic 1, writing to the PLL Divider Control Registers N1 and N2 will cause both the PLL and FIFO to reset. When FIFORST is logic 0, writing to the Divider Control Registers N1 and N2 will cause only the PLL to reset.

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

The recommended value of LIMIT is logic 0.

Register 04CH, 0CCH, 14CH, 1CCH, 24CH, 2CCH, 34CH, 3CCH: TJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the transmit FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the transmit FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

Register 04DH, 0CDH, 14DH, 1CDH, 24DH, 2CDH, 34DH, 3CDH: TJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the reference clock (as selected by the PLLREF1 and PLLREF0 bits of the Transmit Line Interface Timing Options register) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL. If the FIFORST bit of the TJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N1 after a device reset is 47 = 2FH.

Register 04EH, 0CEH, 14EH, 1CEH, 24EH, 2CEH, 34EH, 3CEH: TJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL. If the FIFORST bit of the TJAT Configuration register is set high, a write to this register will reset both the PLL and FIFO.

The default value of N2 after a device reset is 47 = 2FH.

Recommendations

In general, the relationship N1 = N2 must always be true in order for the PLL to operate correctly.

In order to meet jitter transfer specifications for some modes, such as basic E1 operation, N1 and N2 must be large in order to reduce the PLL transfer cutoff frequency. In general, for E1 operation, N2 is set to FFH to meet ETSI jitter transfer specifications.

For T1 mode, the recommended values are N1 = N2 = 2FH. For E1 mode, the recommended values are N1 = N2 = FFH.

Register 04FH, 0CFH, 14FH, 1CFH, 24FH, 2CFH, 34FH, 3CFH: TJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	FIFORST	0
Bit 0	R/W	LIMIT	1

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions.

The recommended value of CENT is logic 1.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INTB output low.

FIFORST:

Setting the FIFORST bit allows the FIFO to reset when the PLL is reset by software. When FIFORST is logic 1, writing to the PLL Divider Control Registers N1 and N2 will cause both the PLL and FIFO to reset. When FIFORST is logic 0, writing to the Divider Control Registers N1 and N2 will cause only the PLL to reset.

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

The recommended value of LIMIT is logic 0.

Register 050H, 0D0H, 150H, 1D0H, 250H, 2D0H, 350H, 3D0H: IBCD Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	DSEL1	0
Bit 2	R/W	DSEL0	0
Bit 1	R/W	ASEL1	0
Bit 0	R/W	ASEL0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register provides the selection of the Activate and De-activate loopback code lengths (from 3 bits to 8 bits) as follows:

Table 12 – Loopback Code Configurations

DEACTIVATE Code		ACTIVATE Code		
DSEL1	**DSEL0**	**ASEL1**	**ASEL0**	**CODE LENGTH**
0	0	0	0	5 bits
0	1	0	1	6 (or 3*) bits
1	0	1	0	7 bits
1	1	1	1	8 (or 4*) bits

Note:

3-bit and 4-bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

The Reserved bit is used for production test purposes only. The Reserved bit must be logic 0 for normal operation.

Register 051H, 0D1H, 151H, 1D1H, 251H, 2D1H, 351H, 3D1H: IBCD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R	LBACP	X
Bit 6	R	LBDCP	X
Bit 5	R/W	LBAE	0
Bit 4	R/W	LBDE	0
Bit 3	R	LBAI	X
Bit 2	R	LBDI	X
Bit 1	R	LBA	X
Bit 0	R	LBD	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

LBACP, LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval.

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the microprocessor INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the microprocessor INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI, LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes generated the interrupt when their state changed. A logic 1 in these bit positions indicates that a state change in that code has generated an interrupt; a logic 0 in these bit positions indicates that no state change has occurred. After the Enable/Status Register has been read, the LBAI and LBDI bits are set to logic 0.

LBA, LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicates the presence of that code has been detected; a logic 0 in these bit positions indicates the absence of that code.

Register 052H, 0D2H, 152H, 1D2H, 252H, 2D2H, 352H, 3D2H: IBCD Activate Code

Bit	Type	Function	Default
Bit 7	R/W	ACT7	0
Bit 6	R/W	ACT6	0
Bit 5	R/W	ACT5	0
Bit 4	R/W	ACT4	0
Bit 3	R/W	ACT3	0
Bit 2	R/W	ACT2	0
Bit 1	R/W	ACT1	0
Bit 0	R/W	ACT0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This 8-bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8-bit register. For example, if code sequence is a repeating 00001, the first 8 bits of two repetitions (0000100001) is programmed into the register, i.e.00001000. Note that bit ACT7 corresponds to the first code bit received.

Register 053H, 0D3H, 153H, 1D3H, 253H, 2D3H, 353H, 3D3H: IBCD Deactivate Code

Bit	Type	Function	Default
Bit 7	R/W	DACT7	0
Bit 6	R/W	DACT6	0
Bit 5	R/W	DACT5	0
Bit 4	R/W	DACT4	0
Bit 3	R/W	DACT3	0
Bit 2	R/W	DACT2	0
Bit 1	R/W	DACT1	0
Bit 0	R/W	DACT0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This 8-bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8-bit register. For example, if code sequence is a repeating 001, the first 8 bits of three repetitions (001001001) is programmed into the register, i.e.00100100. Note that bit DACT7 corresponds to the first code bit received.

Register 054H, 0D4H, 154H, 1D4H, 254H, 2D4H, 354H, 3D4H: CDRC Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	LOS[1]	0
Bit 5	R/W	LOS[0]	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ALGSEL	0
Bit 1	R/W	O162	0
Bit 0	R/W	Reserved	0

Reserved:

These bits must be a logic 0 for correct operation.

O162:

If the AMI bit is logic 0 in E1 mode, the Recommendation O.162 compatibility select bit (O162) allows selection between two line code violation definitions:

If O162 is a logic 0, a line code violation is indicated if the serial stream does not match the verbatim HDB3 definition given in Recommendation G.703. A bipolar violation that is not part of an HDB3 signature or a bipolar violation in an HDB3 signature that is the same polarity as the last bipolar violation results in a line code violation indication.

If O162 is a logic 1, a line code violation is indicated if a bipolar violation is of the same polarity as the last bipolar violation, as per Recommendation O.162.

The O162 bit has no effect in T1 mode.

ALGSEL:

The Algorithm Select (ALGSEL) bit specifies the algorithm used by the DPLL for clock and data recovery. The choice of algorithm determines the high frequency input jitter tolerance of the CDRC. When ALGSEL is set to logic 1, the CDRC jitter tolerance is increased to approach 0.5 Uipp for jitter frequencies above 20 kHz. When ALGSEL is set to logic 0, the jitter tolerance is increased for frequencies below 20 kHz (i.e. the tolerance is improved by 20% over that of ALGSEL=1 at these frequencies), but the tolerance approaches 0.4 Uipp at the higher frequencies.

AMI:

The alternate mark inversion (AMI) bit specifies the line coding of the incoming signal. A logic 1 selects AMI line coding by disabling HDB3 decoding in E1 mode and B8ZS in T1 mode. In E1 mode, a logic 0 selects HDB3 line decoding which entails substituting an HDB3 signature with four zeros. In T1 mode, a logic 0 selects B8ZS line decoding which entails substituting an B8ZS signature with eight zeros.

LOS[1:0]:

The loss of signal threshold is set by the operating mode and the state of the AMI, LOS[1] and LOS[0] bits:

Table 13 – Loss of Signal Thresholds

Mode	AMI	LOS[1]	LOS[0]	Threshold (PCM periods)
E1	0	0	0	10
T1	0	0	0	15
X	1	0	0	15
X	X	0	1	31
X	X	1	0	63
X	X	1	1	175

When the number of consecutive zeros on the incoming PCM line exceeds the programmed threshold, the LOSV status bit is set. For example, if the threshold is set to 10, the 11th zero causes the LOSV bit to be set.

Register 055H, 0D5H, 155H, 1D5H, 255H, 2D5H, 355H, 3D5H: CDRC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	LCVE	0
Bit 6	R/W	LOSE	0
Bit 5	R/W	LCSDE	0
Bit 4	R/W	ZNDE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The bit positions LCVE, LOSE, LCSDE and ZNDE (bits 7 to 4) of this register are interrupt enables to select which of the status events (Line Code Violation , Loss Of Signal, HDB3 signature, B8ZS signature or N Zeros), either singly or in combination, are enabled to generate an interrupt on the microprocessor INTB pin when they are detected. A logic 1 bit in the corresponding bit position enables the detection of these signals to generate an interrupt; a logic 0 bit in the corresponding bit position disables that signal from generating an interrupt.

Register 056H, 0D6H, 156H, 1D6H, 256H, 2D6H, 356H, 3D6H: CDRC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LCVI	X
Bit 6	R	LOSI	X
Bit 5	R	LCSDI	X
Bit 4	R	ZNDI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOSV	X

The ZNDI, LCSDI, LOSI and LCVI (bits 4 to 7) of this register indicate which of the status events have occurred since the last time this register was read. A logic 1 in any of these bit positions indicates that the corresponding event was detected.

Bits ZNDI, LCSDI, LOSI and LCVI are cleared to logic 0 by reading this register.

<u>LOSV:</u>

The LOSV bit reflects the status of the LOS alarm.

<u>ZNDI:</u>

The consecutive zeros detection interrupt (ZNDI) indicates that N consecutive spaces have occurred, where N is four for E1 and eight for T1. This bit can be used to detect an AMI coded signal.

<u>LCSDI:</u>

The line code signature detection interrupt (LCSDI) indicates that a valid line code signature has occurred. In T1 mode, the B8ZS signature is defined as 000+-0-+ if the previous impulse is positive, or 000-+0+- if it is negative. In E1 mode, a valid HDB3 signature is defined as a bipolar violation preceded by two zeros. This bit can be used to detect an HDB3 coded signal in E1 mode and B8ZS coded signal in T1.

<u>LOSI:</u>

The LOSI bit is set to a logic 1 when the LOSV bit changes state.

<u>LCVI:</u>

The line code violation interrupt (LCVI) indicates a series of marks and spaces has occurred in contradiction to the defined line code (AMI, B8ZS or HDB3).

Register 057H, 0D7H, 157H, 1D7H, 257H, 2D7H, 357H, 3D7H: CDRC Alternate Loss of Signal Status

Bit	Type	Function	Default
Bit 7	R/W	ALTLOSE	0
Bit 6	R	ALTLOSI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ALTLOSV	X

The alternate loss of signal status provides a more stringent criteria for the deassertion of the alarm than the LOS indication in the CDRC Interrupt Status register.

ALTLOSE:

If the ALTLOSE bit is a logic 1, the INTB output is asserted low when the ALTLOSV status bit changes state.

ALTLOSI:

The ALTLOSI bit is set high when the ALTLOSV status bit changes state. It is cleared when this register is read.

ALTLOSV:

The ALTLOSV bit is asserted upon the absence of marks for the threshold of bit periods specified by the LOS[1:0] register bits. The ALTLOSV bit is deasserted only after pulse density requirements have been met. In T1 mode, there must be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). In E1 mode, ALTLOSV is deasserted only after 255 bit periods during which no sequence of four zeros has been received.

Register 058H, 0D8H, 158H, 1D8H, 258H, 2D8H, 358H, 3D8H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	XFER	0
Bit 0		Unused	X

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt via the INTB output; a logic 0 bit in the INTE position disables the generation of an interrupt.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations or the Octant PMON Update register, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

Register 05EH, 0DEH, 15EH, 1DEH, 25EH, 2DEH, 35EH, 3DEH: PMON LCV Count (LSB)

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 05FH, 0DFH, 15FH, 1DFH, 25FH, 2DFH, 35FH, 3DFH: PMON LCV Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[12:0]:

The LCV[12:0] bits indicate the number of LCV error events that occurred during the previous accumulation interval. An LCV event is defined as the occurrence of a Bipolar Violation or Excessive Zeros. The counting of Excessive Zeros can be disabled by the BPV bit of the Receive Line Interface Configuration #1 register.

The LCV count registers for a octant are updated by writing to the PMON LCV Count (LSB) register. A write to this location loads count data located in the PMON into the internal holding registers. Alternatively, the LCV count registers for the octant are updated by writing to the Line Interface Interrupt Source #1 / PMON Update register. The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed.

The PMON is loaded with new count data within 3.5 recovered clock periods of the triggering register write. With nominal line rates, the PMON registers should not be polled until 2.3 µsec have elapsed from the triggering register write.

When the OCTLIU is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

Register 060H, 0E0H, 160H, 1E0H, 260H, 2E0H, 360H, 3E0H: PRBS Generator/Checker Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	QRSS	0
Bit 4		Unused	X
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

QRSS:

The quasi-random signal source (QRSS) bit enables the zero suppression feature required when generating a QRSS sequence. When QRSS is a logic 1, a one is forced in the generated PRBS stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

Note that in order to generate the AT&T TR 62411 QRSS sequence, or the 2^{20}-1 sequence as specified in ITU-T O.151, the PATSEL[1:0] field in the PRBS Pattern Select Register must be set to “01” and QRSS set to 1.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

RINV:

The RINV bit controls the logical inversion of the received stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the data is not inverted

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 10 or more bit errors are detected in a fixed 48-bit window. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTOSYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 061H, 0E1H, 161H, 1E1H, 261H, 2E1H, 361H, 3E1H: PRBS Checker Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0		Unused	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the PRBS checker changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV:

The SYNCV bit indicates the synchronization state of the PRBS checker. When SYNCV is a logic 1 the PRBS checker is synchronized (the PRBS checker has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the PRBS checker is out of sync (the PRBS checker has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of the error count has occurred. A logic 1 in this bit position indicates that the error counter holding registers has been updated. This update is initiated by writing to one of the PRBS Error Count register locations, or by writing to the Line Interface Interrupt Source #1 / PMON Update register. XFERI is set to logic 0 when this register is read.

Register 062H, 0E2H, 162H, 1E2H, 262H, 2E2H, 362H, 3E2H: PRBS Pattern Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	PATSEL[1]	0
Bit 0	R/W	PATSEL[0]	0

PATSEL[1:0]:

PATSEL[1:0] determines which of the three PRBS patterns are generated and checked for errors.

PATSEL[1:0]	Pattern
00	2^{15}-1
01	2^{20}-1
10	2^{11}-1
11	Reserved

Register 064H, 0E4H, 164H, 1E4H, 264H, 2E4H, 364H, 3E4H: PRBS Error Count #1

Bit	Type	Function	Default
Bit 7	R	ERRCNT[7]	X
Bit 6	R	ERRCNT[6]	X
Bit 5	R	ERRCNT[5]	X
Bit 4	R	ERRCNT[4]	X
Bit 3	R	ERRCNT[3]	X
Bit 2	R	ERRCNT[2]	X
Bit 1	R	ERRCNT[1]	X
Bit 0	R	ERRCNT[0]	X

Register 065H, 0E5H, 165H, 1E5H, 265H, 2E5H, 365H, 3E5H: PRBS Error Count #2

Bit	Type	Function	Default
Bit 7	R	ERRCNT[15]	X
Bit 6	R	ERRCNT[14]	X
Bit 5	R	ERRCNT[13]	X
Bit 4	R	ERRCNT[12]	X
Bit 3	R	ERRCNT[11]	X
Bit 2	R	ERRCNT[10]	X
Bit 1	R	ERRCNT[9]	X
Bit 0	R	ERRCNT[8]	X

Register 066H, 0E6H, 166H, 1E6H, 266H, 2E6H, 366H, 3E6H: PRBS Error Count #3

Bit	Type	Function	Default
Bit 7	R	ERRCNT[23]	X
Bit 6	R	ERRCNT[22]	X
Bit 5	R	ERRCNT[21]	X
Bit 4	R	ERRCNT[20]	X
Bit 3	R	ERRCNT[19]	X
Bit 2	R	ERRCNT[18]	X
Bit 1	R	ERRCNT[17]	X
Bit 0	R	ERRCNT[16]	X

ERRCNT[23:0]:

ERRCNT[23:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval, up to a maximum (saturation) value of 2^{24}-1. Note that bit errors are not accumulated while the pattern detector is out of sync.

The Error Count registers for each individual PRBS generator/checker are updated by writing to any one of the Error count registers. Alternatively, the Error Count registers are updated with all other octant counter registers by writing to the Line Interface Interrupt Source #1 / PMON Update register.

Register 068H, 0E8H, 168H, 1E8H, 268H, 2E8H, 368H, 3E8H: XLPG Control/Status

Bit	Type	Function	Default
Bit 7	R/W	HIGHZ	1
Bit 6	R/W	ARST	0
Bit 5		Unused	X
Bit 4	R/W	INITRAM	0
Bit 3	R	OVRFLW	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

HIGHZ:

The HIGHZ bit controls tristating of the TXTIP[x] and TXRING[x] outputs. When the HIGHZ bit is set to a logic 0, the outputs are enabled. When the HIGHZ bit is set to a logic 1, the outputs are put into high impedance. Setting HIGHZ to logic 1 has the same effect as setting SCALE[4:0] to 00H.

ARST:

The Analogue Reset bit (ARST) resets the analogue portion of the XLPG (without affecting the digital portion) when set to logic 1.

INITRAM:

The Waveform Storage RAM initialisation bit (INITRAM) causes the XPLG waveform storage RAM to be initialised to 12 standard waveform patterns when set to logic 1. This bit remains at logic 1 while the initialisation is in progress and is cleared to logic 0 when the initialisation has completed.

The 12 waveform patterns to which the RAM is initialised are listed in Table 20 thru Table 29, Table 37 and Table 38.

OVRFLW:

The overflow detection value bit (OVRFLW) indicates the presence or absence of an overflow condition in the waveform computation pipeline. An overflow occurs when the sum of the five unit interval (UI) samples exceeds the maximum D/A value. The XLPG detects overflows and saturates the output value to minimize their impact on the output signal. Overflows can easily be eliminated by changing the waveform programming. This status bit is set to logic 1 when an overflow condition is detected and it is reset to logic 0 only when this register is read. It is suggested that this register be read twice after the programming of a new waveform and transmission of data to ensure the maximum output amplitude is never exceeded.

Reserved:

The Reserved bits must remain in their default state for correct operation.

Register 069H, 0E9H, 169H, 1E9H, 269H, 2E9H, 369H, 3E9H: XLPG Pulse Waveform Scale

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	SCALE[4]	0
Bit 3	R/W	SCALE[3]	0
Bit 2	R/W	SCALE[2]	0
Bit 1	R/W	SCALE[1]	0
Bit 0	R/W	SCALE[0]	0

SCALE[4:0]:

The SCALE[4:0] bits specify a scaling factor to be applied to the amplitude of the D/A output waveform. Each of the 12 waveforms stored in the XLPG's pulse template RAM may have a different scaling factor. When a particular waveform is selected for use (by the PT_SEL[3:0] register bits or LENx[2:0] inputs), the scaling factor corresponding to that waveform is chosen automatically.

When this register is written to, the value of SCALE[4:0] is stored in one of 12 storage locations indexed by the WAVEFORM[3:0] bits of the Pulse Waveform Storage Write Address #2 register. Thus to set up scaling factors for more than one waveform, this register should be written to a number of times, with WAVEFORM[3:0] set to the different waveform numbers, as appropriate.

The SCALE[4:0] bits scale the maximum output amplitude by increments of 11.14 mA. A value of 0 (00H) tristates the output while the maximum value of 21 (15H) sets the full scale current to 234 mA.

Table 14 – Transmit Output Amplitude

SCALE[4:0]	Decimal Equiv.	Output Amplitude
00000	0	0 mA (tristate)
00001-10100	1-20	Increments of 11.14 mA for each scale step
10101	21	234 mA total
10110-11111	>21	Reserved

Register 06AH, 0EAH, 16AH, 1EAH, 26AH, 2EAH, 36AH, 3EAH: XLPG Pulse Waveform Storage Write Address #1

Bit	Type	Function	Default
Bit 7	R/W	SAMPLE[4]	0
Bit 6	R/W	SAMPLE[3]	0
Bit 5	R/W	SAMPLE[2]	0
Bit 4	R/W	SAMPLE[1]	0
Bit 3	R/W	SAMPLE[0]	0
Bit 2	R/W	UI[2]	0
Bit 1	R/W	UI[1]	0
Bit 0	R/W	UI[0]	0

UI[2:0]:

The pulse waveform write address is composed of a unit interval selector, a sample selector and a waveform number. The unit interval selector (UI[2:0]) specifies the unit interval portion of the address. There are 5 unit intervals, numbered from 0 to 4. UI[2:0] can take the values 0H, 1H, 2H, 3H and 4H. The values 5H, 6H and 7H are undefined.

SAMPLE[4:0]:

The pulse waveform write address is composed of a unit interval selector, a sample selector and a waveform number. The sample selector (SAMPLE[4:0]) specifies the sample portion of the address. There are 24 samples, numbered from 0 to 23. SAMPLE[4:0] can thus have any value from 00H to 17H. The values from 18H to 1FH are undefined.

Note – The Pulse Waveform Storage Write Indirect Address Registers #1 and #2 must be written to *before* the Pulse Waveform Storage Data register. In addition, waveform samples must be written in groups of 5. Within each group of 5 writes, the waveform number and sample selector must remain constant and the unit interval selector must be set to 0x0, 0x1, 0x2, 0x3 and 0x4 in sequence. See the Operation section for more details on setting up waveform templates.

Register 06BH, 0EBH, 16BH, 1EBH, 26BH, 2EBH, 36BH, 3EBH: XLPG Pulse Waveform Storage Write Address #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	WAVEFORM[3]	0
Bit 2	R/W	WAVEFORM[2]	0
Bit 1	R/W	WAVEFORM[1]	0
Bit 0	R/W	WAVEFORM[0]	0

WAVEFORM[3:0]:

The pulse waveform write address is composed of a unit interval selector, a sample selector and a waveform number. The waveform number (WAVEFORM[3:0]) specifies the waveform portion of the address. There are 12 waveforms, numbered from 0 to 11. WAVEFORM[3:0] can thus have any value from 0H to BH. The values from CH to FH are undefined.

Note – The Pulse Waveform Storage Write Indirect Address Registers #1 and #2 must be written to *before* the Pulse Waveform Storage Data register. In addition, waveform samples must be written in groups of 5. Within each group of 5 writes, the waveform number and sample selector must remain constant and the unit interval selector must be set to 0x0, 0x1, 0x2, 0x3 and 0x4 in sequence. See the Operation section for more details on setting up waveform templates.

Register 06CH, 0ECH, 16CH, 1ECH, 26CH, 2ECH, 36CH, 3ECH: XLPG Pulse Waveform Storage Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	W	WDAT[6]	X
Bit 5	W	WDAT[5]	X
Bit 4	W	WDAT[4]	X
Bit 3	W	WDAT[3]	X
Bit 2	W	WDAT[2]	X
Bit 1	W	WDAT[1]	X
Bit 0	W	WDAT[0]	X

WDAT[6:0]:

The WDAT[6:0] bits contain the write data to be stored in the pulse template RAM, as addressed by the UI[2:0], SAMPLE[4:0] and WAVEFORM[3:0] bits in the Pulse Waveform Storage Write Address registers. When writing to the RAM, the address must first be written to the Pulse Waveform Storage Write Address registers. Writing to the Pulse Waveform Storage Data register triggers the transfer of data. If the UI portion of the address is 0, 1, 2 or 3, WDAT[6:0] are transferred to internal holding registers. If the UI portion of the address is 4, WDAT[6:0] are combined with the contents of the holding registers to form a 35-bit long word which is then stored in the pulse template RAM. Waveform samples must therefore be written in groups of 5 and within each group of 5 writes, the waveform number and sample selector must remain constant and the unit interval selector must be set to 0x0, 0x1, 0x2, 0x3 and 0x4 in sequence.

WDAT[6:0] are coded in signed magnitude representation. WDAT[6] is the sign bit, WDAT[5] is the most significant data bit and WDAT[0] is the least significant data bit. The data values thus can range from –63 to +63.

See the Operation section for more details on setting up custom waveform templates.

Register 070H, 0F0H, 170H, 1F0H, 270H, 2F0H, 370H, 3F0H: RLPS Configuration and Status

Bit	Type	Function	Default
Bit 7	R	ALOSI	X
Bit 6	R	ALOSV	X
Bit 5	R/W	ALOSE	0
Bit 4	R/W	SQUELCHE	0
Bit 3	R/W	IDDQ_EN	0
Bit 2	R	DB_VALID	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

Reserved:

The Reserved bit must be logic 1 for correct operation.

DB_VALID:

The DB_VALID bit indicates if the adaptive equalizer has stabilized. This bit is set if the equalisation has not changed by more than 2dB (or +/-8 steps in the RAM table) in more than a selectable count of sampling periods.

IDDQ_EN:

The IDDQ enable bit (IDDQ_EN) is used to configure the analogue receiver for IDDQ tests. When IDDQ_EN is a logic 1, or the IDDQEN bit in the Master Test Control #1 register (004H) is a logic 1, the digital outputs of the analogue receiver are pulled to ground.

SQUELCHE:

The output data squelch enable (SQUELCHE) allows control of data squelching in response to an analogue loss of signal (ALOS) condition. When SQUELCHE is set to logic 1, the recovered data are forced to all-zeros if the ALOSV register bit is asserted. When SQUELCHE is set to logic 0, squelching is disabled.

ALOSE:

The loss of signal interrupt enable bit (ALOSE) enables the generation of device level interrupt on a change of Loss of Signal status. When ALOSE is a logic 1, an interrupt is generated by asserting INTB low when there is a change of the ALOSV status. When ALOSE is set to logic 0, interrupts are disabled.

ALOSV:

The loss of signal value bit (ALOSV) indicates the loss of signal alarm state.

ALOSI:

The loss of signal interrupt bit (ALOSI) is a logic 1 whenever the Loss of Signal indicator state (ALOSV) changes. This bit is cleared when this register is read.

Register 071H, 0F1H, 171H, 1F1H, 271H, 2F1H, 371H, 3F1H: RLPS ALOS Detection/Clearance Threshold

Bit	Type	Function	Default
Bit 7	R/W	CLR_THR[3]	0
Bit 6	R/W	CLR_THR[2]	0
Bit 5	R/W	CLR_THR[1]	0
Bit 4	R/W	CLR_THR[0]	0
Bit 3	R/W	DET_THR[3]	0
Bit 2	R/W	DET_THR[2]	0
Bit 1	R/W	DET_THR[1]	0
Bit 0	R/W	DET_THR[0]	0

Table 15 – ALOS Detection/Clearance Thresholds

THR	Signal level (dB)	Applicable Standard	Detection/Clearance
0000	8		
0001	9		
0010	10	G.775(E1)	Clearance (if <= 9dB)
0011	11		
0100	20		
0101	21	I.431 (E1) ETSI 300 233	Detection (if > 20dB) and Clearance
0110	22		
0111	30		
1000	31	I.431 (T1)	Detection (if > 30dB) and Clearance
1001	32		
1010	33		
1011	34		
1100	35	G.775 (E1)	Detection (if >= 35dB)
1101	36		
1110	37		
1111	38		

DET_THR[3:0]:

DET_THR[3:0] references one of the threshold settings in Table 15 as the ALOS detection criteria. If the equalised cable loss is greater than or equal to the threshold for N consecutive pulse periods, where N = 16 * DET_PER stored in the RLPS ALOS Detection Period Register, ALOS is declared and interrupt set.

CLR_THR[3:0]:

CLR_THR[3:0] references one of the threshold settings listed in Table 15 as the ALOS clearance criteria. ALOS is cleared when the equalised cable loss is less than the threshold for N consecutive pulse intervals, where N = 16 * CLR_PER stored in the RLPS ALOS Clearance Period Register.

Register 072H, 0F2H, 172H, 1F2H, 272H, 2F2H, 372H, 3F2H: RLPS ALOS Detection Period

Bit	Type	Function	Default
Bit 7	R/W	DET_PER[7]	0
Bit 6	R/W	DET_PER[6]	0
Bit 5	R/W	DET_PER[5]	0
Bit 4	R/W	DET_PER[4]	0
Bit 3	R/W	DET_PER[3]	0
Bit 2	R/W	DET_PER[2]	0
Bit 1	R/W	DET_PER[1]	0
Bit 0	R/W	DET_PER[0]	1

DET_PER[7:0]:

This register specifies the time duration that the equalised cable loss has to remain above the detection threshold in order for the ALOS to be issued. This duration is equal to DET_PER * 16 number of pulse intervals, the resulting range is from 16 to 4080 and thus compliant with all the presently available E1/T1 ALOS detection standards/recommendations.

Register 073H, 0F3H, 173H, 1F3H, 273H, 2F3H, 373H, 3F3H: RLPS ALOS Clearance Period

Bit	Type	Function	Default
Bit 7	R/W	CLR_PER[7]	0
Bit 6	R/W	CLR_PER[6]	0
Bit 5	R/W	CLR_PER[5]	0
Bit 4	R/W	CLR_PER[4]	0
Bit 3	R/W	CLR_PER[3]	0
Bit 2	R/W	CLR_PER[2]	0
Bit 1	R/W	CLR_PER[1]	0
Bit 0	R/W	CLR_PER[0]	1

CLR_PER[7:0]:

This register specifies the time duration that the equalised cable loss has to remain below the clearance threshold in order for the ALOS to be cleared. This duration is equal to CLR_PER * 16 number of pulse intervals resulting in a range from 16 to 4080 and thus compliant with all the presently available E1/T1 ALOS clearance standards/ recommendations.

Register 074H, 0F4H, 174H, 1F4H, 274H, 2F4H, 374H, 3F4H: RLPS Equalization Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	EQ_ADDR[7]	0
Bit 6	R/W	EQ_ADDR[6]	0
Bit 5	R/W	EQ_ADDR[5]	0
Bit 4	R/W	EQ_ADDR[4]	0
Bit 3	R/W	EQ_ADDR[3]	0
Bit 2	R/W	EQ_ADDR[2]	0
Bit 1	R/W	EQ_ADDR[1]	0
Bit 0	R/W	EQ_ADDR[0]	0

EQ_ADDR [7:0]:

Writing to this register initiates an internal uP access request cycle to the RAM. Depending on the setting of the RWB bit inside the RLPS Equalization Read/WriteB Select, a read or a write will be performed. During a write cycle, the indirect data bits located in the RLPS Equalization Indirect Data registers are written into the RAM. For a read request, the content of the addressed RAM location is written into the RLPS Equalization Indirect Data registers. This register should be the last register to be written for a uP access.

A waiting period of at least three line rate cycles is needed from when this register is written until the next indirect data bits are written into any of the respective octant's RLPS Equalization Indirect Data registers.

Register 075H, 0F5H, 175H, 1F5H, 275H, 2F5H, 375H, 3F5H: RLPS Equalization Read/WriteB Select

Bit	Type	Function	Default
Bit 7	R/W	RWB	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

RWB:

This bit selects the operation to be performed on the RAM: when RWB is ‘1’, a read from the equalization RAM is requested; when RWB is set to ‘0’, a write to the RAM is desired.

Register 076H, 0F6H, 176H, 1F6H, 276H, 2F6H, 376H, 3F6H:
RLPS Equalizer Loop Status and Control

Bit	Type	Function	Default
Bit 7	R/W	LOCATION[7]	0
Bit 6	R/W	LOCATION[6]	0
Bit 5	R/W	LOCATION[5]	0
Bit 4	R/W	LOCATION[4]	0
Bit 3	R/W	LOCATION[3]	0
Bit 2	R/W	LOCATION[2]	0
Bit 1	R/W	LOCATION[1]	0
Bit 0	R/W	LOCATION[0]	0

LOCATION[7:0]:

Writing to this register overwrites a counter which serves as the read address to the equalization RAM. Reading this register returns the current value of the counter and thus an indication of the cable loss as estimated by the equaliser.

Register 077H, 0F7H, 177H, 1F7H, 277H, 2F7H, 377H, 3F7H: RLPS Equalizer Configuration

Bit	Type	Function	Default
Bit 7	R/W	VALID_PER[1]	0
Bit 6	R/W	VALID_PER[0]	0
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	EQ_EN	0
Bit 2	R/W	EQ_FREQ[2]	0
Bit 1	R/W	EQ_FREQ[1]	1
Bit 0	R/W	EQ_FREQ[0]	1

EQ_FREQ[2:0]:

The EQ_FREQ[2:0] field selects the frequency of the EQ feedback loop as indicated by Table 16.

Table 16 – Equalization Feedback Frequencies

EQ_FREQ[2:0]	EQ Feedback Frequency		How Frequency Derived
	T1 mode	E1 mode	
000	24.125 kHz	32.000 kHz	Line rate ÷ 64
001	12.063 kHz	16.000 kHz	Line rate ÷ 128
010	8.0417 kHz	10.667 kHz	Line rate ÷ 192
011	6.0313 kHz	8.0000 kHz	Line rate ÷ 256
100	4.8250 kHz	6.40 kHz	Line rate ÷ 320
101	4.0208 kHz	5.333 kHz	Line rate ÷ 384
110	3.4464 kHz	4.5714 kHz	Line rate ÷ 448
111	3.0156 kHz	4.0 kHz	Line rate ÷ 512

EQ_EN:

The EQ_EN bit enables operation of the equaliser when set to logic 1. This bit defaults to logic 0 after reset and must be set to logic 1, but only after the equalisation RAM has been initialised.

Reserved:

This bit must be programmed to logic 0 for normal operation.

VALID_PER[1:0]:

The VALID_PER[1:0] bits select the length of time that the dB loss counter must be stable before DB_VALID is asserted. The duration is measured in number of periods of the EQ feedback loop (specified by the EQ_FREQ bits) as indicated by Table 17.

Table 17 – Valid Period

VALID_PER	Number of periods
00	32
01	64
10	128
11	256

Register 078H, 0F8H, 178H, 1F8H, 278H, 2F8H, 378H, 3F8H: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[31]	0
6	R/W	EQ_DATA[30]	0
5	R/W	EQ_DATA[29]	0
4	R/W	EQ_DATA[28]	0
3	R/W	EQ_DATA[27]	0
2	R/W	EQ_DATA[26]	0
1	R/W	EQ_DATA[25]	0
0	R/W	EQ_DATA[24]	0

EQ_DATA[31:24]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the most significant byte of the input-data to the equalization RAM. Reading it returns the MSB of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 079H, 0F9H, 179H, 1F9H, 279H, 2F9H, 379H, 3F9H: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[23]	0
6	R/W	EQ_DATA[22]	0
5	R/W	EQ_DATA[21]	0
4	R/W	EQ_DATA[20]	0
3	R/W	EQ_DATA[19]	0
2	R/W	EQ_DATA[18]	0
1	R/W	EQ_DATA[17]	0
0	R/W	EQ_DATA[16]	0

EQ_DATA[23:16]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the second most significant byte of the input-data to the equalization RAM. Reading it returns the second MSB of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 07AH, 0FAH, 17AH, 1FAH, 27AH, 2FAH, 37AH, 3FAH: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[15]	0
6	R/W	EQ_DATA[14]	0
5	R/W	EQ_DATA[13]	0
4	R/W	EQ_DATA[12]	0
3	R/W	EQ_DATA[11]	0
2	R/W	EQ_DATA[10]	0
1	R/W	EQ_DATA[9]	0
0	R/W	EQ_DATA[8]	0

EQ_DATA[15:8]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the second least significant byte of the input-data to the equalization RAM. Reading it returns the corresponding bits of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 07BH, 0FBH, 17BH, 1FBH, 27BH, 2FBH, 37BH, 3FBH: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[7]	0
6	R/W	EQ_DATA[6]	0
5	R/W	EQ_DATA[5]	0
4	R/W	EQ_DATA[4]	0
3	R/W	EQ_DATA[3]	0
2	R/W	EQ_DATA[2]	0
1	R/W	EQ_DATA[1]	0
0	R/W	EQ_DATA[0]	0

EQ_DATA[7:0]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the least significant byte of the input-data to the equalization RAM. Reading it returns the LSB of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 07CH, 0FCH, 17CH, 1FCH, 27CH, 2FCH, 37CH, 3FCH: RLPS Equalizer Voltage Thresholds #1

Bit	Type	Function	Default
7		unused	X
6		unused	X
5	R/W	VREF[5]	1
4	R/W	VREF[4]	1
3	R/W	VREF[3]	0
2	R/W	VREF[2]	1
1	R/W	VREF[1]	0
0	R/W	VREF[0]	1

VREF[5:0]:

The VREF[5:0] bits set the voltage thresholds of amplitude comparators within the RLPS. For T1 mode, the VREF[5:0] bits must be programmed to 35H (‘b110101). For E1 mode, the VREF[5:0] bits must be programmed to 35H (‘b110101).

Register 07DH, 0FDH, 17DH, 1FDH, 27DH, 2FDH, 37DH, 3FDH: RLPS Equalizer Voltage Thresholds #2

Bit	Type	Function	Default
7	R/W	CUTOFF[1]	0
6	R/W	CUTOFF[0]	0
5		Unused	X
4		Unused	X
3		Unused	X
2	R/W	VREF[8]	0
1	R/W	VREF[7]	1
0	R/W	VREF[6]	1

CUTOFF[1:0]:

The CUTOFF[1:0] bits control cutoff frequencies of the bandlimiter and equaliser within the RLPS. For T1 mode, the CUTOFF[1:0] bits must be programmed to 3H (‘b11). For E1 mode, the CUTOFF[1:0] bits must be programmed to 0H (‘b00).

VREF[8:6]:

The VREF[8:6] bits set the voltage thresholds of amplitude comparators within the RLPS. For T1 mode, the VREF[8:6] bits must be programmed to 3H (‘b011). For E1 mode, the VREF[8:6] bits must be programmed to 3H (‘b011).

11 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

11.1 JTAG Test Port

The OCTLIU JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Instruction Register

Length – 3 bits

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Identification Register

Length – 32 bits

Version number – 0H for Rev A.

Part Number – 4318H

Manufacturer’s identification code – 0CDH

Device identification – 043180CDH for Rev. A

Boundary Scan Register

Length – 131

Table 18 – Boundary Scan Register

Pin/Enable	Scan Register Bit	Cell Type	Device ID		Pin/Enable	Scan Register Bit	Cell Type	
A[10]	130	IN_CELL	0		RDN[8]	64	OUT_CELL	-
A[9]	129	IN_CELL	0		OEB_RDP[8]	63	OUT_CELL	-
A[8]	128	IN_CELL	0		RDP[8]	62	OUT_CELL	-
A[7]	127	IN_CELL	0		OEB_RCLK[8]	61	OUT_CELL	-
A[6]	126	IN_CELL	0		RCLK[8]	60	OUT_CELL	-
A[5]	125	IN_CELL	1		TDN[5]	59	IN_CELL	-
A[4]	124	IN_CELL	0		TDP[5]	58	IN_CELL	-
A[3]	123	IN_CELL	0		TCLK[5]	57	IN_CELL	-
A[2]	122	IN_CELL	0		TDN[6]	56	IN_CELL	-
A[1]	121	IN_CELL	0		TDP[6]	55	IN_CELL	-
A[0]	120	IN_CELL	1		TCLK[6]	54	IN_CELL	-
TCLK[1]	119	IN_CELL	1		TDN[7]	53	IN_CELL	-
TDP[1]	118	IN_CELL	0		TDP[7]	52	IN_CELL	-
TDN[1]	117	IN_CELL	0		TCLK[7]	51	IN_CELL	-
TCLK[2]	116	IN_CELL	0		TDN[8]	50	IN_CELL	-
TDP[2]	115	IN_CELL	1		TDP[8]	49	IN_CELL	-
TDN[2]	114	IN_CELL	1		TCLK[8]	48	IN_CELL	-
TCLK[3]	113	IN_CELL	0		HW_ONLY	47	IN_CELL	-
TDP[3]	112	IN_CELL	0		SRCASC	46	IN_CELL	-
TDN[3]	111	IN_CELL	0		OEB_SREN	45	OUT_CELL	-
TCLK[4]	110	IN_CELL	0		SREN	44	IO_CELL	-
TDP[4]	109	IN_CELL	0		OEB_SRCLK	43	OUT_CELL	-
TDN[4]	108	IN_CELL	0		SRCLK	42	IO_CELL	-
OEB_RCLK[1]	107	OUT_CELL	0		OEB_SRDI	41	OUT_CELL	-
RCLK[1]	106	OUT_CELL	1		SRDI	40	OUT_CELL	-
OEB_RDP[1]	105	OUT_CELL	1		SRDO	39	IN_CELL	-
RDP[1]	104	OUT_CELL	0		OEB_SRCEN	38	OUT_CELL	-
OEB_RDN[1]	103	OUT_CELL	0		SRCEN	37	OUT_CELL	-
RDN[1]	102	OUT_CELL	1		OEB_SRCCLK	36	OUT_CELL	-
OEB_RCLK[2]	101	OUT_CELL	1		SRCCLK	35	OUT_CELL	-
RCLK[2]	100	OUT_CELL	0		OEB_SRCDO	34	OUT_CELL	-
OEB_RDP[2]	99	OUT_CELL	1		SRCDO	33	OUT_CELL	-
RDP[2]	98	OUT_CELL	-		SRCODE	32	IN_CELL	-
OEB_RDN[2]	97	OUT_CELL	-		OEB_LOS_L1	31	OUT_CELL	-
RDN[2]	96	OUT_CELL	-		LOS_L1	30	OUT_CELL	-
OEB_RCLK[3]	95	OUT_CELL	-		OEB_LOS	29	OUT_CELL	-
RCLK[3]	94	OUT_CELL	-		LOS	28	OUT_CELL	-

OEB_RDP[3]	93	OUT_CELL	-		OEB_RSYNC	27	OUT_CELL	-
RDP[3]	92	OUT_CELL	-		RSYNC	26	OUT_CELL	-
OEB_RDN[3]	91	OUT_CELL	-		RES[1]	25	IN_CELL	-
RDN[3]	90	OUT_CELL	-		RSTB	24	IN_CELL	-
OEB_RCLK[4]	89	OUT_CELL	-		XCLK	23	IN_CELL	-
RCLK[4]	88	OUT_CELL	-		SBI_EN	22	IN_CELL	-
OEB_RDP[4]	87	OUT_CELL	-		OEB_D[7]	21	OUT_CELL	-
RDP[4]	86	OUT_CELL	-		D[7]	20	IO_CELL	-
OEB_RDN[4]	85	OUT_CELL	-		OEB_D[6]	19	OUT_CELL	-
RDN[4]	84	OUT_CELL	-		D[6]	18	IO_CELL	-
OEB_RDN[5]	83	OUT_CELL	-		OEB_D[5]	17	OUT_CELL	-
RDN[5]	82	OUT_CELL	-		D[5]	16	IO_CELL	-
OEB_RDP[5]	81	OUT_CELL	-		OEB_D[4]	15	OUT_CELL	-
RDP[5]	80	OUT_CELL	-		D[4]	14	IO_CELL	-
OEB_RCLK[5]	79	OUT_CELL	-		OEB_D[3]	13	OUT_CELL	-
RCLK[5]	78	OUT_CELL	-		D[3]	12	IO_CELL	-
OEB_RDN[6]	77	OUT_CELL	-		OEB_D[2]	11	OUT_CELL	-
RDN[6]	76	OUT_CELL	-		D[2]	10	IO_CELL	-
OEB_RDP[6]	75	OUT_CELL	-		OEB_D[1]	9	OUT_CELL	-
RDP[6]	74	OUT_CELL	-		D[1]	8	IO_CELL	-
OEB_RCLK[6]	73	OUT_CELL	-		OEB_D[0]	7	OUT_CELL	-
RCLK[6]	72	OUT_CELL	-		D[0]	6	IO_CELL	-
OEB_RDN[7]	71	OUT_CELL	-		OEB_INTB	5	OUT_CELL	-
RDN[7]	70	OUT_CELL	-		INTB	4	IO_CELL	-
OEB_RDP[7]	69	OUT_CELL	-		CSB	3	IN_CELL	-
RDP[7]	68	OUT_CELL	-		RDB	2	IN_CELL	-
OEB_RCLK[7]	67	OUT_CELL	-		WRB	1	IN_CELL	-
RCLK[7]	66	OUT_CELL	-		ALE	0	IN_CELL	-
OEB_RDN[8]	65	OUT_CELL	-					

Notes:

1. OEB signals, when set low, will set the corresponding bidirectional signal to an output.
2. OEB signals, when set high, will set the corresponding output to high impedance.
3. ALE is the first bit in the boundary scan chain scanned in and out. It is closest to TDO in the scan chain.

12 OPERATION

12.1 Configuring the OCTLIU from Reset

After a system reset (either via the RSTB pin or via the RESET register bit), the OCTLIU will default to the following settings:

Table 19 – Default Settings

Setting	Receiver Section	Transmitter Section
T1/E1 mode	T1	T1
Line Code	B8ZS	B8ZS
Line interface	Pins RXTIP[x] and RXRING[x] active short haul analogue inputs	TXTIP1[x], TXTIP2[x], TXRING1[x], TXRING2[x] tristated
Timing Options	Not applicable	Jitter attenuation enabled, with output clock frequency referenced to TCLK[n]
Diagnostics	All diagnostic modes disabled	All diagnostic modes disabled

12.2 Servicing Interrupts

The OCTLIU will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the bits of the Master Interrupt Source registers (002H and 003H) to identify which octants and/or SBI interface blocks generated the interrupt. For example, a logic one read in the LIU[2] bit of the Master Interrupt Source #1 register indicates that octant #2 produced the interrupt.

2. Read the bits of the second level Line Interface Interrupt Source registers to identify the block within the octant generating the interrupt.
   The Interrupt Source registers for octant #1 are at addresses 00CH and 00DH.
   The Interrupt Source registers for octant #2 are at addresses 08CH and 08DH.
   The Interrupt Source registers for octant #3 are at addresses 10CH and 10DH.
   The Interrupt Source registers for octant #4 are at addresses 18CH and 18DH.
   The Interrupt Source registers for octant #5 are at addresses 20CH and 20DH.
   The Interrupt Source registers for octant #6 are at addresses 28CH and 28DH.
   The Interrupt Source registers for octant #7 are at addresses 30CH and 30DH.
   The Interrupt Source registers for octant #8 are at addresses 38CH and 38DH.

3. Read the third level Interrupt Source bits to identify the interrupt source. (These bits are contained within the registers for the various functional blocks.)

4. Service the interrupt.

5. If the INTB pin is still logic 0, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB

12.3 Using the Performance Monitoring Features

The PMON blocks are provided for performance monitoring purposes. The PMON blocks within each LIU are used to monitor LCV events. An accumulation interval is initiated by writing to one of the PMON event counter register addresses or by writing to the Line Interface Interrupt Source / PMON Update register. After initiating an accumulation interval, 3.5 recovered clock periods must be allowed to elapse to permit the PMON counter values to be properly transferred before the PMON registers may be read.

12.4 Using the Transmit Line Pulse Generator

The internal D/A pulse waveform template RAM, accessible via the microprocessor bus, can be used to create up to 12 custom waveforms. The RAM is accessed indirectly through the XLPG Pulse Waveform Storage Write Address and XLPG Pulse Waveform Storage Data registers. The values written into the pulse waveform storage registers correspond to one of 127 quantized levels. 24 samples are output during every transmit clock cycle.

The waveform being programmed is completely arbitrary and programming must be done properly in order to meet the various T1 and E1 template specifications. The SCALE[4:0] bits of Line Driver Configuration Register bits are used to obtain a proper output amplitude. It must also be noted that since samples from the 5 UI are added before driving the DAC, it is possible to create arithmetic overflows. The XLPG detects overflows and saturates the resulting value to –62 or +62 as appropriate. However, it is recommended that the pulse amplitude be programmed such that overflows are avoided. It is possible to verify if an overflow condition occurred by reading the OVRFLW register bit after programming a new waveform and transmission of data.

The following tables contain the waveform values to be programmed for different situations. Table 20 to Table 29 specify waveform values typically used for T1 long haul and short haul transmission. Table 30 to Table 36 specify waveform values for compliance to the AT&T TR62411 ACCUNET T1.5 pulse template. Table 37 and Table 38 specify waveform values for E1 transmission. The T1 and E1 waveforms shown in these tables (but not the TR62411 waveforms) are also stored in a ROM within the OCTLIU. The ROM contents can be automatically loaded into the waveform template RAM by setting the INITRAM bit in XLPG Control/Status register.

Note that the programming of template values must observe the following sequencing rule: Samples must be written in groups of 5 at a time, each group consisting of the 5 UI values corresponding to a particular waveform and sample number. For example, the following programming sequence fragment is legal:

```
:
Write data for WAVEFORM=0, SAMPLE=0, UI=0
Write data for WAVEFORM=0, SAMPLE=0, UI=1
Write data for WAVEFORM=0, SAMPLE=0, UI=2
Write data for WAVEFORM=0, SAMPLE=0, UI=3
Write data for WAVEFORM=0, SAMPLE=0, UI=4
Write data for WAVEFORM=1, SAMPLE=12, UI=0
Write data for WAVEFORM=1, SAMPLE=12, UI=1
Write data for WAVEFORM=1, SAMPLE=12, UI=2
Write data for WAVEFORM=1, SAMPLE=12, UI=3
Write data for WAVEFORM=1, SAMPLE=12, UI=4
:
```

whereas the following sequence fragment is illegal:

```
:
Write data for WAVEFORM=0, SAMPLE=0, UI=0
Write data for WAVEFORM=0, SAMPLE=1, UI=0
Write data for WAVEFORM=0, SAMPLE=2, UI=0
Write data for WAVEFORM=0, SAMPLE=3, UI=0
Write data for WAVEFORM=0, SAMPLE=4, UI=0
Write data for WAVEFORM=0, SAMPLE=5, UI=0
Write data for WAVEFORM=0, SAMPLE=6, UI=0
Write data for WAVEFORM=0, SAMPLE=7, UI=0
Write data for WAVEFORM=0, SAMPLE=8, UI=0
Write data for WAVEFORM=0, SAMPLE=9, UI=0
:
```

This restriction is necessary because each group of five 7-bit samples is stored in a temporary holding register as it is written. The 5 samples are then transferred to the pulse template RAM as a single 35-bit word when the 5^{th} sample (i.e. the sample whose UI[2:0] address field is set to 4) is written.

Prior to commencing normal operation, the HIGHZ bit of the octant's XLPG Line Driver Configuration register must be programmed to logic 0 to remove the high impedance state from the TXTIP1[x], TXTIP2[x], TXRING1[x] and TXRING2[x] Transmit outputs.

Table 20 – T1.102 Transmit Waveform Values for T1 Long Haul (LBO 0 dB)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	44	00	00	00
2	08	44	00	00	00
3	15	43	00	00	00
4	28	43	00	00	00
5	36	42	00	00	00
6	3A	42	00	00	00
7	3A	41	00	00	00
8	38	41	00	00	00
9	38	00	00	00	00
10	38	00	00	00	00
11	38	00	00	00	00
12	37	00	00	00	00
13	36	00	00	00	00
14	34	00	00	00	00
15	30	00	00	00	00
16	1B	00	00	00	00
17	00	00	00	00	00
18	4E	00	00	00	00
19	4C	00	00	00	00
20	49	00	00	00	00
21	47	00	00	00	00
22	47	00	00	00	00
23	46	00	00	00	00
24	46	00	00	00	00

Note: SCALE[4:0] programmed to 0AH.

Table 21 – T1.102 Transmit Waveform Values for T1 Long Haul (LBO 7.5 dB)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	10	00	00	00
2	01	0E	00	00	00
3	02	0C	00	00	00
4	04	0A	00	00	00
5	08	08	00	00	00
6	0C	06	00	00	00
7	10	04	00	00	00
8	16	02	00	00	00
9	1A	01	00	00	00
10	1E	00	00	00	00
11	22	00	00	00	00
12	26	00	00	00	00
13	2A	00	00	00	00
14	2B	00	00	00	00
15	2C	00	00	00	00
16	2D	00	00	00	00
17	2C	00	00	00	00
18	28	00	00	00	00
19	24	00	00	00	00
20	20	00	00	00	00
21	1C	00	00	00	00
22	18	00	00	00	00
23	14	00	00	00	00
24	12	00	00	00	00

Note: SCALE[4:0] programmed to 06H.

Table 22 – T1.102 Transmit Waveform Values for T1 Long Haul (LBO 15 dB)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	22	07	01	00
2	00	20	06	01	00
3	00	1E	06	01	00
4	00	1D	06	01	00
5	01	1B	06	01	00
6	02	1A	05	00	00
7	04	18	05	00	00
8	06	16	04	00	00
9	08	15	04	00	00
10	0A	14	04	00	00
11	0D	13	03	00	00
12	10	12	03	00	00
13	13	11	03	00	00
14	16	0F	02	00	00
15	18	0E	02	00	00
16	1A	0D	02	00	00
17	1D	0C	02	00	00
18	1F	0B	02	00	00
19	22	0A	02	00	00
20	23	0A	01	00	00
21	24	09	01	00	00
22	25	08	01	00	00
23	25	08	01	00	00
24	23	07	01	00	00

Note: SCALE[4:0] programmed to 03H.

Table 23 – T1.102 Transmit Waveform Values for T1 Long Haul (LBO 22.5 dB)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	31	23	0A	01
2	00	33	22	09	01
3	00	35	21	08	01
4	00	36	20	08	01
5	00	37	1E	07	00
6	00	38	1D	06	00
7	01	39	1C	06	00
8	02	39	1B	05	00
9	03	38	1A	05	00
10	04	38	19	05	00
11	05	37	18	04	00
12	08	36	17	04	00
13	0B	35	16	04	00
14	0E	33	15	03	00
15	12	31	13	03	00
16	16	2F	12	03	00
17	1A	2E	11	03	00
18	1E	2D	10	03	00
19	22	2B	0F	02	00
20	25	2A	0E	02	00
21	28	29	0D	02	00
22	2B	27	0D	02	00
23	2E	25	0B	02	00
24	30	24	0A	01	00

Note: SCALE[4:0] programmed to 01H.

Table 24 – T1.102 Transmit Waveform Values for T1 Short Haul (0 – 110 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	44	00	00	00
2	0A	44	00	00	00
3	1A	43	00	00	00
4	28	43	00	00	00
5	3D	42	00	00	00
6	3C	42	00	00	00
7	3B	41	00	00	00
8	39	41	00	00	00
9	39	00	00	00	00
10	38	00	00	00	00
11	38	00	00	00	00
12	37	00	00	00	00
13	36	00	00	00	00
14	34	00	00	00	00
15	30	00	00	00	00
16	1D	00	00	00	00
17	00	00	00	00	00
18	56	00	00	00	00
19	53	00	00	00	00
20	4F	00	00	00	00
21	4C	00	00	00	00
22	49	00	00	00	00
23	47	00	00	00	00
24	46	00	00	00	00

Note: SCALE[4:0] programmed to 0AH.

Table 25 – T1.102 Transmit Waveform Values for T1 Short Haul (110 – 220 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	45	00	00	00
2	0A	44	00	00	00
3	1B	43	00	00	00
4	29	43	00	00	00
5	33	42	00	00	00
6	33	42	00	00	00
7	30	41	00	00	00
8	2F	41	00	00	00
9	2E	00	00	00	00
10	2E	00	00	00	00
11	2D	00	00	00	00
12	2C	00	00	00	00
13	2C	00	00	00	00
14	29	00	00	00	00
15	26	00	00	00	00
16	00	00	00	00	00
17	54	00	00	00	00
18	51	00	00	00	00
19	4D	00	00	00	00
20	49	00	00	00	00
21	48	00	00	00	00
22	47	00	00	00	00
23	46	00	00	00	00
24	45	00	00	00	00

Note: SCALE[4:0] programmed to 0DH.

Table 26 – T1.102 Transmit Waveform Values for T1 Short Haul (220 – 330 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	44	00	00	00
2	0A	44	00	00	00
3	1E	43	00	00	00
4	2D	43	00	00	00
5	36	42	00	00	00
6	34	42	00	00	00
7	30	41	00	00	00
8	2F	41	00	00	00
9	2D	00	00	00	00
10	2D	00	00	00	00
11	2C	00	00	00	00
12	2B	00	00	00	00
13	2A	00	00	00	00
14	29	00	00	00	00
15	26	00	00	00	00
16	00	00	00	00	00
17	58	00	00	00	00
18	54	00	00	00	00
19	4F	00	00	00	00
20	4A	00	00	00	00
21	49	00	00	00	00
22	47	00	00	00	00
23	47	00	00	00	00
24	46	00	00	00	00

Note: SCALE[4:0] programmed to 0EH.

Table 27 – T1.102 Transmit Waveform Values for T1 Short Haul (330 – 440 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	44	00	00	00
2	0A	44	00	00	00
3	24	43	00	00	00
4	2C	43	00	00	00
5	36	42	00	00	00
6	34	42	00	00	00
7	2F	41	00	00	00
8	2D	41	00	00	00
9	2C	00	00	00	00
10	2C	00	00	00	00
11	2B	00	00	00	00
12	2A	00	00	00	00
13	29	00	00	00	00
14	28	00	00	00	00
15	1C	00	00	00	00
16	00	00	00	00	00
17	5A	00	00	00	00
18	54	00	00	00	00
19	4F	00	00	00	00
20	4A	00	00	00	00
21	49	00	00	00	00
22	47	00	00	00	00
23	47	00	00	00	00
24	46	00	00	00	00

Note: SCALE[4:0] programmed to 0FH.

Table 28 – T1.102 Transmit Waveform Values for T1 Short Haul (440 – 550 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	44	00	00	00
2	0A	44	00	00	00
3	25	43	00	00	00
4	37	43	00	00	00
5	33	42	00	00	00
6	31	42	00	00	00
7	2F	41	00	00	00
8	2D	41	00	00	00
9	2B	00	00	00	00
10	2B	00	00	00	00
11	2A	00	00	00	00
12	2A	00	00	00	00
13	28	00	00	00	00
14	25	00	00	00	00
15	1A	00	00	00	00
16	00	00	00	00	00
17	5E	00	00	00	00
18	59	00	00	00	00
19	4F	00	00	00	00
20	4A	00	00	00	00
21	49	00	00	00	00
22	47	00	00	00	00
23	47	00	00	00	00
24	46	00	00	00	00

Note: SCALE[4:0] programmed to 10H.

Table 29 – T1.102 Transmit Waveform Values for T1 Short Haul (550 – 660 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	45	00	00	00
2	08	45	00	00	00
3	30	43	00	00	00
4	3B	43	00	00	00
5	3B	42	00	00	00
6	31	42	00	00	00
7	30	41	00	00	00
8	2F	41	00	00	00
9	2E	00	00	00	00
10	2D	00	00	00	00
11	2C	00	00	00	00
12	2B	00	00	00	00
13	2A	00	00	00	00
14	28	00	00	00	00
15	0C	00	00	00	00
16	00	00	00	00	00
17	68	00	00	00	00
18	5D	00	00	00	00
19	51	00	00	00	00
20	4B	00	00	00	00
21	4A	00	00	00	00
22	48	00	00	00	00
23	48	00	00	00	00
24	47	00	00	00	00

Note: SCALE[4:0] programmed to 10H.

Table 30 – TR62411 Transmit Waveform Values for T1 Long Haul (LBO 0 dB)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	08	00	00	00	00
3	15	00	00	00	00
4	28	00	00	00	00
5	36	00	00	00	00
6	3A	00	00	00	00
7	3A	00	00	00	00
8	38	00	00	00	00
9	38	00	00	00	00
10	38	00	00	00	00
11	38	00	00	00	00
12	37	00	00	00	00
13	36	00	00	00	00
14	34	00	00	00	00
15	30	00	00	00	00
16	1B	00	00	00	00
17	00	00	00	00	00
18	4E	00	00	00	00
19	4C	00	00	00	00
20	49	00	00	00	00
21	46	00	00	00	00
22	43	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 0AH.

Table 31 – TR62411 Transmit Waveform Values for T1 Short Haul (0 – 110 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	0A	00	00	00	00
3	1A	00	00	00	00
4	28	00	00	00	00
5	3D	00	00	00	00
6	3C	00	00	00	00
7	3B	00	00	00	00
8	39	00	00	00	00
9	39	00	00	00	00
10	38	00	00	00	00
11	38	00	00	00	00
12	37	00	00	00	00
13	36	00	00	00	00
14	34	00	00	00	00
15	30	00	00	00	00
16	1D	00	00	00	00
17	00	00	00	00	00
18	4F	00	00	00	00
19	4C	00	00	00	00
20	49	00	00	00	00
21	46	00	00	00	00
22	43	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 0AH.

Table 32 – TR62411 Transmit Waveform Values for T1 Short Haul (110 – 220 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	0A	00	00	00	00
3	1B	00	00	00	00
4	29	00	00	00	00
5	33	00	00	00	00
6	33	00	00	00	00
7	30	00	00	00	00
8	2F	00	00	00	00
9	2E	00	00	00	00
10	2E	00	00	00	00
11	2D	00	00	00	00
12	2C	00	00	00	00
13	2C	00	00	00	00
14	29	00	00	00	00
15	26	00	00	00	00
16	00	00	00	00	00
17	54	00	00	00	00
18	50	00	00	00	00
19	4C	00	00	00	00
20	48	00	00	00	00
21	45	00	00	00	00
22	42	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 0DH.

Table 33 – TR62411 Transmit Waveform Values for T1 Short Haul (220 – 330 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	0A	00	00	00	00
3	1E	00	00	00	00
4	2D	00	00	00	00
5	36	00	00	00	00
6	34	00	00	00	00
7	30	00	00	00	00
8	2F	00	00	00	00
9	2D	00	00	00	00
10	2D	00	00	00	00
11	2C	00	00	00	00
12	2B	00	00	00	00
13	2A	00	00	00	00
14	29	00	00	00	00
15	26	00	00	00	00
16	00	00	00	00	00
17	58	00	00	00	00
18	54	00	00	00	00
19	4F	00	00	00	00
20	4B	00	00	00	00
21	47	00	00	00	00
22	43	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 0EH.

Table 34 – TR62411 Transmit Waveform Values for T1 Short Haul (330 – 440 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	0A	00	00	00	00
3	24	00	00	00	00
4	2C	00	00	00	00
5	36	00	00	00	00
6	34	00	00	00	00
7	2F	00	00	00	00
8	2D	00	00	00	00
9	2C	00	00	00	00
10	2C	00	00	00	00
11	2B	00	00	00	00
12	2A	00	00	00	00
13	29	00	00	00	00
14	28	00	00	00	00
15	1C	00	00	00	00
16	00	00	00	00	00
17	5A	00	00	00	00
18	54	00	00	00	00
19	4F	00	00	00	00
20	4B	00	00	00	00
21	47	00	00	00	00
22	43	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 0FH.

Table 35 – TR62411 Transmit Waveform Values for T1 Short Haul (440 – 550 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	0A	00	00	00	00
3	25	00	00	00	00
4	37	00	00	00	00
5	33	00	00	00	00
6	31	00	00	00	00
7	2F	00	00	00	00
8	2D	00	00	00	00
9	2B	00	00	00	00
10	2B	00	00	00	00
11	2A	00	00	00	00
12	2A	00	00	00	00
13	28	00	00	00	00
14	25	00	00	00	00
15	1A	00	00	00	00
16	00	00	00	00	00
17	5E	00	00	00	00
18	59	00	00	00	00
19	53	00	00	00	00
20	4E	00	00	00	00
21	49	00	00	00	00
22	44	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 10H.

Table 36 – TR62411 Transmit Waveform Values for T1 Short Haul (550 – 660 ft.)

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	08	00	00	00	00
3	30	00	00	00	00
4	3B	00	00	00	00
5	3B	00	00	00	00
6	31	00	00	00	00
7	30	00	00	00	00
8	2F	00	00	00	00
9	2E	00	00	00	00
10	2D	00	00	00	00
11	2C	00	00	00	00
12	2B	00	00	00	00
13	2A	00	00	00	00
14	28	00	00	00	00
15	0C	00	00	00	00
16	00	00	00	00	00
17	68	00	00	00	00
18	5D	00	00	00	00
19	53	00	00	00	00
20	4D	00	00	00	00
21	49	00	00	00	00
22	44	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 10H.

Table 37 – Transmit Waveform Values for E1 120 Ohm

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	00	00	00	00	00
3	0A	00	00	00	00
4	26	00	00	00	00
5	32	00	00	00	00
6	32	00	00	00	00
7	32	00	00	00	00
8	32	00	00	00	00
9	32	00	00	00	00
10	32	00	00	00	00
11	32	00	00	00	00
12	32	00	00	00	00
13	32	00	00	00	00
14	32	00	00	00	00
15	26	00	00	00	00
16	0A	00	00	00	00
17	00	00	00	00	00
18	00	00	00	00	00
19	00	00	00	00	00
20	00	00	00	00	00
21	00	00	00	00	00
22	00	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 0AH.

Table 38 – Transmit Waveform Values for E1 75 Ohm

Sample number	UI #0	UI #1	UI #2	UI #3	UI #4
1	00	00	00	00	00
2	00	00	00	00	00
3	0A	00	00	00	00
4	28	00	00	00	00
5	34	00	00	00	00
6	34	00	00	00	00
7	34	00	00	00	00
8	34	00	00	00	00
9	34	00	00	00	00
10	34	00	00	00	00
11	34	00	00	00	00
12	34	00	00	00	00
13	34	00	00	00	00
14	34	00	00	00	00
15	2D	00	00	00	00
16	0A	00	00	00	00
17	00	00	00	00	00
18	00	00	00	00	00
19	00	00	00	00	00
20	00	00	00	00	00
21	00	00	00	00	00
22	00	00	00	00	00
23	00	00	00	00	00
24	00	00	00	00	00

Note: SCALE[4:0] programmed to 0CH.

12.5 Using the Line Receiver

The line receiver must be properly initialized for correct operation. Several register bits must be programmed and the equalizer RAM table must be initialized according to the appropriate table below.

The RLPS equalizer RAM content is programmed by the RLPS Equalization Indirect Data registers for each address location. The address location is given by the octant's RLPS Equalization Indirect Address register. A read or write request is done by setting the RWB bit in the octant's RLPS Equalization Read/WriteB Select register.

Note that several registers are not their default values. The EQ_EN bit of the RLPS Equalizer Configuration register must be set to logic 1. The CUTOFF[1:0] bits of the RLPS Voltage Thresholds #2 register must be programmed to 3H (11B) for T1 mode or 0H (00B) for E1 mode. Table 39 summarizes the values the RLPS registers are to contain.

Table 39 – RLPS Register Programming

Register	Data Value	
	Bin	Hex
RLPS Configuration and Status	XX000XX1	01H
RLPS ALOS Detection/ Clearance Threshold	X000X000	00H
RLPS ALOS Detection Period	00000001	01H
RLPS ALOS Clearance Period	00000001	01H
RLPS Equalization Indirect Address	00000000	00H
RLPS Equalization RAM Read/WriteB Select	1XXXXXXX	80H
RLPS Equalizer Loop Status and Control	00000000	00H
RLPS Equalizer Configuration	00X01011	0BH
RLPS Equalization Indirect Data[31:24]	*	*
RLPS Equalization Indirect Data[23:16]	*	*
RLPS Equalization Indirect Data[15:8]	*	*
RLPS Equalization Indirect Data[7:0]	*	*
RLPS Voltage Thresholds #1	XX101110	2EH
RLPS Voltage Thresholds #2 (T1 mode) (E1 mode)	 11XXX011 00XXX011	 C3H 03H

Since the line receiver supports both E1 and T1 standards over either short haul or long haul cables, the line receiver has two normal modes of operation, as selected by the E1/T1B bit of the Global Configuration register.

Access to the Equalizer RAM is provided by means of Indirect Access Registers A typical programming sequence follows. This programming sequence is repeated for each of the 256 Equalizer RAM Addresses.

```
WRITE RLPS Indirect Data Register  <31 – 24 Bits of Data>

WRITE RLPS Indirect Data Register  <23 – 16 Bits of Data>

WRITE RLPS Indirect Data Register  <15 – 8 Bits of Data>

WRITE RLPS Indirect Data Register  <7 – 0 Bits of Data>

ACTION RLPS Equalisation Read/WriteB Select Register
    <A=80H for "read"; A=00H for "write" action>

WRITE RLPS Equalisation Indirect Address Register
    <address from 0 to 255>

PAUSE  <wait 3 line rate clock cycles>
```

Table 40 – RLPS Equalizer RAM Table (T1 mode)

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
00D	03061C3BH	128D	766B38BBH
01D	03061C3BH	129D	766B38BBH
02D	03061C3BH	130D	766B38BBH
03D	03061C3BH	131D	7E6B38BBH
04D	03061C3BH	132D	7E7338BBH
05D	03062C3BH	133D	7E73393BH
06D	03062C3BH	134D	7E733D3BH
07D	03062C3BH	135D	7E7B3D3BH
08D	03062C3BH	136D	7E7B3D3BH
09D	03062C3BH	137D	867B3D3BH
10D	030E2C3BH	138D	867B4D3BH
11D	030E2C3BH	139D	867B4D3BH
12D	030E2C3BH	140D	867B4D3BH
13D	03162C3BH	141D	867B5D3BH
14D	03162C3BH	142D	867B5D3BH
15D	03162C3BH	143D	8E7B5D3BH
16D	03162C3BH	144D	8E7B6D3BH
17D	03163C3BH	145D	8E7B6D3BH
18D	03163C3BH	146D	8E7B6D3BH
19D	03163C3BH	147D	8E7B7D3BH
20D	03163C3BH	148D	8E7B7D3BH
21D	03163C3BH	149D	967B7D3BH
22D	03163C3BH	150D	967B7D3BH
23D	031E3C3BH	151D	967B7D3BH
24D	031C3C3BH	152D	967B793BH
25D	031C3C3BH	153D	967B793BH

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
26D	031C3C3BH	154D	967B793BH
27D	031C3C3BH	155D	9E7B793BH
28D	031C3C3BH	156D	9E7B793BH
29D	03243C3BH	157D	9E7B793BH
30D	03244C3BH	158D	9E83793BH
31D	03244C3BH	159D	9D83793BH
32D	03244C3BH	160D	9D83793BH
33D	03244C3BH	161D	9D83793BH
34D	03244C3BH	162D	A583793BH
35D	032C4C3BH	163D	A583893BH
36D	032E4C3BH	164D	A583893BH
37D	032E5C3BH	165D	A583893BH
38D	032E6C3BH	166D	A583993BH
39D	032E6C3BH	167D	A583993BH
40D	032E6C3BH	168D	AD83993BH
41D	032E7C3BH	169D	AD8B993BH
42D	032E7C3BH	170D	AD8BA93BH
43D	032E7C3BH	171D	AD89A93BH
44D	072E8C3BH	172D	AD89A93BH
45D	072E8C3BH	173D	AD89A93BH
46D	0F2E8C3BH	174D	B589A93BH
47D	0F2E8C3BH	175D	B589A93BH
48D	0F368C3BH	176D	B589B93BH
49D	0F368C3BH	177D	B589B53BH
50D	0F368C3BH	178D	B589B53BH
51D	0F368C3BH	179D	B589B53BH
52D	17368C3BH	180D	BD89B53BH
53D	17369C3BH	181D	BD89B53BH
54D	17369C3BH	182D	BD91B53BH
55D	17369C3BH	183D	BD91B53BH
56D	1736AC3BH	184D	BD91B53BH
57D	1736AC3BH	185D	BD91B53BH
58D	1F3EAC3BH	186D	C591B53BH
59D	1F3E9C3BH	187D	C591C53BH
60D	1F3E9C3BH	188D	C591C53BH
61D	1F469C3BH	189D	C591C53BH
62D	1E469C3BH	190D	C591D53BH
63D	1E469C3BH	191D	C591D53BH
64D	26469C3BH	192D	CD91D53BH
65D	2646AC3BH	193D	CD99D53BH
66D	2646AC3BH	194D	CC99D53BH
67D	2646AC3BH	195D	CC99D4BBH
68D	2646BC3BH	196D	CCA1D4BBH

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
69D	2646BC3BH	197D	CCA1D4BBH
70D	2E46BC3BH	198D	D4A1D4BBH
71D	2E46BC3BH	199D	D4A1D4BBH
72D	2E4EBC3BH	200D	D4A1D53BH
73D	2E4ECC3BH	201D	D4A1D13BH
74D	2E4ECC3BH	202D	D4A3D13BH
75D	2E4ECC3BH	203D	D4A3D13BH
76D	364ECC3BH	204D	DCA3D13BH
77D	364ECC3BH	205D	DCA3D13BH
78D	3656CC3BH	206D	DCABD13BH
79D	3656DC3BH	207D	DCA9D13BH
80D	3656DC3BH	208D	DCA9D13BH
81D	3656DC3BH	209D	DCA9D13BH
82D	3E56DC3BH	210D	E4A9D13BH
83D	3E56DC3BH	211D	E4A9D1BBH
84D	3E56EC3BH	212D	E4B1D1BBH
85D	3E54EC3BH	213D	E4B1D1BBH
86D	3E54EC3BH	214D	E4B1C1BBH
87D	3E54EC3BH	215D	E4B1C1BBH
88D	4654EC3BH	216D	ECB1C1BBH
89D	4654EC3BH	217D	ECB1C1BBH
90D	465CEC3BH	218D	ECB1D1BBH
91D	465CEC3BH	219D	ECB1D1BBH
92D	465CEC3BH	220D	ECB1D1BBH
93D	465CEC3BH	221D	ECB1D1BBH
94D	4E5CEC3BH	222D	F4B1D1BBH
95D	4E5CEC3BH	223D	F4B1D1BBH
96D	4E5CFC3BH	224D	F4B1D23BH
97D	4E5EFC3BH	225D	F4B9D23BH
98D	4E5EF83BH	226D	F4B9C23BH
99D	4E5EF83BH	227D	F4B9C23BH
100D	4E5EF83BH	228D	F4B9C23BH
101D	565EF83BH	229D	FCB9C23BH
102D	565F083BH	230D	FCB9D23BH
103D	565F083BH	231D	FCB9D23BH
104D	565F083BH	232D	FCB9D23BH
105D	565F183BH	233D	FCB9E23BH
106D	565F183BH	234D	FCB9E23BH
107D	5E5F183BH	235D	FCB9E23BH
108D	5E5F183BH	236D	FCB9E23BH
109D	5E5F283BH	237D	FCB9E2BBH
110D	5E67283BH	238D	FCB9D2BBH
111D	5E67283BH	239D	FCB9D2BBH

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
112D	5E67283BH	240D	FCB9D2BBH
113D	6667283BH	241D	FCB9D2BBH
114D	6665283BH	242D	FCB9D2BBH
115D	6665283BH	243D	FCB9E2BBH
116D	6665283BH	244D	FCB9E2BBH
117D	6663283BH	245D	FCB9E2BBH
118D	6663283BH	246D	FCB9E2BBH
119D	6E63283BH	247D	FCB9E2BBH
120D	6E6B283BH	248D	FCB9E2BBH
121D	6E6B28BBH	249D	FCB9E2BBH
122D	6E6B2CBBH	250D	FCB9E2BBH
123D	6E732CBBH	251D	FCB9E2BBH
124D	6E732CBBH	252D	FCB9F2BBH
125D	76732CBBH	253D	FCB9F2BBH
126D	767328BBH	254D	FCB9F2BBH
127D	767338BBH	255D	FCB9F2BBH

Table 41 – RLPS Equalizer RAM Table (E1 mode)

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
00D	03062C3BH	128D	8A80F93BH
01D	03062C3BH	129D	8A80F9BBH
02D	03062C3BH	130D	8A80F9BBH
03D	03062C3BH	131D	9280F9BBH
04D	030E2C3BH	132D	928109BBH
05D	030E2C3BH	133D	918109BBH
06D	03162C3BH	134D	918119BBH
07D	03162C3BH	135D	918119BBH
08D	03162C3BH	136D	998129BBH
09D	03163C3BH	137D	998125BBH
10D	031E3C3BH	138D	998135BBH
11D	031E3C3BH	139D	998135BBH
12D	031E3C3BH	140D	998131BBH
13D	031E3C3BH	141D	A18131BBH
14D	031E3C3BH	142D	A18931BBH
15D	031E4C3BH	143D	A18931BBH
16D	031E4C3BH	144D	A18931BBH
17D	031E4C3BH	145D	A19131BBH
18D	031E4C3BH	146D	A19131BBH
19D	031E4C3BH	147D	A99131BBH
20D	03264C3BH	148D	A99131BBH
21D	03264C3BH	149D	A991323BH
22D	032E4C3BH	150D	A991323BH
23D	032E4C3BH	151D	A991323BH

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
24D	032E4C3BH	152D	B191323BH
25D	032E4C3BH	153D	B191323BH
26D	032E5C3BH	154D	B199323BH
27D	032E5C3BH	155D	B199323BH
28D	032E5C3BH	156D	B199323BH
29D	032E5C3BH	157D	B999323BH
30D	032E5C3BH	158D	B999323BH
31D	03365C3BH	159D	B999423BH
32D	03366C3BH	160D	B9A1423BH
33D	03366C3BH	161D	B9A1423BH
34D	03366C3BH	162D	B9A1423BH
35D	03366C3BH	163D	C1A1423BH
36D	03366C3BH	164D	C1A1523BH
37D	03367C3BH	165D	C1A1523BH
38D	03367C3BH	166D	C1A1623BH
39D	03367C3BH	167D	C1A1623BH
40D	0B367C3BH	168D	C9A1623BH
41D	0B3E7C3BH	169D	C9A1623BH
42D	0B3E8C3BH	170D	C9A1723BH
43D	0B3E8C3BH	171D	C9A172BBH
44D	0B3E8C3BH	172D	C9A172BBH
45D	133E8C3BH	173D	D1A172BBH
46D	13468C3BH	174D	D1A972BBH
47D	13469C3BH	175D	D1A972BBH
48D	13469C3BH	176D	D1A972BBH
49D	13469C3BH	177D	D1B172BBH
50D	13469C3BH	178D	D1B172BBH
51D	1B469C3BH	179D	D9B172BBH
52D	1B4E9C3BH	180D	D9B172BBH
53D	1B4EAC3BH	181D	D9B972BBH
54D	1B4EAC3BH	182D	D9B972BBH
55D	1B4EAC3BH	183D	D9B972BBH
56D	234EAC3BH	184D	E1B982BBH
57D	2346AC3BH	185D	E1BB82BBH
58D	2346ACBBH	186D	E0BB82BBH
59D	2346ACBBH	187D	E0BB92BBH
60D	2346ACBBH	188D	E0BB92BBH
61D	2B46ACBBH	189D	E8BB92BBH
62D	2B4EACBBH	190D	E8BB92BBH
63D	2B4EBCBBH	191D	E8BBA2BBH
64D	2B4EBCBBH	192D	E8C3A2BBH
65D	2B56BCBBH	193D	E8C3A2BBH
66D	2B56BCBBH	194D	E8C3A2BBH

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
67D	3356BCBBH	195D	F0C3A2BBH
68D	3356BCBBH	196D	F0C3A2BBH
69D	3356CCBBH	197D	F0CBA2BBH
70D	3356CCBBH	198D	F0CBA2BBH
71D	3356CCBBH	199D	F0CBA2BBH
72D	3B56CCBBH	200D	F8CBA2BBH
73D	3B5ECCBBH	201D	F8C3A2BBH
74D	3B5EDCBBH	202D	F8C3A33BH
75D	3B5EDCBBH	203D	F8C3A33BH
76D	3B5EDCBBH	204D	F8C3A33BH
77D	435EDCBBH	205D	F8C3A33BH
78D	435EDCBBH	206D	F8C3A33BH
79D	4366DCBBH	207D	F8CBA33BH
80D	4364DCBBH	208D	F8C9A33BH
81D	4364DCBBH	209D	F8C9A33BH
82D	4364DCBBH	210D	F8C9A33BH
83D	4B64DCBBH	211D	F8C9A33BH
84D	4B6CDCBBH	212D	F8C9A73BH
85D	4B6CECBBH	213D	F8C9A7BBH
86D	4B6CECBBH	214D	F8C9B7BBH
87D	4B6CECBBH	215D	F8C9B7BBH
88D	536CECBBH	216D	F8C9B7BBH
89D	536CE8BBH	217D	F8C9BBBBH
90D	536CF8BBH	218D	F8D1BBBBH
91D	536CF83BH	219D	F8D1BBBBH
92D	536CF83BH	220D	F8D1BBBBH
93D	5B6CF83BH	221D	F8D1BBBBH
94D	5B6CF83BH	222D	F8D1BBBBH
95D	5B6CF8BBH	223D	F8D1CBBBH
96D	5B64F8BBH	224D	F8D1CBBBH
97D	5B64F8BBH	225D	F8D1CBBBH
98D	5B64F8BBH	226D	F8D1CBBBH
99D	6364F8BBH	227D	F8D1CBBBH
100D	636CF8BBH	228D	F8D9CBBBH
101D	626CF8BBH	229D	F8D9CBBBH
102D	6274F8BBH	230D	F8E1CBBBH
103D	6274F8BBH	231D	F8E1CBBBH
104D	6A74F8BBH	232D	F8E1CBBBH
105D	6A74F8BBH	233D	F8E1CBBBH
106D	6A74F93BH	234D	F8E1C7BBH
107D	6A74F93BH	235D	F8D9C7BBH
108D	6A74F93BH	236D	F8D9D7BBH
109D	7274F93BH	237D	F8D9D7BBH

RAM Address	Content (MSB..LSB)	RAM Address	Content (MSB..LSB)
110D	7274F93BH	238D	F8D9D7BBH
111D	7274F93BH	239D	F8D9E7BBH
112D	7272F93BH	240D	F8D9E3BBH
113D	7272F93BH	241D	F8D9E3BBH
114D	7272F93BH	242D	F8D9E3BBH
115D	7A72F93BH	243D	F8D9E3BBH
116D	7A70F93BH	244D	F8D9E3BBH
117D	7A70E93BH	245D	F8D9F3BBH
118D	7A78E93BH	246D	F8D9F3BBH
119D	7A78E93BH	247D	F8D9F3BBH
120D	8278E93BH	248D	F8D9F3BBH
121D	8278E93BH	249D	F8D9F3BBH
122D	8278E8BBH	250D	F8D9F3BBH
123D	8278E8BBH	251D	F8D9F3BBH
124D	8278E8BBH	252D	F8D9F3BBH
125D	8A78E8BBH	253D	F8D9F3BBH
126D	8A78E93BH	254D	F8D9F3BBH
127D	8A78F93BH	255D	F8D9F3BBH

Table 42 – RLPS Equalizer RAM Table (Monitor Mode)

TBD

12.6 Using the PRBS Generator and Detector

PRBS patterns may be generated and detected in either the transmit or receive directions, as configured by the TX_GEN, RX_GEN and TX_DET bits of the Line Interface PRBS Position registers.

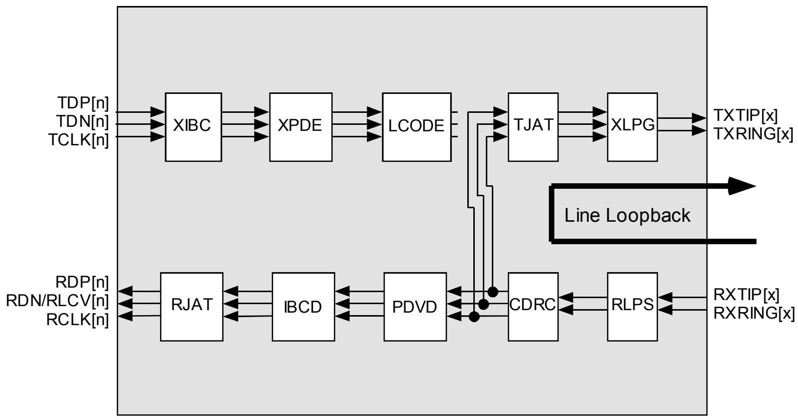
12.7 Loopback Modes

The OCTLIU provides two loopback modes to aid in network and system diagnostics. The network (line) loopback can be initiated at any time via the µP interface, but is usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the LIU.

12.7.1 Line Loopback

When LINE loopback (LINELB) is initiated by setting the LINELB bit in the Line Interface Diagnostics Register to logic 1, the LIU is configured to internally connect the recovered data to the transmit jitter attenuator, TJAT. The data sent to the TJAT is the recovered data from the output of the CDRC block. Note that when line loopback is enabled, the contents of the TJAT Reference Clock Divisor and Output Clock Divisor registers should be programmed to 2FH in T1 mode / FFH in E1 mode to correctly attenuate the jitter on the receive clock. Conceptually, the data flow through a single octant of the OCTLIU in this loopback mode is illustrated in Figure 18.

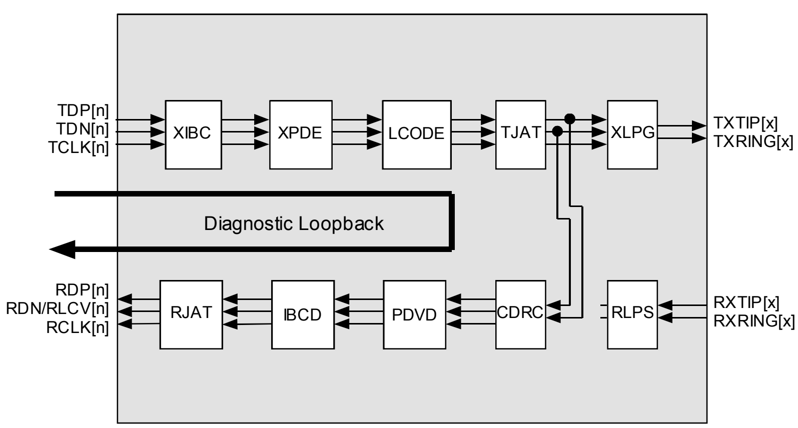
Figure 18 – Line Loopback



12.7.2 Diagnostic Digital Loopback

When Diagnostic Digital loopback (DDLB) mode is initiated by setting the DDLB bit in the Line Interface Diagnostics Register to logic 1, the OCTLIU octant is configured to internally direct the output of the TJAT to the inputs of the receiver section. The dual-rail RZ outputs of the TJAT are directed to the dual-rail inputs of the CDRC. Conceptually, the data flow through a single octant of the OCTLIU in this loopback condition is illustrated in Figure 19.

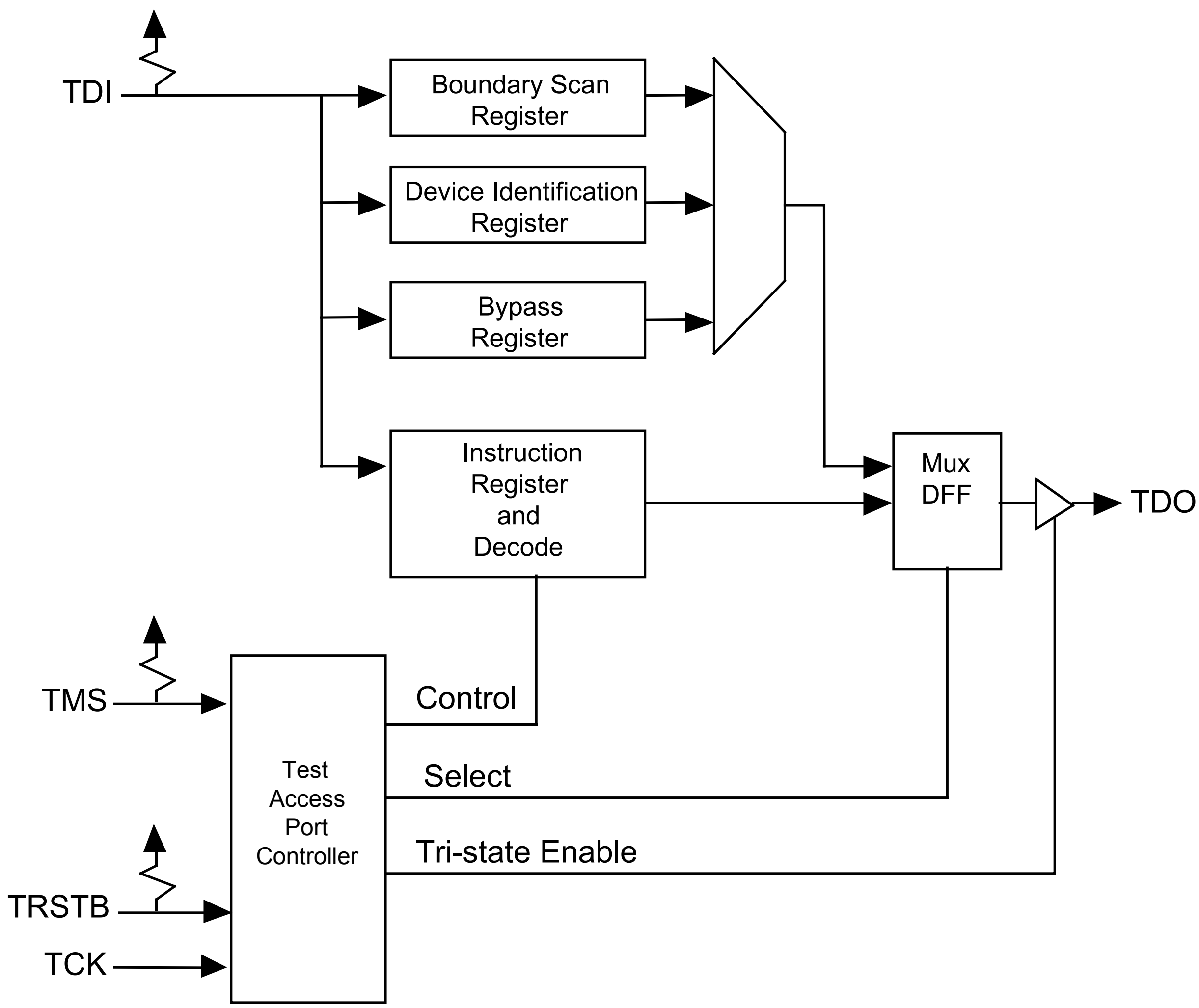
Figure 19 – Diagnostic Digital Loopback



12.8 JTAG Support

The OCTLIU supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on the TDI primary input and to output data on the TDO primary output. The TMS primary input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 20 – Boundary Scan Architecture



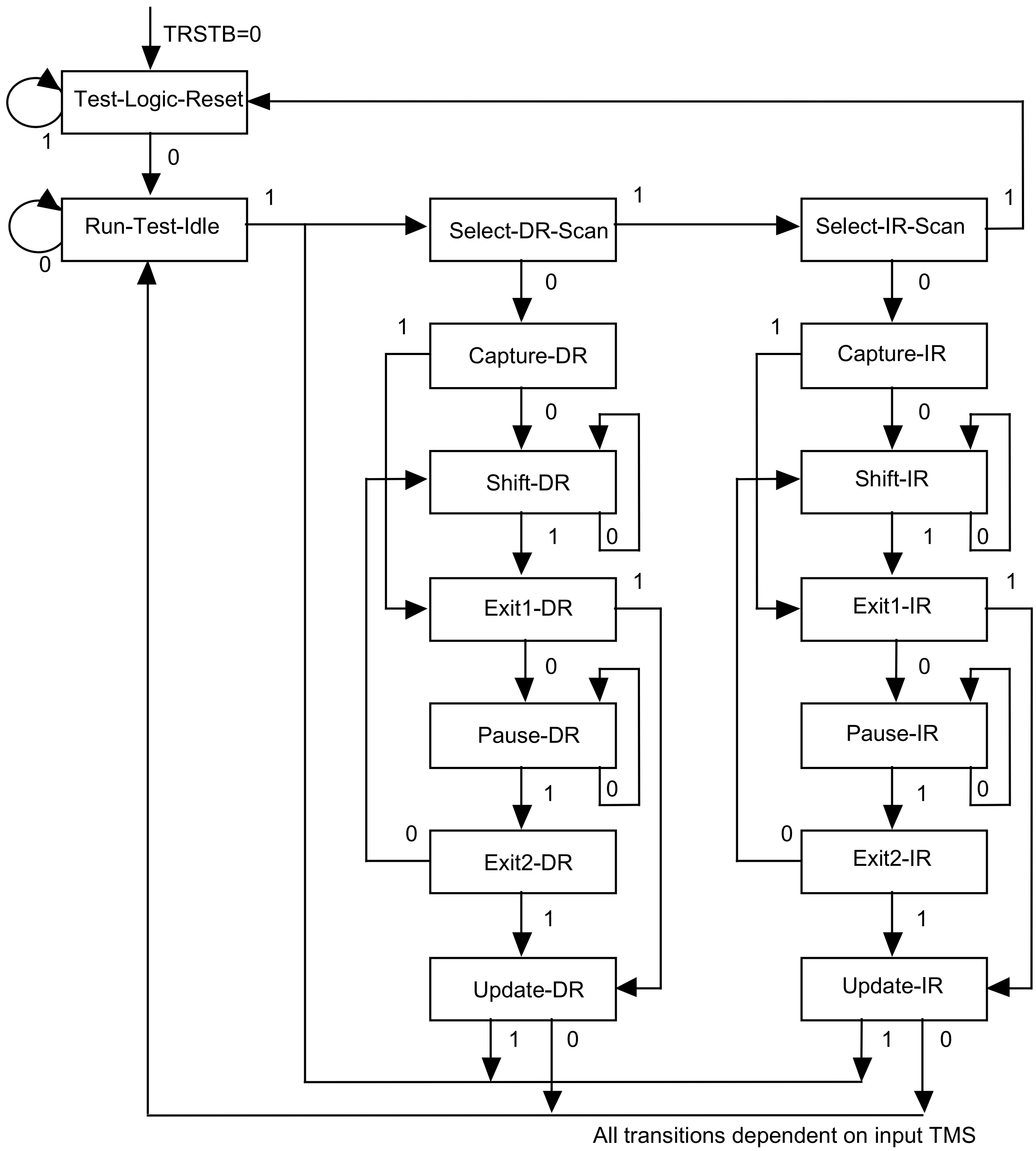
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI, and forced onto all digital outputs.

12.8.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 21 – TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run/test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register’s parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register’s parallel output latches are used to control the device’s outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out of the output, TDO, using the Shift-DR state.

Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table in the JTAG Test Port section 11.2.

Figure 22 – Input Observation Cell (IN_CELL)

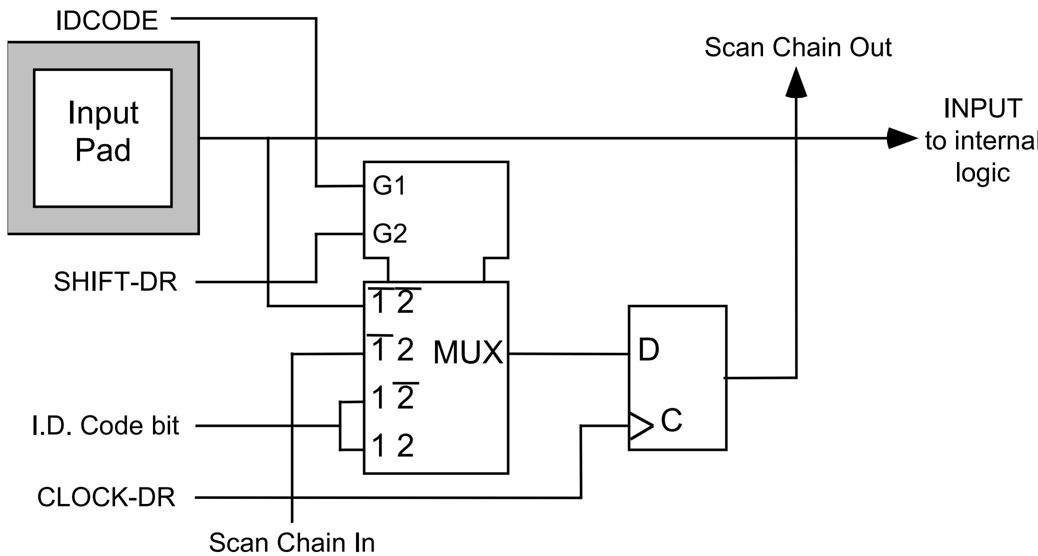


Figure 23 – Output Cell (OUT_CELL) or Enable Cell (ENABLE)

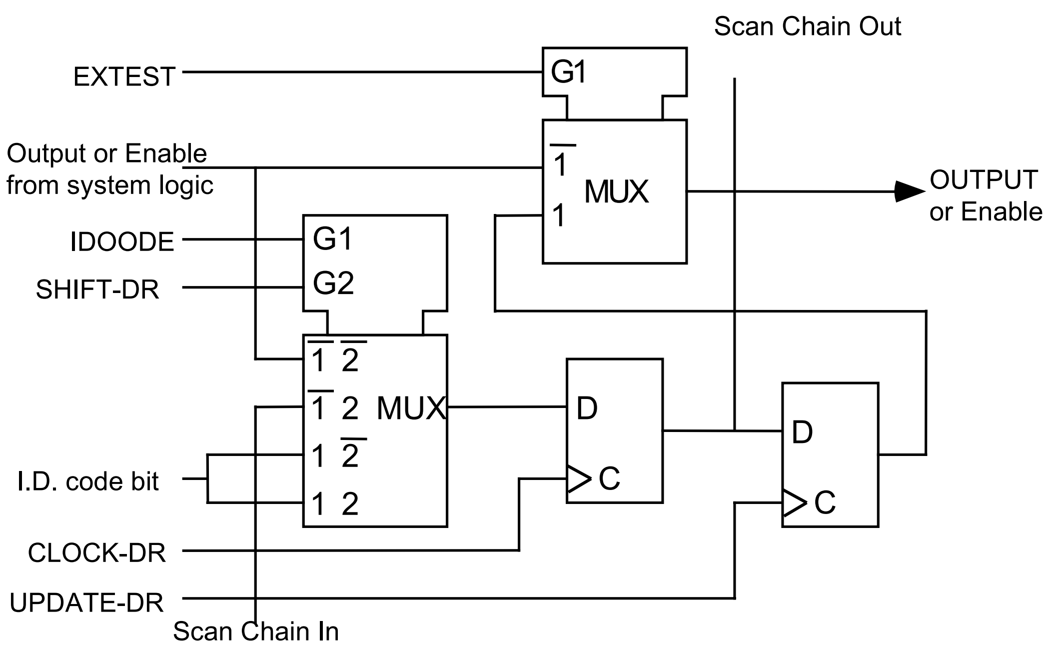


Figure 24 – Bidirectional Cell (IO_CELL)

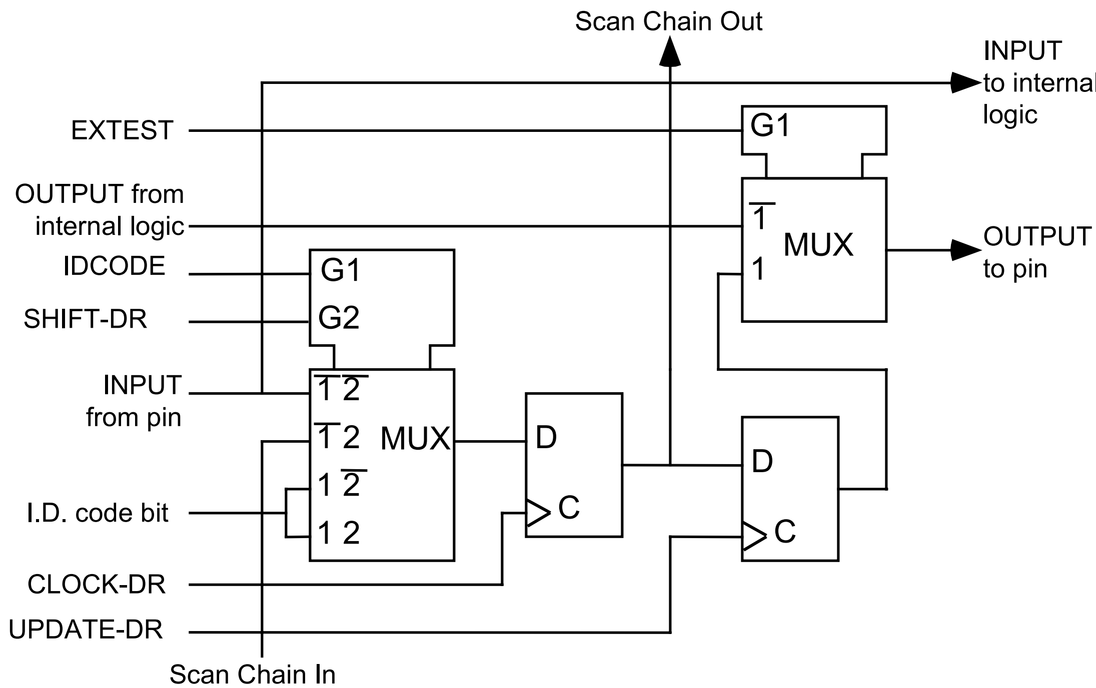
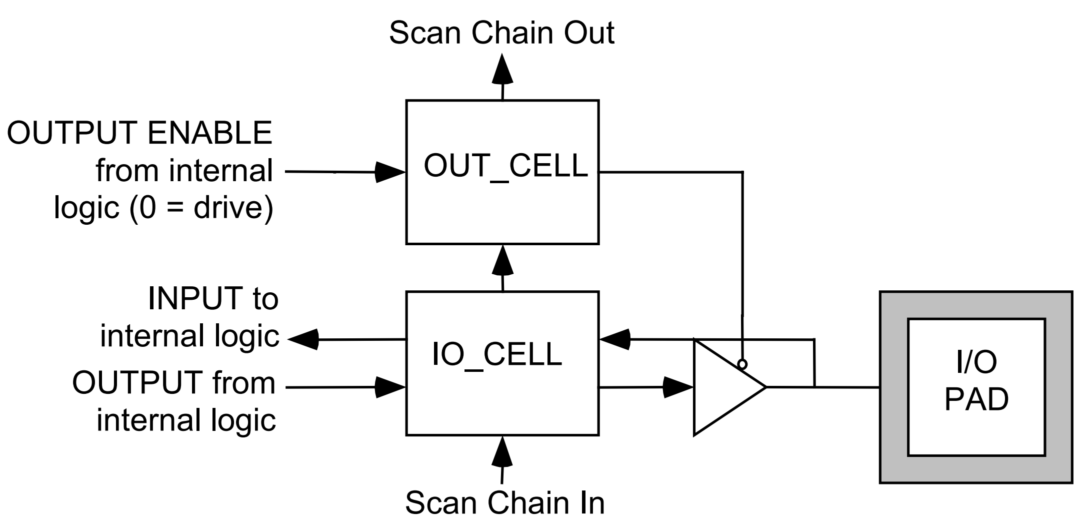


Figure 25 – Layout of Output Enable and Bidirectional Cells



13 FUNCTIONAL TIMING

13.1 SBI BUS Interface Timing

Figure 26 – SBI BUS Functional Timing

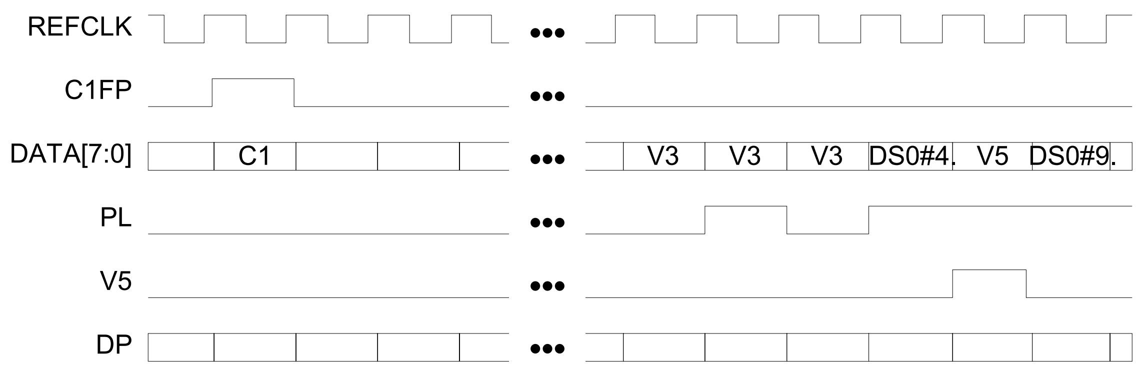
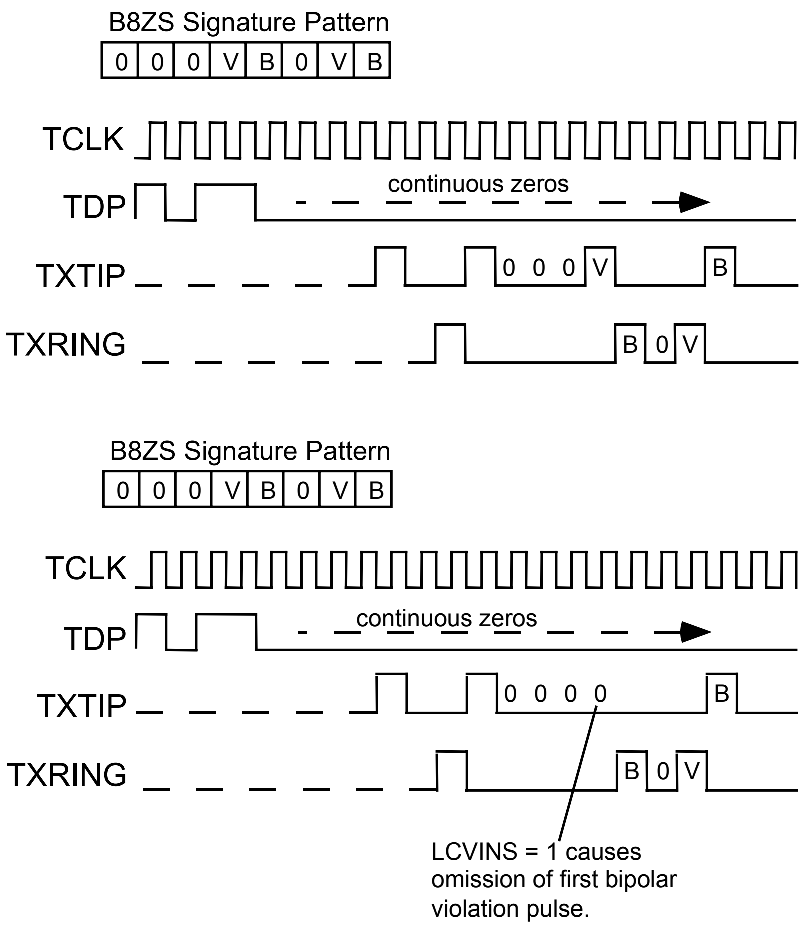


Figure 26 illustrates the operation of the SBI Bus, using a negative justification on the second to last V3 octet as an example. The justification is indicated by asserting PL high during the V3 octet. The timing diagram also shows the location of one of the tributaries by asserting V5 high during the V5 octet.

Note – the SBI ADD and DROP busses operate in an identical manner. Signal names on the ADD bus have an A prepended to the names shown in Figure 26 (e.g, AC1FP, ADATA[7:0], etc.) and those on the DROP bus have an D prepended to them (e.g, DC1FP, DDATA[7:0], etc.)

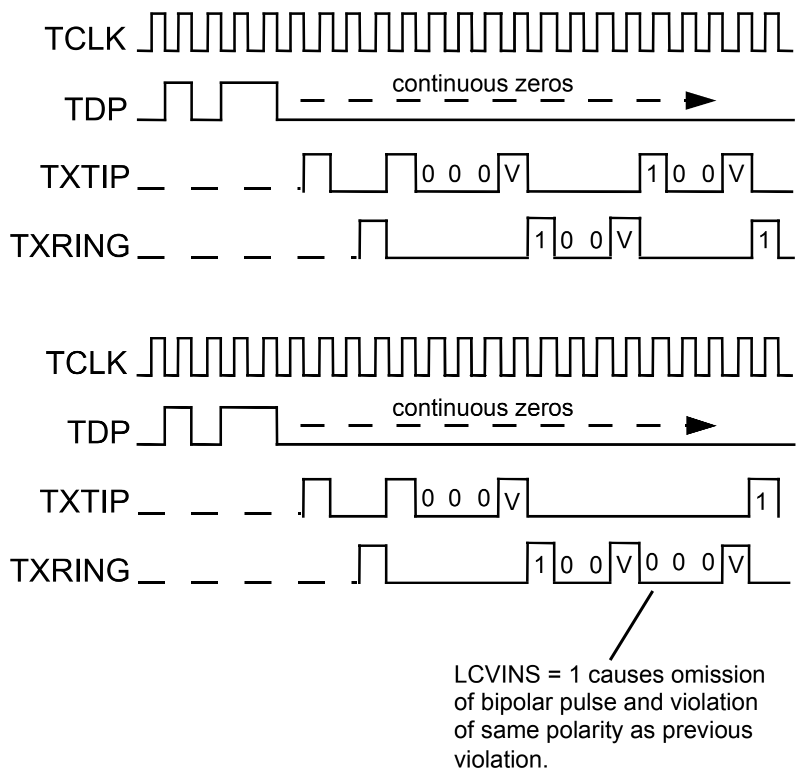
13.2 Line Code Violation Insertion

Figure 27 – B8ZS Line Code Violation Insertion



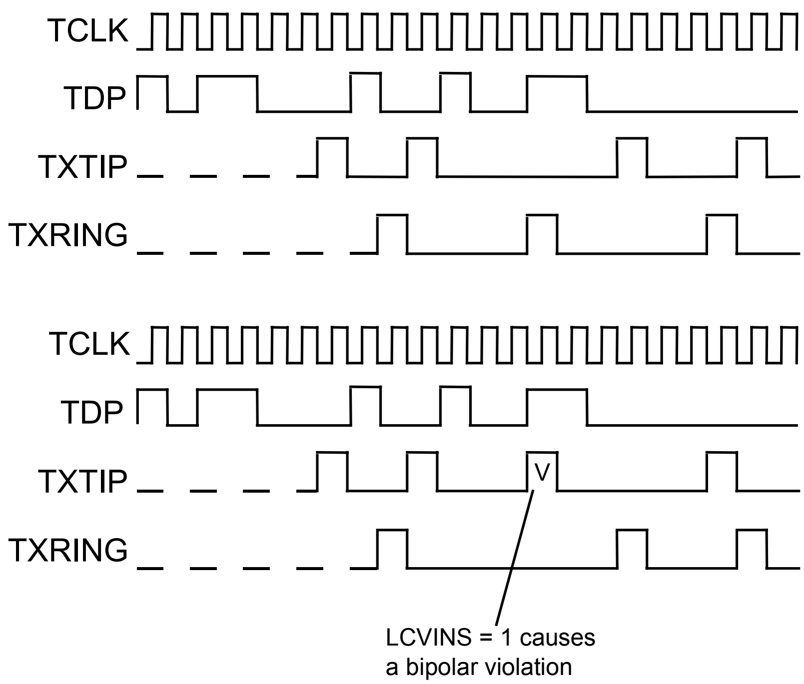
The effect of setting the LCVINS bit of the Line Interface Diagnostics register is shown in Figure 27. TXTIP[X] and TXRING[X] have been shown as square NRZ pulses for illustrative purposes. Setting LCVINS to a logic 1 generates one line code violation and 3 bit errors by causing the omission of the first line code violation pulse when a string of 8 consecutive zeros occurs in the unipolar data stream TDP. To generate another line code violation, the LCVINS bit must be reset to logic 0 and then set to logic 1 again.

Figure 28 – HDB3 Line Code Violation Insertion



The effect of setting the LCVINS bit of the Line Interface Diagnostics register is shown in Figure 28. TXTIP[X] and TXRING[X] have been shown as square NRZ pulses for illustrative purposes. Setting LCVINS to a logic 1 generates one line code violation by causing the omission of a bipolar pulse and hence a bipolar violation pulse of the same polarity as the previous bipolar violation pulse when a string of 4 consecutive zeros occurs in the unipolar data stream TDP. To generate another line code violation, the LCVINS bit must be reset to logic 0 and then set to logic 1 again.

Figure 29 – AMI Line Code Violation Insertion



The effect of setting the LCVINS bit of the Line Interface Diagnostics register is shown in Figure 29. TXTIP[X] and TXRING[X] have been shown as square NRZ pulses for illustrative purposes. Setting LCVINS to a logic 1 generates one line code violation by causing the next pulse to be of the same polarity as the previous pulse. Subsequent pulses will be of alternate polarity. To generate another line code violation, the LCVINS bit must be reset to logic 0 and then set to logic 1 again.

13.3 Alarm Interface

Figure 30 – LOS Alarm Serial Output

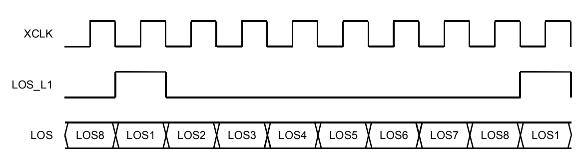


Figure 30 shows the operation of the Alarm Interface. The LOS status of the 8 LIU octants is output continuously in a serial format with a marker signal LOS_L1 to indicate the presence of the LOS status for LIU #1.

14 ABSOLUTE MAXIMUM RATINGS

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 43 – Absolute Maximum Ratings

Case Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage $V_{DDall33}$[1]	-0.3V to +4.6V
Supply Voltage V_{DD1V8}	-0.3V to +3.6V
Voltage on Any Pin	-0.3V to $V_{DDall33}$ + 0.3V
Static Discharge Voltage	±1000V
Latch-Up Current	±100mA
DC Input Current	±20mA
Lead Temperature	+230°C
Junction Temperature	+150°C

Not Withstanding the values in the above table 3.3V power supplies must always be at a voltage greater than or equal to the 1.8V power supplies.

[1] The OCTLIU 3.3 Volt digital and analogue power pins are collectively referred to as $V_{DDall33}$.

15 D.C. CHARACTERISTICS

T_A = -40°C to +85°C, $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5% (Typical Conditions: T_A = 25°C, $V_{DDall33}$ = 3.3V, V_{DD1V8} = 1.8V)

Table 44 – D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDD3V3, TAVD1, TAVD2, TAVD3, CAVD, RAVD1, RAVD2, QAVD	Power Supply	3.135	3.3	3.465	Volts	Note 5.
VDD1V8	Power Supply	1.71	1.8	1.89	Volts	Note 5.
VIL	Input Low Voltage			0.8	Volts	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage		0.1	0.4	Volts	VDD = min, IOL = -6mA for LOS, LOS_L1, TDO and Serial PROM interface outputs; -8mA for others. Notes 3, 5
VOH	Output or Bidirectional High Voltage	2.4	2.7		Volts	VDD = min, IOH = 6mA for LOS, LOS_L1, TDO and Serial PROM interface outputs; 8mA for others. Notes 3,5
VT+	Reset Input High Voltage	2.0	1.6		Volts	Applies to TTL Schmidt-triggered inputs (RSTB, TRSTB) only. Note 5.
VT-	Reset Input Low Voltage		1.1	0.8	Volts	Applies to TTL Schmidt-triggered inputs (RSTB, TRSTB) only. Note 5.
VTH	Reset Input Hysteresis Voltage		0.5		Volts	Applies to TTL Schmidt-triggered inputs (RSTB, TRSTB) only. Note 5.
IILPU	Input Low Current	+20	+83	+200	µA	VIL = GND. Notes 1, 3, 5
IIHPU	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 1, 3, 5
IILPD	Input Low Current	-10	0	+10	µA	VIL = GND. Notes 4, 3, 5
IIHPD	Input High Current	-200	-83	-20	µA	VIH = VDD. Notes 4, 3, 5
IIL	Input Low Current	-10	0	+10	µA	VIL = GND. Notes 2, 3, 5
IIH	Input High Current	-10	0	+10	µA	VIH = VDD. Notes 2, 3, 5
CIN	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF. Note 5.
COUT	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF. Note 5.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
CIO	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF. Note 5.
IDDOP 3V3	3.3V Operating Current			400	mA	Digital output pads loaded wih max capacitance. Transmission of pattern containing 50% ones.
IDDOP 1V8	1.8V Operating Current			150	mA	

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up or pull-down resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Input pin or bi-directional pin with internal pull-down resistor.
5. Typical values are given as a design aid. This product is not tested to the typical values given in the datasheet.

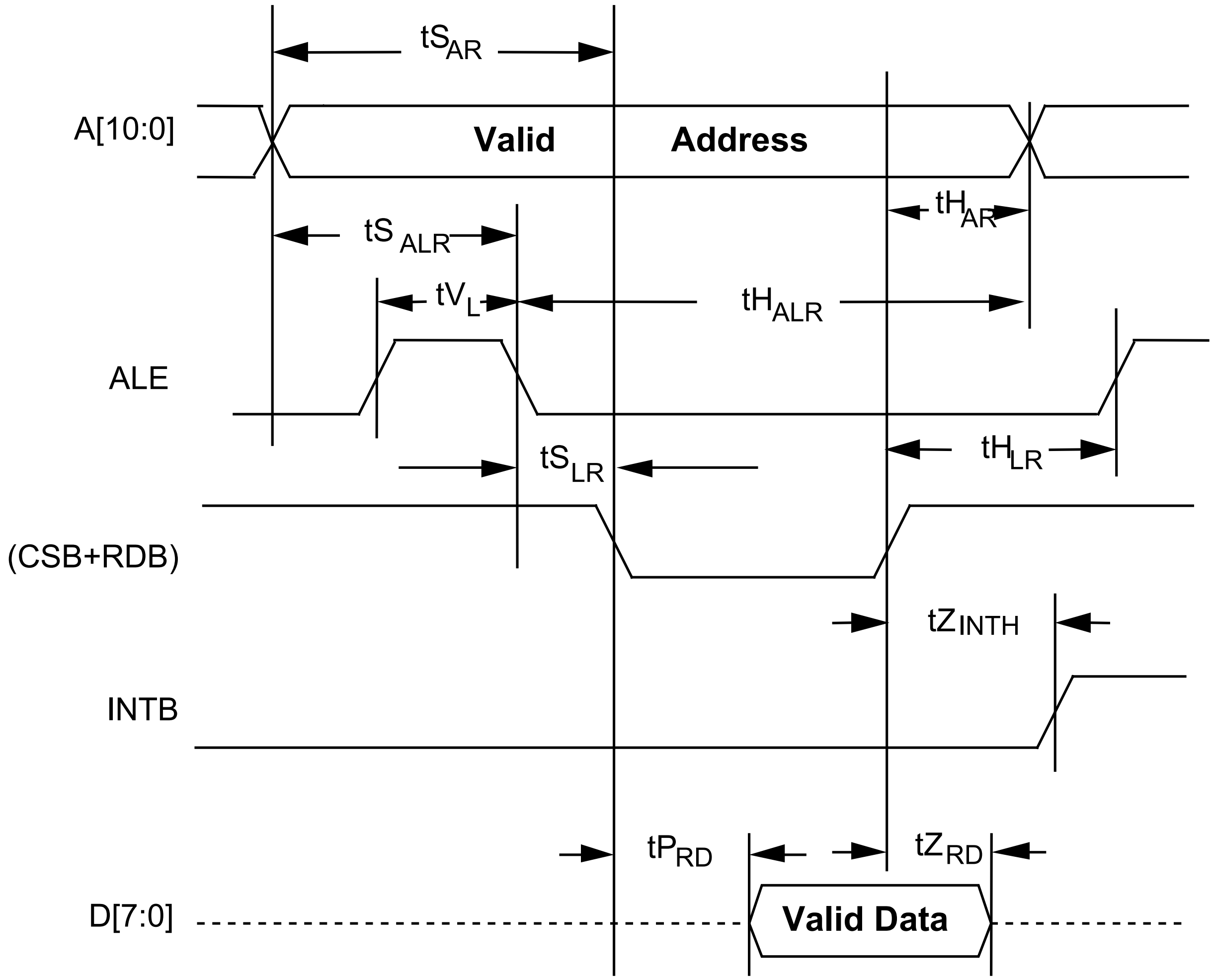
16 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 45 – Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	10		ns
tHAR	Address to Valid Read Hold Time	5		ns
tSALR	Address to Latch Set-up Time	10		ns
tHALR	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns
tSLR	Latch to Read Set-up	0		ns
tHLR	Latch to Read Hold	5		ns
tPRD	Valid Read to Valid Data Propagation Delay		70	ns
tZRD	Valid Read Negated to Output Tri-state		20	ns
tZINTH	Valid Read Negated to Output Tri-state		50	ns

Figure 31 – Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

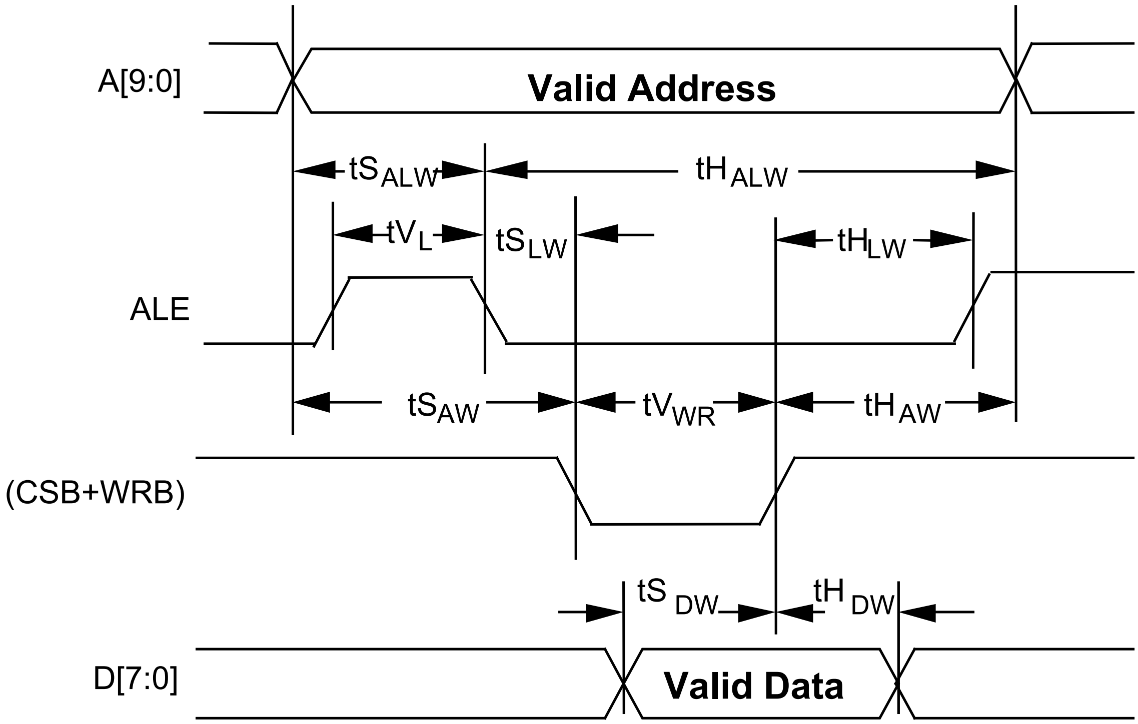
1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable.
5. Parameter tHAR is not applicable if address latching is used.

6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 46 – Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	10		ns
tSDW	Data to Valid Write Set-up Time	20		ns
tSALW	Address to Latch Set-up Time	10		ns
tHALW	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	5		ns
tSLW	Latch to Write Set-up	0		ns
tHLW	Latch to Write Hold	5		ns
tHDW	Data to Valid Write Hold Time	5		ns
tHAW	Address to Valid Write Hold Time	5		ns
TVWR	Valid Write Pulse Width	40		ns

Figure 32 – Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, tSLW and tHLW are not applicable.
3. Parameter tHAW is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

17 OCTLIU TIMING CHARACTERISTICS

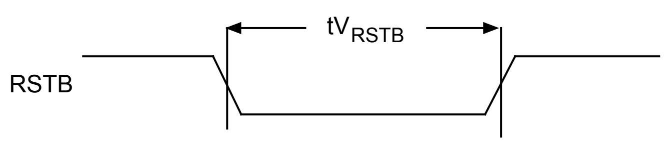
17.1 RSTB Timing (Figure 33)

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 47 – RTSB Timing

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 33 – RSTB Timing

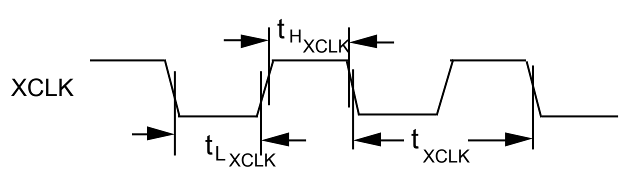


17.2 XCLK Input Timing (Figure 34)

Table 48 – XCLK Input Timing

Symbol	Description	Min	Max	Units
t_{XCLK}	XCLK Frequency (1.544 MHz or 2.048 MHz ± 100ppm)	1.544 – 100ppm	2.048 +100ppm	MHz
tL_{XCLK}	XCLK Low Pulse Width (Note 1)	160		ns
tH_{XCLK}	XCLK High Pulse Width (Note 1)	160		ns

Figure 34 – XCLK Input Timing



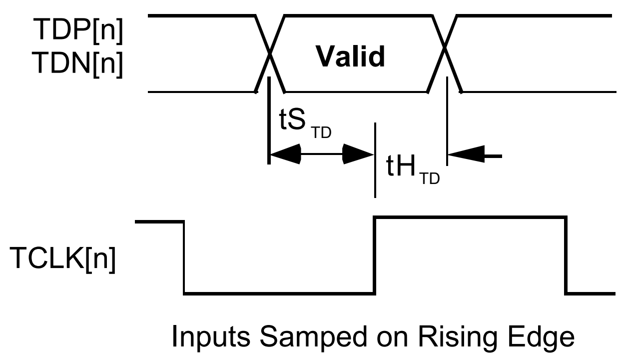
17.3 Transmit Serial Interface (Figure 35)

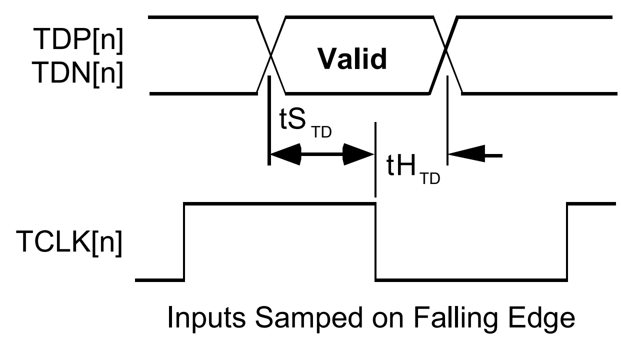
(T_A = -40°C to +85°C, $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 49 – Transmit Serial Interface

Symbol	Description	Min	Max	Units
	TCLK[8:1] Frequency (1.544MHz ±200ppm or 2.048MHz ±200 ppm)	1.544 – 200ppm	2.048 +200ppm	MHz
	TCLK[8:1] Jitter	-50	50	ns
	TCLK[8:1] Duty Cycle	35	65	%
tS_{TD}	TDP[n], TDN[n] to TCLK[n] Set-up Time	20		ns
tH_{TD}	TDP[n], TDN[n] to TCLK[n] Hold Time	20		ns

Figure 35 – Transmit Serial Interface Timing Diagram





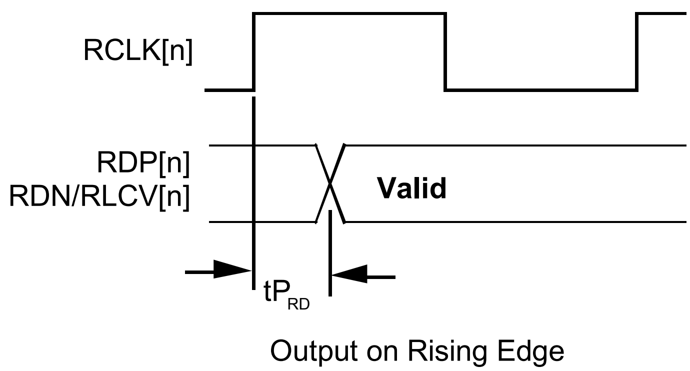
17.4 Receive Serial Interface (Figure 36)

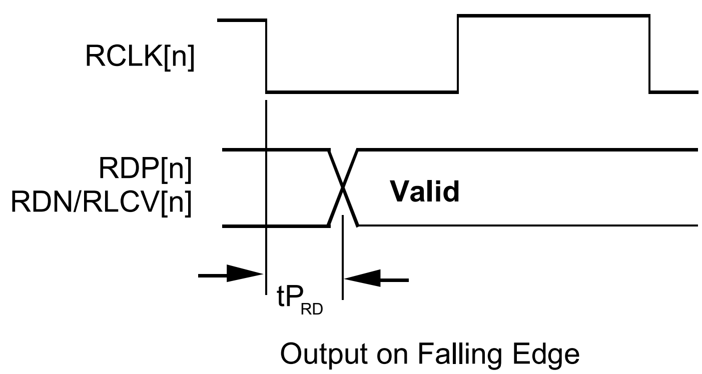
(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 50 – Receive Serial Interface

Symbol	Description	Min	Max	Units
tP_{RD}	RCLK[n] to RDP[n], RDN/RLCV[n] Propagation Delay	-20	50	ns

Figure 36 – Receive Serial Interface Timing Diagram





17.5 SBI Interface (Figure 37 to Figure 39)

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 51 – Clocks and SBI Frame Pulse

Symbol	Description	Min	Max	Units
	REFCLK Frequency	19.44 – 50ppm	19.44 +50ppm	MHz
	REFCLK Duty Cycle	40	60	%
TS_{C1FP}	AC1FP, DC1FP Set-Up Time to REFCLK	4		ns
TH_{C1FP}	AC1FP, DC1FP Hold Time to REFCLK	0		ns
$TP_{C1FPOUT}$	REFCLK to C1FPOUT Valid	1	20	ns

Figure 37 – SBI Frame Pulse Timing

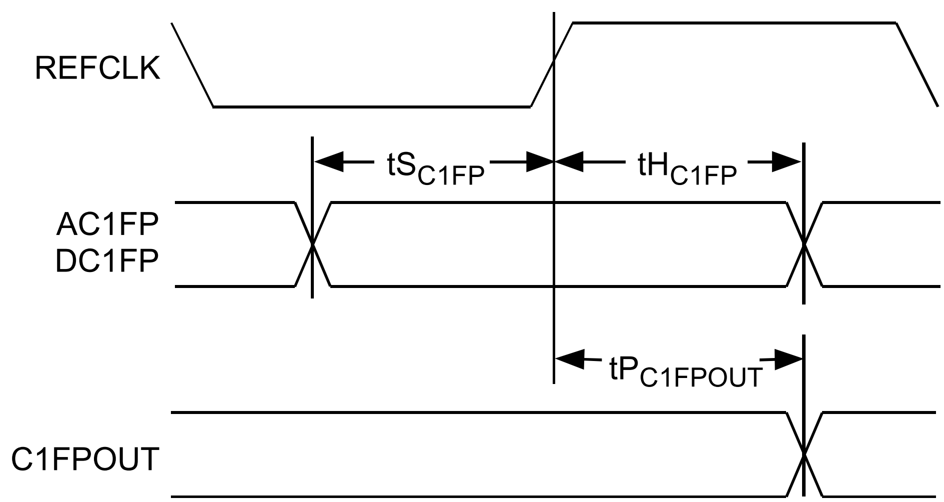


Table 52 – SBI ADD BUS

Symbol	Description	Min	Max	Units
$t_{S_{SBIADD}}$	All SBI ADD BUS Inputs Set-Up Time to REFCLK	4		ns
$t_{H_{SBIADD}}$	All SBI ADD BUS Inputs Hold Time to REFCLK	0		ns

Figure 38 – SBI ADD BUS Timing

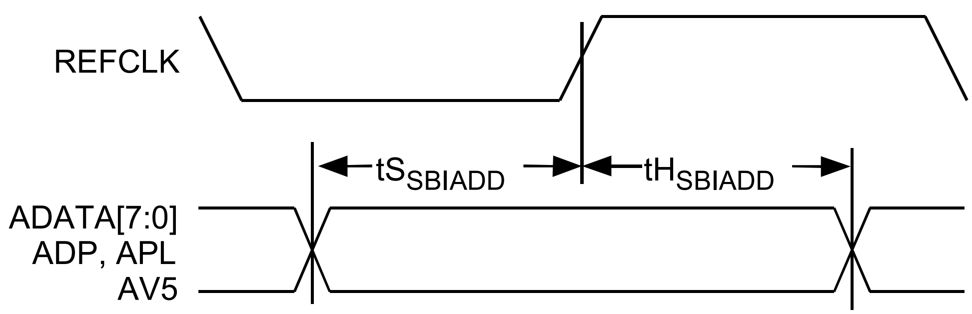
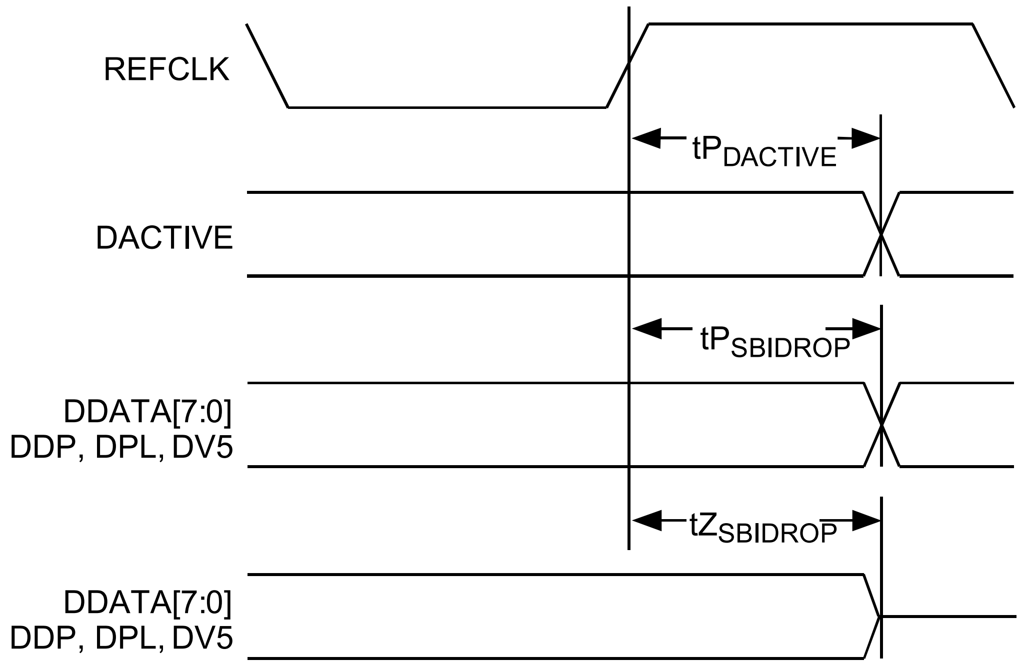


Table 53 – SBI DROP BUS

Symbol	Description	Min	Max	Units
$t_{P_{DACTIVE}}$	REFCLK to DACTIVE Valid	2	15	ns
$t_{P_{SBIDROP}}$	REFCLK to All SBI DROP BUS Outputs (except DACTIVE) Valid	2	20	ns
$t_{Z_{SBIDROP}}$	REFCLK to All SBI DROP BUS Outputs (except DACTIVE) Tristate	2	20	ns

Figure 39 – SBI DROP BUS Timing



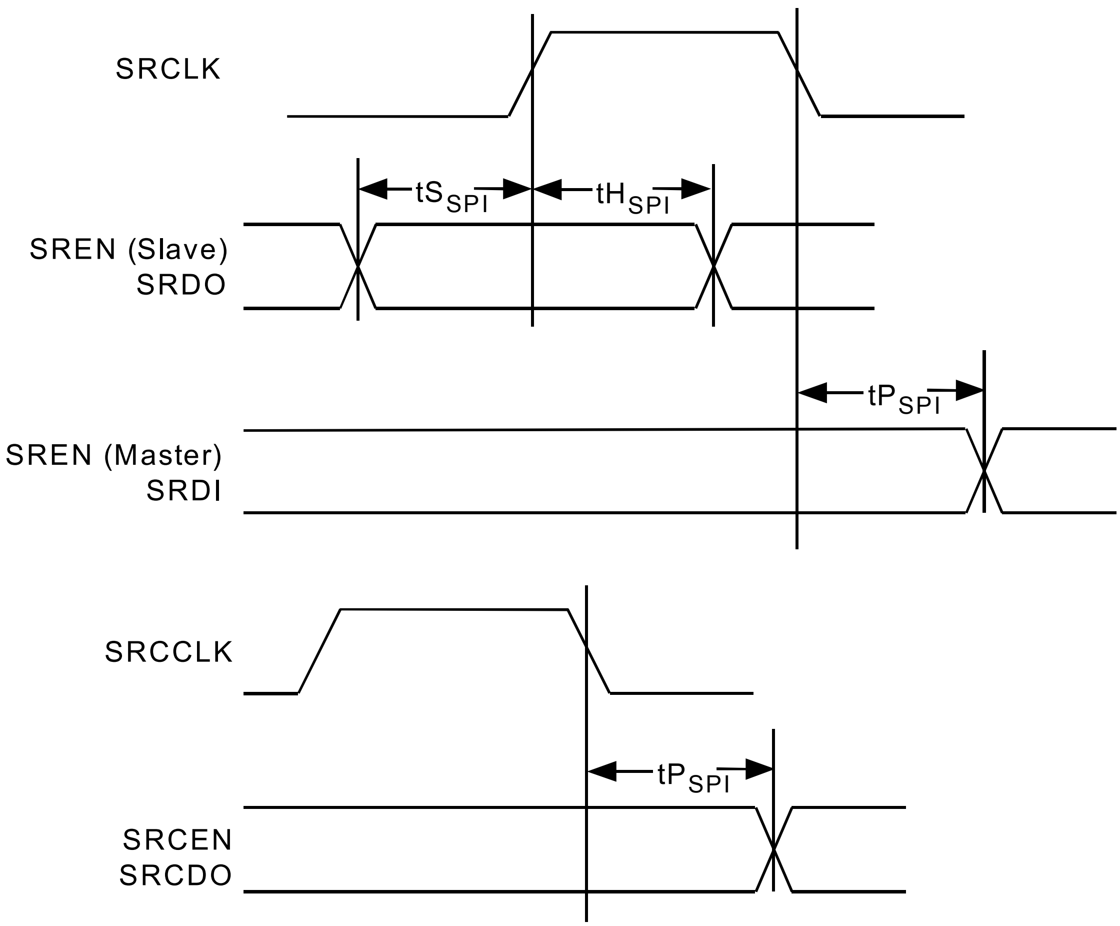
17.6 Serial PROM (SPI) Interface (Figure 40)

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 54 – SPI Interface

Symbol	Description	Min	Max	Units
	SRCLK Frequency	XCLK frequency ÷ 4		
	SRCCLK Frequency	XCLK frequency ÷ 4		
TS_{SPI}	SPI Input Set-Up Time to SRCLK, SRRCLK	50		ns
TH_{SPI}	SPI Input Set-Up Time to SRCLK, SRRCLK	50		ns
TP_{SPI}	SRCLK, SRRCLK to SPI Output Prop. Time	-50	50	ns

Figure 40 – SPI Interface Timing



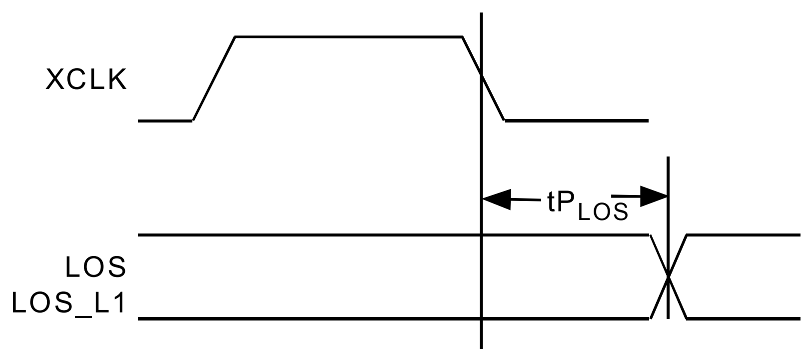
17.7 Alarm Interface (Figure 41)

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 55 – Alarm Interface

Symbol	Description	Min	Max	Units
T_{PLOS}	XCLK to LOS, LOS_L1 Output Prop. Time	-50	50	ns

Figure 41 – Alarm Interface Timing

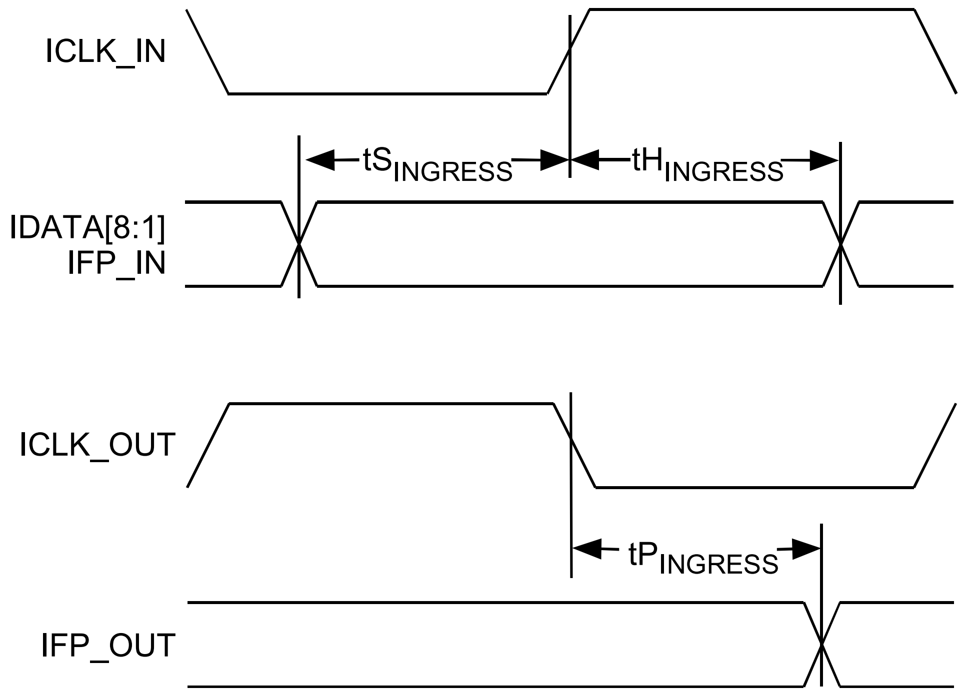


17.8 Ingress Clk/Data Interface (Figure 42)

Table 56 – Ingress Clk/Data Interface

Symbol	Description	Min	Max	Units
	ICLK_IN Frequency (1.544MHz ±200ppm or 2.048MHz ±200 ppm)	1.544 – 200ppm	2.048 +200ppm	MHz
	ICLK_IN Duty Cycle	35	65	%
$tS_{INGRESS}$	IDATA[8:1], IFP_IN Set-up Time	20		ns
$tH_{INGRESS}$	IDATA[8:1], IFP_IN Hold Time	20		ns
$tP_{INGRESS}$	ICLK_OUT to IFP_OUT Propagation Delay	-20	50	ns

Figure 42 – Ingress Clk/Data Interface Timing Diagram

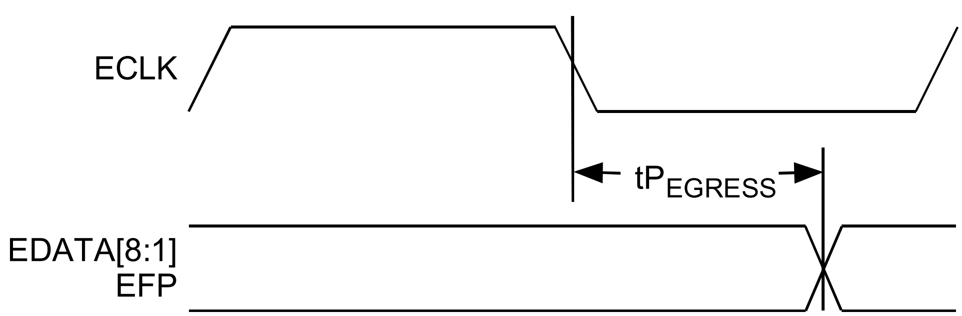


17.9 Egress Clk/Data Interface (Figure 43)

Table 57 – Engress Clk/Data Interface

Symbol	Description	Min	Max	Units
tP_{EGRESS}	ECLK to EDATA[8:1], EFP Propagation Delay	-20	50	ns

Figure 43 – Egress Clk/Data Interface Timing Diagram



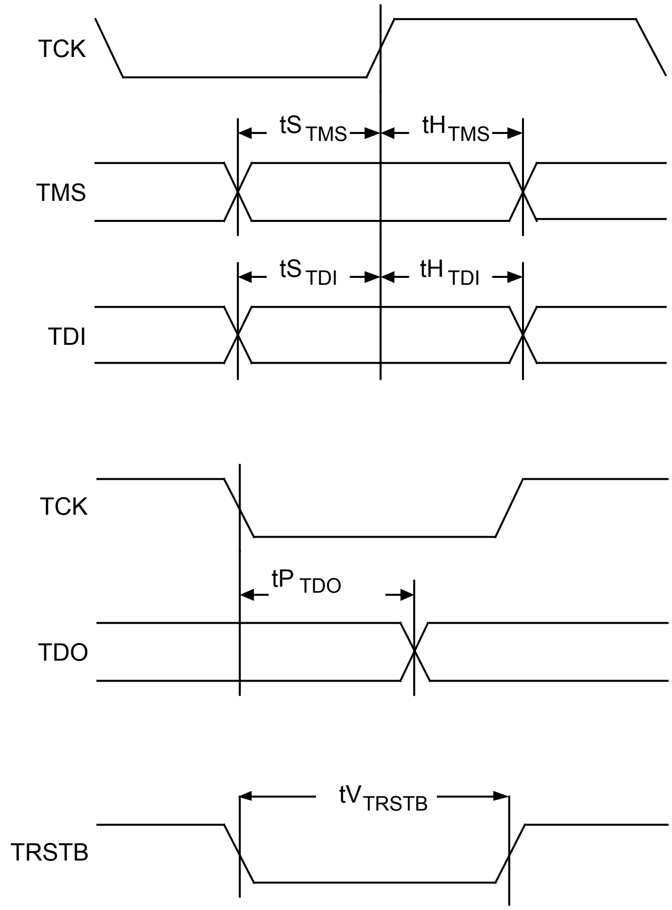
17.10 JTAG Port Interface (Figure 44)

(T_A = -40°C to +85°C $V_{DDall33}$ = 3.3V ±5%, V_{DD1V8} = 1.8V ±5%)

Table 58 – JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	50		ns
tH_{TMS}	TMS Hold time to TCK	50		ns
tS_{TDI}	TDI Set-up time to TCK	50		ns
tH_{TDI}	TDI Hold time to TCK	50		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

Figure 44 – JTAG Port Interface Timing



Notes on OCTLIU Timing:

1. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

2. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

3. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

4. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

5. Maximum output propagation delays are measured with a 100 pF load on the SBI DROP Bus outputs (except DACTIVE) and a 50 pF load on DACTIVE and all other outputs. Minimum output propagation delays are measured with a 0 pF load on the outputs.

18 ORDERING AND THERMAL INFORMATION

Table 59 – Ordering Information

Part No.	Description
PM4318-BI	288-pin Tape Super Ball Grid Array (TSBGA)

Table 60 – OCTLIU Theta Jc

PART NO.	CASE TEMPERATURE	Theta Jc
PM4318-BI	-40°C to +85°C	1.0 °C/W

Table 61 – OCTLIU Junction Temperature

PM4318-BI	Maximum Junction Temperature for Long Term Reliability	110 °C

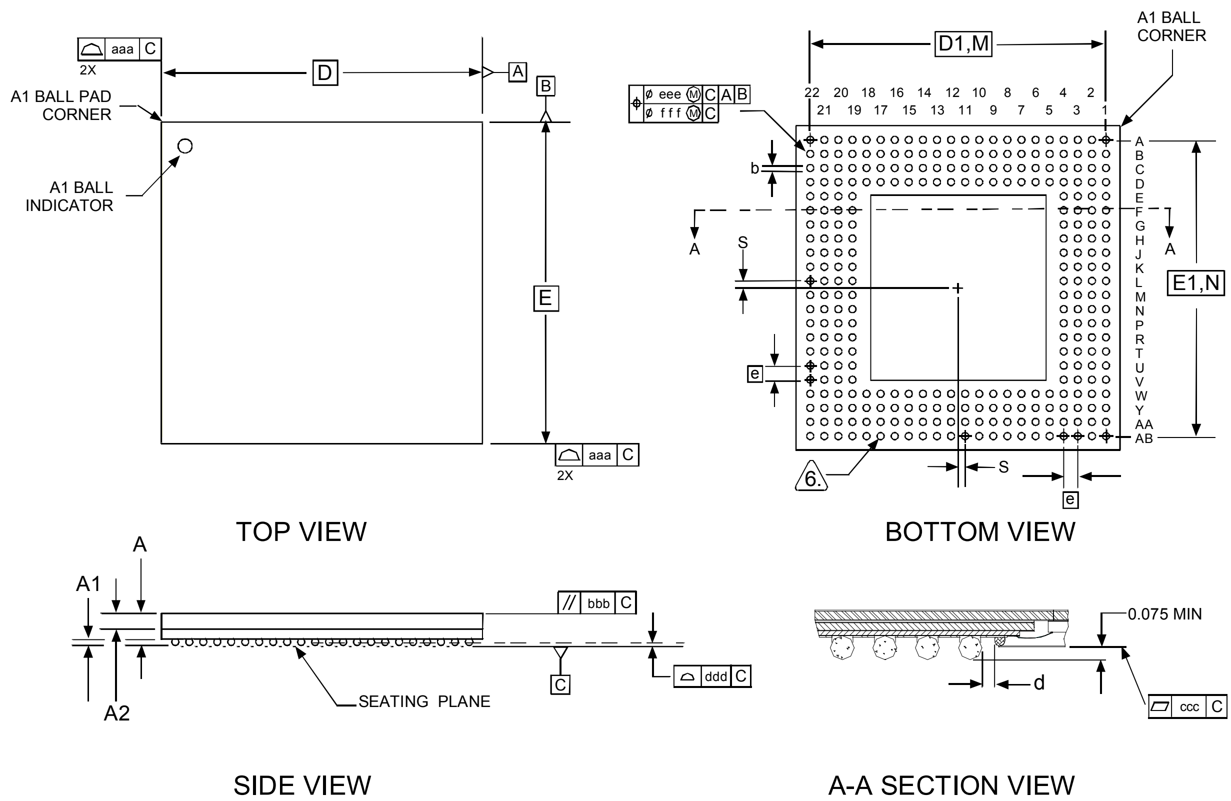
Table 62 – OCTLIU Theta Ja vs. Airflow

				Forced Air (Linear Feet per Minute)				
Part No.	Case Temperature	Theta J-A at 2.5 Watts	Conv	100	200	300	400	500
PM4318-BI	-40°C to 85°C	Dense Board[1]	32.8	30.1	28.3	27.2	26.7	26.5
		JEDEC Board[2]	13.7	12.0	10.8	10.0	9.4	9.0

1. – Dense Board is defined as a 3S3P board and consists of a 3x3 array of PM4318-BI devices located as close to each other as board design rules allow. All PM4318-BI devices are assumed to be dissipating maximum power. Theta J-A listed is for the device in the middle of the array.

2. – JEDEC Board Theta J-A is the measured value for a single thermal device in the same package on a 2S2P board following EIA/JESD 51-3.

19 MECHANICAL INFORMATION



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.
6) DIAMETER OF SOLDER MASK OPENING IS 0.550 MM (SMD).

PACKAGE TYPE : 288 TAPE SUPER BALL GRID ARRAY - TSBGA																	
BODY SIZE : 23 x 23 x 1.60 MM																	
Dim.	**A**	**A_1**	**A_2**	**D**	**D_1**	**E**	**E_1**	**M,N**	**b**	**e**	**aaa**	**bbb**	**ccc**	**ddd**	**eee**	**f f f**	**S**
Min.	-	0.40	0.80	-	-	-	-	-	0.50	-	-	-	-	-	-	-	-
Nom.	-	0.50	0.91	23.00 BSC	21.00 BSC	23.00 BSC	21.43 BSC	22x22	0.65	1.00 BSC	-	-	-	-	-	-	-
Max.	1.60	0.60	1.00	-	-	-	-	-	0.80	-	0.20	0.25	0.20	0.20	0.30	0.10	0.50

NOTES

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