# P4C116
# ULTRA HIGH SPEED 2K x 8
# STATIC CMOS RAMS

## FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15/20/25/35 ns (Commercial)**
  - **– 15/20/25/35 ns (Military)**
- **Low Power Operation**
  - **– 633/715 mW Active — 15, 20**
  - **– 550/633 mW Active — 25, 35**
  - **– 193/220 mW Standby (TTL Input)**
- **Output Enable Control Function**
- **Single 5V±10% Power Supply**
- **Common Data I/O**
- **Fully TTL Compatible Inputs and Outputs**
- **Produced with PACE II Technology™**
- **Standard Pinout (JEDEC Approved)**
  - **– 24-Pin 300 mil DIP, SOIC, SOJ**
  - **– 24-Pin Rectangular LCC (300 x 400 mils)**
  - **– 28-Pin Square LCC (450 x 450 mils)**

## DESCRIPTION

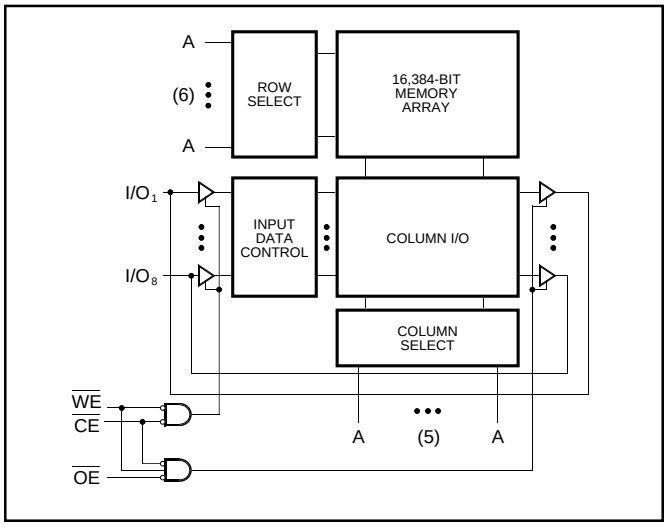
The P4C116 is a 16,384-bit ultra high-speed static RAMs organized as 2K x 8. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V±10% tolerance power supply. Current drain is typically 10 µA from a 2.0V supply.

Access times as fast as 10 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption to a low 633 mW active, 193 mW standby.

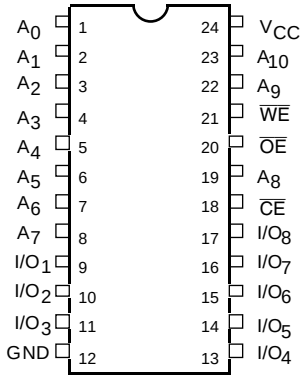
The P4C116 is available in 24-pin 300 mil DIP, SOJ and SOIC packages providing excellent board level densities.

The P4C116 is also available in 24-pin rectangular and 28-pin square LCC packages.

## FUNCTIONAL BLOCK DIAGRAM




## PIN CONFIGURATIONS




DIP (P4, D4), SOJ (J4), SOIC (S4)
TOP VIEW

See Selection Guide Page for LCC

## MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Pin with Respect to GND | –0.5 to +7 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | –55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

## RECOMMENDED OPERATING CONDITIONS

| Grade[2] | Ambient Temp | Gnd | Vcc |
|---|---|---|---|
| Commercial | 0°C to 70°C | 0V | 5.0V ±10% |

## CAPACITANCES[4]

($V_{CC}$ = 5.0V, $T_A$ = 25°C, f = 1.0MHz)

| Symbol | Parameter | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$= 0V | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

| Symbol | Parameter | Test Conditions | P4C116 | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{IH}$ | Input High Voltage | | 2.2 | $V_{CC}$ +0.5 | V |
| $V_{IL}$ | Input Low Voltage | | –0.5[3] | 0.8 | V |
| $V_{HC}$ | CMOS Input High Voltage | | $V_{CC}$–0.2 | $V_{CC}$+0.5 | V |
| $V_{LC}$ | CMOS Input Low Voltage | | –0.5[3] | 0.2 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18 mA | | –1.2 | V |
| $V_{OL}$ | Output Low Voltage (TTL Load) | $I_{OL}$ = +8 mA, $V_{CC}$ = Min. | | 0.4 | V |
| $V_{OH}$ | Output High Voltage (TTL Load) | $I_{OH}$ = –4 mA, $V_{CC}$ = Min. | 2.4 | | V |
| $I_{LI}$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | –5 | +5 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | –5 | +5 | µA |
| $I_{CC}$ | Dynamic Operating Current – 10, 12 | $V_{CC}$ = Max., f = Max., Outputs Open | | 130 | mA |
| $I_{CC}$ | Dynamic Operating Current – 15, 20 | $V_{CC}$ = Max., f = Max., Outputs Open | — | 115 | mA |
| $I_{CC}$ | Dynamic Operating Current – 25, 35 | $V_{CC}$ = Max., f = Max., Outputs Open | — | 100 | mA |
| $I_{SB}$ | Standby Power Supply Current (TTL Input Levels) | $\overline{CE}$ ≥$V_{IH}$, $V_{CC}$ = Max., f = Max., Outputs Open | — | 35 | mA |
| $I_{SBI}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE}$ ≥$V_{HC}$, $V_{CC}$ = Max., f = 0, Outputs Open $V_{IN}$ ≤$V_{LC}$ or $V_{IN}$ ≥ $V_{HC}$ | — | 17 | mA |

## POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Symbol | Parameter | Temperature Range | –10 | –12 | –15 | –20 | –25 | –35 | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current* | Commercial | 180 | 170 | 160 | 155 | 150 | 140 | mA |
| | | Military | N/A | N/A | 170 | 160 | 155 | 150 | mA |

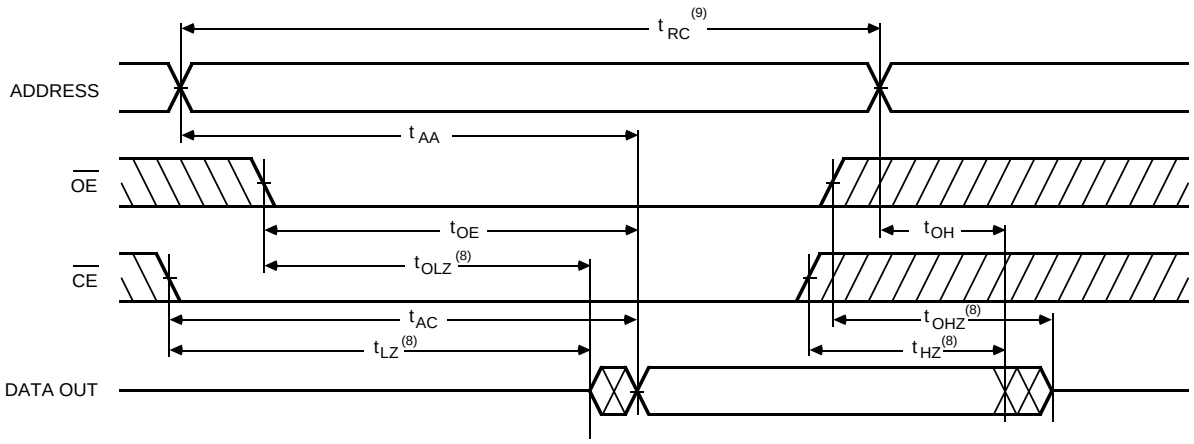
*$V_{CC}$ = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$.

## AC ELECTRICAL CHARACTERISTICS—READ CYCLE

($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | –10 | | –12 | | –15 | | –20 | | –25 | | –35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{AA}$ | Address Access Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{AC}$ | Chip Enable Access Time | | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{OH}$ | Output Hold from Address Change | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{LZ}$ | Chip Enable to Output in Low Z | 2 | | 2 | | 2 | | 2 | | 3 | | 3 | | ns |
| $t_{HZ}$ | Chip Disable to Output in High Z | | 5 | | 6 | | 7 | | 8 | | 10 | | 15 | ns |
| $t_{OE}$ | Output Enable Low to Data Valid | | 6 | | 8 | | 10 | | 10 | | 15 | | 20 | ns |
| $t_{OLZ}$ | Output Enable Low to Low Z | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OHZ}$ | Output Enable High to High Z | | 6 | | 7 | | 8 | | 9 | | 12 | | 15 | ns |
| $t_{PU}$ | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | Chip Disable to Power Down | | 10 | | 12 | | 15 | | 20 | | 20 | | 25 | ns |

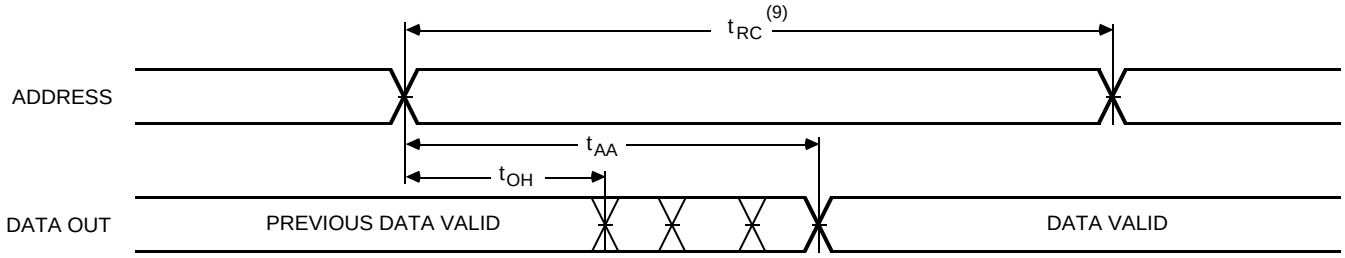
## TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[5]



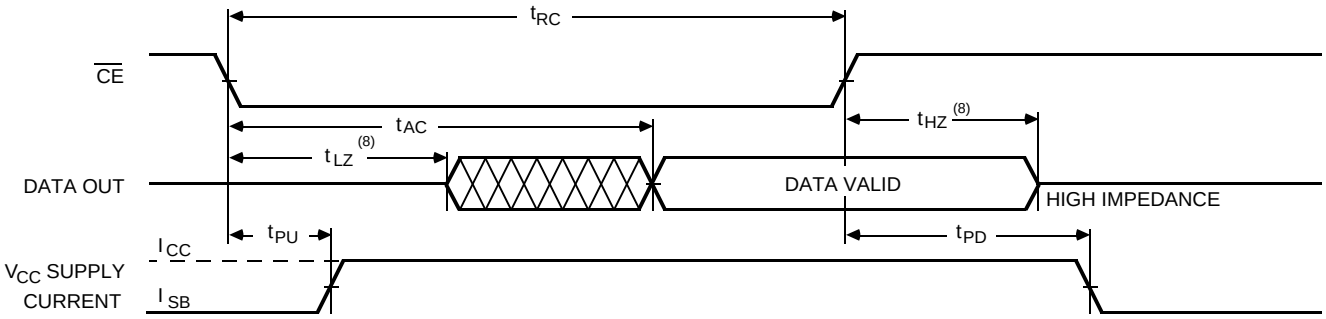

**Notes:**

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with $V_{IL}$ and $I_{IL}$ not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$ is LOW and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ transition LOW.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

## TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)[5,6]




## TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)[5,7]

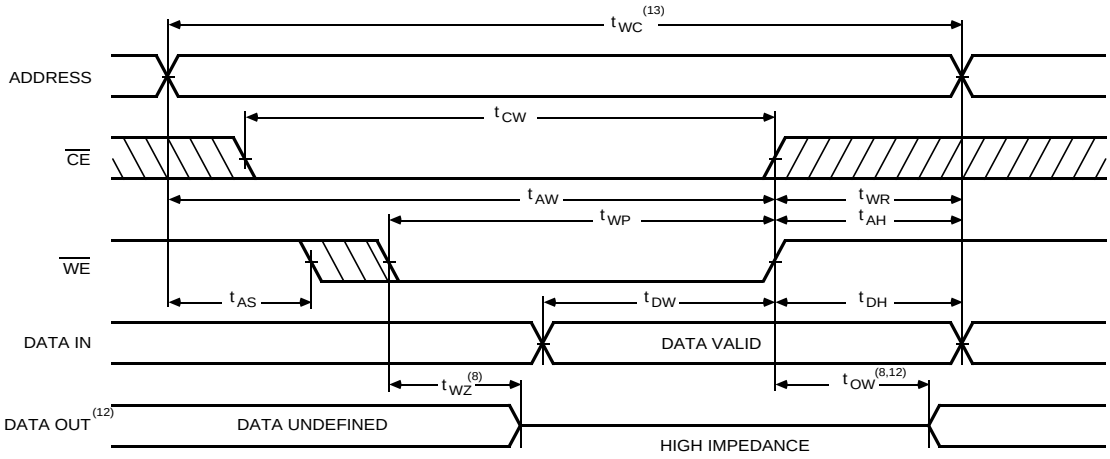


## AC CHARACTERISTICS—WRITE CYCLE

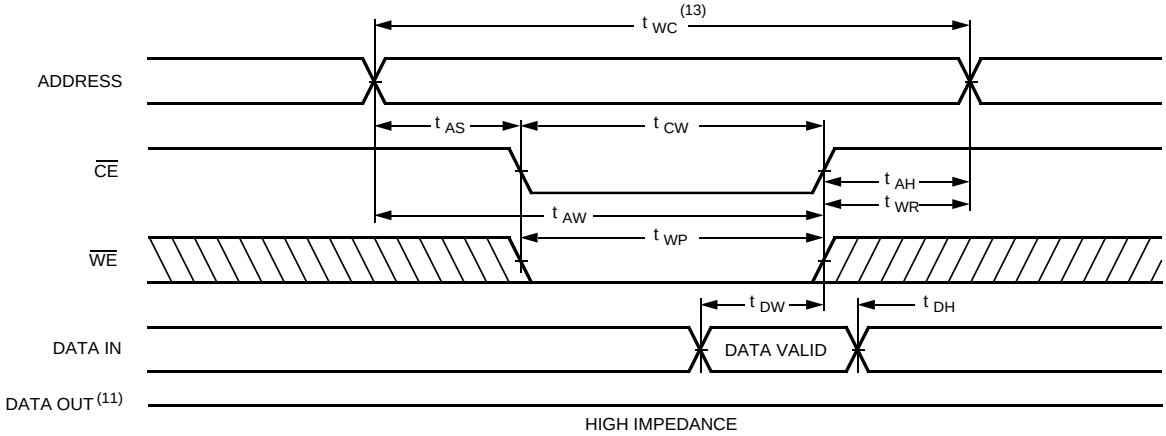
($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | –10 | | –12 | | –15 | | –20 | | –25 | | –35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | Write Cycle Time | 10 | | 12 | | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{CW}$ | Chip Enable Time to End of Write | 8 | | 10 | | 12 | | 15 | | 18 | | 25 | | ns |
| $t_{AW}$ | Address Valid to End of Write | 8 | | 10 | | 12 | | 15 | | 18 | | 25 | | ns |
| $t_{AS}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 8 | | 10 | | 12 | | 15 | | 18 | | 20 | | ns |
| $t_{AH}$ | Address Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Data Valid to End of Write | 7 | | 8 | | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WZ}$ | Write Enable to Output in High Z | | 6 | | 7 | | 8 | | 10 | | 15 | | 15 | ns |
| $t_{OW}$ | Output Active from End of Write | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[10,11]




## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[10]




**Notes:**

10. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. $\overline{OE}$ is LOW for this WRITE cycle to show $t_{WZ}$ and $t_{OW}$.
12. If CE goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
13. Write Cycle Time is measured from the last valid address to the first transitioning address.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

## TRUTH TABLE

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O | Power |
|---|---|---|---|---|---|
| Standby | H | X | X | High Z | Standby |
| $D_{OUT}$ Disabled | L | H | H | High Z | Active |
| Read | L | L | H | $D_{OUT}$ | Active |
| Write | L | X | L | High Z | Active |

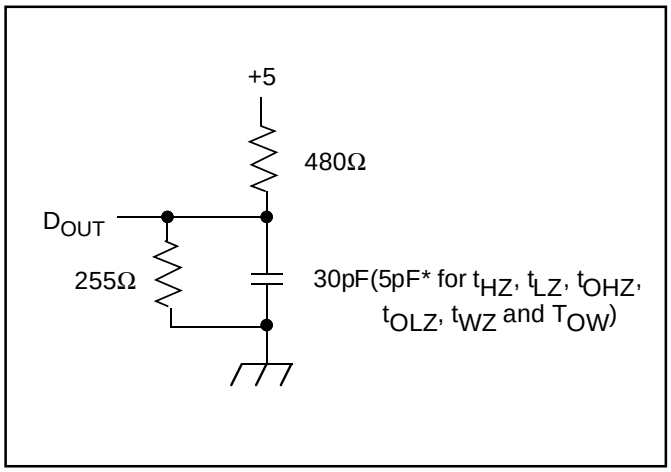



**Figure 1. Output Load**

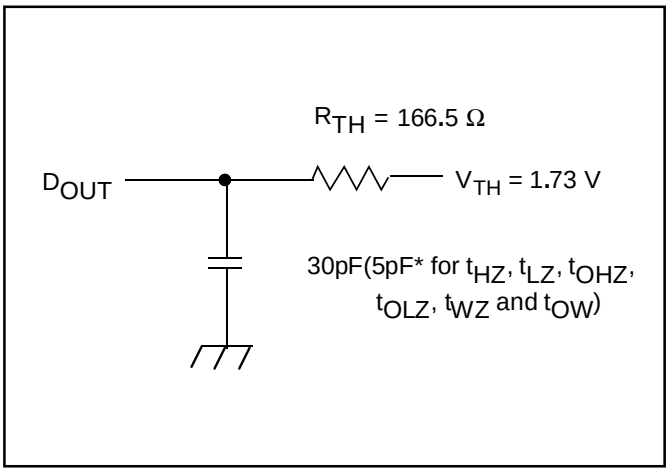
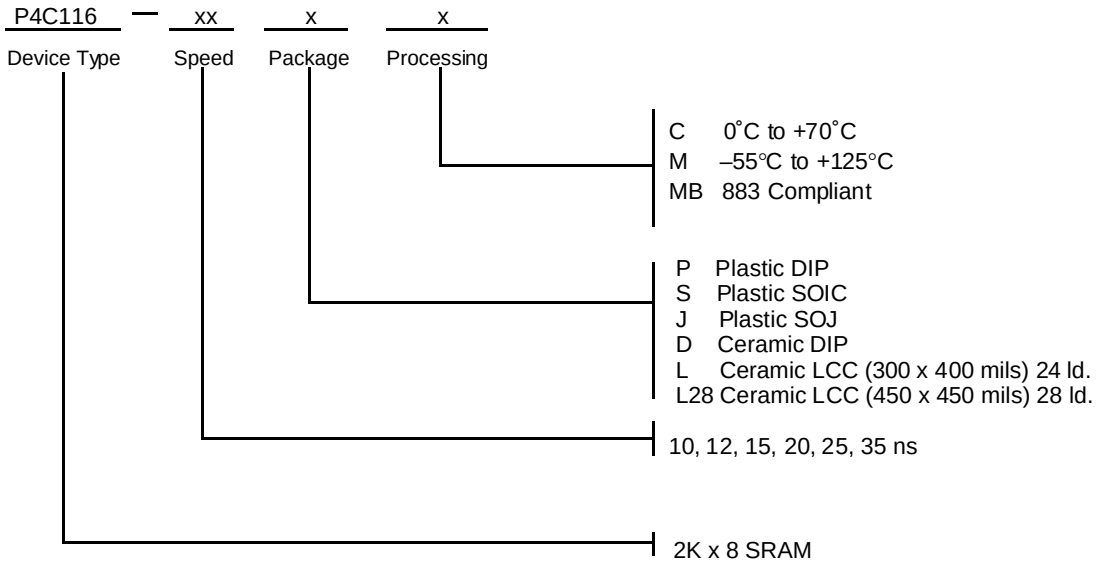



**Figure 2. Thevenin Equivalent**

* including scope and test fixture.

**Note:**
Because of the ultra-high speed of the P4C116/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the $V_{CC}$ and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between $V_{CC}$ and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with $D_{OUT}$ to match 166Ω (Thevenin Resistance).

## ORDERING INFORMATION




The P4C116 is also available to SMD-5962-89690 & 5962-84036

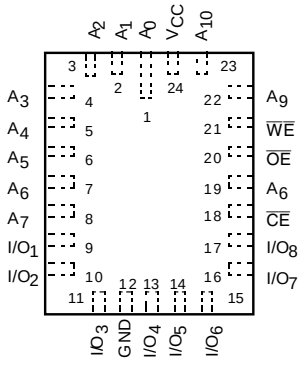
## SELECTION GUIDE

The P4C116 is available in the following temperature, speed and package options.

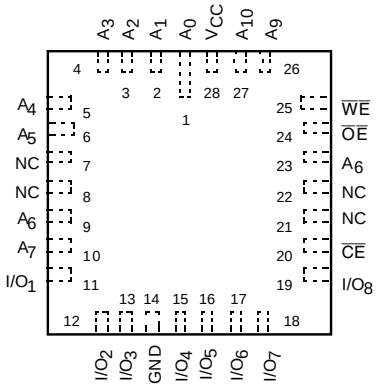
| Temperature Range | Package \ Speed (ns) | 10 | 12 | 15 | 20 | 25 | 35 |
|---|---|---|---|---|---|---|---|
| Commercial | Plastic DIP | –10PC | –12PC | –15PC | –20PC | –25PC | –35PC |
| | Plastic SOIC | –10SC | –12SC | –15SC | –20SC | –25SC | –35SC |
| | Plastic SOJ | –10JC | –12JC | –15JC | –20JC | –25JC | –35JC |
| Military Temp. | CERDIP (300 mil) | N/A | N/A | –15DM | –20DM | –25DM | –35DM |
| | LCC (rectangular) | N/A | N/A | –15LM | –20LM | –25LM | –35LM |
| | LCC (square) | N/A | N/A | –15L28M | –20L28M | –25L28M | –35L28M |
| Military Processed* | CERDIP (300 mil) | N/A | N/A | –15DMB | –20DMB | –25DMB | –35DMB |
| | LCC (rectangular) | N/A | N/A | –15LMB | –20LMB | –25LMB | –35LMB |
| | LCC (square) | N/A | N/A | –15L28MB | –20L28MB | –25L28MB | –35L28MB |

* Military temperature range with MIL-STD-883, Class B processing.
N/A = Not Available

## LCC PIN CONFIGURATIONS




LCC (L8)
TOP VIEW




LCC (L5-1)
TOP VIEW