GENERAL DESCRIPTION

The BW1219A is a CMOS 12Bit D/A converter for general application.

This digital to analog converter consists of a R-2R ladder block and an Op amp block.

Its maximum conversion rate is 10MSPS.

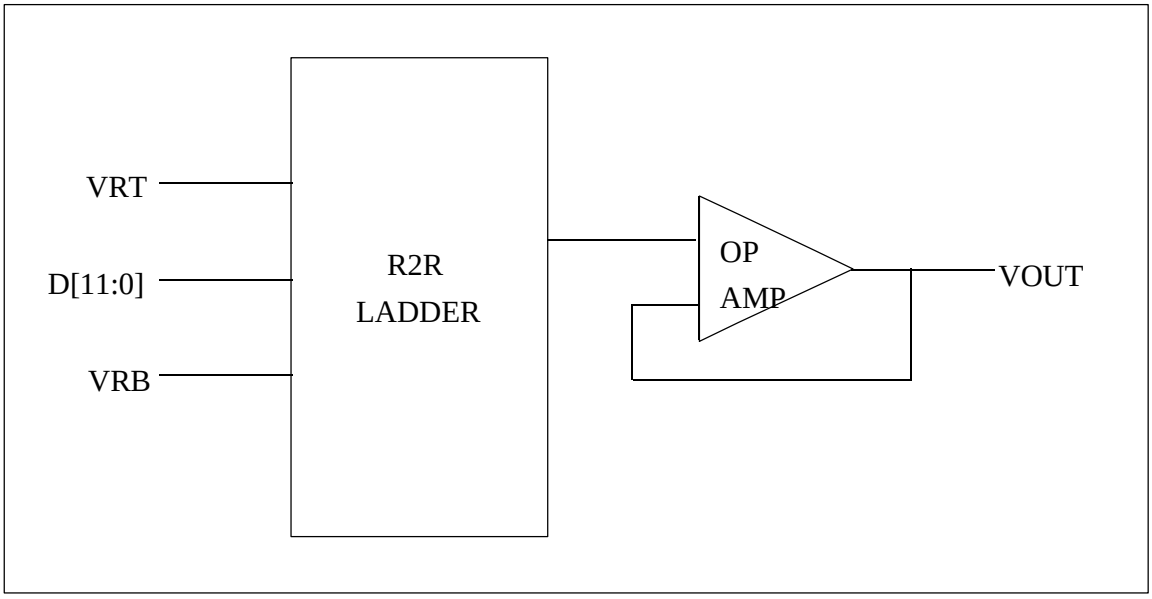
FEATURES

- **Resolution : 12Bits**
- **Differential Linearity Error : ±1.0 LSB(MAX)**
- **Maximum Conversion Rate : 10MSPS**
- **Supply Voltage : 3.3V**
- **External Voltage Reference : 0.1V, 2.1V**
- **Output Swing : 0.1V - 2.1V**
- **Operation Temperature Range : 0°C - 70°C**

TYPICAL APPLICATIONS

- HDD
- General purpose Digital to Analog Converter

FUNCTIONAL BLOCK DIAGRAM



CORE PIN DESCRIPTION

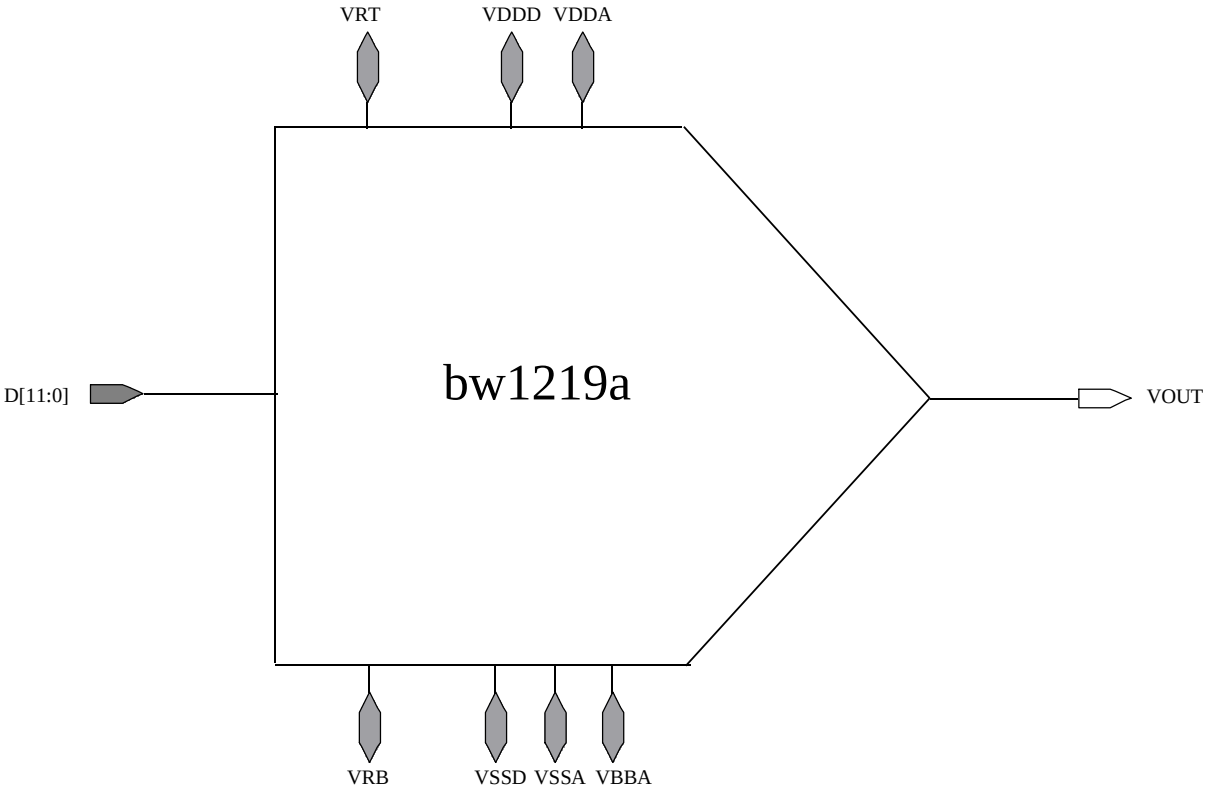
	I/O TYPE	I/O PAD	PIN DESCRIPTION
D[11:0]	DI	picc_bb	Digital Input Data
VRB	AB	poa_bb	Voltage Reference Bottom (0.1V)
VRT	AB	poa_bb	Voltage Reference Top (2.1V)
VOUT	AO	poa_bb	Analog Voltage Output
VDDD	DP	vddd	Digital Power
VSSD	DG	vssd	Digital Ground
VDDA	AP	vdda	Analog Power
VSSA	AG	vssa	Analog Ground
VBBA	AG	vbba	Analog Ground

I/O TYPE ABBR
* AI : Analog Input
* DI : Digital Input
* AO : Analog Output
* DO : Digital Output

* AP : Analog Power
* AG : Analog Ground
* DP : Digital Power
* DG : Digital Ground

* AB : Analog Bidirection
* DB : Digital Bidirection

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

	Symbol	Typ	Unit
Supply Voltage	VDDD VDDA	5	V
Reference Input Voltage	VRT VRB	2.1 0.1	V V
Digital Input Voltage HIGH LOW	Vinh Vinl	5 0.0	V V
Operating Temperature	Top	0 to 70	°C

NOTES :

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions not implied.

2. All voltages are measured with respect to VSS unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDD VDDA	3.15	3.3	3.45	V
Reference Input Voltage	VRT VRB	- -	2.1 0.1	- -	V V
Digital Input Voltage HIGH LOW	Vinh Vinl	0.7 VDDD -	- -	- 0.3 VDDD	V V
Operating Temperature	Top	0	-	70	°C

NOTE :
It is strongly recommended that to avoid power latch-up all the supply pins(VDDA,VDDD) be driven from the same source.

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications : VDDD=VDDA=3.3V, VSSD=VSSA=VBBA=0V, Load Cap=25pF
Top=55°C, VRT=2.1V, VRB=0.1V unless otherwise specified.)

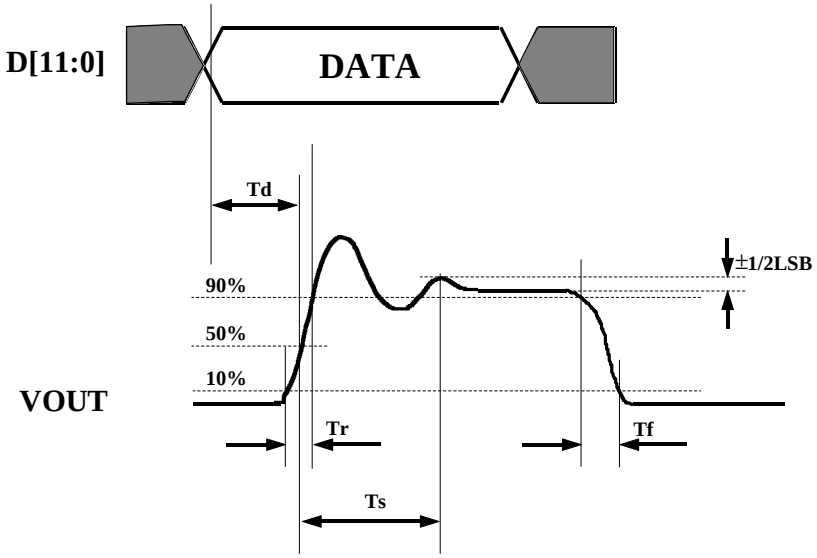
	Symbol	Min	Typ	Max	Unit
Resolution	-	-	12	-	Bits
Differential Linearity Error	DLE	-	-	±1	LSB
Integral Linearity Error	ILE	-	-	±8	LSB
Maximum Output Voltage	-	-	2.1	-	V
LSB Size	-	-	488	-	uV

AC ELECTRICAL CHARACTERISTICS

(Converter Specifications : VDDD=VDDA=3.3v, VSSD=VSSA=VBBA=0V, load cap=25pF
Top=55°C, VRT=2.1V, VRB=0.1V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Maximum Conversion Rate	f_c	-	10	-	MSPS	data = 10MHz
Dynamic Supply Current	Ivdd	-	25	-	mA	f_c=10MHz
Analog Output Delay	Td	-	50	-	ns	f_c=10MHz Data : All High
Analog Output Rise Time	Tr	-	50	-	ns	f_c=10MHz Data : All Low→All High
Analog Output Fall Time	Tf	-	50	-	ns	f_c=10MHz Data : All High→All Low
Analog Output Settling Time	Ts	-	70	-	ns	f_c=10MHz Data : All Low→All High

TIMING DIAGRAM



1. Output delay measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within ±1/2 LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

FUNCTION DESCRIPTION

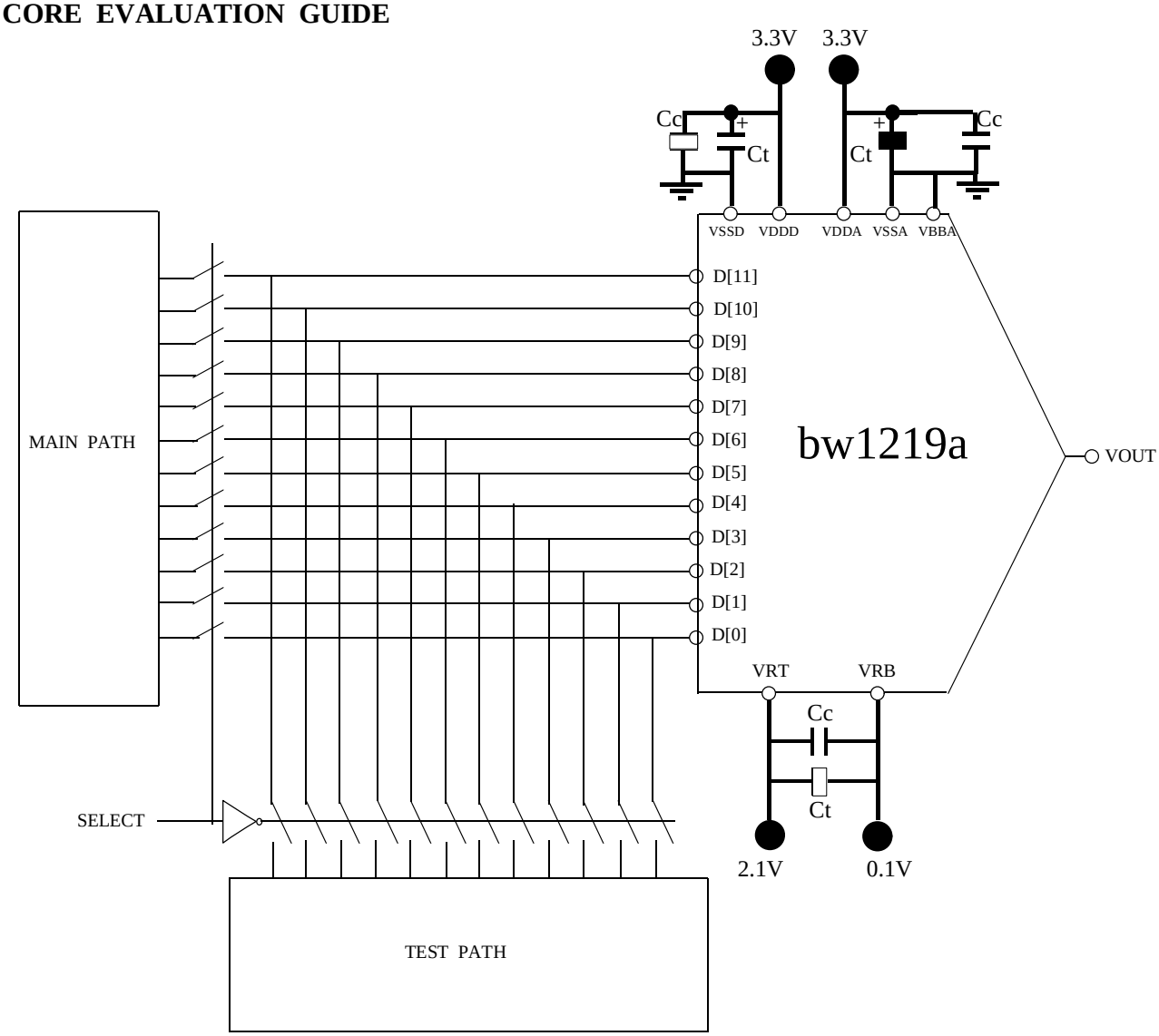
1. The BW1219A has a R-2R Ladder Block for 12bit and an Opamp Block for driving Output.

2. The R-2R Ladder Block generates binary weighted voltage (VRT/2^1 VRT/2^2 VRT/2^3 ¡¥¡¥¡¥¡¥ VRT/$2^{n)}$ corresponding to Digital Input Data for n-bit DAC and Output total voltage is summing of each values.

3. In Output voltage, MSB = VRT/2^1
   LSB = VRT/2^n

4. Output of the R2R Ladder Block is driven by Opamp

CORE EVALUATION GUIDE



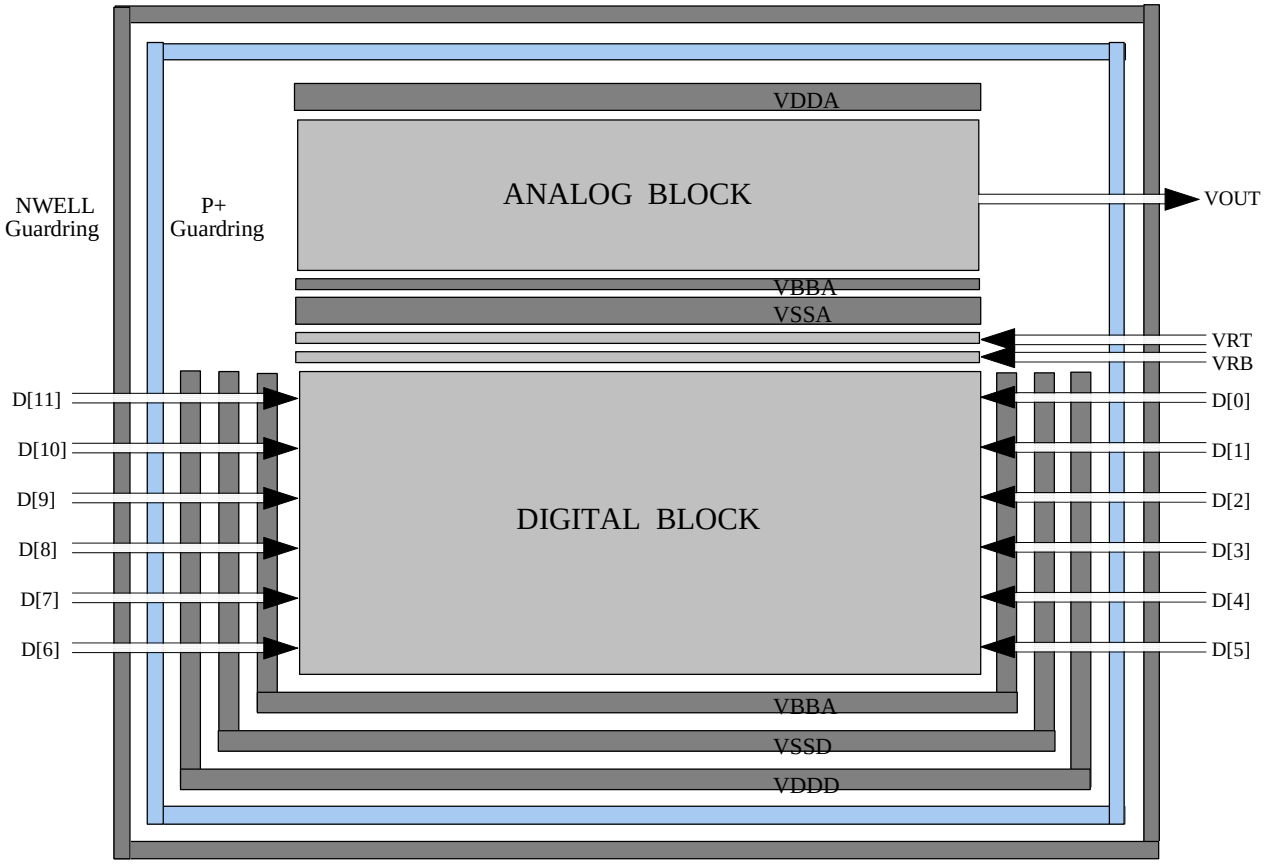
LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR

TESTABILITY

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[11:0]).

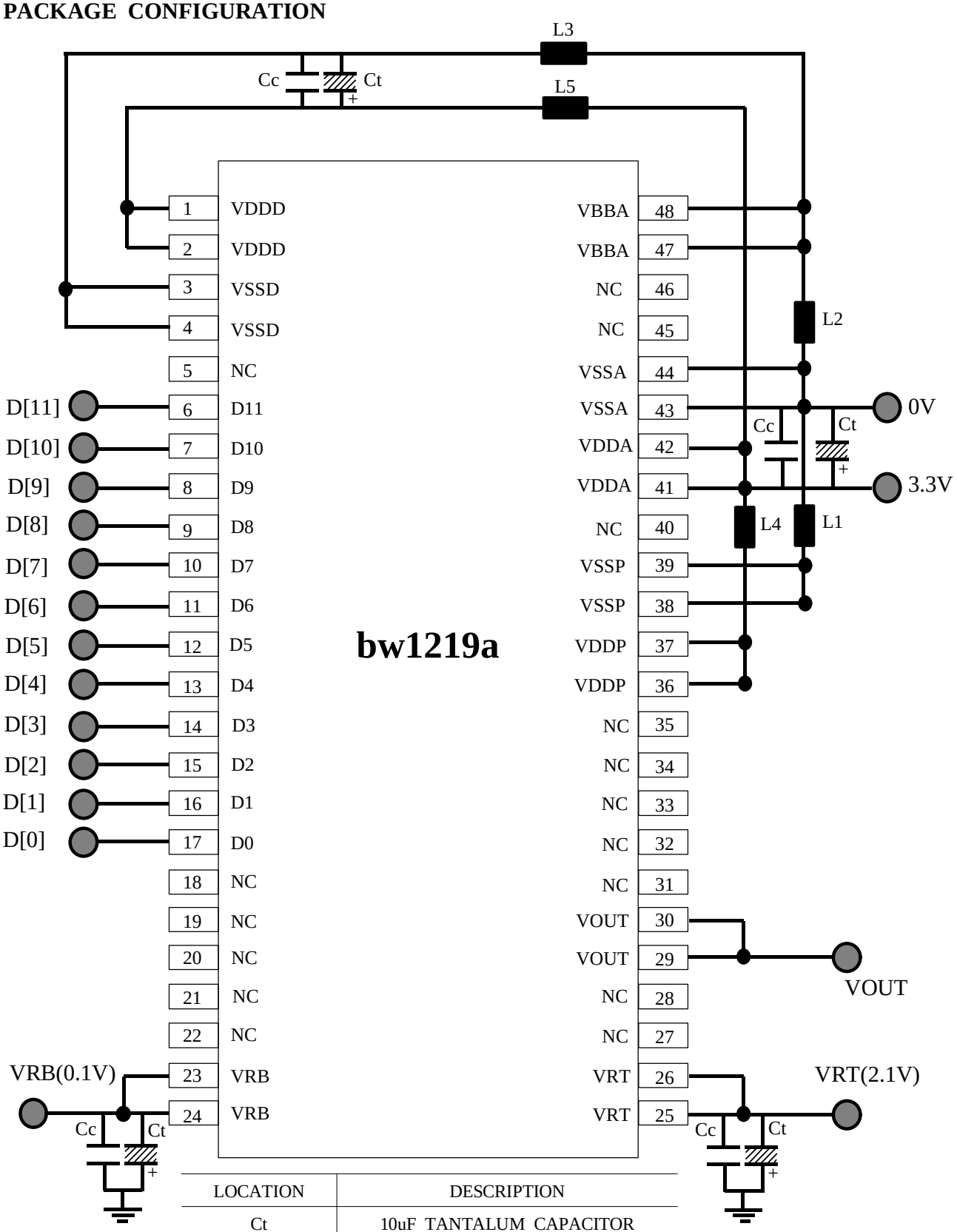
See above figure. Only if it is, you can check the main functon (Linearity)

CORE LAYOUT GUIDE



1. It is recommended that you use thick analog power metal. when connecting to PAD, the path should be kept as short as possible.
2. Digital power and analog power are separately used.
3. When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise.
   In that case, the power metal should be connected to PAD directly.
4. The Bulk power is used to reduce the influence of substrate noise.
5. Digital input signal lines must be same length to reduce the difference of delay.

PACKAGE CONFIGURATION



LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR
L1~L5	FERRITE BEAD (0.1mh)

PACKAGE PIN DESCRIPTION

	PIN NO	I/O TYPE	PIN DESCRIPTION
VDDD	1,2	DP	Digital Power
VSSD	3,4	DG	Digital Ground
D[11:0]	6~17	DI	Digital Input Data
VRB	23,24	AB	Voltage Reference Bottom (0V)
VRT	25,26	AB	Voltage Reference Top (2V)
VOUT	29,30	AO	Analog Voltage Output
VDDP	36,37	AP	Analog Power
VSSP	38,39	AG	Analog Ground
VDDA	41,42	AP	Pad Power
VSSA	43,44	AG	Pad Ground
VBBA	47,48	AG	Analog Sub Bias
NC	5,18,19,20 21,22,27,28 31,32,33,34 35,40,45,46	DO	No Connection

I/O TYPE ABBR

* AI : Analog Input
* DI : Digital Input
* AO : Analog Output
* DO : Digital Output

* AP : Analog Power
* AG : Analog Ground
* DP : Digital Power
* DG : Digital Ground

* AB : Analog Bidirection
* DB : Digital Bidirection

FEEDBACK REQUEST

We appreciate your interest in out products. If you have further questions, please specify in the attached form. Thank you very much.

Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				Ω	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

VOLTAGE OUTPUT DAC					
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

CURRENT OUTPUT DAC					
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				Ω	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Interal Reference Voltage(BGR)?
- Which do you want to Serial Input TYPE or parallel Input TYPE?
- Do you need 3.3v and 5v power supply in your system?

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of VDD (VDDA,VDDD) and VSS (VSSA,VSSD) pins should be as short as possible so as to minimize inductive ringing.

Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, 0.1uF ceramic capacitor is used in parallel with a 10uF tantalum capacitor.
The digital power plane(VDDD) and analog power plane(VDDA) are connected through a ferrite bead, and also the digital ground plane(VSSD) and the analog ground plane(VSSA). This ferrite bead should be located within 3inches of the BW1219A. The analog power plane supplies power to the BW1219A of the analog output pin and related devices.

Digital Signal Interconnect

The PCB line between the TTL driver and the input to the BW1219A has a low impedance source and is terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of BW1219A.
to reduce ringing caused by transmission line mismatch, either the line length should be shortened or the line termination method should be used.
The line termination method includes serial and parallel terminations.
The recommended technique is to use serial termination. Serial termination is achieved by installing a resistor of about 50Ω between the TTL driver output and the BW1219A digital input.

Analog Signal Interconnect

To minimized noise pickup and reflections due to impedance mismatch, the BW1219A should be located as close as possible to the output connector.
The line between DAC output and monitor input should also be regarded as a transmission line. Due to the fact, it can cause problems in transmission line mismatch. As a solution to these problems, the double-termination method is used. By using this, both ends of the termination lines are matched, providing an ideal, non-reflective system.