Document Title

Multi-Chip Package Memory

32M Bit (2Mx16 bit) Uni-Transistor RAM / 16M(1Mx16 bit) Full CMOS SRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft - Design target	March 13, 2001	Preliminary
0.1	Revise - Released t_{WC} for continuous write operation from 100ns to 110ns. - Released t_{CW} for continuous write operation from 90ns to 100ns. - Released t_{AW} for continuous write operation from 90ns to 100ns. - Released t_{BW} for continuous write operation from 90ns to 100ns. - Released t_{WP} for continuous write operation from 90ns to 100ns.	April 3, 2001	Preliminary
0.2	Revise - Improved standby current for UtRAM from 250uA to 150uA - Added product list	June 6, 2001	Preliminary
1.0	Finalize - Added 70ns product for SRAM - Improved standby current for SRAM from 40uA to 20uA - Released deep power down suspend time from 1us to 0.5us	July 12, 2001	Final

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Multi-Chip Package Memory

32M Bit (2Mx16 bit) Uni-Transistor RAM / 16M(1Mx16 bit) Full CMOS SRAM

FEATURES

- Power Supply voltage : 2.7~3.3 V
- Organization
  - UtRAM : 2M x 16 bit
  - SRAM : 1M x 16 bit
- Access Time : UtRAM 100ns, SRAM 70/100ns
- Power Consumption (typical value)
  - UtRAM Standby Current : 120µA
    Operating Current : 18mA
  - SRAM Standby Current : 1µA
    Operating Current : 25 mA
- SRAM Data Retention : 1.5 V (min.)
- UtRAM Deep Power Down: Memory cell data hold invalid
- Three State Outputs
- Extended Temperature : -25°C ~ 85°C
- Package : 69-TBGA-9.0x12.5

GENERAL DESCRIPTION

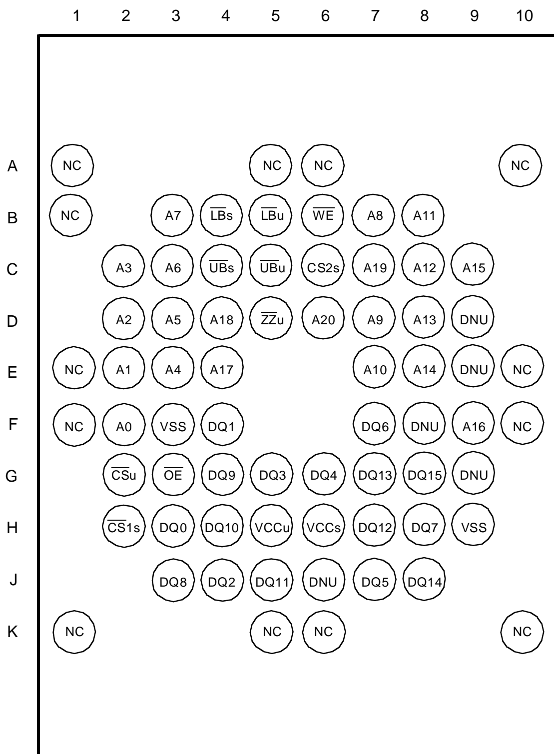
The K5S3216Y0M is a Multi Chip Package Memory which combines 32Mbit Uni-Transistor RAM and 16Mbit full CMOS SRAM.

The 32Mbit Uni-Transistor RAM is organized as 2M x16 bit and the 16Mbit SRAM is organized as 1M x16 bit.

The 32Mbit Uni-Transistor RAM supports deep power down mode for low standby current.

The 16Mbit SRAM supports low data retention voltage for battery backup operation with low data retention current.

BALL CONFIGURATION

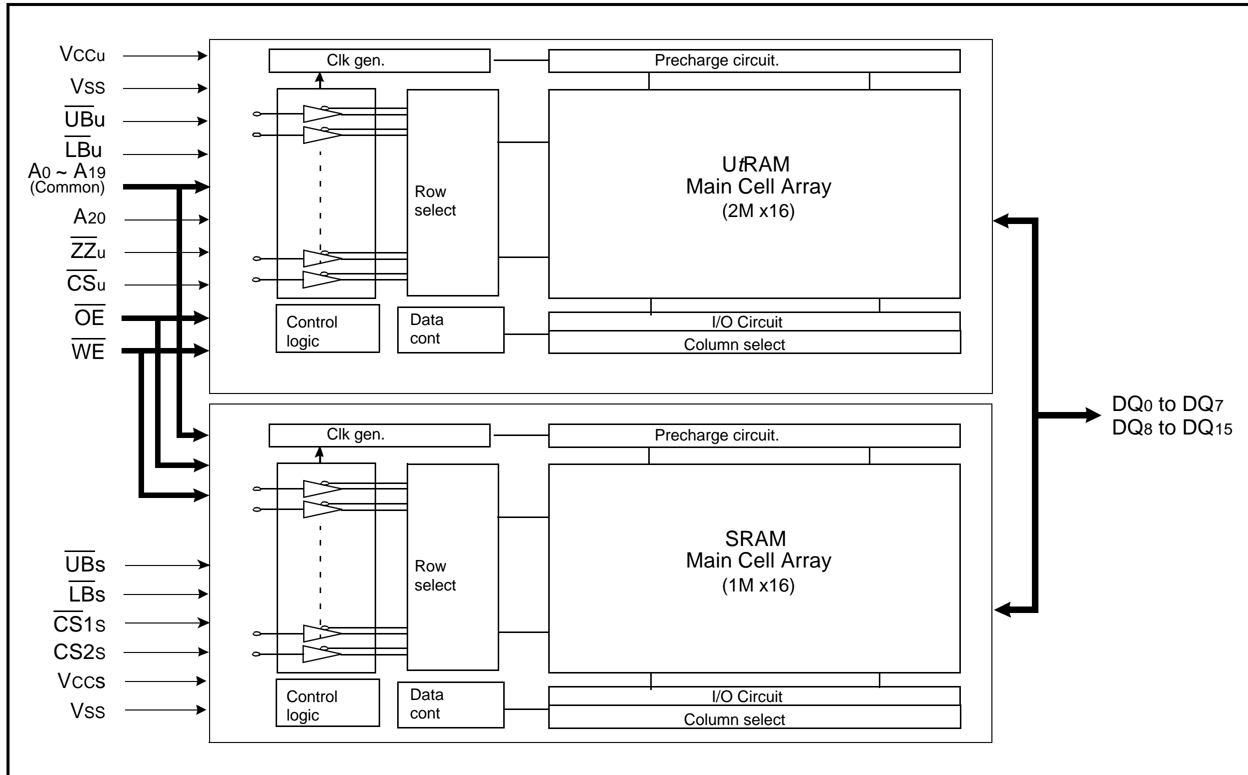


69-TBGA Top View (Ball Down)

BALL DESCRIPTION

Ball Name	Description
A_0 ~ A_{19}	Address Input (Common)
A_{20}	Address Input (UtRAM)
DQ_0 ~ DQ_{15}	Data Input/Output (Common)
Vccs	Power Supply (SRAM)
Vccu	Power Supply (UtRAM)
Vss	Ground (Common)
$\overline{CS1}$s	Chip Enable (SRAM)
CS2s	Chip Enable (SRAM)
$\overline{CS}$u	Chip Enable (UtRAM)
$\overline{ZZ}$u	Deep Power Down (UtRAM)
$\overline{UB}$s	Upper Byte Enable (SRAM)
$\overline{LB}$s	Lower Byte Enable (SRAM)
$\overline{UB}$u	Upper Byte Enable (UtRAM)
$\overline{LB}$u	Lower Byte Enable (UtRAM)
$\overline{WE}$	Write Enable (Common)
$\overline{OE}$	Output Enable (Common)
DNU	Do Not Use(Reserved for future use)
NC	No Connection (Dummy Ball)

Figure 1. FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Extended Temperature Products(-25~85°C)	
Part Name	**Function**
K5S3216Y0M-T010 K5S3216Y0M-T070	69-TBGA with 69 ball, UtRAM100ns, SRAM 100ns, 3.0V 69-TBGA with 69 ball, UtRAM100ns, SRAM 70ns, 3.0V

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions longer than 1seconds may affect reliability.

FUNCTIONAL DESCRIPTION for U*t*RAM

$\overline{CS}$u	$\overline{ZZ}$u	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$u	$\overline{UB}$u	I/O0~7	I/O8~15	Mode	Power
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Deep Power Down
L	H	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don′t care.(Must be low or high state)

FUNCTIONAL DESCRIPTION for SRAM

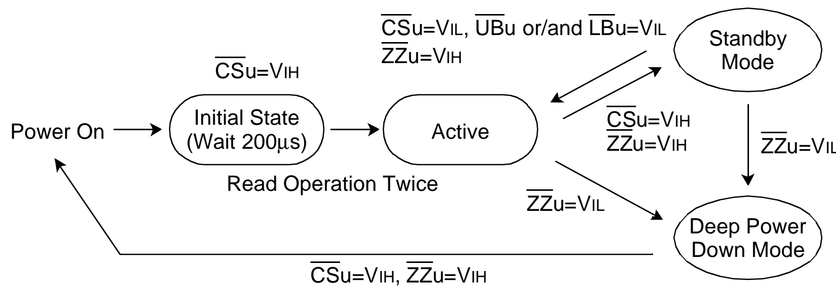
$\overline{CS}$1s	CS2s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$s	$\overline{UB}$s	I/O0~7	I/O8~15	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	X[1]	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don′t care. (Must be low or high state)

POWER UP SEQUENCE for U*t*RAM

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minium 200µs with $\overline{CS}$u=high.
3. Issue read operation at least twice.

STANDBY MODE STATE MACHINES for U*t*RAM



RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0	3.3	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	18	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	25	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Item	Symbol	Test Conditions	Min	Typ[1)]	Max	Unit
Common	Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-2	-	2	µA
	Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{ZZ}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-2	-	2	µA
	Output low voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
	Output high voltage	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V
UtRAM	Average operating current	I_{CC1u}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, $\overline{ZZ}$≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	2	5	mA
		I_{CC2u}	Cycle time=100ns, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{ZZ}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	18	25	mA
	Standby Current(CMOS)	I_{SB1u}	$\overline{CS}$≥Vcc-0.2V, $\overline{ZZ}$≥Vcc-0.2V, Other inputs=Vss to Vcc	-	120	150	µA
	Deep Power Down	I_{SBDu}	$\overline{ZZ}$≤0.2V, Other inputs=Vss to Vcc	-	5	20	µA
SRAM	Average operating current	I_{CC1s}	Cycle time=1µs, 100%duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, $\overline{LB}$≤0.2V or/and $\overline{UB}$≤0.2V, CS_2≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	4	mA
		I_{CC2s}	Cycle time=100ns, I_{IO}=0mA, 100% duty, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, $\overline{LB}$=V_{IL} or/and $\overline{UB}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}	-	-	35	mA
	Standby Current (CMOS)	I_{SB1s}	Other input =0~Vcc 1) $\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V ($\overline{CS_1}$ controlled) or 2) 0V≤CS_2≤0.2V(CS_2 controlled) or 3) $\overline{LB}$=$\overline{UB}$≥Vcc-0.2V, CS_2≥Vcc-0.2V ($\overline{LB}$/$\overline{UB}$ controlled)	-	1.0	20	µA

1. Typical values are tested at V_{CC}=3.0V, T_A=25°C and not guaranteed.

STANDBY MODE CHARACTERISTIC for UtRAM

Power Mode	Memory Cell Data	Standby Current(µA)	Wait Time(µs)
Standby	Valid	150	0
Deep Power Down	Invaild	20	200

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load: C_L=50pF

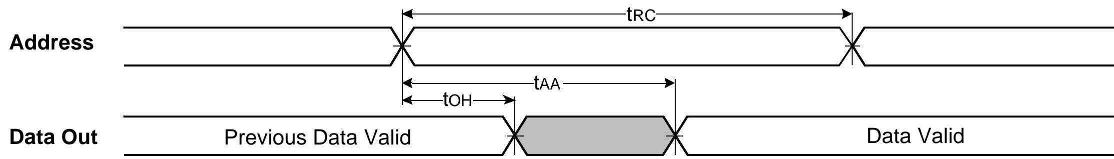
AC CHARACTERISTICS(V_{CC}=2.7~3.3V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bins								Units
			UtRAM				SRAM				
			100ns[1]		100ns[2]		70ns		100ns		
			Min	Max	Min	Max	Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	100	-	100	-	70	-	100	-	ns
	Address Access Time	t_{AA}	-	100	-	100	-	70	-	100	ns
	Chip Select to Output	t_{CO}	-	100	-	100	-	70	-	100	ns
	Output Enable to Valid Output	t_{OE}	-	50	-	50	-	35	-	50	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	100	-	100	-	70	-	100	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	10	-	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	0	25	0	25	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	0	25	0	25	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	0	25	0	25	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	5	-	ns
Write	Write Cycle Time	t_{WC}	100	-	110	-	70	-	100	-	ns
	Chip Select to End of Write	t_{CW}	80	-	100	-	60	-	80	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	80	-	100	-	60	-	80	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	80	-	100	-	60	-	80	-	ns
	Write Pulse Width	t_{WP}	70	-	100	-	55	-	70	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	30	0	30	0	25	0	30	ns
	Data to Write Time Overlap	t_{DW}	40	-	40	-	30	-	40	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	5	-	5	-	ns

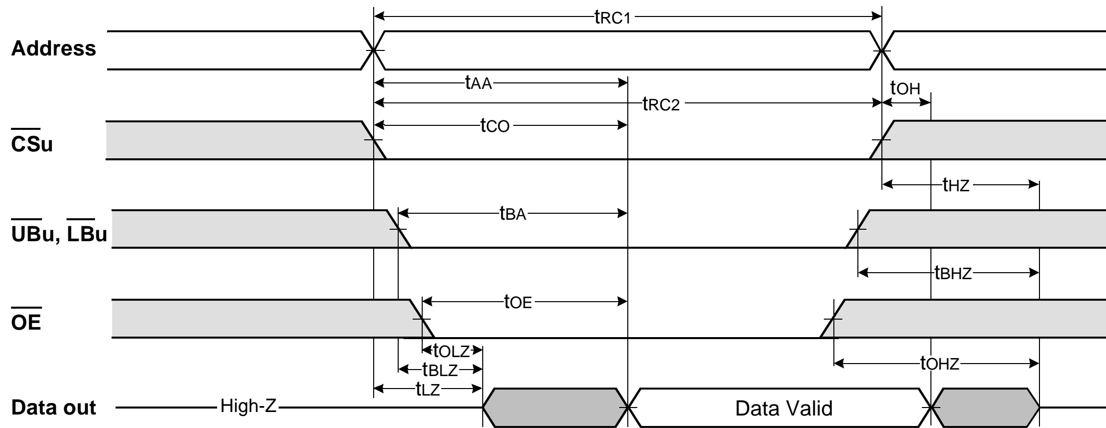
1. The characteristics which is restricted for continuous write operation over 20 times, please refer to technical note.
2. The characteristics for continuous write operation.

TIMING DIAGRAMS for U*t*RAM

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, CSu=OE=VIL, ZZu=WE=VIH, UBu or/and LBu=VIL)



TIMING WAVEFORM OF READ CYCLE(2)(ZZu=WE=VIH)



(READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. The minimum read cycle(tRC) is determined later one of the tRC1 and tRC2.

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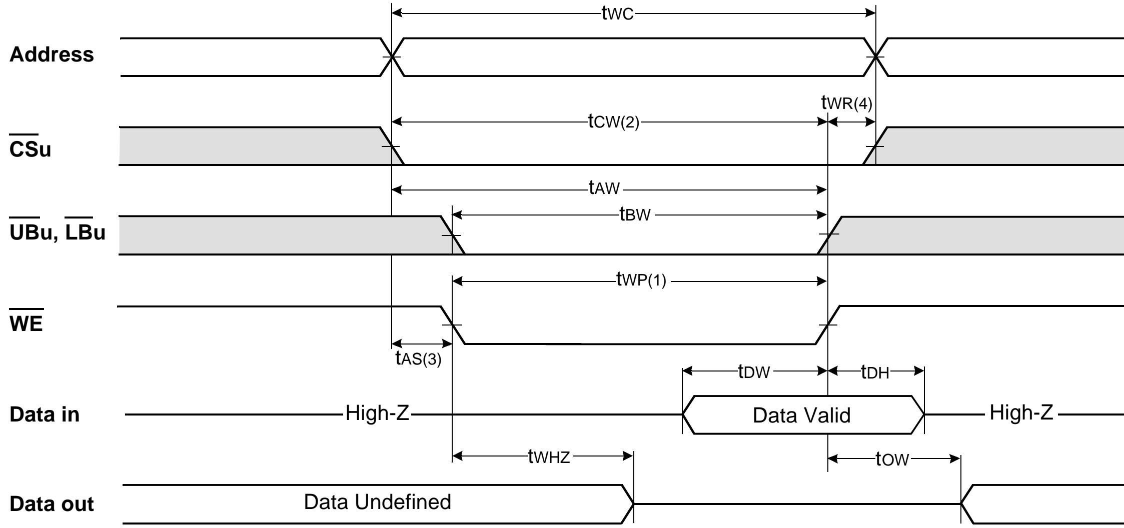
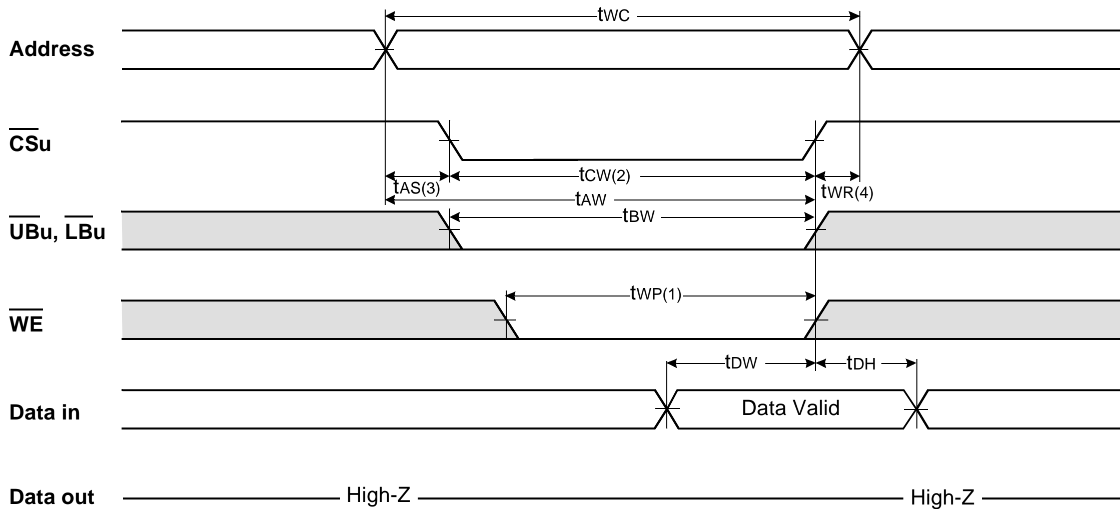
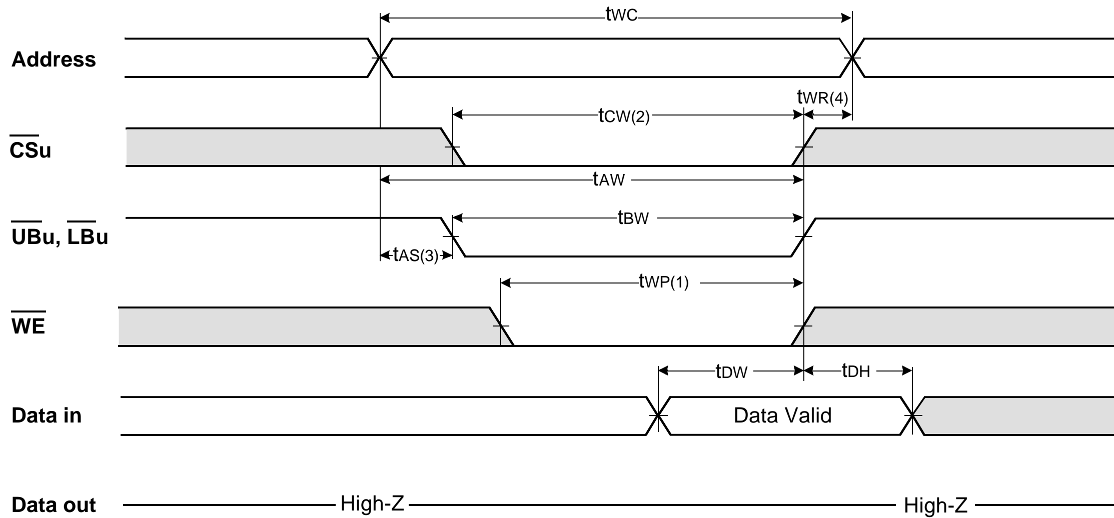
TIMING WAVEFORM OF WRITE CYCLE(1)(WE Controlled, ZZu=VIH)



TIMING WAVEFORM OF WRITE CYCLE(2)(CSu Controlled, ZZu=VIH)



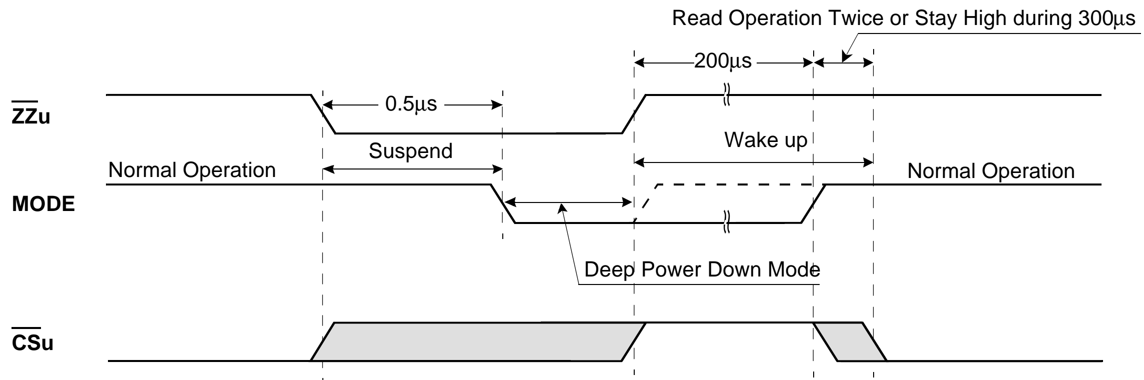
TIMING WAVEFORM OF WRITE CYCLE(3)(UBu, LBu Controlled, ZZu=VIH)



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low CSu and low WE. A write begins when CSu goes low and WE goes low with asserting UBu or LBu for single byte operation or simultaneously asserting UBu and LBu for double byte operation. A write ends at the earliest transition when CSu goes high and WE goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CSu going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CSu or WE going high.

TIMING WAVEFORM OF DEEP POWER DOWN MODE for UtRAM



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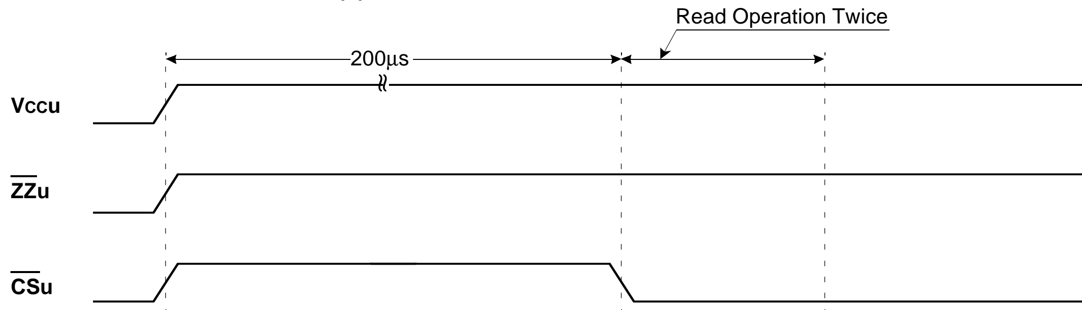
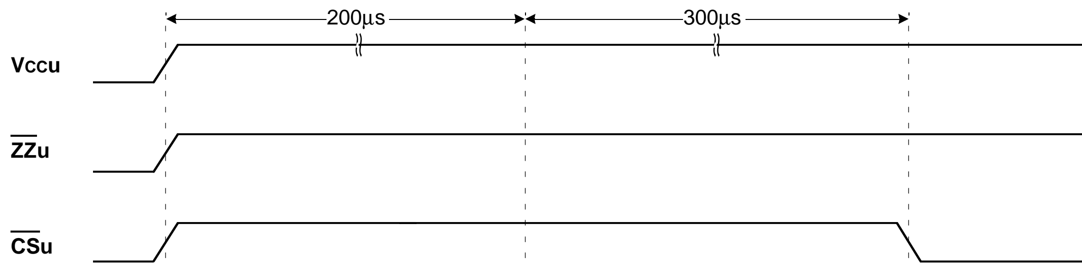
TIMING WAVEFORM OF POWER UP(1) for U*t*RAM

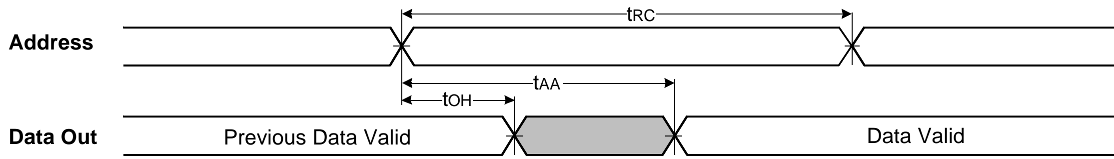


TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle) **for U*t*RAM**

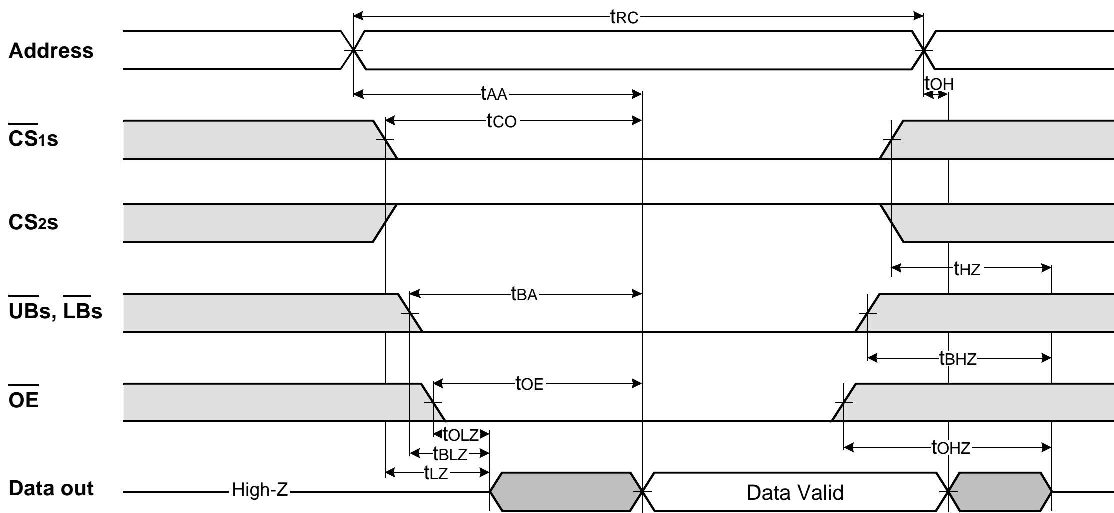


TIMING DIAGRAMS for SRAM

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1s}$=$\overline{OE}$=V_{IL}, CS2s=$\overline{WE}$=V_{IH}, $\overline{UBs}$ or/and $\overline{LBs}$=V_{IL})



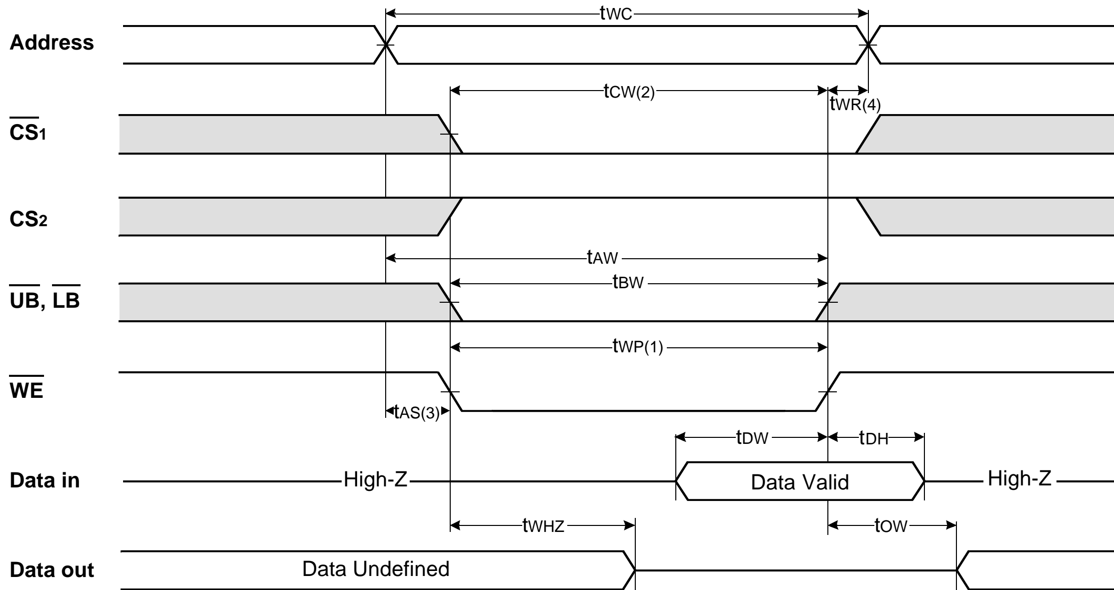
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



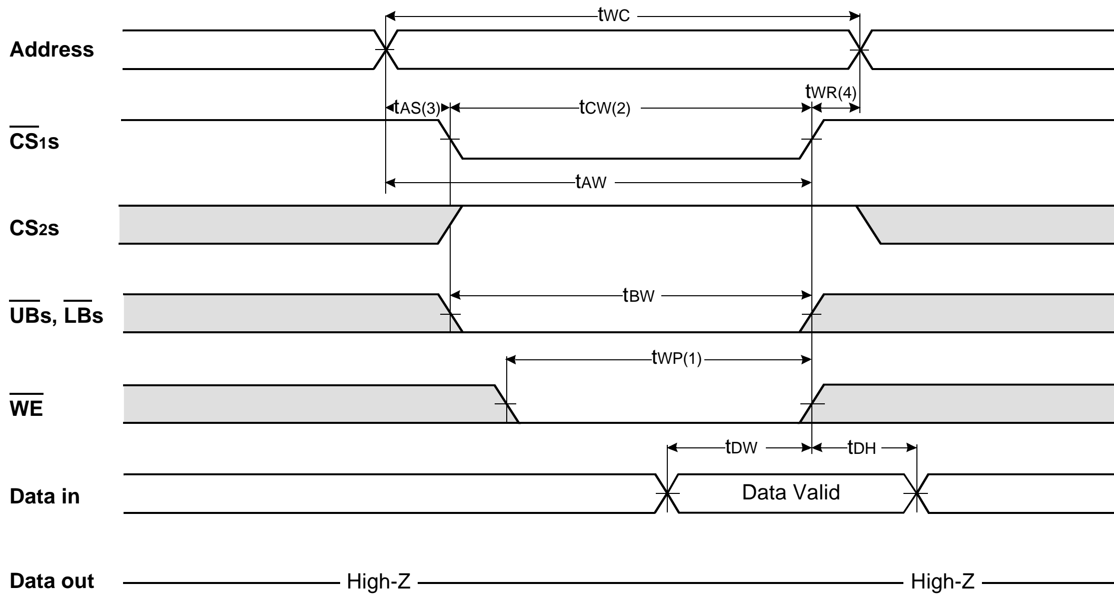
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

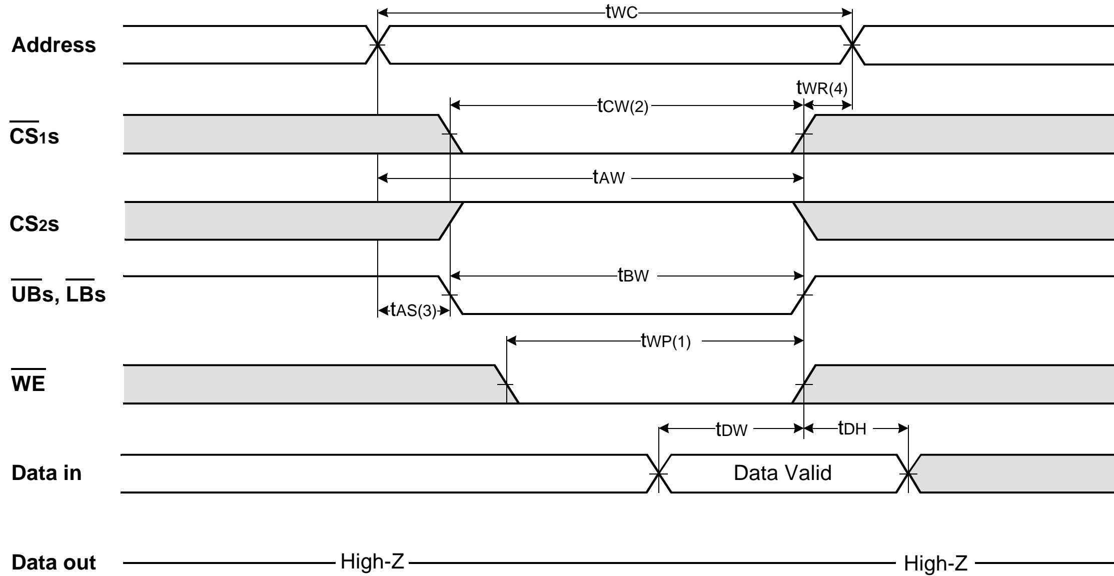
TIMING WAVEFORM OF WRITE CYCLE(1) (WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (CS1s Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (UBs, LBs Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low CS1s and low WE. A write begins when CS1s goes low and WE goes low with asserting UBs or LBs for single byte operation or simultaneously asserting UBs and LBs for double byte operation. A write ends at the earliest transition when CS1s goes high and WE goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS1s going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CS1s or WE going high.

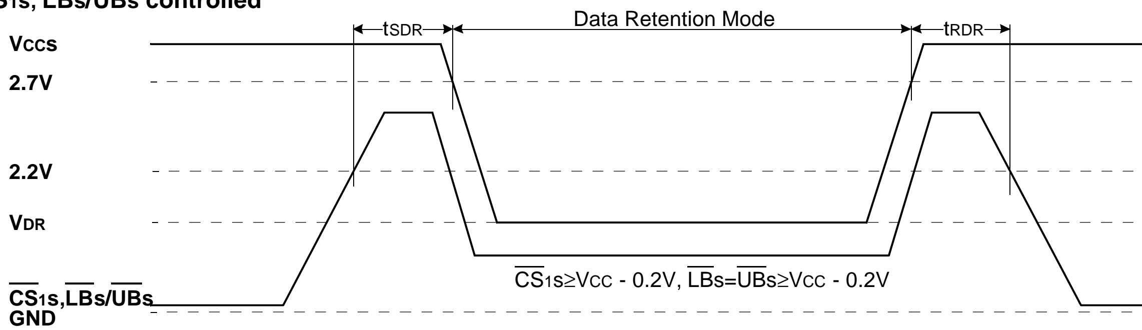
DATA RETENTION CHARACTERISTICS for SRAM

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_{1s}\geq Vcc-0.2V$[1], $V_{IN}\geq 0V$	1.5	-	3.3	V
Data retention current	IDR	Vcc=1.5V, $\overline{CS}_{1s}\geq Vcc-0.2V$[1], $V_{IN}\geq 0V$	-	1.0[2]	15	µA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

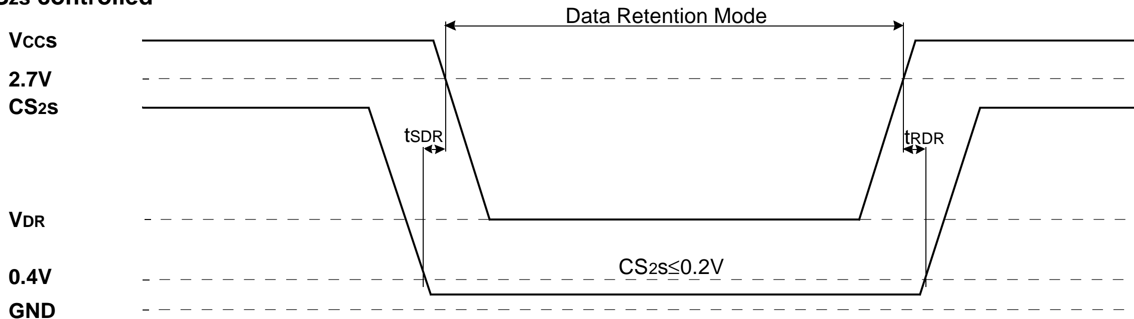
1. 1) $\overline{CS}_{1s}\geq Vcc-0.2V$, $CS_{2s}\geq Vcc-0.2V$($\overline{CS}_{1s}$ controlled) or
   2) $0\leq CS_{2s}\leq 0.2V$(CS_{2s} controlled) or
   3) $\overline{LB}s=\overline{UB}s\geq Vcc-0.2V$, $CS_{2s}\geq Vcc-0.2V$($\overline{LB}s/\overline{UB}s$ controlled)
2. Typical value are measured at T_A=25°C and not 100% tested.

DATA RETENTION WAVE FORM for SRAM

$\overline{CS}_{1s}$, $\overline{LB}s/\overline{UB}s$ controlled

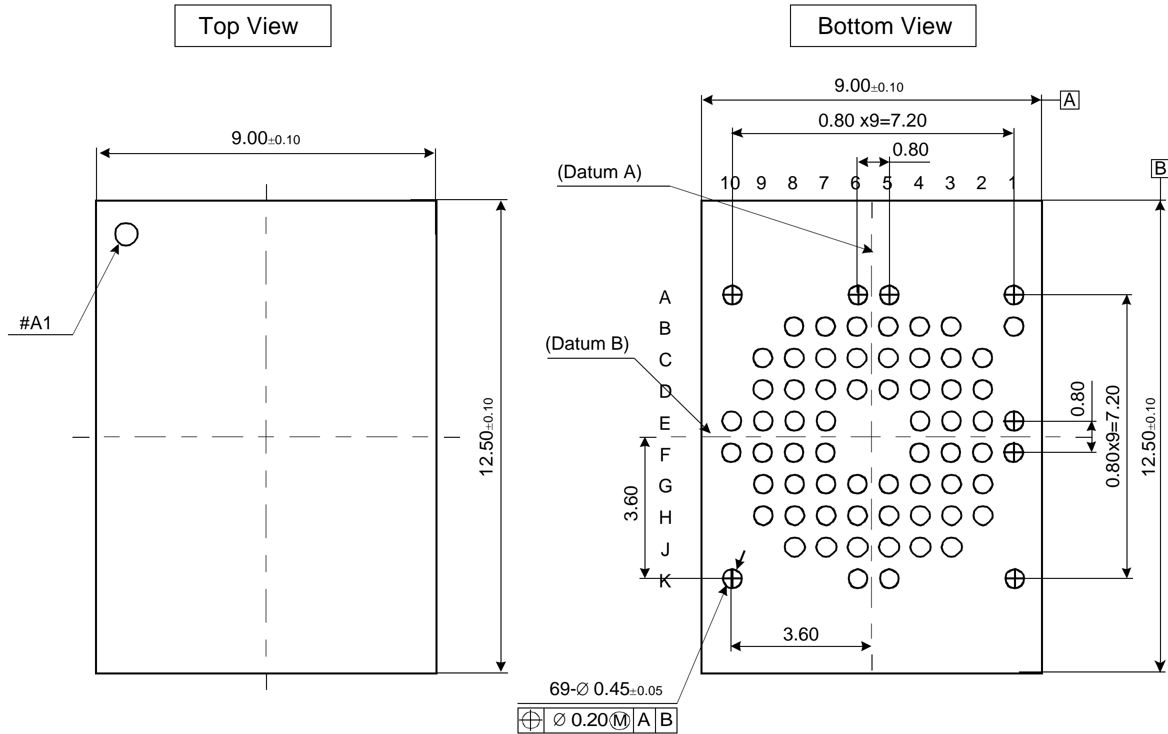


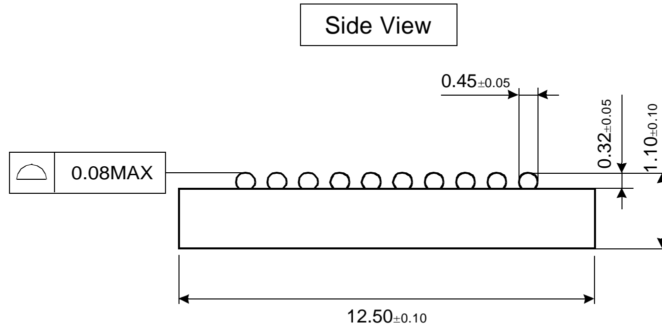
CS_{2s} controlled



PACKAGE DIMENSION

69 TAPE BALL GRID ARRAY(0.80mm ball pitch)





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TECHNICAL NOTE

U*t*RAM USAGE AND TIMING

INTRODUCTION

U*t*RAM is based on single-transistor DRAM cells. As with any other DRAM, the data in these cells must be periodically refreshed to prevent data loss. What makes the U*t*RAM unique is that it offers a true SRAM style interface that hides all refresh operations from the memory controller.

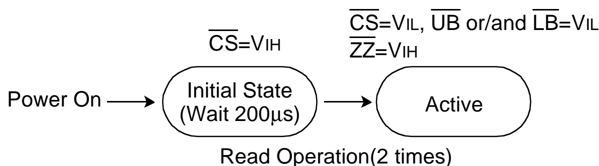
START WITH A DRAM TECHNOLOGY

The key to the U*t*RAM is its high speed and low power. This speed comes from the use of many small blocks, often just 32Kbits each, to create U*t*RAM arrays. The small blocks have short word lines with little capacitance, eliminating a major source of operating current in conventional DRAM blocks.

Each independent macro-cell on a U*t*RAM device consists of a number of these blocks. Each chip has one or more macro.

The address decoding logic is also fast. U*t*RAM perform a complete read operation in every tRC, but U*t*RAM needs power up sequence like a DRAM.

Power Up Sequence and Diagram
1. Apply power.
2. Maintain stable power for a minium 200µs with $\overline{CS}$=high.
3. Issue read operation at least 2 times.



DESIGN ACHIEVES SRAM SPECIFIC OPERATIONS

The U*t*RAM design works just like an SRAM, with no wait states or other overhead for precharging or refreshing its internal DRAM cells. SAMSUNG Electronics(SAMSUNG) hides these operations with advanced design. Precharging takes place during every access, overlapped with the end of the cycle and the decoding portion of the next cycle.

Hiding refresh is more difficult, Every row in every block must be refreshed at least once during the refresh interval to prevent data loss. SAMSUNG provides a internal refresh controller for devices. When all accesses during a refresh interval are directed to one macro-cell, as can happen in signal processing applications, a more sophisticated approach is required to hide refresh. The pseudo SRAM, sometimes used on these applications, which is required a memory controller that can hold off accesses when a refresh operation is needed. SAMSUNG unique qualitative advantage over these parts(in addition to quantitative improvements in access speed and power consumption) is that the U*t*RAM never needs to hold off accesses, and indeed it has no hold off signal. The circuitry that gives SAMSUNG this advantage is fairly simple but has not previously been disclosed.

AVOID TIMING

Following figures show you a abonormal timing which is not supported on U*t*RAM and their solution.

At read operation, if your system have a timing which sustain invalid states over 4us at read mode like Figure 1. There are some guide line for proper operation of U*t*RAM.

When your system have multiple invalid address signal shorter than tRC on the timing which showed in Figure 1, U*t*RAM need a normal read timing during that cycle(Figure 2) or toggle the $\overline{CS}$ to high'about tRC(Figure 3).

Figure 1.

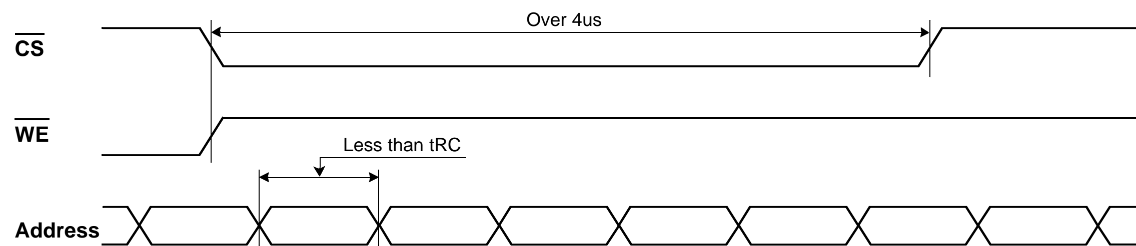


Figure 2.

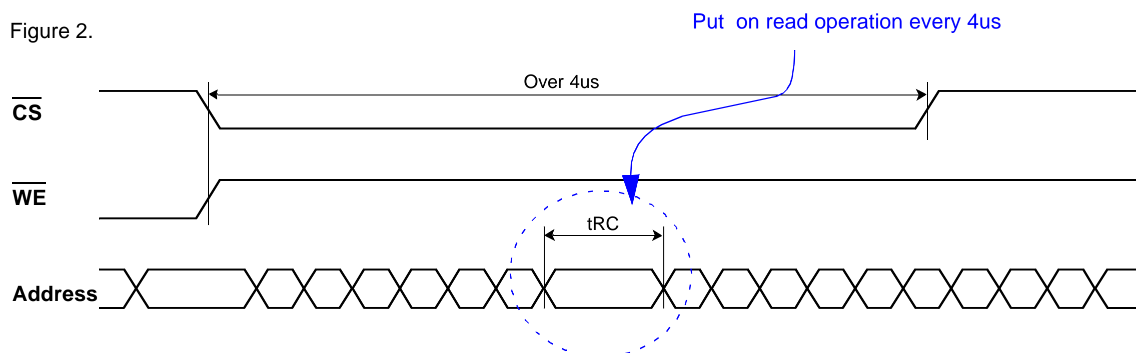


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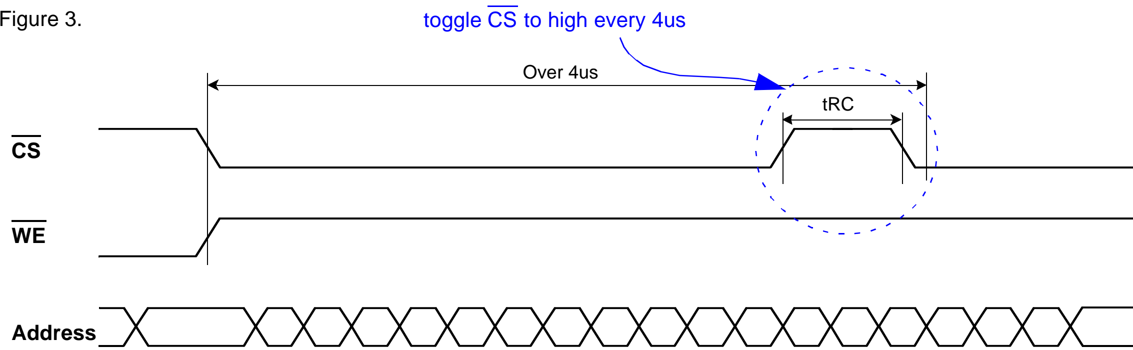
Figure 3.



Write operation have similar restricted operation with Read. If your system have a timing which sustain invalid states over 4us at write mode and system have continuous write signal with Min. tWC over 4us like Figure 4.

You must put read timing on the cycle(Figure 5) or toggle the CS to high about tRC(Figure 6).

Figure 4.

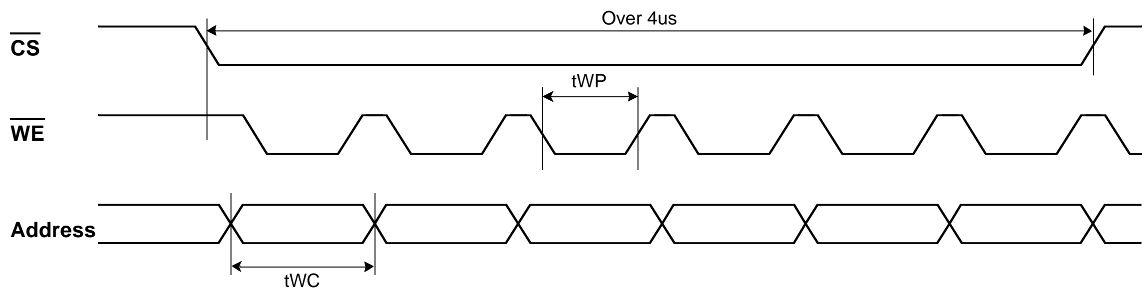


Figure 5.

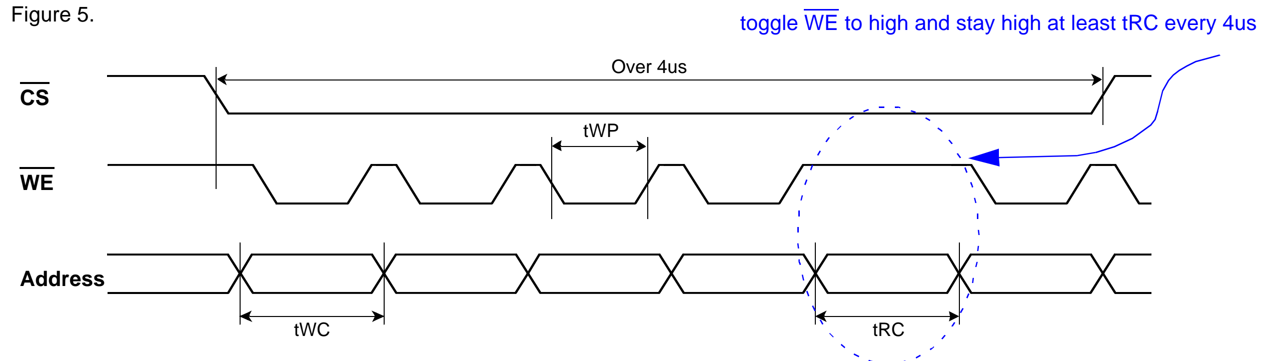
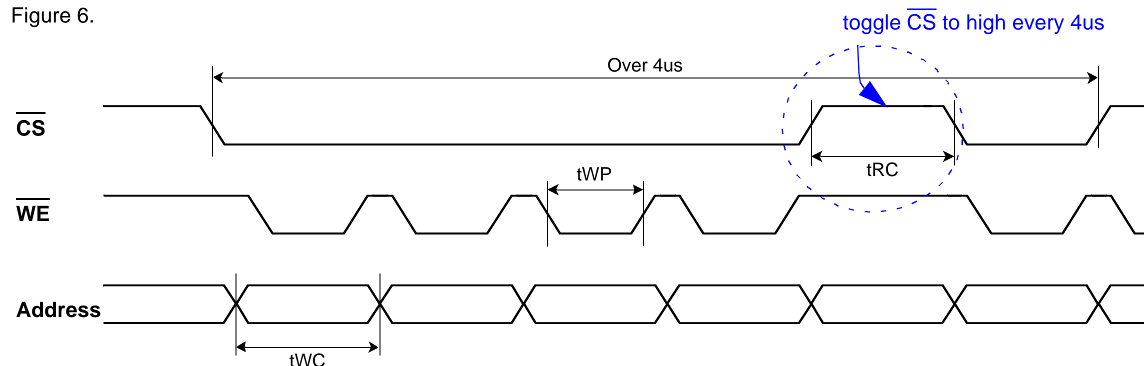


Figure 6.



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