32Kx8 bit Low Power & Low Vcc CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.7µm CMOS
- Organization : 32K x 8
- Power Supply Voltage
  KM62V256C family : 3.3V ± 0.3V
  KM62U256C family : 3.0V ± 0.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  28-SOP, 28-TSOP(I)-Forward/Reverse

GENERAL DESCRIPTION

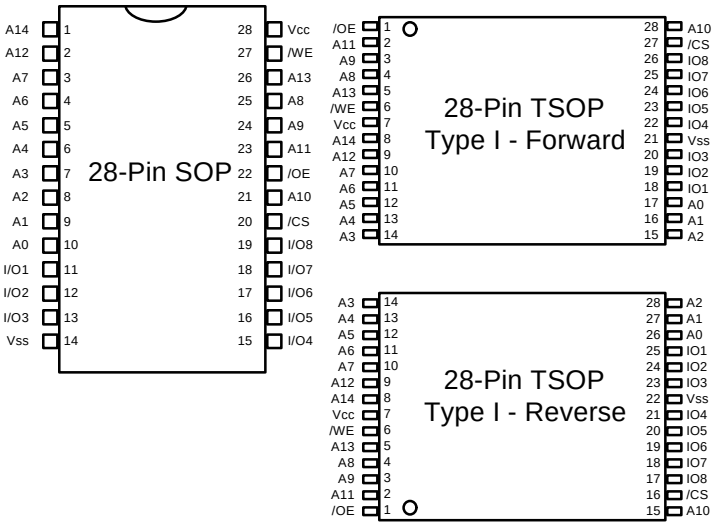
The KM62V256C and KM62U256C family are fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

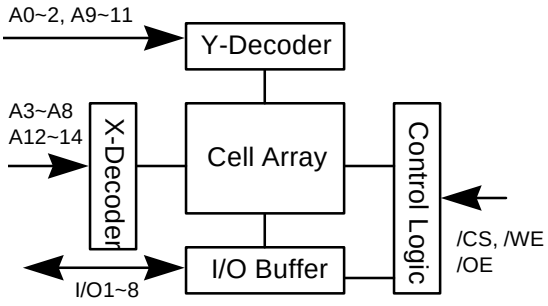
Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM62V256CL-L	Commercial	3.0~3.6V	70*/100	28-SOP**	10 µA	35mA
KM62U256CL-L	(0~70 °C)	2.7~3.3V	85*/100	28-TSOP(I) R/F	10 µA	
KM62V256CLE-L	Extended	3.0~3.6V	70*/100	28-SOP**	20 µA	
KM62U256CLE-L	(-25~85 °C)	2.7~3.3V	85*/100	28-TSOP(I) R/F	15 µA	
KM62V256CLI-L	Industrial	3.0~3.6V	70*/100	28-SOP**	20 µA	
KM62U256CLI-L	(-40~85 °C)	2.7~3.3V	85*/100	28-TSOP(I) R/F	15 µA	

* measured with 30pF test load
** the device with 100ns SOP package in 3.0~3.6V Vcc range is not produced.

PIN DESCRIPTION



FUNCTIONAL BLOCK DIAGRAM



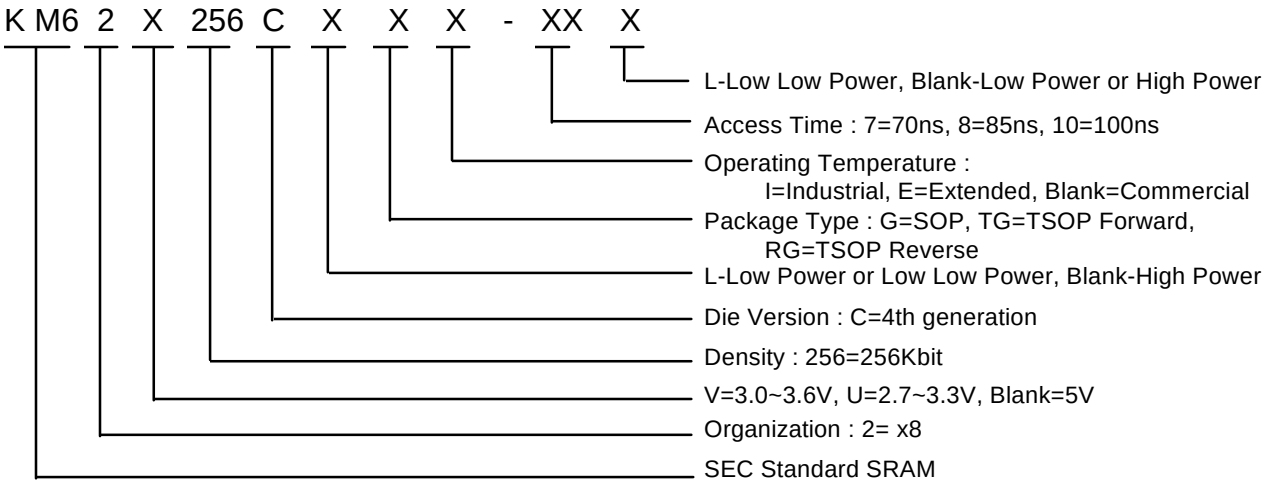
Pin Name	Function
A0~A14	Address Inputs
/WE	Write Enable Input
/CS	Chip Select Input
/OE	Output Enable Input
I/O1~I/O8	Data Input/Output
Vcc	Power
Vss	Ground

PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Extended Temp Products (-25~85 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**	**Part Name**	**Function**
KM62V256CLG-7L	28-SOP, 70ns, 3.3V	KM62V256CLGE-7L	28-SOP, 70ns, 3.3V	KM62V256CLGI-7L	28-SOP, 70ns, 3.3V
KM62V256CLTG-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGE-7L	28-TSOP F, 70ns, 3.3V	KM62V256CLTGI-7L	28-TSOP F, 70ns, 3.3V
KM62V256CLTG-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGE-10L	28-TSOP F, 100ns, 3.3V	KM62V256CLTGI-10L	28-TSOP F, 100ns, 3.3V
KM62V256CLRG-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGE-7L	28-TSOP R, 70ns, 3.3V	KM62V256CLRGI-7L	28-TSOP R, 70ns, 3.3V
KM62V256CLRG-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGE-10L	28-TSOP R, 100ns, 3.3V	KM62V256CLRGI-10L	28-TSOP R, 100ns, 3.3V
KM62U256CLG-8L	28-SOP, 85ns, 3.0V	KM62U256CLGE-8L	28-SOP, 85ns, 3.0V	KM62U256CLGI-8L	28-SOP, 85ns, 3.0V
KM62U256CLTG-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGE-8L	28-TSOP F, 85ns, 3.0V	KM62U256CLTGI-8L	28-TSOP F, 85ns, 3.0V
KM62U256CLRG-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGE-8L	28-TSOP R, 85ns, 3.0V	KM62U256CLRGI-8L	28-TSOP R, 85ns, 3.0V
KM62U256CLG-10L	28-SOP, 100ns, 3.0V	KM62U256CLGE-10L	28-SOP, 100ns, 3.0V	KM62U256CLGI-10L	28-SOP, 100ns, 3.0V
KM62U256CLTG-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGE-10L	28-TSOP F, 100ns, 3.0V	KM62U256CLTGI-10L	28-TSOP F, 100ns, 3.0V
KM62U256CLRG-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGE-10L	28-TSOP R, 100ns, 3.0V	KM62U256CLRGI-10L	28-TSOP R, 100ns, 3.0V

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Pd	0.7	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM62V256CL-L, KM62U256CL-L
		-25 to 85	°C	KM62V256CLE-L, KM62U256CLE-L
		-40 to 85	°C	KM62V256CLI-L, KM62U256CLI-L
Soldering temperature and time	Tsolder	260 °C, 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Product	Min	Typ**	Max	Unit
Supply voltage	Vcc	KM62V256C Family	3.0	3.3	3.6	V
		KM62U256C Family	2.7	3.0	3.3	V
Ground	Vss	All	0	0	0	V
Input high voltage	Vih	KM62V256C Family	2.2	-	Vcc+0.3	V
		KM62U256C Family	2.2	-	Vcc+0.3	V
Input low voltage	Vil	KM62V256C Family	-0.3	-	0.4	V
		KM62U256C Family	-0.3***	-	0.4	V

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ¡ Â30ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	6	pF
Input/Output capacitance	Cio	Vio=0V	-	8	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions[1]		Min	Typ [2]	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or Vil or /WE=Vil Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS=Vil, Vin=Vih or Vil, Iio=0mA		-	1.0	2.0	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS¡ Ø0.2V, Vil¡ Ø0.2V, Vin¡ ×Vcc-0.2V, Iio=0mA		-	2.5	5	mA
		Icc2	Min cycle, 100% duty /CS=Vil, Iio=0mA		-	20 [3]	35[4]	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.2	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	0.3	mA
Standby Current (CMOS)	KM62V256CL-L	Isb1	/CS¡ ×Vcc-0.2V Vin¡ Ø0.2V or Vin¡ ×Vcc-0.2V	Low Low PWR	-	1.5	10	uA
	KM62V256CLE-L			Low Low PWR	-	1.5	20	uA
	KM62V256CLI-L			Low Low PWR	-	1.5	20	uA
	KM62U256CL-L			Low Low PWR	-	1.0	10	uA
	KM62U256CLE-L			Low Low PWR	-	1.0	15	uA
	KM62U256CLI-L			Low Low PWR	-	1.0	15	uA

1) - Commercial Product : Ta=0 to 70 °C , Vcc=3.0 +/- 0.3V(62U256C Family), Vcc=3.3 +/- 0.3V(62V256C Family)
- Extended Product : Ta=-25 to 85 °C , Vcc=3.0 +/- 0.3V(62U256CE Family), Vcc=3.3 +/- 0.3V(62V256CE Family)
- Industrial Product : Ta=-40 to 85 °C , Vcc=3.0 +/- 0.3V(62U256CI Family), Vcc=3.3 +/- 0.3V(62V256CI Family)

2) Ta=25 °C

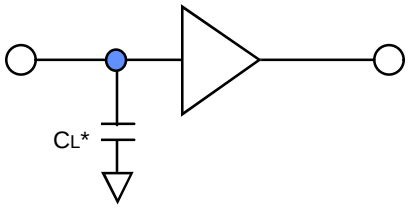
3) 25mA for KM62V256C family

4) 30mA for KM62U256C family but it is not 100% tested but obtained statistically

A.C CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference*)

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	CL=100pF+1TTL	-
	CL=30pF+1TTL	



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics

TEST CONDITIONS (2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM62V256CL-L	0~70 °C	3.3V +/- 0.3	70*/100ns	Commercial
KM62V256CLE-L	-25~85 °C	3.3V +/- 0.3	70*/100ns	Extended
KM62V256CLI-L	-40~85 °C	3.3V +/- 0.3	70*/100ns	Industrial
KM62U256CL-L	0~70 °C	3.0V +/- 0.3	85*/100ns	Commercial
KM62U256CLE-L	-25~85 °C	3.0V +/- 0.3	85*/100ns	Extended
KM62U256CLI-L	-40~85 °C	3.0V +/- 0.3	85*/100ns	Industrial

* all the AC parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

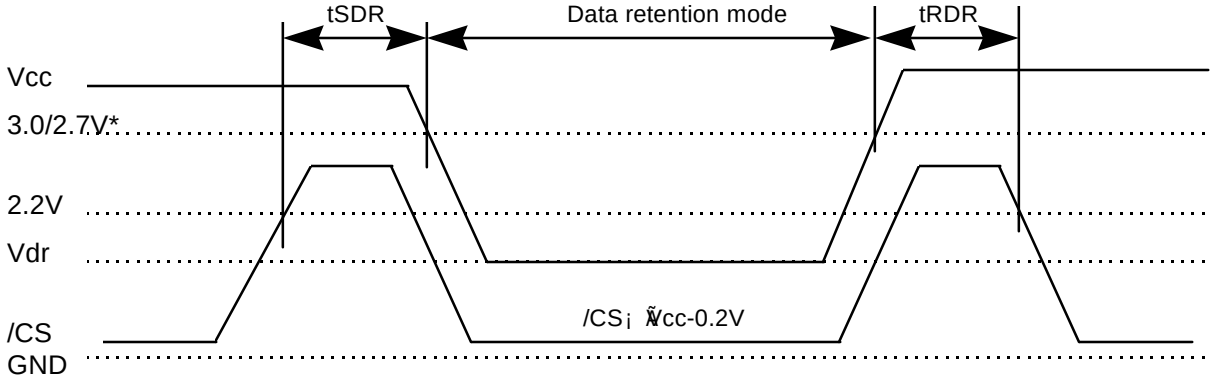
Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	30	0	35	0	35	ns
	Output disable to high-Z output	tOHZ	0	30	0	35	0	35	ns
	Output hold from address change	tOH	5	-	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	70	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	70	-	ns
	Write pulse width	tWP	50	-	60	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	50	-	60	-	60	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	10	-	10	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*	Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS¡ ÃVcc-0.2V	2.0	-	3.6	V
Data retention current	Idr	KM62V256CL-L	Vcc=3.0V	-	1	8	uA
		KM62U256CL-L	/CS¡ ÃVcc-0.2V	-	0.6	8	
		KM62V256CLE-L		-	1	10	
		KM62U256CLE-L		-	0.6	10	
		KM62V256CLI-L		-	1	10	
		KM62U256CLI-L		-	0.6	10	
Data retention set-up time	tSDR		See data retention waveform	0	-	-	ms
Recovery time	tRDR			5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C, unless otherwise specified
2) Extended Product : Ta=-25 to 85 °C, unless otherwise specified
3) Industrial Product : Ta=-40 to 85 °C, unless otherwise specified
** Ta=25 °C

DATA RETENTION TIMING DIAGRAM



* 3.0V for KM62V256C family, 2.7V for KM62U256C family

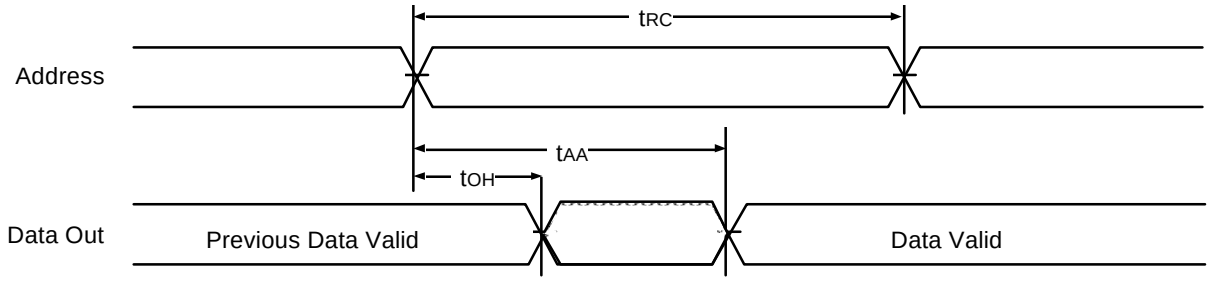
FUNCTIONAL DESCRIPTION

/CS	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

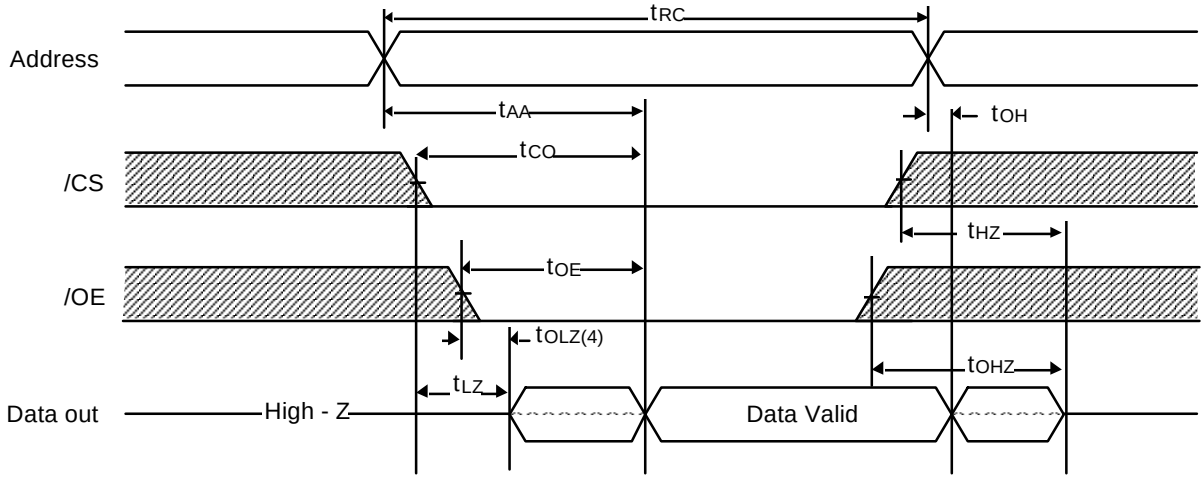
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih)



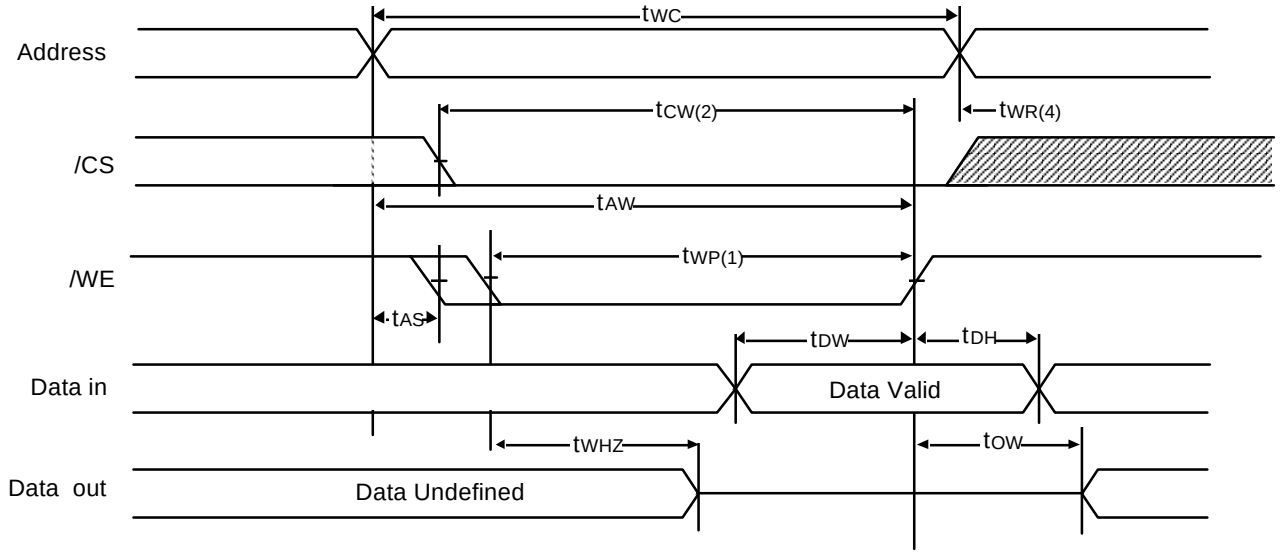
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



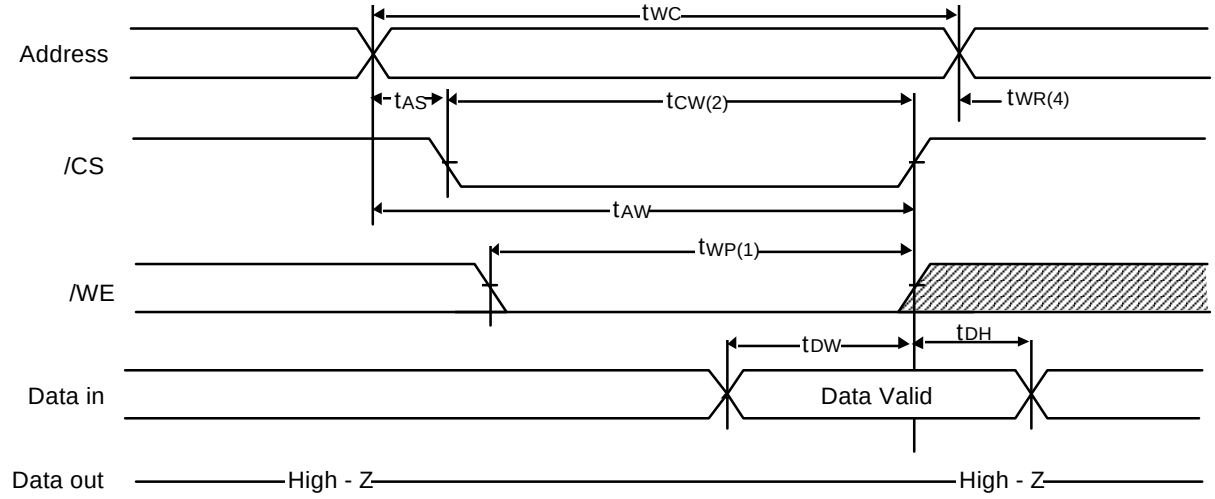
Notes (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ (max.) is less than tLZ(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



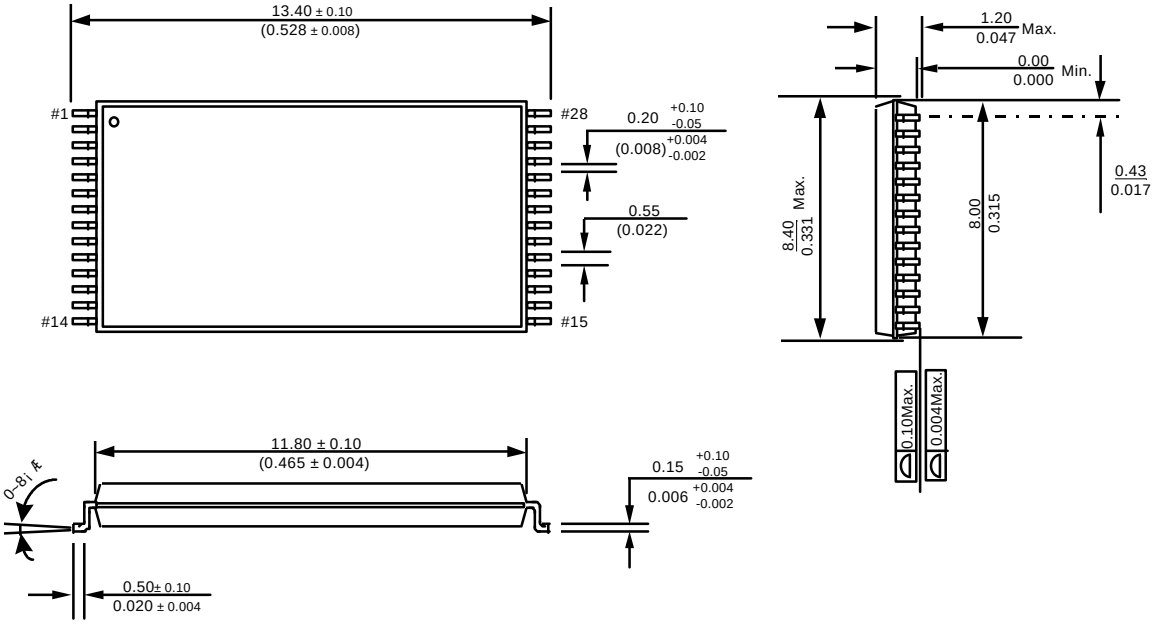
Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CS and low /WE. A write begins at the latest transition among /CS going low and /WE going low : A write end at the earliest transition among /CS going high and /WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS, or /WE going high.

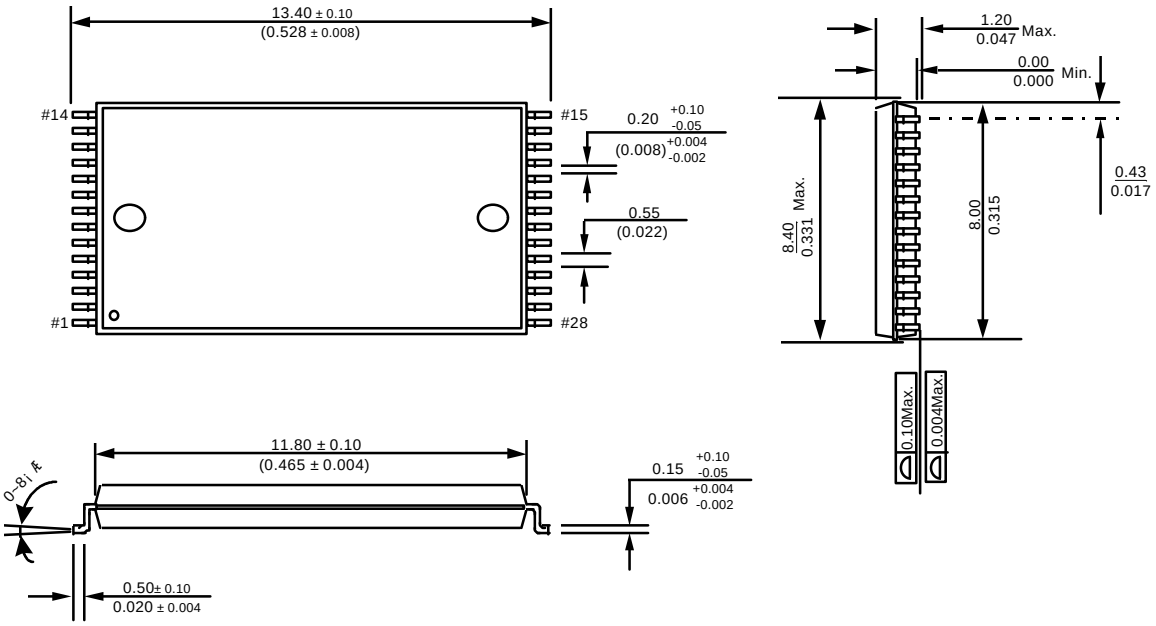
PACKAGE DIMENSION

Unit : Millimeters (Inches)

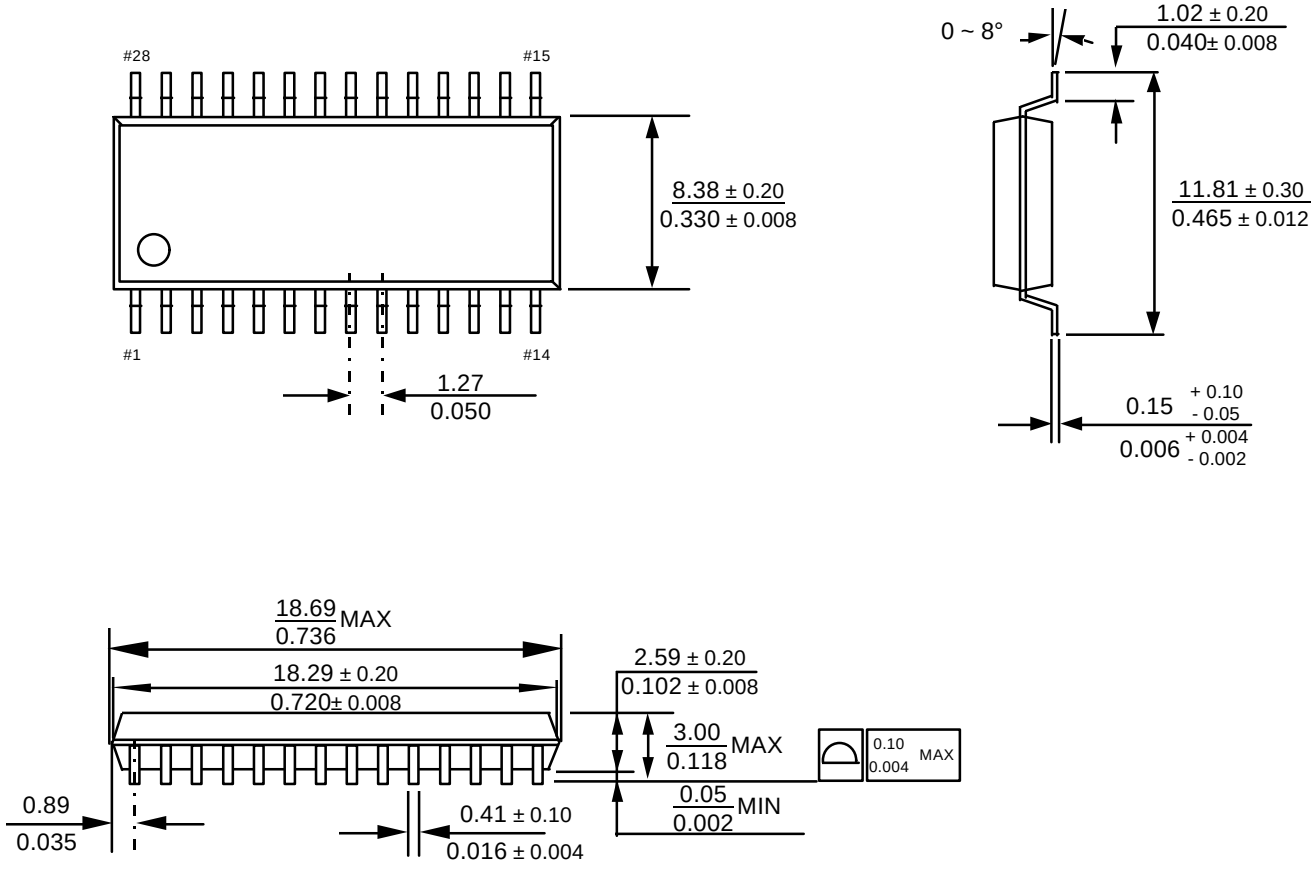
28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



28 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)



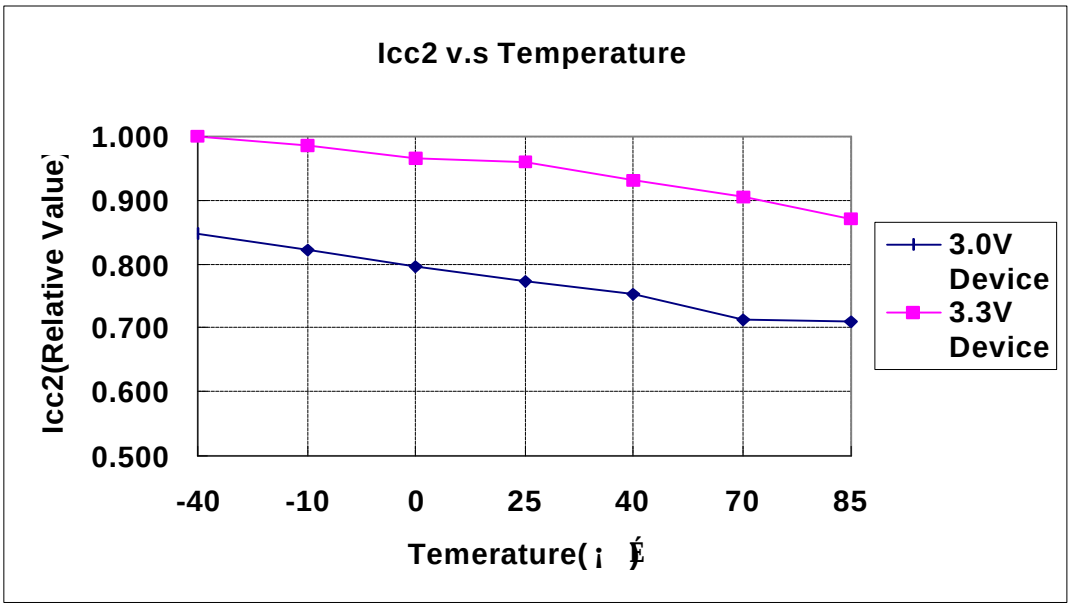
28 PIN PLASTIC SMALL OUTLINE PACKAGE (450mil)



TECHNICAL INFORMATION

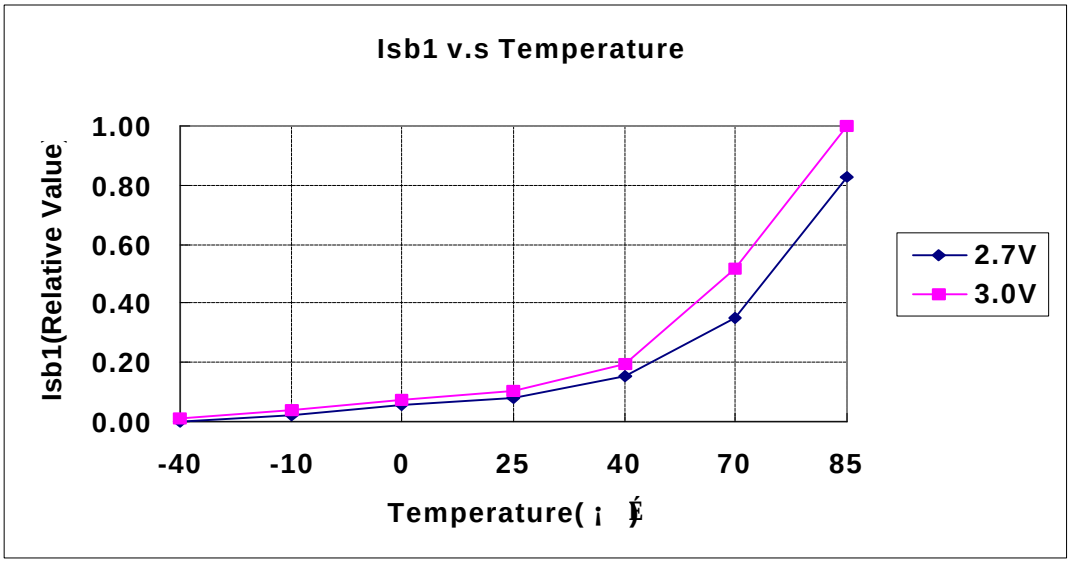
1) Icc2 characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 3.3V Vcc and -40° ctemperature. The basic relative value of Icc2 at that condition is set into 1.



2) Isb1(CMOS Level Standby Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at 3.0V Vcc and 85° ctemperature. The basic relative value of Isb1 at that condition is set into 1.



3) Idr(Data Retention Current) characteristics by temperature variation

All the values in this graph are depicted by the relative value with the maximum value measured at Vdr=3.0V and 85 ctemperature. The basic relative value of Idr at that condition is set into 1.