Contents

LCD Controller-Driver   S-4561A

The S-4561A is a 17-common x 60-segment output character LCD controller-driver with built-in serial and parallel interfaces. The S-4561A incorporates CGROM, making character display possible. Independently of the CPU, display on the LCD panel is executed via the internal oscillating circuit or clock input. The S-4561A has a wide variety of command instructions which minimize the load of the CPU. It also features a wide voltage range, low power consumption, and it is provided with a power save function, making the S-4561A a suitable display device for applications in portable electronics.

■ Features

- Display Area
    5-dot font
        12-column x 2-line (+4 columns)
        24-column x 1-line (+8 columns)
    6-dot font
        10-column x 2-line (+6 columns)
        20-column x 1-line (+12 columns)
        Values in parentheses indicate the number of columns
        outside the display area.
- Icon Display
        60 icons (max.)
        Icons can be displayed on the upper and lower panel.
- Fonts: 5-dot display mode and 6-dot display mode
- Interface
        4-bit, 8-bit high-speed parallel interface (80-/68-Family CPU)
        Serial interface
- Driver Output
        60 segments
        16 commons+ Icon common :
- Character Generator ROM (CGROM)
        9600 bits, 5×8 bits character font, 240 characters
- Character Generator RAM (CGRAM)
        8 character x 5 x 8=320 bits
- Display Data RAM (DDRAM)

        2 lines x 16 characters=2 x 16 x 8=256 bits
        (4 characters are displayed outside the display area)
- Display Clock
        Either internal CR oscillating circuit or external clock input :
        CR oscillation: 34 kHz
                        (Frame Frequency=76.9 Hz)

- Duty Cycle: 1/17
- Internal LCD Drive Bias Voltage Generator
    Internal Bias Resistor :
        Command selection 1/5 or 1/4 bias
    External Bias Resistor :
        Free setting of 1/2 bias or more
- Normal Instructions
        Display Clear, Cursor Home, Display
        ON/OFF, Display Character Blink,
        Cursor Shift, Display Shift, Cursor
        ON/OFF
- Extended Instructions
        Contrast Adjustment, Smooth Scroll
        Control, Icon Control, Icon Blink, Bias
        Resistor Select, Change of Number of
        Display Columns, Power Save, Icon Only
        Display, Booster Drive Frequency Select
- Reset Circuit : Hardware Reset
- Internal Booster : Dual Booster
- Power Supply Voltage Range
        Logic Power :   2.4 V to 5.5 V
        LCD Drive Power : 2.7 V to 6.5 V
- Low Current Consumption :
        Approx. 0 μA (during power save
                operation)
- Delivered on gold bump bare chips,
- Notice that isolation of the IC from light exposure
    is not taken into account for this IC design.
    Be sure to take measures not to expose light to
    the surface, back, or side of the IC in order to
    prevent this IC from malfunctioning.
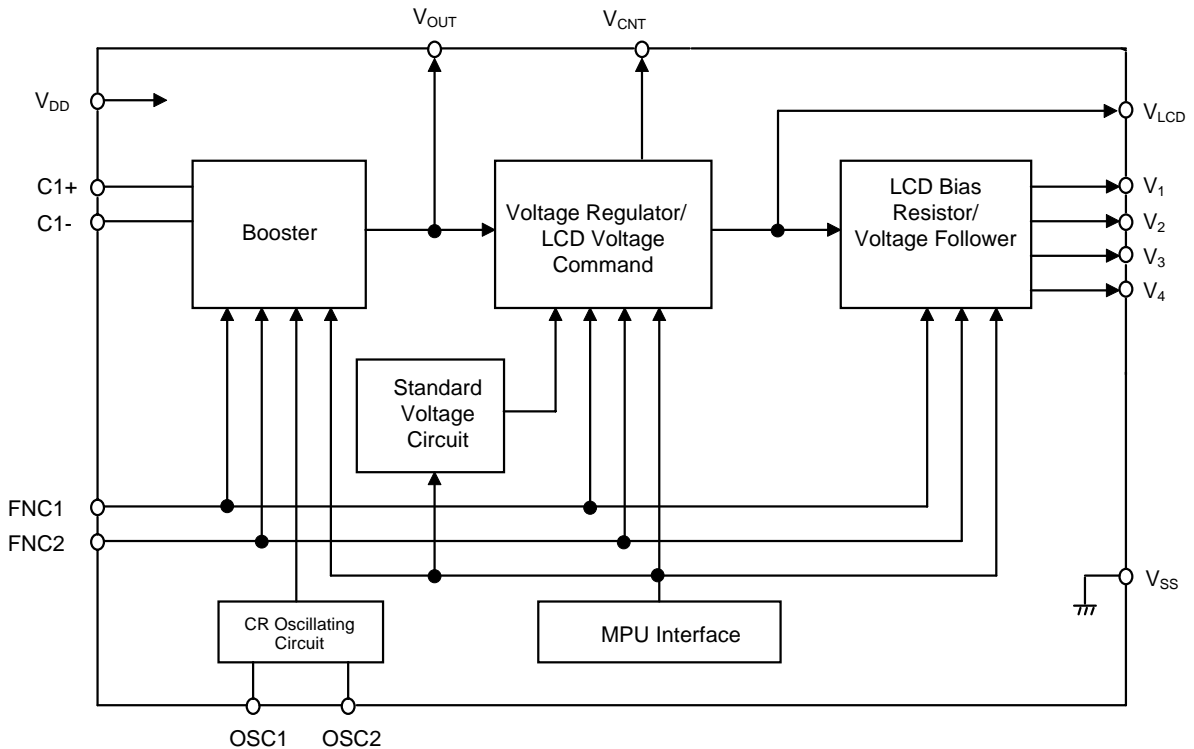
LCD Controller-Driver
S-4561A

■ **Block Diagram**

1. Block Overview
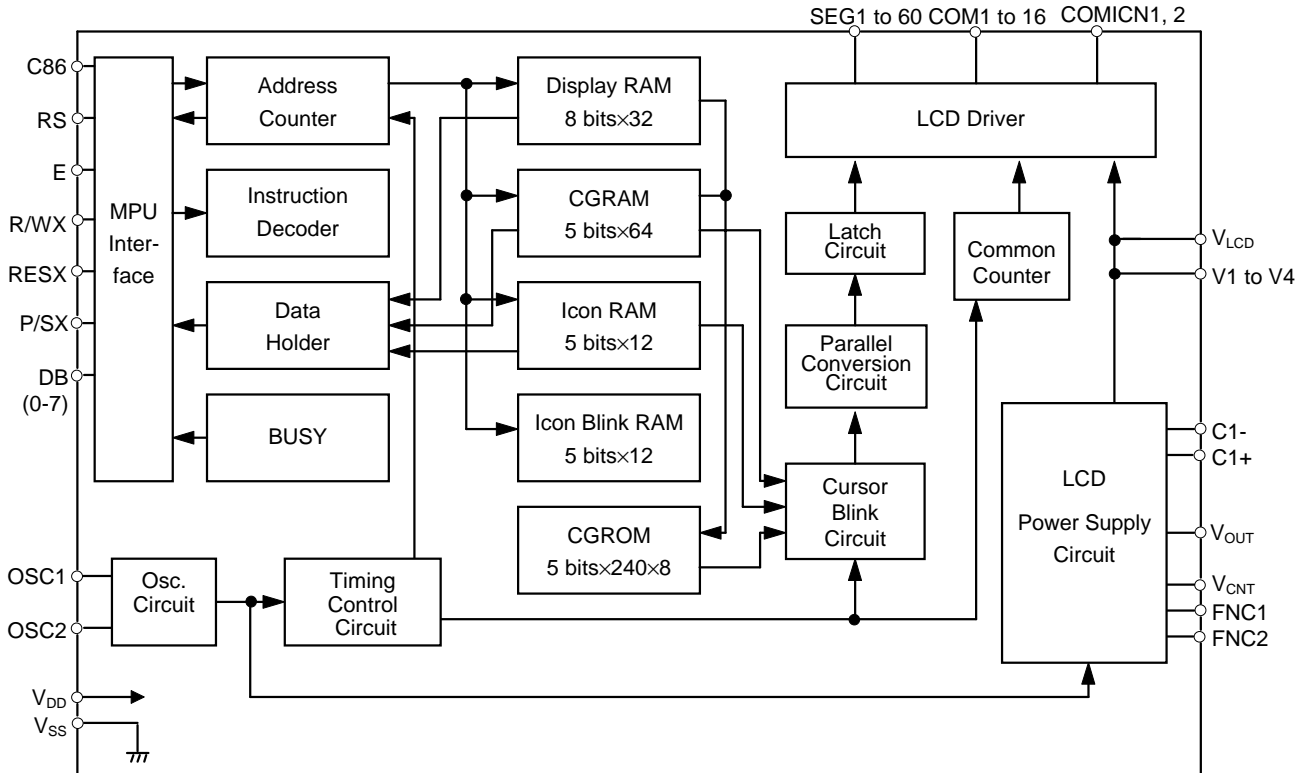
Figure 1 Block Diagram

2. LCD Power Supply Circuit

Figure 2 LCD Power Supply Circuit

Seiko Instruments Inc.

■ Pin Description

1. Logic Power Supply Pins

Table 1 Logic Power Supply Pins

Pin No.	Pin Name	Description
47	V_{SS}	Negative Power Pin: Usually connected to 0 V (GND)
33	V_{DD}	Positive Power Pin: Usually connected to +3 V

2. Control Pins

Table 2 Control Pins

Pin No.	Pin Name	Description

7, 9
11, 13
15, 17
19, 21
	DB0 to DB7	• When an 8-bit parallel interface is selected:
		   8-Bit Parallel Data Bus 3-State Input/Output Pin
		• When a 4-bit parallel interface is selected:
		   DB0 to DB3 : Open
		   DB4 to DB7 : 4-Bit Parallel Data Bus 3-State Input/Output Pins
		• When a serial interface is selected:
		   DB0 : Serial Data Input Pin
		   DB1 : Clock Input Pin
		   DB2 to DB7 : Open

25	R/WX	• When a 4-bit/8-bit parallel interface is selected:
		   68-Family MPU Read/Write Signal Input Pin
		   R/WX="H" : Read
		   R/WX="L" : Write
		   80-Family MPU: Write Signal Input Pin
		   Active "L" Data Bus Input State
		• When a serial interface is selected:
		   High Impedance

27	P/SX	• Parallel/Serial Interface Changeover Pin
		   P/SX="H" : 4-Bit/8-Bit Parallel Interface
		   P/SX="L" : Serial Interface

29	RS	• When 4-bit/8-bit parallel interface is selected:
		   Register Select Signal Input Pin
		   RS="0" : Instruction Register Write
		            Each Address Counter Read
		            BUSY Flag Read
		   RS="1" : Data Register Write/Read
		• When a serial interface is selected:
		   RS="0" : Instruction Register Write
		   RS="1" : Data Register Write

31	E	• When a 4-bit/8-it parallel interface is selected:
		   68-Family MPU Enable Clock Signal Input Pin
		   Active "H"
		   80-Family MPU Read Signal Input Pin
		   Active "L" Data Bus Output State
		• When a serial interface is selected:
		   Chip-Select Input Pin
		   E= "L" : Active

23	RESX	• Reset Input Pin
		   Active "L"
		   Internal Pullup Register

39	C86	• When 4-bit/8-bit parallel interface is selected:
		   C86="H".................... 68-Family Interface
		   C86="L" .... 80-Family Interface
		• When a serial interface is selected:
		   Don't care.

3. CR Oscillating Circuit Input/Output Pins

Table 3 CR Oscillating Circuit Input/Output Pins

Pin No.	Pin Name	Description
5	OSC2	CR Oscillating Circuit Output Pin: Connects oscillating resistor Rf; while an external clock is being used, "Open."
3	OSC1	CR Oscillating Circuit Input Pin: Connects oscillating resistor Rf; An external clock can be input.

4. LCD Drive Voltage Pins

Table 4 LCD Drive Voltage Pins

Pin No.	Pin Name	Description
35	FNC2	LCD Power Circuit Operation Control Pin 2
37	FNC1	LCD Power Circuit Operation Control Pin 1
49	VOUT	Booster Drive Voltage Output Pin
51	C1-	1st Boosting Negative Side Connection Pin
53	C1+	1st Boosting Positive Side Connection Pin
59	VCNT	LCD Power Supply Voltage Control Pin
65	V_{LCD}	LCD Drive Voltage Input/Output Pin
67	V1	LCD Drive Bias Voltage Pin. While an internal LCD power supply circuit is being used, outputs the LCD drive bias voltage.
69	V2	$\qquad$ 1/4-Bias $\qquad$ 1/5-Bias V1 $\quad 3/4 \times V_{LCD} \quad 4/5 \times V_{LCD}$ V2 $\quad 2/4 \times V_{LCD} \quad 3/5 \times V_{LCD}$
71	V3	V3 $\quad 2/4 \times V_{LCD} \quad 2/5 \times V_{LCD}$ V4 $\quad 1/4 \times V_{LCD} \quad 1/5 \times V_{LCD}$ While an external LCD power supply circuit is being used, inputs the LCD drive bias voltage.
73	V4	$V_{LCD} \geq$ V1, V2, V3, V4 $\geq$ VSS $V_{LCD} \geq V_{DD}$

5. Driver Output Pins

Table 5 Driver Output Pins

Pin No.	Pin Name	Description
91 to 150	SEG1 to SEG60	Segment Drive Output Pins
76 to 83 159 to 166	COM1 to COM16	Common Drive Output Pins
75	COMICN1	Common Drive Output Pins for Icon
158	COMICN2	COMICN1 and 2 output the same phase waveform.

6. Other Pins

Table 6 Logic Power Supply Pins

Pin No.	Pin Name	Description
—	Dummy	Dummy Pin Insulated from the inside of the IC.
45	TEST0	Pins for IC delivery inspection:
43	TEST1	Cannot be wired to the outside.
41	TEST2	When in actual use, "Open."
57	TEST3	
63	TEST4	

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■ **Pad Assignment**

Gold bump size
70 x 94 μm
Pad pitch
100 μm

Chip Identification Mark
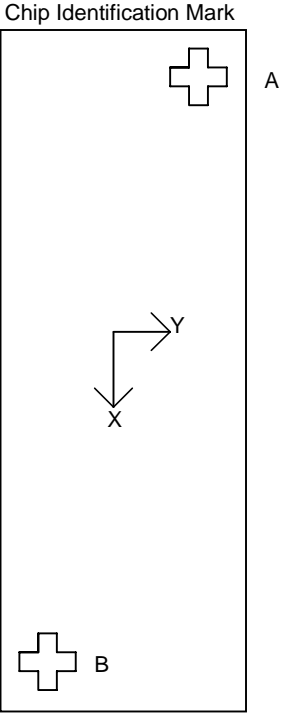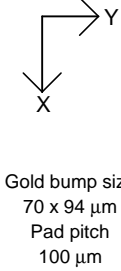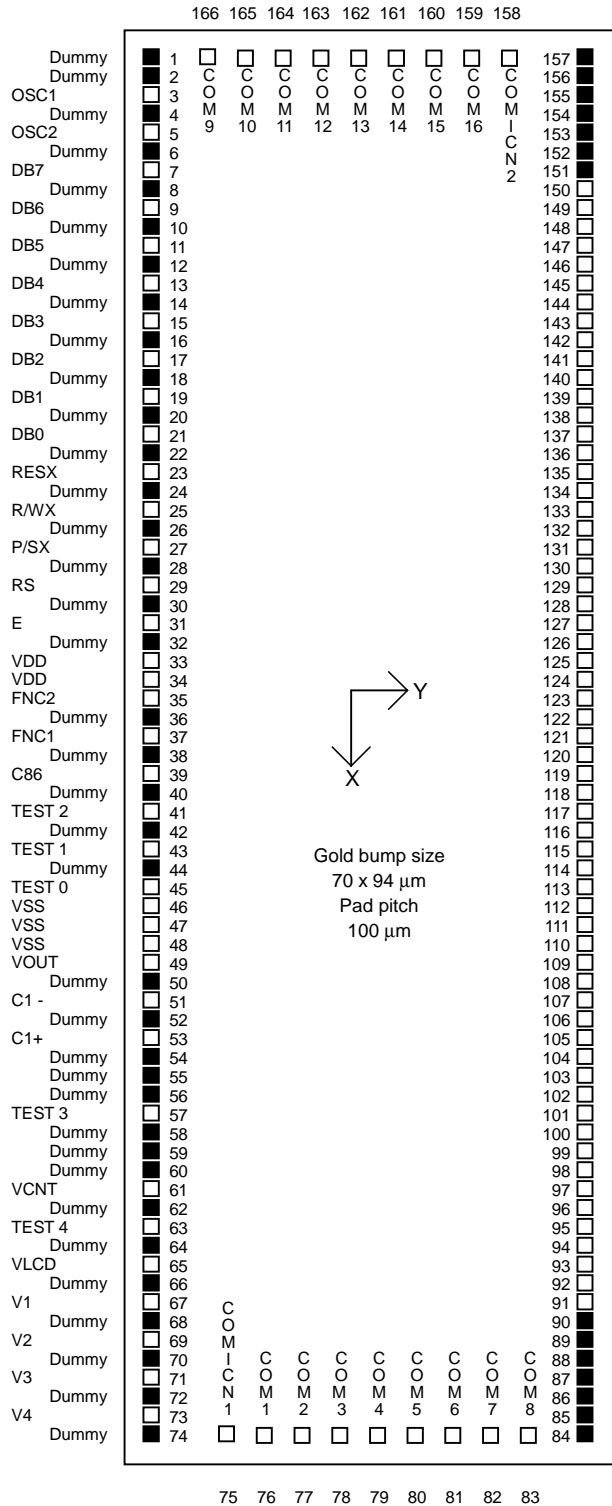
(The identification marks are larger than the actual scaling.)

(-3660, 625)

0.056   0.168   A

0.168

(3669, -590)

0.05   0.15   B

0.15
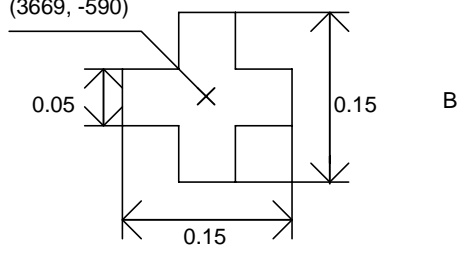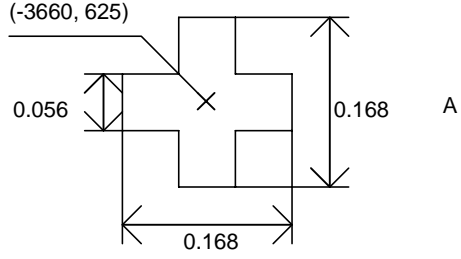
- Chip size: 7.65 × 2.00 mm
- Gold bump size: 70 × 94 μm
- Gold bump height: 22 ± 7 μm
- Pad pitch   100 μm
- Chip thickness: 400 ± 30 μm

■ **Pad Coordinates**

No.	Symbol	X	Y	No.	Symbol	X	Y	No.	Symbol	X	Y
1	Dummy	-3700.5	-863.5	57	TEST3	1950	-863.5	113	SEG23	750	863.5
2	Dummy	-3550	-863.5	58	Dummy	2050	-863.5	114	SEG24	650	863.5
3	OSC1	-3450	-863.5	59	Dummy	2150	-863.5	115	SEG25	550	863.5
4	Dummy	-3350	-863.5	60	Dummy	2250	-863.5	116	SEG26	450	863.5
5	OSC2	-3250	-863.5	61	VCNT	2350	-863.5	117	SEG27	350	863.5
6	Dummy	-3150	-863.5	62	Dummy	2450	-863.5	118	SEG28	250	863.5
7	DB7	-3050	-863.5	63	TEST4	2550	-863.5	119	SEG29	150	863.5
8	Dummy	-2950	-863.5	64	Dummy	2650	-863.5	120	SEG30	50	863.5
9	DB6	-2850	-863.5	65	VLCD	2750	-863.5	121	SEG31	-50	863.5
10	Dummy	-2750	-863.5	66	Dummy	2850	-863.5	122	SEG32	-150	863.5
11	DB5	-2650	-863.5	67	V1	2950	-863.5	123	SEG33	-250	863.5
12	Dummy	-2550	-863.5	68	Dummy	3050	-863.5	124	SEG34	-350	863.5
13	DB4	-2450	-863.5	69	V2	3150	-863.5	125	SEG35	-450	863.5
14	Dummy	-2350	-863.5	70	Dummy	3250	-863.5	126	SEG36	-550	863.5
15	DB3	-2250	-863.5	71	V3	3350	-863.5	127	SEG37	-650	863.5
16	Dummy	-2150	-863.5	72	Dummy	3450	-863.5	128	SEG38	-750	863.5
17	DB2	-2050	-863.5	73	V4	3550	-863.5	129	SEG39	-850	863.5
18	Dummy	-1950	-863.5	74	Dummy	3700.5	-863.5	130	SEG40	-950	863.5
19	DB1	-1850	-863.5	75	COMICN1	3688.5	-400	131	SEG41	-1050	863.5
20	Dummy	-1750	-863.5	76	COM1	3688.5	-300	132	SEG42	-1150	863.5
21	DB0	-1650	-863.5	77	COM2	3688.5	-200	133	SEG43	-1250	863.5
22	Dummy	-1550	-863.5	78	COM3	3688.5	-100	134	SEG44	-1350	863.5
23	RESX	-1450	-863.5	79	COM4	3688.5	0	135	SEG45	-1450	863.5
24	Dummy	-1350	-863.5	80	COM5	3688.5	100	136	SEG46	-1550	863.5
25	R/WX	-1250	-863.5	81	COM6	3688.5	200	137	SEG47	-1650	863.5
26	Dummy	-1150	-863.5	82	COM7	3688.5	300	138	SEG48	-1750	863.5
27	P/SX	-1050	-863.5	83	COM8	3688.5	400	139	SEG49	-1850	863.5
28	Dummy	-950	-863.5	84	Dummy	3700.5	863.5	140	SEG50	-1950	863.5
29	RS	-850	-863.5	85	Dummy	3550	863.5	141	SEG51	-2050	863.5
30	Dummy	-750	-863.5	86	Dummy	3450	863.5	142	SEG52	-2150	863.5
31	E	-650	-863.5	87	Dummy	3350	863.5	143	SEG53	-2250	863.5
32	Dummy	-550	-863.5	88	Dummy	3250	863.5	144	SEG54	-2350	863.5
33	VDD	-450	-863.5	89	Dummy	3150	863.5	145	SEG55	-2450	863.5
34	VDD	-350	-863.5	90	Dummy	3050	863.5	146	SEG56	-2550	863.5
35	FNC2	-250	-863.5	91	SEG1	2950	863.5	147	SEG57	-2650	863.5
36	Dummy	-150	-863.5	92	SEG2	2850	863.5	148	SEG58	-2750	863.5
37	FNC1	-50	-863.5	93	SEG3	2750	863.5	149	SEG59	-2850	863.5
38	Dummy	50	-863.5	94	SEG4	2650	863.5	150	SEG60	-2950	863.5
39	C86	150	-863.5	95	SEG5	2550	863.5	151	Dummy	-3050	863.5
40	Dummy	250	-863.5	96	SEG6	2450	863.5	152	Dummy	-3150	863.5
41	TEST2	350	-863.5	97	SEG7	2350	863.5	153	Dummy	-3250	863.5
42	Dummy	450	-863.5	98	SEG8	2250	863.5	154	Dummy	-3350	863.5
43	TEST1	550	-863.5	99	SEG9	2150	863.5	155	Dummy	-3450	863.5
44	Dummy	650	-863.5	100	SEG10	2050	863.5	156	Dummy	-3550	863.5
45	TEST0	750	-863.5	101	SEG11	1950	863.5	157	Dummy	-3700.5	863.5
46	VSS	850	-863.5	102	SEG12	1850	863.5	158	COMICN2	-3688.5	400
47	VSS	950	-863.5	103	SEG13	1750	863.5	159	COM16	-3688.5	300
48	VSS	1050	-863.5	104	SEG14	1650	863.5	160	COM15	-3688.5	200
49	VOUT	1150	-863.5	105	SEG15	1550	863.5	161	COM14	-3688.5	100
50	Dummy	1250	-863.5	106	SEG16	1450	863.5	162	COM13	-3688.5	0
51	C1-	1350	-863.5	107	SEG17	1350	863.5	163	COM12	-3688.5	-100
52	Dummy	1450	-863.5	108	SEG18	1250	863.5	164	COM11	-3688.5	-200
53	C1+	1550	-863.5	109	SEG19	1150	863.5	165	COM10	-3688.5	-300
54	Dummy	1650	-863.5	110	SEG20	1050	863.5	166	COM9	-3688.5	-400
55	Dummy	1750	-863.5	111	SEG21	950	863.5				
56	Dummy	1850	-863.5	112	SEG22	850	863.5				

Table 8 Chip Identification Mark Coordinates

Chip Identification Mark	X-Coordinates	Y-Coordinates
A	- 3660	625
B	3669	- 590

■ Function Explanation

1. Interface

Serial and parallel interfaces are built in. Either one can be selected by changing over the P/SX terminal. The parallel interface can respond to both 4- and 8-bit parallel data transmission. Namely, data is transmitted once in the 8-bit interface or twice in the 4-bit interface. The CPU interfaces with respective instruction codes and several kinds of data via the instruction decoder and the data holder.

Data is read from each memory via the data holder. Through the ADDRESS SETTING Command, the contents of the memory are read once into the data holder, and are output through the next READ command. Then, the next data is read into the data holder.

Parallel and serial interfaces execute and finish all instructions within the Enable or Clock cycle specified in accordance with timing characteristics. Because the "BUSY" state is cleared within the cycle time, instructions can be executed in succession without confirming the "BUSY."

1.1 Parallel Interface

The parallel interface is engaged when the P/SX terminal is "H." Connect and fix the P/SX terminal to VDD.

Table 9 Interface

Pin Name	C86=0: 80-Family MPU	C86=1: 68-Family MPU
RS	RS	RS
E	$\overline{RD}$	E
R/WX	$\overline{WR}$	R/WX
DB(7:0)	DB(7:0)	DB(7:0)

[Example: 8-Bit Length Parallel Interface] (68-Family CPU)
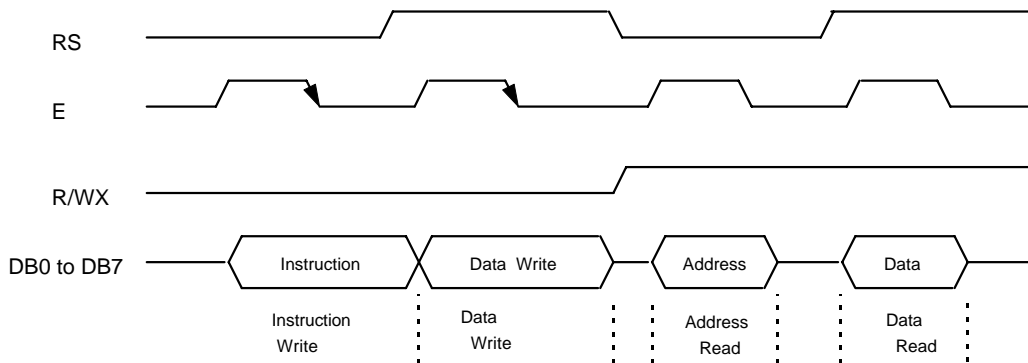
Figure 3 8-Bit Length Parallel Interface (68-Family CPU)

[Example: 8-Bit Length Parallel Interface] (80-Family CPU)
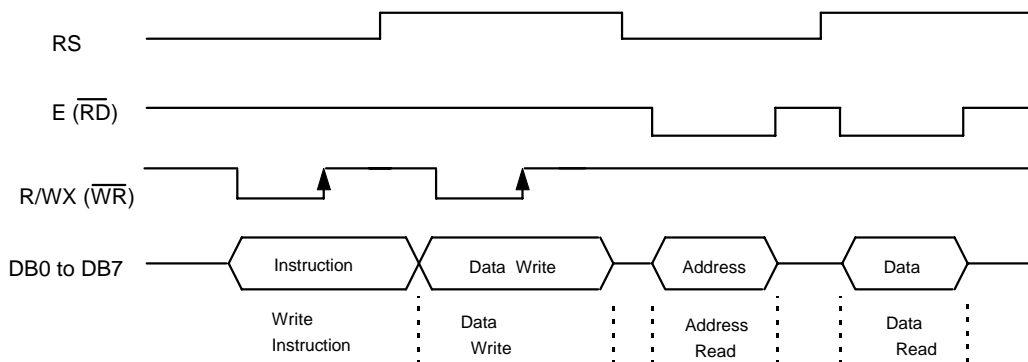
Figure 4 8-Bit Length Parallel Interface (80-Family CPU)

[Example: 4-Bit Length Parallel Interface] (68-Family CPU)
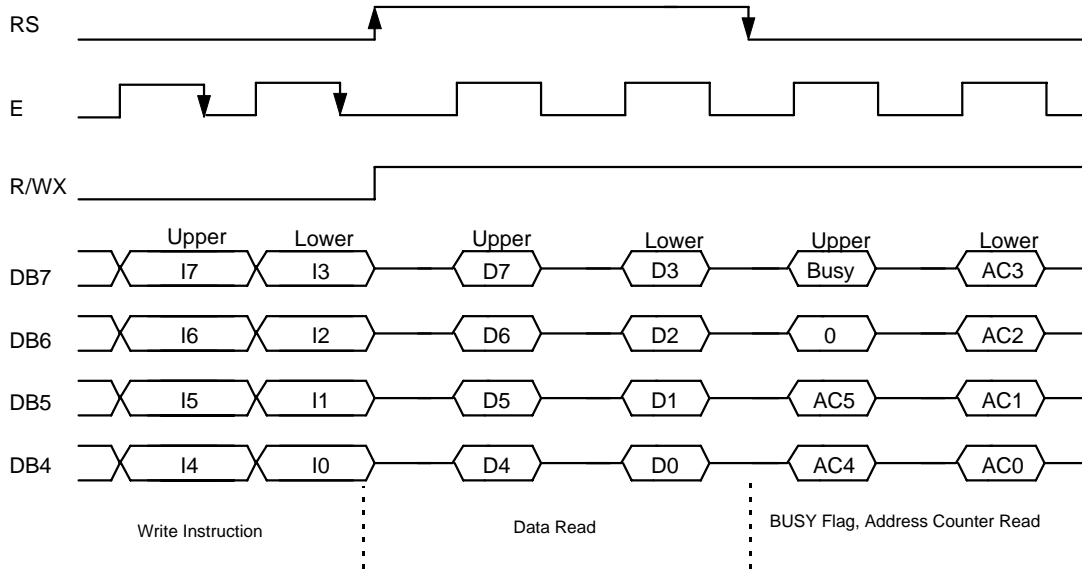
Figure 5 4-Bit Length Parallel Interface (68-Family CPU)

[Example: 4-Bit Length Parallel Interface] (80-Family CPU)
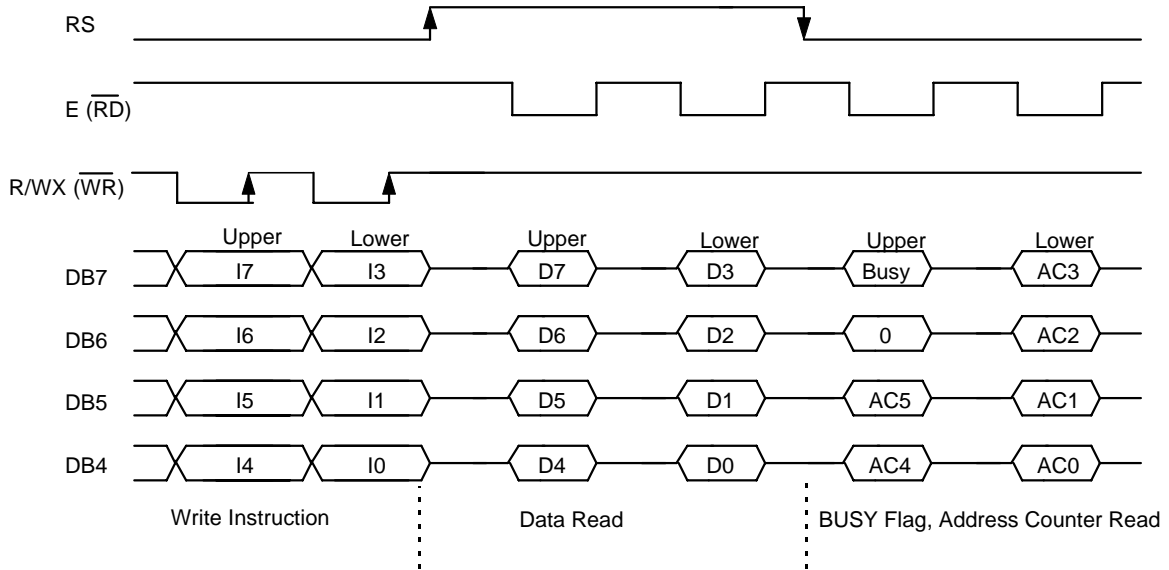
Remarks: • In case of a 4-bit length interface, data is transmitted through the four buses DB4 to DB7 (buses DB0 to DB3 are not used. Set DB0 to DB3 "Open").
• The data transmission to the CPU is completed by transmitting 4-bit data twice. The data transmission is executed in the order from upper 4 bits to lower 4 bits. The upper 4 bits of data immediately after the output level of the RS pin changes are transmitted. Leave the RS pin unchanged until lower bits finish the data transmission.

1.2 Serial Interface

Serial interface is engaged when the P/SX terminal is "L." The instruction code is read at the rising edge of the serial clock (SCLK). Serial data is input in numerical order from DB0 to DB7. The instruction code is the same as that for the parallel data. Connect and fix the P/SX terminal to VSS. Connect pins DB2 through DB7, R/WX, and C86 to "OPEN."

P/SX:	"L" Serial Interface Operation/Fix to V_{SS}.
RS:	Write in the "L" Instruction Register.
	Write in the "H" Data Register.
E:	"L" Active
DB0:	Serial Data Input Pin (SDI)
DB1:	Serial Clock Input Pin (SCLK)
DB2 to DB7:	OPEN
R/WX:	OPEN
C86:	OPEN
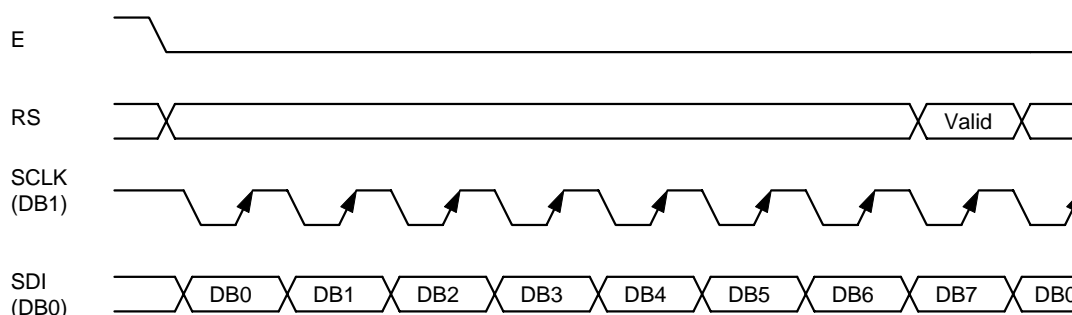
Figure 7 Serial Interface

Table 10 Serial Interface

E	RS	Operation
L	L	Write/Input to Instruction Register
L	H	Write to Data Register
H	L	——
H	H	——

Taking into consideration external or reflective noises, optimize the serial clock wiring. Always check operations after mounting the IC on your device.

2. Busy

When the BUSY flag points "1," it shows that an instruction is being executed. The BUSY flag is read to DB7 by the ADDRESS READ command. In case of commands other than the RESET or the DISPLAY CLEAR, there is no need for confirming the BUSY flag. This is because that the instruction is completed within the cycle time specified in accordance with the timing characteristics. After confirming that BUSY flag points "0" during RESET or DISPLAY CLEAR operation or after the specified wait time, write the next command. When the BUSY flag points "1," any command other than the ADDRESS READ cannot be accepted.
When a serial interface is selected, the BUSY READ is not available.

3. Address Counter

The Address Counter (AC) gives respective addresses for DDRAM, CGRAM, ICONRAM or ICON BLINK RAM according to the contents of the AC. Only one RAM among the four kinds of RAMs is selected by the RAM ADDRESS SETTING command. After the ADDRESS SETTING command is executed, the display data can be read and written in the selected RAM. The contents of the RAM AC, where the ADDRESS READ command, is also selected are read. Increment and decrement of the AC are automatically executed after the READ or WRITE command is executed. Once an address is set, READ and WRITE commands can be input in succession.

4. Display Data RAM (DDRAM)

The display data RAM (DDRAM) holds the display data as an 8-bit character code.   The DDRAM responds to 32 characters 00H to 1EH and has a capacity of 32×8=256 bits. When any character code is written in the DDRAM, a character which corresponds to the character code appears on the LCD panel.   As the figure shows, the DDRAM is provided with a non-displayed character area as well as a normally-displayed character area.   The non-displayed character area is shifted to the display area by the DISPLAY SHIFT or SMOOTH SCROLL command.

Addresses in the DDRAM are assigned to 5 bits DB0 to DB4 by the DDRAM ADDRESS SETTING command.

The 8-bit character code corresponds to characters stored in the CGROM.

Table 11 Display Data

	DB4	DB3	DB2	DB1	DB0
Address Counter	AC4	AC3	AC2	AC1	AC0
Example of (1D)H	1	1	1	0	1

5. Character Generator ROM (CGROM)

The character generator ROM (CGROM) generates 5 x 8-dot character patterns from the 8-bit character code.   The CGROM holds 9600 bits which correspond to 240 character character patterns.   Character codes of the Character Code List are assigned from "0001   0000" to "1111 1111."

6. Character Generator RAM (CGRAM)

The character generator RAM (CGRAM) holds character patterns of 5×8 dots per character, in which users can freely write. The CGRAM holds 8 characters×5×8 dots=320 bits.

The character patterns are written for every 5 bits DB0 to DB4 by setting the address by the CGRAM ADDRESS SETTING command.   The CGRAM address consists of upper 3 bits and lower 3 bits.

The written character patterns are assigned as the 8-bit character code from "0000 *000" to "0000 *111" (* : don't care) of the CGRAM.   The upper 3 bits of the CGRAM address corresponds to the lower 3 bits of the character code, and also corresponds to the far-left character code in the "Character Code List."   The contents written in the CGRAM are displayed when the respective character codes are written in the DDRAM.

7. Icon Display RAM (ICONRAM)

The icon display RAM (ICONRAM) stores data being lit on the icon display.   The ICONRAM holds 60 bits corresponding to 60 marks.   Data is output to SEG1 to 60 in accordance with LCD drive outputs COMICN1 and 2.

To light the icon, write "1" in the ICONRAM.   With data being lit on the icon display, write it using 5 bits DB0 to DB4 after executing the ICONRAM ADDRESS SETTING command.   For example, to light the icon at SEG31, input icon lighting data "***1 0000" after setting the ICONRAM address to "0110."

8. Icon Display Blink RAM (ICON BLINK RAM)

The icon display blink RAM (ICON BLINK RAM) stores individual icons with respect to their necessity of blinking.   The ICON BLINK RAM holds 60 bits the same as the ICON RAM, and its bit map corresponding to the segment drive output is in accordance with the ICONRAM.   For example, to blink the icon corresponding to SEG31, input the icon blink data "***1 0000" after setting the ICON BLINK RAM address to "0110." However, it is necessary to write "1" in the ICONRAM in advance.

[1-line x 24-character display]

Set to the 1-line x 24-character display mode.

● Without Display Shift ── COM1 to COM8 ── ── COM9 to COM16 ──

Display Locations — 1st line

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Non-Displayed Character								DDRAM Address
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	

● Display Left Shift

Display Locations — 1st line

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Non-Displayed Character								DDRAM Address
01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	00	

● Display Right Shift

Display Locations — 1st line

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Non-Displayed Character								DDRAM Address
1F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	

Figure 8   DDRAM Addresses and Display Locations (1-line x 24-character display)

[2-line x 12-character display]

● Without Display Shift ── COM1 to COM16 ──

Display Locations

	1	2	3	4	5	6	7	8	9	10	11	12	Non-Displayed Character				
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DDRAM Address
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	

● Display Left Shift

Display Locations

	1	2	3	4	5	6	7	8	9	10	11	12	Non-Displayed Character				
1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00	DDRAM Address
2nd line	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	

● Display Right Shift

Display Locations

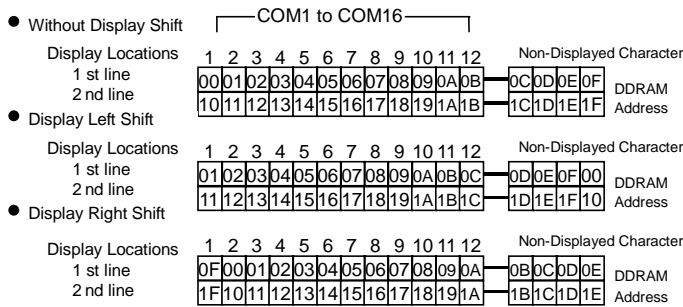|	1	2	3	4	5	6	7	8	9	10	11	12	Non-Displayed Character				
1st line	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DDRAM Address
2nd line	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	

Figure 9   DDRAM Addresses and Display Locations (2-line x 12-character display)

Table 11 Relationship between CGRAM Addresses/Character Codes and Character Patterns

Character Code List Address Upper	Lower	CGRAM Address A5 A4 A3	A2 A1 A0	Write Character Patterns D7 D6 D5 D4	D3 D2 D1 D0
0 0 0 0 0	0 0 0	0 0 0	0 0 0	* * * 0	1 1 1 0
		0 0 0	0 0 1	* * * 1	0 0 0 1
		0 0 0	0 1 0	* * * 1	0 0 0 0
		0 0 0	0 1 1	* * * 0	1 1 1 0
		0 0 0	1 0 0	* * * 0	0 0 0 1
		0 0 0	1 0 1	* * * 1	0 0 0 1
		0 0 0	1 1 0	* * * 0	1 1 1 0
		0 0 0	1 1 1	* * * 0	0 0 0 0
0 0 0 0 0	0 0 1	0 0 1	0 0 0	* * * 0	1 1 1 0
		0 0 1	0 0 1	* * * 0	0 1 0 0
		0 0 1	0 1 0	* * * 0	0 1 0 0
		0 0 1	0 1 1	* * * 0	0 1 0 0
		0 0 1	1 0 0	* * * 0	0 1 0 0
		0 0 1	1 0 1	* * * 0	0 1 0 0
		0 0 1	1 1 0	* * * 0	1 1 1 0
		0 0 1	1 1 1	* * * 0	0 0 0 0
• • •		• • •		• • •	
0 0 0 0 0	1 1 1	1 1 1	0 0 0	* * * 0	1 1 1 0
		1 1 1	0 0 1	* * * 0	0 1 0 0
		1 1 1	0 1 0	* * * 0	0 1 0 0
		1 1 1	0 1 1	* * * 0	0 1 0 0
		1 1 1	1 0 0	* * * 0	0 1 0 0
		1 1 1	1 0 1	* * * 0	0 1 0 0
		1 1 1	1 1 0	* * * 0	1 1 1 0
		1 1 1	1 1 1	* * * 0	0 0 0 0

Remarks • The lower 3 bits of the Character Code List correspond to the upper 3 bits (A5 A4 A3) of the CGRAM.

• The lower 3 bits (A2 A1 A0) of the CGRAM correspond to the respective lines of the character patterns.

• The 8th line of the character pattern is the cursor position. By turning the cursor display ON, thelogic sum of the cursor and the character pattern is displayed. The upper 3 bits (D7 D6 D5) are ignored.

Table 12 ICONRAM Address and Segment Drive Output Drive Bit Map

ICONRAM Address				Icon Display Data and SEG Output							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	*	*	*	S1	S2	S3	S4	S5
0	0	0	1	*	*	*	S6	S7	S8	S9	S10
0	0	1	0	*	*	*	S11	S12	S13	S14	S15
0	0	1	1	*	*	*	S16	S17	S18	S19	S20
0	1	0	0	*	*	*	S21	S22	S23	S24	S25
0	1	0	1	*	*	*	S26	S27	S28	S29	S30
0	1	1	0	*	*	*	S31	S32	S33	S34	S35
0	1	1	1	*	*	*	S36	S37	S38	S39	S40
1	0	0	0	*	*	*	S41	S42	S43	S44	S45
1	0	0	1	*	*	*	S46	S47	S48	S49	S50
1	0	1	0	*	*	*	S51	S52	S53	S54	S55
1	0	1	1	*	*	*	S56	S57	S58	S59	S60
1	1	0	0	*	*	*	*	*	*	*	*
1	1	0	1	*	*	*	*	*	*	*	*
1	1	1	0	*	*	*	*	*	*	*	*
1	1	1	1	*	*	*	*	*	*	*	*

Remarks • S1 to S60 correspond to segment drive output pins SEG1 to SEG60.

Table 13 ICON BLINK RAM Address and Segment Drive Output Drive Bit Map

ICON Blink RAM Address				ICON Blink Display Data and SEG Output							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	*	*	*	S1	S2	S3	S4	S5
0	0	0	1	*	*	*	S6	S7	S8	S9	S10
0	0	1	0	*	*	*	S11	S12	S13	S14	S15
0	0	1	1	*	*	*	S16	S17	S18	S19	S20
0	1	0	0	*	*	*	S21	S22	S23	S24	S25
0	1	0	1	*	*	*	S26	S27	S28	S29	S30
0	1	1	0	*	*	*	S31	S32	S33	S34	S35
0	1	1	1	*	*	*	S36	S37	S38	S39	S40
1	0	0	0	*	*	*	S41	S42	S43	S44	S45
1	0	0	1	*	*	*	S46	S47	S48	S49	S50
1	0	1	0	*	*	*	S51	S52	S53	S54	S55
1	0	1	1	*	*	*	S56	S57	S58	S59	S60
1	1	0	0	*	*	*	*	*	*	*	*
1	1	0	1	*	*	*	*	*	*	*	*
1	1	1	0	*	*	*	*	*	*	*	*
1	1	1	1	*	*	*	*	*	*	*	*

Remark: S1 to S60 correspond to segment drive output pins SEG1 to SEG60.

9. Cursor Blink Controller

Controls the cursor display as well as the blink display (Character Blink Display).   Displays and blinks the character indicated by the DDRAM address counter. To change the cursor or blink display position, execute the DDRAM SETTING ADDRESS command or the DATA WRITE command.   The cursor display and the blink display positions are not changed by executing the CGRAM, ICONRAM or ICON BLINK RAM ADDRESS command or executing data write. The cursor is displayed on the 8th line of the character font of a 5-bit length, and with the logic sum of the CGROM character patterns. The blink display comes in four types and can be set by the BLINK SELECT command. Refer to "Instruction Description" (page 25 of this specification).

10. CR Oscillating Circuit

Generates a basic clock that serves as display timing.
The oscillating frequency can be reduced to fosc=approx. 34 kHz via an oscillating resistor (Rf=500 kΩ).
By inputting the external clock in OSC1, operation through the external clock is possible. In this case, set OSC2 to "Open."

Duty	Rf	fosc	Frame Frequency
1/17 Duty	500 kΩ	34 kHz	76.9 Hz

$$\text{Frame Frequency} \quad \frac{fosc}{2\times13\times17} \quad [Hz]$$

11. LCD Driver

Has 16 common output pins, two ICON common output pins, and 60 segment output pins for driving the LCD, and generates 2-frame AC drive waveform (type B). Two ICON common output pins, each of which is configured orgthogonally to the chip, generate the drive waveform at the same timing. The ICON display can be configured over and under the top and the bottom of the LCD panel. When the ICON display is in no use, set the icon common output pin to "Open."

12. LCD Power Supply Circuit

Consists of a doubler, an LCD voltage controller, an LCD bias resistor, and a voltage follower. The LCD voltage controller consists of a voltage regulator and an LCD voltage command fine adjustment circuit. The LCD power supply circuit can be controlled by pins FNC1 and 2 and BIAS SELECT command. For power supply, an internal type for the booster, voltage regulator and LCD voltage adjustment circuit or any external type can be switched by setting pins FNC1 or 2.
All of internal LCD power supplies will be automatically turned OFF by setting FNC1 to "H", and FNC2 to "L."
Because of this, the LCD bias voltage produced via the externally-divided resistor can be supplied to pins VLCD, and V1 to V4.

Table 14 LCD Power Supply Circuit

FNC 1	FNC 2	Doubler	LCD Voltage Adjustment Circuit	LCD Bias Resistor	Voltage Follower	Remarks
H	H	O	O	O	O	Use all internal LCD power supply circuits.
H	L	×	×	×	×	Use an external bias resistance.
L	H	×	×	×	×	Setting is not needed.
L	L	×	×	O	O	Externally generates and inputs VLCD.

O: Valid
× : Invalid

Remarks • Always connect FNC1 and 2 to VDD or VSS.
   • Externally-connected pins VOUT, VLCD and V1 through V4 cannot be used as a drive power supply of other circuits.
   • Connecting the power supply externally with the internal LCD power supply circuit ON may lead to a breakdown of the IC.

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12.1 Doubler

Doubles the voltage through oscillating frequency of the CR Oscillating Circuit. The voltage is boosted from the V_{SS} level and output to V_{OUT}. Capacitors between C1+ and C1- as well as between V_{SS} and V_{OUT} are connected. Use the doubler in the range of $V_{DD} \leq 3.6$ V.
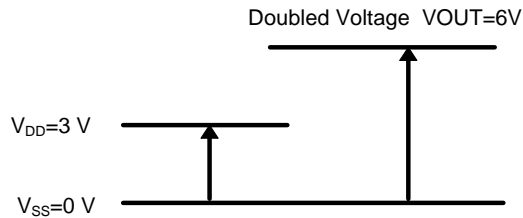
Doubled Voltage VOUT=6V

V_{DD}=3 V

V_{SS}=0 V

Figure 10   Example of Booster Output

12.2 LCD Voltage Adjustment Circuit

LCD drive voltage V can be adjusted by the following two voltage controllers:

- Voltage Regulator
  Adjusts voltage regulator output VLCD by externally- divided resistors Ra and Rb.
  VLCD can be calculated as the division ratio of the internal reference voltage VREF. VREF has temperature characteristics of approx. 0.01%/ C and -0.13%/ C and the LCD temperature gradient can be compensated. VREF differs depending upon the temperature characteristics of the reference voltage to select a command.

$$V_{LCD} = \frac{Ra+Rb}{Ra} \ V_{REF} \ (V)$$
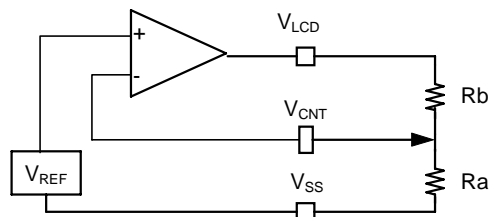
V_{LCD}

V_{CNT}

V_{REF}

V_{SS}

Rb

Ra

Figure 11   Example of LCD Voltage Adjustment Circuit

VLCD can be used as a "variable" by using the volume resistor as the divided resistor. Feedback voltage noises occurring at VCNT pin directly affect VLCD. Take appropriate measures against noises.

12.3 LCD Bias Resistor

The internally-divided resistor creates a bias potential for the LCD drive. Either 1/5 or 1/4 bias potential can be selected by executing a command. Because the bias potential is supplied from bias resistor via the voltage follower to the LCD driver, the bias current consumption is significantly reduced.

When setting FNC1 to "H" and FNC2 to "L," the externally-attached bias resistor can be connected directly to pins V1 through V4. The bias resistor of a 1/2 or more bias ratio can be freely supplied to the LCD driver as an LCD drive voltage. Regardless of its level, the voltage can be input to pins V1 through V4. Select an appropriate resistance value of the divided resistor in accordance with the size and the capacity of of the LCD panel. A deflection may occur in the LCD drive waveform depending upon the size and the capacity of the LCD panel. If so, adjust the value of the bias resistor or the capacitor. When the external bias is selected, the bias voltage is also supplied via the voltage follower to the LCD driver. The internal booster or the LCD voltage adjustment circuit cannot be used.

Supply VLCD via the externally-attached LCD power supply circuit.

12.4 Voltage Follower

Buffers the bias potential via the internal bias resistor and supplies it to the LCD driver.

12.5 Reference Voltage Circuit

Generates reference voltage VREF. The VREF has the following three values:

Table 15 V_{REF}

DV1	DV0	V_{REF}	
		Temperature Characteristics	Reference Voltage
0	0	-0.13%/°C	1.7 V (Standard)
0	1	0.01%/°C	1.7 V (Standard)
1	*	—	V_{DD}

■ **Instruction Explanation**

The instruction comes in two types - - namely, normal instructions and extended instructions.   All instructions excluding the DISPLAY CLEAR are completed within the instruction command cycle time. Because of this, the CPU does not need for checking the BUSY flag, and instructions can be input in succession.

1. Normal Instructions

1.1 DISPLAY CLEAR

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0		0	0	0	0	0	0	0	1

Clears the display and initializes the state. The display of marks remains unchanged.

DDRAM	:	Writes 20H in hexadecimal scale.
DDRAM Address Counter	:	Sets address 0. Clears the DISPLAY SHIFT and returns to the default.
Entry Mode	:	Sets to ID=1 [increment]. "S" remains unchanged.
Cursor	:	The CURSOR DISPLAY position moves to the 1st line, left end. "C" remains unchanged.
Blink	:	The BLINK DISPLAY position moves to the 1st line, left end. "B" remains unchanged.
Amount of smooth scroll	:	Resets the amount of scroll.

The DISPLAY CLEAR needs the time for writing space codes in succession in all of DDRAMs. Confirm the completion of the DISPLAY CLEAR command by checking the BUSY flag.   When you wait for the time expressed by equation (1) after executing the DISPLAY CLEAR command, the BUSY flag does not need to be checked (the value twice as many as the value expressed in equation (1) is recommended as the wait time).
The contents of the CGRAM, ICONRAM, and ICON BLINK RAM remain unchanged.
The DISPLAY CLEAR command is ignored during the POWER SAVE.

Remark: Always set all space codes in "20" (hexadecimal scale).

$$\text{Time until DISPLAY CLEAR is completed} = \frac{35}{fosc(kHz)} \text{ msec} \qquad \bullet\bullet\bullet \text{ Equation (1)}$$

1.2 CURSOR HOME

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0		0	0	0	0	0	0	1	CH

Initializes the cursor position and the blink position. The contents of the CHARACTER DISPLAY and the ICON DISPLAY remain unchanged. After this instruction is executed, data is read from the CPU and written in the DDRAM.

● CH=1 (Cursor Home)

DDRAM Address Counter	: Sets the address to 0.
DISPLAY SHIFT	: Clears the amount of the DISPLAY SHIFT and returns to the initial display screen.
CURSOR	: The CURSOR DISPLAY position moves to the 1st line, left end. "C" remains unchanged.
BLINK	: The BLINK DISPLAY position moves to the 1st line, left end. "B" remains unchanged.
Amount of SMOOTH SCROLL	: Resets the amount of the SCROLL and returns to the initial display screen.

● CH=0 (Cursor Return)

DDRAM Address Counter	: Sets the 1st address on the CURSOR DISPLAY line.
DISPLAY SHIFT	: Clears the amount of the DISPLAY SHIFT and returns to the initial display screen.
CURSOR	: The CURSOR DISPLAY position moves to the same line, left end. "C" remains unchanged.
BLINK	: The BLINK DISPLAY position moves to the 1st line, left end. "B" remains unchanged.
Amount of SMOOTH SCROLL	: Resets the amount of the SCROLL and returns to the initial display screen.

1.3 ENTRY MODE SETTING

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0		0	0	0	0	0	1	ID	S

When data is written in and read from the DDRAM, CGRAM, ICONRAM, or the ICON BLINK RAM in accordance with the ID, set ID=1 [increment] or ID=0 [decrement] of the selected RAM address counter.

"S" determines whether or not the whole display shifts during the write in the DDRAM. The display shifts left when ID=1, and shifts right when ID=0.

Table 16 Operations of Address Counter

ID	Access from/to RAM	Operations of Address Counter
0	DDRAM CGRAM: After write ICONRAM: After read ICON BLINK RAM	• Decrements the address counter of the RAM (-1) after executing write and read.
1	DDRAM CGRAM: After write ICONRAM: After read ICON BLINK RAM	• Increments the address counter of the RAM (+1) after executing write and read.

Table 17 Display Shift

Access from/to RAM	ID	S	Display Shift
Write in DDRAM	1	1	• Shifts the whole display left. • CURSOR and BLINK positions remain unchanged.*
		0	• The display does not shift. • CURSOR and BLINK positions shift right.
	0	1	• Shifts the whole display right. • CURSOR and BLINK positions remain unchanged.
		0	• The display does not shift. • CURSOR and BLINK positions shift left.
Read from DDRAM	1	-	• The display does not shift. • CURSOR and BLINK positions shift right.
	0	-	• The display does not shift. • CURSOR and BLINK positions shift left.
CGRAM Write in ICONRAM Read from ICON BLINK RAM	-	-	• The display does not shift. • CURSOR and BLINK positions do not shift.

Notes: -- : Don't care.

   *   : The display shifts. CURSOR and BLINK positions seem to be standstill on the display screen.

        CURSOR and BLINK displays are valid only when "1" is set to DISPLAY ON/OFF command C or B.

1.4 DISPLAY ON/OFF

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0		0	0	0	0	1	D	C	B

"D", "C" and "B" set the DISPLAY ON/OFF, CURSOR DISPLAY ON/OFF and BLINK DISPLAY ON/OFF.

Table 18   D

D	Functions
1	Turns ON the display (display start).
0	• Turns OFF the CHARACTER DISPLAY, MARK DISPLAY, CURSOR DISPLAY, and BLINK DISPLAY. • Data of the DDRAM, CGRAM, ICONRAM, and ICON BLINK RAM remain unchanged. • Displays again when turning ON the display. Remark: There is no change in the current consumption when turning OFF the display.

Table 19   C

C	Functions
1	Displays the cursor at the position of the DDRAM address counter.
0	Turns OFF the CURSOR DISPLAY. There is no change in setting values such as ID.

Table 20   B

B	Functions
1	Continues blinking the characters at the position of the DDRAM address counter. Can set the CURSOR and BLINK at the same time. $\text{Blink Frequency} = \dfrac{fosc}{32768}\ [\text{Hz}]$
0	Aborts the blink.

1.5 CURSOR/DISPLAY SHIFT

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0		0	0	0	1	SC	RL	-	-

- : Don't care

Shifts CURSOR and BLINK positions without writing in and reading from the display data. Used for character correction and retrieval.
Data is written in and read from the CPU to the DDRAM after executing this command.

Table 21 Cursor/Display Shift

SC	RL	Functions
0	0	Shifts CURSOR and BLINK positions left. Decrements the DDRAM address counter (-1). Repetitious operations of the CURSOR SHIFT move the cursor to other line.
0	1	Shifts CURSOR and BLINK positions right. Increments the DDRAM address counter (+1). Repetitious operations of the CURSOR SHIFT move the cursor to other line.
1	0	Shifts the whole display left. Shifts CURSOR and BLINK positions left, together with characters. There is no change in the DDRAM address counter. Characters do not shift to other line even when the DISPLAY SHIFT is executed in succession.
1	1	Shifts the whole display right. Shifts CURSOR and BLINK positions right, together with characters. There is no change in the DDRAM address counter. Characters do not shift to other line even when the DISPLAY SHIFT is executed in succession.

1.6 FUNCTION SET

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0		0	0	1	DL	N	MS	DT	-

1.6.1 DL

Sets the length of data for parallel interface.

> 0 : 4-bit data length interface
>
> 1 : 8-bit data length interface

1.6.2 N

Sets the display screen.

> N : 0 Selects a 2-line x 12 column display.
>
> N : 1 Selects a 1-line x 24 column display.

1.6.3 MS

Selects the instruction table.

Table 22 MS

MS	Functions
0	Selects the Normal Instruction Table. Sets "0" when changing from the Extended Instruction Table.
1	Selects the Extended Instruction Table. Sets "1" when changing from the Normal Instruction Table.

1.6.4 DT

Table 22 DT

DT	Functions
0	5-dot display mode
1	6-dot display mode

1.7 CGRAM ADDRESS SETTING

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0	0	1	A_5	A_4	A_3	A_2	A_1	A_0

Sets binary "A5A4A3A2A1A0" to the CGRAM Address Counter.
After executing this command, data is written from the CPU and read in the CGRAM.

1.8 DDRAM ADDRESS SETTING

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	0	1	-	-	A_4	A_3	A_2	A_1	A_0

- : Don't care

Sets binary "A4A3A2A1A0" to the DDRAM Address Counter.
After executing this command, data is written from the CPU and read in the DDRAM.

1.9 BUSY FLAG/ADDRESS READ

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	0	1	BF	0	A_5	A_4	A_3	A_2	A_1	A_0

Reads the BUSY flag and the content of " A5A4A3A2A1A0" of the Address Counter. Outputs BUSY flag BF"1" to DB7 during execution of a command. Execution of any command excluding the DISPLAY CLEAR is completed within the command cycle time. Therefore, confirmation of the BUSY flag is not needed.
The Read Address Counter reads the contents of the RAM address counter accessed just before executing this command among DDRAM, CGRAM, ICONRAM, and ICON BLINK RAM.

1.10 DATA WRITE

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Writes binary data "D7D6D5D4D3D2D1D0" in CGRAM, DDRAM, ICONRAM, and ICON BLINK RAM. Prior to data write, execute the desired RAM ADDRESS SETTING command to select an appropriate RAM. Addresses after write are incremented or decremented depending upon the ID value in the entry mode.

Table 24 Length of Data of Each Memory

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DDRAM	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CGRAM	*	*	*	D_4	D_3	D_2	D_1	D_0
ICONRAM	*	*	*	D_4	D_3	D_2	D_1	D_0
ICON BLINK RAM	*	*	*	D_4	D_3	D_2	D_1	D_0

1.11 DATA READ

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

Reads binary "D7D6D5D4D3D2D1D0" from CGRAM, DDRAM, ICONRAM, ICON BLINK RAM. Prior to data write, execute the desired RAM ADDRESS SETTING command to select an appropriate RAM. Addresses after write are incremented or decremented depending upon the ID value in the entry mode.

2. Extended Instructions

2.1 POWER SAVE SETTING

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Extended	0	0		0	0	0	0	-	-	-	PS	- : Don't care

PS : 1 Power Save

- Aborts the oscillating circuit and the LCD power supply circuit.
- Aborts the LCD driver. Segment, and common LCD drive outputs are fixed to VSS.
- Aborts the LCD.
- Leaves the setting of individual data, common and address in the DDRAM, CGRAM, ICONRAM, ICON BLINK RAM unchanged.

PS : 0 Cancels Power Save

In the Power Save mode, the current consumption is minimized to approximate the value during standstill.

When the external power supply is used, it is necessary to stop it and go to the floating or the VSS level. Also, a switching transistor and other circuit which cut the current flowing through the external bias resistor are needed.

2.2 SELECTING ICON ONLY DISPLAY, BOOSTER DRIVE FREQUENCY

	RS	R/WX		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Extended	0	0		0	0	0	1	-	MD	DC1	DC0	- : Don't care

MD : 0   Normal Display
MD : 1   Icon Only Display
DC :   Booster Drive Frequency Setting

DC1	DC0		Booster Drive Frequency [kHz]
			1/17 Duty fosc=34 kHz
0	0		4.25 (1/8 osc)
0	1	Default	2.13 (1/16 osc)
1	0		1.06 (1/32 osc)
1	1		0.53 (1/64 osc)

Regardless of the contents of the DDRAM, the icon only is displayed and display screens excluding marks go out when MD=1. When setting the booster drive frequency, it is possible to minimize the current consumption by reducing the booster drive frequency in accordance with the boosting control data.

When the booster drive frequency is reduced, the contrast of the display icon differs depending upon the display panel size and the value of the capacitor for the booster. Determine the ability of the booster by experimentally optimizing the contrast of the LCD panel. In addition, take into careful consideration noises which may affect the system due to the booster drive frequency.

After resetting, the booster drive frequency is the default value.

2.3 SELECT COM/SEG OUTPUT MODE, SELECT BIAS

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	0	1	0	0	MLC	MLS	—	BS5

The MLC determines how the common output waveform is output to COM (1-16) terminals.

MLC=0: The common output waveform is output in the order of COM1, COM2, ···, COM15, COM16.

MLC=1: The common output waveform is output in the order of COM16, COM15, ···, COM2, COM1.

The MLS determines how the segment output waveform is output to SEG (1-60) terminals.

The output form also varies depending upon N=0 or N=1.

[N=0 (2-line x 12-column) display]

MLS=0: The segment output waveform to be displayed on the DDRAM addresses from 00 to 0B is output to terminals from SEG1 to SEG60.
The segment output waveform to be displayed on the DDRAM addresses from 10 to 1B is output to terminals from SEG1 to SEG60.

MLS=1: The segment output waveform to be displayed on the DDRAM addresses from 00 to 0B is output to terminals from SEG60 to SEG1.
The segment output waveform to be displayed on the DDRAM addresses from 10 to 1B is output to terminals from SEG60 to SEG1.

[N=1 (1-line x 24-column) display]

MLS=0: The segment output waveform to be displayed on the DDRAM addresses from 00 to 0B is output to terminals from SEG1 to SEG60.
The segment output waveform to be displayed on the DDRAM addresses from 10 to 1B is output to terminals from SEG60 to SEG1.

MLS=1: The segment output waveform to be displayed on the DDRAM addresses from 00 to 0B is output to terminals from SEG60 to SEG1.
The segment output waveform to be displayed on the DDRAM addresses from 10 to 1B is output to terminals from SEG1 to SEG60.

Both the MLC and the MLS allow viewers to see characters correctly regardless of the mounting position of the IC to the LCD panel (upper, lower, front or rear mounting position).

Determine the bias voltage for the LCD power supply circuit.

BS5	Select Bias
0	1/4 Bias
1	1/5 Bias

While the bias voltage is being externally determined, the booster, the LCD voltage adjustment circuit, the voltage follower, and the bias circuit stop.

2.4 BLINK SELECT

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Extended	0	0	0	1	0	1	-	-	BK1	BK0	- : Don't care

Four kinds of blink display are set up.

	BK1	BK0	Cursor Display OFF C=0	Cursor Display ON C=1
			B=0	B=0
Black Blink	0	0		
White Blink	0	1		
Cursor Blink	1	0		
White/Black Inversion Blink	1	1		

2.5 SMOOTH SCROLL DOT SHIFT AMOUNT SETTING

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Extended	0	0	1	0	0	0	–	Scroll Amount			- : Don't care

Set the dot scroll amount of the selected line to the smooth scroll line and shift it. The display shifts left by the dot scroll amount. The dot scroll amount is from 0 dot up to 5 dots. The dot scroll amount of over 6 dots is deemed to be 0 dot. To continue smooth scroll, execute the SMOOTH SCROLL CHARACTER command. The scroll amount can be reset by executing the SMOOTH SCROLL CHARACTER SHIFT, DISPLAY CLEAR or CURSOR HOME command.

The smooth scroll amount is cleared by resetting the smooth scroll amount character shift amount.

2.6 SETTING UP SMOOTH SCROLL LINE

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	1	0	0	1	-	-	L_2	L_1

Set the smooth scroll line. The line where "1" is set on L1, L2 is selected. To scroll two lines simultaneously, set "1" to L1 and L2.

L2: 2nd line
L1: 1st line

To scroll another line while a line is being scrolled, release the smooth scroll character amount and line setup, then set a new scroll line.

2.7 SMOOTH SCROLL CHARACTER SHIFT AMOUNT SETTING

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	1	0	1	S_4	S_3	S_2	S_1	S_0

Shift the required number of characters of the selected line to the smooth scroll line.

S4	S3	S2	S1	S0	Shift Amount
0	0	0	0	0	Does not shift.
0	0	0	0	1	1 character shifts left.
0	0	0	1	0	2 characters shift left.
		:			:
1	0	0	0	0	16 characters shift left.
		:			:
1	1	1	1	1	31 characters shift left.

2.8 ICONRAM ADDRESS SETTING

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	1	1	0	0	A_3	A_2	A_1	A_0

Set binary "A3A2A1A0" to the ICONRAM Address Counter.
After this command is executed, data is written from the CPU and read to ICONRAM. Write the mark display data which corresponds to each address of the ICONRAM for every 5 bits.

2.9 ICON BLINK RAM ADDRESS SETTING

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	1	1	0	1	A_3	A_2	A_1	A_0

Set binary "A3A2A1A0" to the ICON BLINK RAM Address Counter. When writing "1" in the ICON BLINK RAM, the respective marks blink. ICONRAM addresses correspond to respective ICON BLINK RAM addresses. After this command is executed, data is written from the CPU and read to ICON BLINK RAM.

2.10 (TEST)

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	1	1	1	0	D_3	D_2	D_1	D_0

Testbits:D_3~D_0 = all 0 at reset.

DO NOT write any values other than "0000" into this testbits.

2.11 REFERENCE VOLTAGE CHARACTERISTICS SELECT

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	1	1	1	1	-	-	DV1	DV0

Select the temperature characteristics for the reference voltage. The reference voltage also varies depending upon the temperature characteristics.

DV1	DV0	Temperature Characteristics(%/°C) $\triangle V_{REF}$	Reference Voltage(Ta=25°C) V_{REF} (V)
0	0	-0.13	1.7
0	1	0.01	1.7
1	—	0	VDD

2.12 FUNCTION SETTING

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	0	0	0	1	DL	N	MS	DT	-

The same as the function setting for the Normal Instructions.

2.13 BUSY FLAG/ADDRESS READ

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	0	1	BF	0	A_5	A_4	A_3	A_2	A_1	A_0

The same as the functions for the Normal Instructions.

2.14 DATA WRITE

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

The same as the functions for the Normal Instructions.

2.15 DATA READ

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Extended	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

The same as the functions for the Normal Instructions.

■ **Instruction List**

1. **Normal Instructions**

Table 25 Normal Instructions

Command	Code										Description	Execution Time V_{DD}=3V
	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
NOP	0	0	0	0	0	0	0	0	0	0	Don't care.	
DISPLAY CLEAR	0	0	0	0	0	0	0	0	0	1	Writes the space code in the entire DDRAM.	OSC 35 Clock
CURSOR HOME	0	0	0	0	0	0	0	0	1	CH	CH: 1/0= Cursor Return/Cursor Home	1 μsec or less
ENTRY MODE	0	0	0	0	0	0	0	1	ID	S	ID: 1/0= Address Counter Increment/Decrement S: 1/0= Display Shift during DDRAM write	1 μsec or less
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	D: 1/0= Display ON/OFF C: 1/0= Cursor Display ON/OFF B: 1/0= Cursor Position Blink ON/OFF	1 μsec or less
CURSOR DISPLAY SHIFT	0	0	0	0	0	1	SC	RL	-	-	SC: 1/0= Whole Display Shift/Cursor Shift RL: 1/0= Cursor/Display Right /Left Shift	1 μsec or less
FUNCTION SETTING	0	0	0	0	1	DL	N	MS	DT	-	DL: 1/0= 8-bit/4-bit Data Length Interface N: 1/0= 1-line x 24-column/2-line x 12- column MS: 1/0= Extended/Normal Interface DT: 1/0= 6-dot front/5-dot font	1 μsec or less
CGRAM ADDRESS SETTING	0	0	0	1	CGRAM Address						CGRAM Address Setting	1 μsec or less
DDRAM ADDRESS SETTING	0	0	1	-	-	DDRAM Address					DDRAM Address Setting	1 μsec or less
BUSY ADDRESS READ	0	1	BF	0	Address Counter						BF: BUSY Output Address Counter Read	1 μsec or less
DATA WRITE	1	0	Write Data								Write Data	1 μsec or less
DATA READ	1	1	Address Counter								Data Read	1 μsec or less

-:Don't care

2. Extended Instructions

Table 26 Extended Instructions

Command	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time V_{DD}=3V
								Code				
POWER SAVE SETTING	0	0	0	0	0	0	0	0	0	PS	PS : 1/0= Power Save Operation/Normal Display	1 μsec or less
ICON ONLY DISPLAY BOOSTER DRIVE FREQUENCY	0	0	0	0	0	1	-	MD	DC1	DC0	MD : 1/0= Icon Only Display/Normal Entire Display DC1, DC0: Booster Drive Frequency Select	1 μsec or less
COM/SEG OUTPUT MODE SELECT BIAS SELECT	0	0	0	1	0	0	MLC	MLS	-	BS5	MLC: COM Output Mode MLS: SEG Output Mode BS5: 1 (1/5 Bias) 0 (1/4 Bias)	1 μsec or less
BLINK SELECT	0	0	0	1	0	1	-	-	BK1	BK0	BK1 BK0 0 0 Black Blink 0 1 White Blink 1 0 Cursor Blink 1 1 Black/White Inverse Blink	1 μsec or less
SMOOTH SCROLL DOT SHIFT	0	0	1	0	0	0	-	Dot Shift Amount			Dot Shift Amount : Sets and executes the Dot Shift Amount in the Smooth Scroll Select lines.	1 μsec or less
SCROLL LINE SETTING	0	0	1	0	0	1	-	-	L2	L1	L1: Selects the 1st line to Smooth Scroll line. L2: Select the 2nd line to the Smooth Scroll line.	1 μsec or less
SMOOTH SCROLL CHARACTER SHIFT	0	0	1	0	1	Character Shift Amount					Character Shift Amount: Setting and Operation of the Character Shift Amount in the Smooth Scroll Select lines.	1 μsec or less
ICON RAM ADDRESS SETTING	0	0	1	1	0	0	Icon RAM Address				Icon RAM Address Assignment	1 μsec or less
ICON BLINK RAM ADDRESS SETTING	0	0	1	1	0	1	Icon Blink RAM Address				Icon Blink RAM Address Assignment/ Sets the Icon to blink.	1 μsec or less
** (TEST)	0	0	1	1	1	0	Testbits				**	1 μsec or less
REFERENCE VOLTAGE CHARACTERISTI-CS SELECT	0	0	1	1	1	1	-	-	DV1	DV0	DV1 DV0 Characteristics Reference V 0 0 -0.13%/°C 1.7 V 0 1 0.01%/°C 1.7 V 1 ∗ — VDD	1 μsec or less
FUNCTION SETTING	0	0	0	0	1	DL	N	MS	DT	-	DL:1/0= 8-bit/4-bit data Length Interface N:1/0= 1-line x 24-column/2-line x 12-column MS: 1/0= Extended/Normal Instructions DT: 1/0= 6-dot/5-dot font	1 μsec or less
BUSY ADDRESS READ	0	1	BF	0	Address Counter						BF : BUSY Output Address Counter Read	1 μsec or less
DATA WRITE	1	0	Write Data								Write Data	1 μsec or less
DATA READ	1	1	Read Data								Read Data	1 μsec or less

IMPORTANT: The FUNCTION SETTING, BUSY ADDRESS READ, DATA WRITE, and DATA READ commands are common to Normal and Extended Instructions.

** This is for Biastest. Testbits="all0" at reset. DO NOT write any values other than "0000" into this testbits.

■ **Operation Description**

1. Powering ON

After powering ON, the S-4561A is initialized by inputting the RESX signal.

In order to prevent the unstable state of the inside of the IC due to momentary stop or gradually raised power voltage waveform, reset hardware by inputting the RESX signal.

If the S-4561A is not initialized by inputting the RESX signal, the IC may malfunction. Chattering occurring in the RESX signal may lead to an initialization error. Input the signal free of chattering. Always connect and fix pins P/SX, FNC1 and FNC2 to V_{DD} or V_{SS}.

2. Reset

The following operations and instructions are executed by initialization through the RESX signal input:

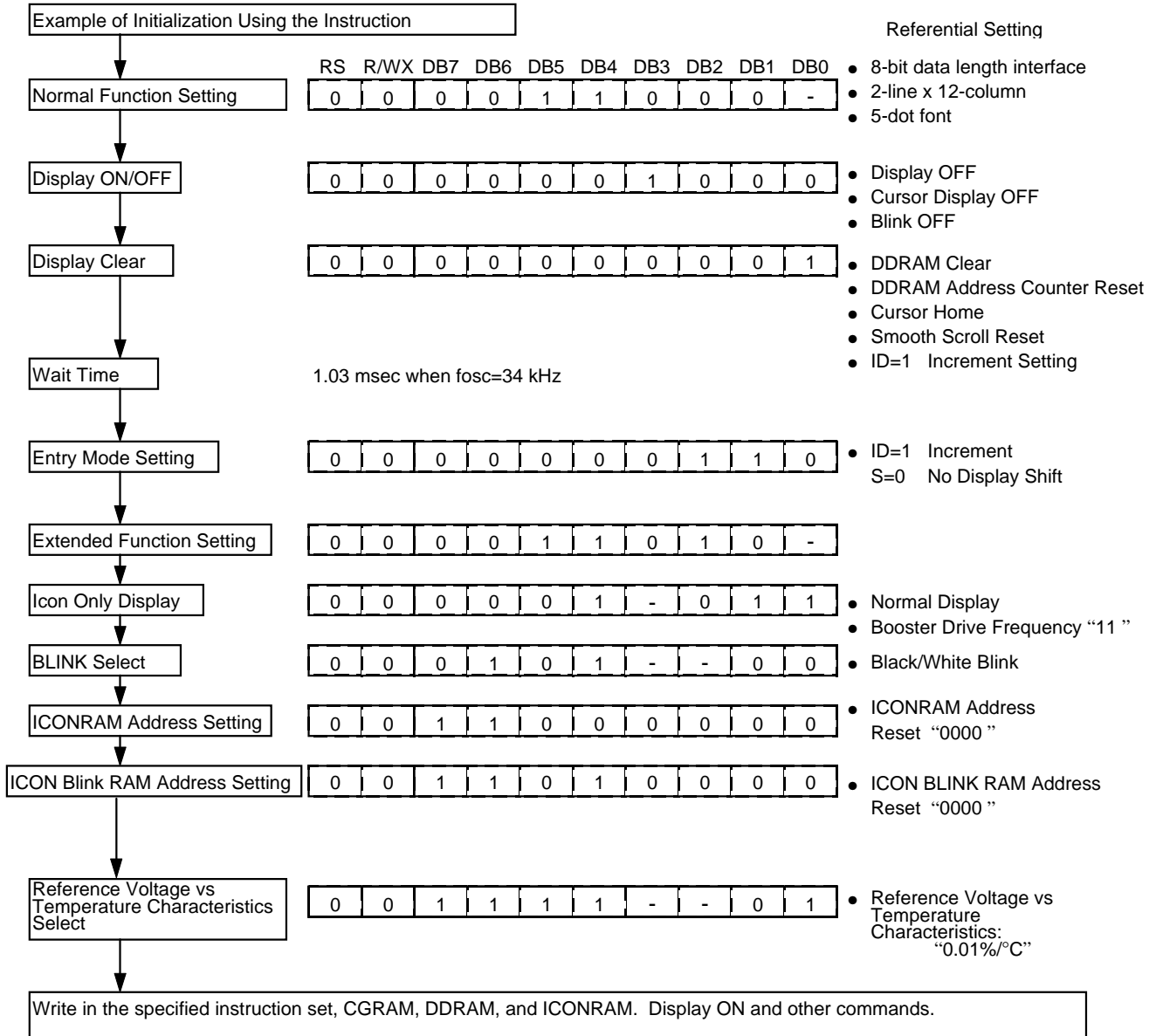|		
1	Entire Circuitry Reset	
2	Bias Select	BS5=1 (1/5 Bias)
3	Display OFF	D=0, C=0, B=0
4	Display Clear	
	● DDRAM Address	Reset "00000"
	● Smooth Scroll Dot shift Amount	Reset "000"
	● Smooth scroll line	Reset "0000"
	● Smooth Scroll Dot Shift Amount	Reset "00000"
5	Entry Mode	ID=1, S=0
6	Icon Only Display	OFF (MD=0)
	● Booster Drive Frequency	01
7	Blink mode	Black blink "00"
8	ICONRAM Address	Reset "0000"
9	ICON BLINK RAM Address	Reset "0000"
10	(TEST)	Reset "0000"
11	Function Setting	Set to the normal instruction set
		DL=1, N=0, MS=0, DT=0
12	Address Counter	Select DDRAM
13	Reference Voltage Temperature Characteristics Select	00 (- 0.13%/ °C)
14	Power Save	After resetting, the state moves to PS=1.
	● Booster	OFF
	● LCD power Supply Voltage Controller	OFF
	● Voltage Regulator	OFF
	● Bias Resistor	OFF

Remark: After resetting, the state automatically moves to the Power Save mode.

3. **Initialization by Instruction**

When initializing the IC by instruction, input the necessary command and set to the appropriate mode, referring to the following order.

After powering ON, reset the state by inputting the RESX signal, instead of initializing the IC by the instruction.
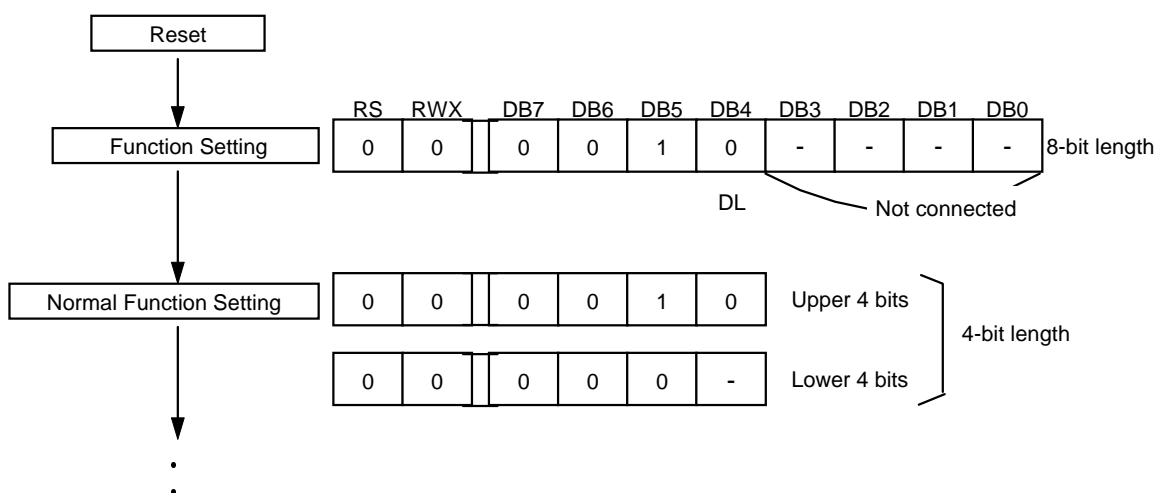
Step	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Referential Setting
Example of Initialization Using the Instruction											Referential Setting
Normal Function Setting	0	0	0	0	1	1	0	0	0	-	• 8-bit data length interface • 2-line x 12-column • 5-dot font
Display ON/OFF	0	0	0	0	0	0	1	0	0	0	• Display OFF • Cursor Display OFF • Blink OFF
Display Clear	0	0	0	0	0	0	0	0	0	1	• DDRAM Clear • DDRAM Address Counter Reset • Cursor Home • Smooth Scroll Reset • ID=1 Increment Setting
Wait Time				1.03 msec when fosc=34 kHz							
Entry Mode Setting	0	0	0	0	0	0	0	1	1	0	• ID=1 Increment S=0 No Display Shift
Extended Function Setting	0	0	0	0	1	1	0	1	0	-	
Icon Only Display	0	0	0	0	0	1	-	0	1	1	• Normal Display • Booster Drive Frequency "11"
BLINK Select	0	0	0	1	0	1	-	-	0	0	• Black/White Blink
ICONRAM Address Setting	0	0	1	1	0	0	0	0	0	0	• ICONRAM Address Reset "0000"
ICON Blink RAM Address Setting	0	0	1	1	0	1	0	0	0	0	• ICON BLINK RAM Address Reset "0000"
Reference Voltage vs Temperature Characteristics Select	0	0	1	1	1	1	-	-	0	1	• Reference Voltage vs Temperature Characteristics: "0.01%/°C"

Write in the specified instruction set, CGRAM, DDRAM, and ICONRAM. Display ON and other commands.

Initialization Examples

<4-Bit Data Length Interface>

When executing a 4-bit operation, it is necessary to set respective functions on a program. After resetting, first write the upper 4-bits of the function setting command to reset DL (DL = 0). Then this IC is set for the 4-bit data-length interface. Next write the function setting command again for each upper 4-bits and lower 4-bits to complete the function command. Then write commands to initialize this IC for 4-bit data-length interface. (See an example shown in the previous page.)

For the 4-bit data-length interface, the upper 4-bits are written first, followed by the lower 4-bits. The RS terminal for register selection is used to distinguish instruction from data for a command. For the 4-bit data-length interface, do not change the RS signal during the period when both the upper and lower 4-bits are written.

Reset		RS	RWX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Function Setting		0	0	0	0	1	0	-	-	-	-	8-bit length

DL   Not connected

Normal Function Setting		0	0	0	0	1	0	Upper 4 bits
		0	0	0	0	0	-	Lower 4 bits

4-bit length

For the 4-bit data-length interface, open the lower 4-bit terminals of the data bus (DB3-DB0).

Notice that output short-circuit current will flow at READ phase if they are connected to the power supply (VDD or VSS)

4. Procedures from Powering ON to Display Start

The procedures from powering ON to Display Start are as follows:

| Powering ON |

| RESX Input | Initialize.

| Wait Time | Wait for BUSY cancellation.
When you do not want monitor BUSY*, wait for 2.0 msec at f_{osc}=34 kHz.

* Set the wait time twice as long as f_{osc}35 clock.
When BUSY is canceled, this IC is set to the power save mode (PS=1).

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Normal Function Setting	0	0	0	0	1	1	0	0	0	-
Entry Mode Setting	0	0	0	0	0	0	0	1	0	0
Display ON/OFF	0	0	0	0	0	0	1	1	1	0
Extended Function Setting	0	0	0	0	1	1	0	1	0	-
Bias Select	0	0	0	1	0	1	0	0	-	1
Power Save Release	0	0	0	0	0	0	0	0	0	0

Setting Examples:

Normal Function Setting:
- DL=1 8-bit data length interface
- N=0   2-line x 12-column
- MS=0 Normal Instruction
- DT=0 5-dot font

Entry Mode Setting:
- ID=0 Decrement
- S=0   No Display Shift

Display ON/OFF:
- D=1   Display ON
- C=1   Cursor Display ON
- B=0   Cursor Blink OFF

Extended Function Setting:
- DL=1 8-bit data length interface
- N=0   2-line x 12-column
- MS=1 Extended Instruction
- DT=0 5-dot font

Bias Select:
- MLC=0 No COM output inversion
- MLS=0 No SEG output inversion
- BS5=1 1/5 bias

Power Save Release:
- PS=0 Power Save Cancel

| Write in the specified instruction set, CGRAM, DDRAM, and ICONRAM. |

Mode Setting Examples after Powering ON

5. Instruction Execution Time

Any instructions other than the DISPLAY CLEAR are completed within the cycle time (tcyc) represented with the instruction input timing characteristics. For instance, when the instruction input cycle time is 500 μsec, the instruction can be completed within 500 μsec. Consequently, instructions can be input in succession without confirming the BUSY flag. Also, load to the MPU and the current consumption can be drastically reduced. Inputting the next command within the cycle time is prohibited.
In the DISPLAY CLEAR mode, it is necessary to write a space code in all of DDRAMs. For the write execution time, refer to page 18, "Instruction Explanation" of this specification.

6. Read and Write Display Data from and In MPU

The Display Data is accessed from the MPU to DDRAM, CGRAM, ICONRAM or ICON BLINK RAM by executing the READ or WRITE command following the ADDRESS SETTING command of individual RAMs. Always execute the ADDRESS SETTING command before executing the READ command. When the ADDRESS SETTING command is not executed, correct display data cannot be read. After executing the READ or WRITE command, the column address is incremented or decremented depending upon the value of the ID of the ENTRY MODE Setting. Consequently, when the cycle time represented

7. Dot Display Mode

5- or 6-dot display mode can be selected by the FUNCTION SETTING command. The 5-dot display mode is used for the dot matrix for every character; and the 6-dot display mode is used for a full dot matrix.

Display data written in the CGRAM, ICONRAM or other RAM on the 5-or 6-dot display mode is for every 5 bits, and there is no change in the data length regardless of the dot display mode. The 6-dot display mode controls data inside the IC so that left one column of each for every character is NOT-LIT. The cursor for the 6-dot display mode appears on the 8th line of the character in a 5-dot size.

5-dot display mode   6-dot display mode

Character Display Example for Every Dot Display Mode

Difference of Display Area for Every Dot Display Mode

5-dot mode display area	6-dot mode display area
2-line x 12-column+ 4-column non-displayed character	2-line x 10-column+ 6-column non-displayed character
1-line x 24-column+ 8-column non-displayed character	1-line x 20-column+ 12-column non-displayed character

8. Smooth Scroll

Right and left smooth scroll for every dot is possible by executing one ore more command. The lines to be scrolled smoothly can be selected freely and two lines can be scrolled at the same time.

Smooth scrolling is possible in both 5- and 6-dot display modes. In the 5-dot display mode smooth scroll, individual space rows are inserted between characters. This allows for easy-to-see smooth scroll display without deformation in characters. Also, the cursor and the blink shift together with characters.

	5-dot smooth scroll	6-dot smooth scroll
No Shift		
1 dot shifts left		
2 dot shifts left		
3 dot shifts left		
4 dot shifts left		
5 dot shifts left		
Dots corresponding to 1 character shift left		
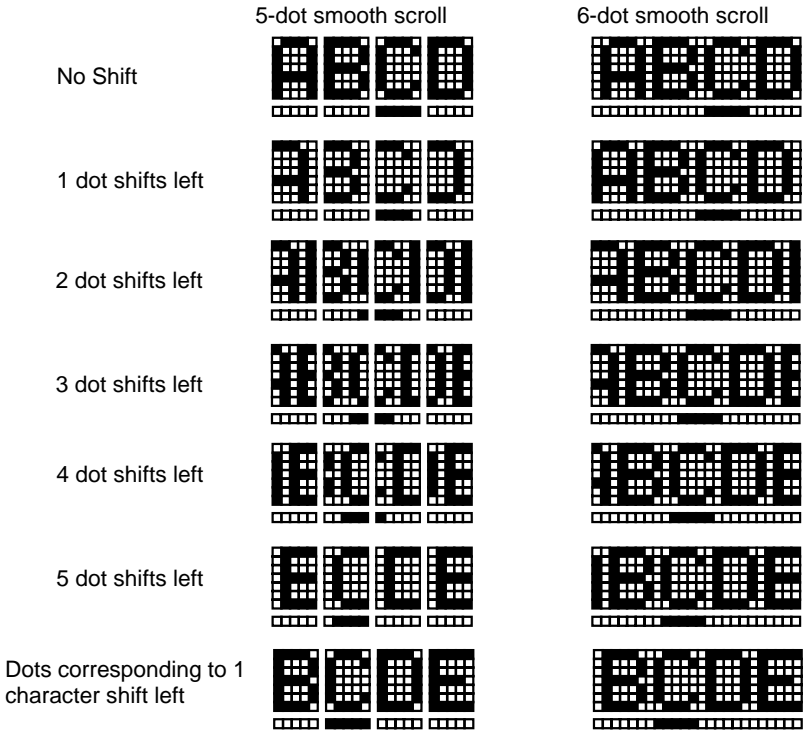
Smooth Scroll Examples

	RS	R/WX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
● Extended Instruction Select	0	0	0	0	1	1	0	1	0	-
● 2nd Line Select	0	0	1	0	0	1	-	-	1	0
● 1 dot shifts left	0	0	1	0	0	1	-	0	0	1
● 2 dots shift left	0	0	1	0	0	1	-	0	1	0
● 3 dots shift left	0	0	1	0	0	1	-	0	1	1
● 4 dots shift left	0	0	1	0	0	1	-	1	0	0
● 5 dots shift left	0	0	1	0	0	1	-	1	0	1
● 1 character shifts left (6 dots shift left)	0	0	1	0	1	0	0	0	0	1
● 1 dot shifts left (7 dots shift left)	0	0	1	0	0	1	-	0	0	1
● 2 dots shift left (8 dots shift left)	0	0	1	0	0	1	-	0	1	0
● 15 characters shift left (90 dots shift left)	0	0	1	0	1	0	1	1	1	1
● 5 dots shift left (95 dots shift left)	0	0	1	0	0	1	-	1	0	1
● No character shifts (Original Display Position)	0	0	1	0	1	0	0	0	0	0

Remarks • After Dot Shift, set a wait time for the next shift so as to make the display legible.
 • To execute the Smooth Scroll, shift characters left by the amount corresponding to the display column (including non-displayed characters) and input the instruction so that the amount of the shift is reduced.

Examples of Smooth Scroll of 2nd Lines of a 5-Dot 2-Line x 12-Column Display

9. Icon Only Display

Regardless of the contents of the display data RAM (DDRAM), the icon only is displayed and the LCD panel is compelled to be off. Since the contents of the DDRAM do not change, the state is returned to the original display by canceling the Icon Only Display mode. While the icon only is being displayed, the LCD panel is driven at low power consumption. This allows for the reduction in the boosting level and also the reduction in the current consumption. Four levels of booster drive frequency can be selected by the lower 2 bits of the ICON ONLY DISPLAY command (refer to Instruction Explanation: page 18). The booster drive frequency differs depending upon the size of the LCD panel and wiring capacity. Determine the appropriate frequency on the actual LCD panel.

10. Power Save

After inputting the POWER SAVE command, the CR oscillating circuit and the LCD power supply circuit stop, and the current consumption of the IC goes down nearly to the value during standstill simultaneously with display OFF. This is valid for reducing the current consumption when the display is not needed or during wait.
The DDRAM and instruction state still remains unchanged and is returned to the original display by canceling the Power Save.

11. Connection to LCD

Common output terminals are mounted on both right and left of the chip.   Common wiring is needed with respect to the panel configuration and also display columns.

■ **Examples of Connection to LCD Panel**

1. When the IC is mounted from the front view (Viewing Side):
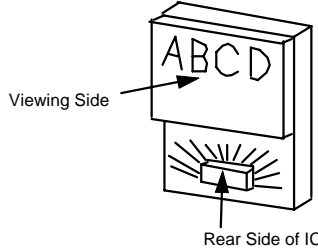
N=0: 2 -line x 12 -character LCD panel
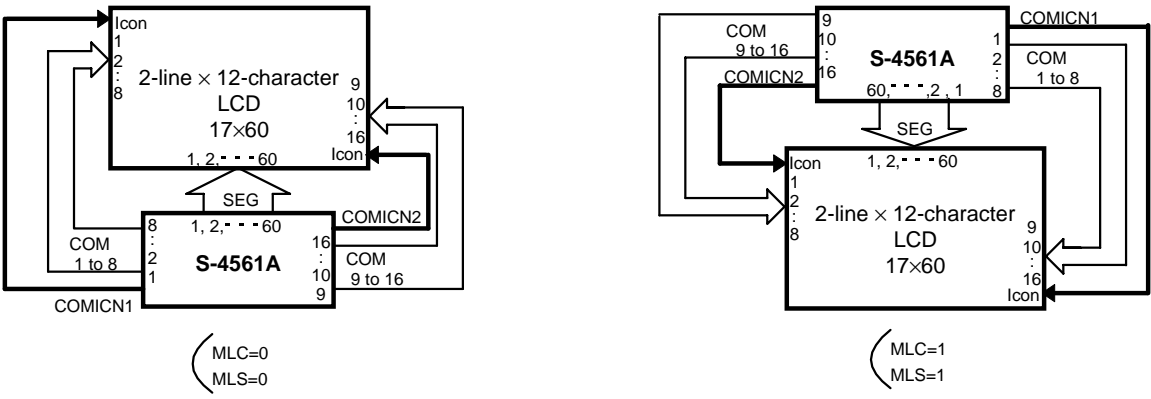
Figure 12: 2-line x 12-character LCD panel

N=1: 1-line 24 -character LCD panel
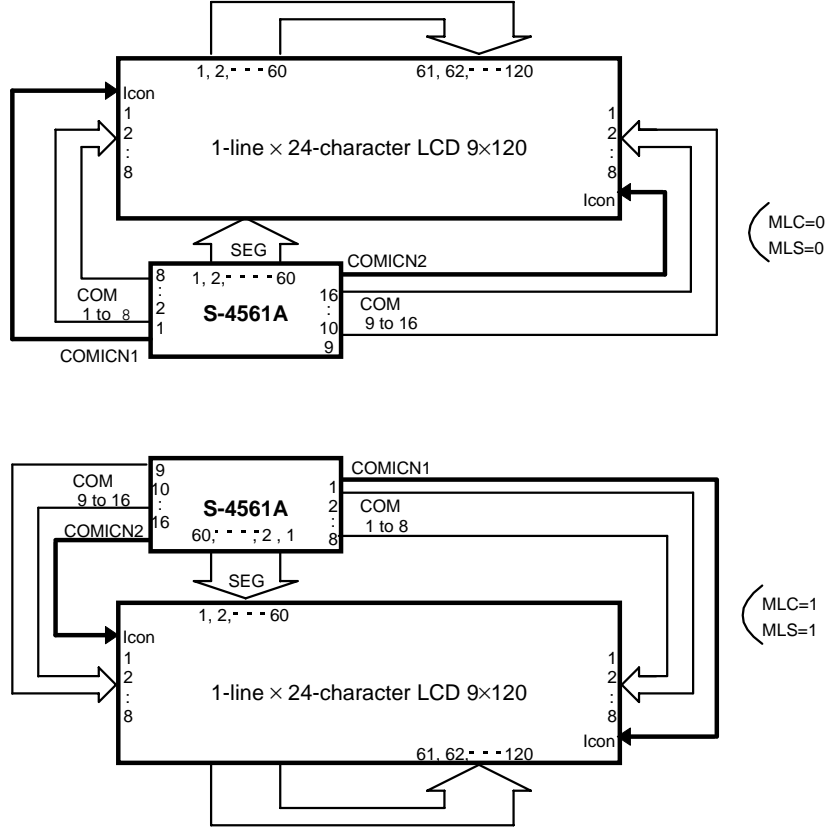
Figure 13: 1-line x 24-character LCD panel
Seiko Instruments Inc.

35

2. When the IC is mounted from the rear side:
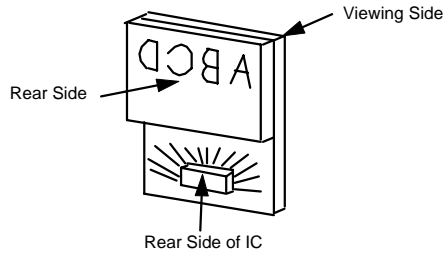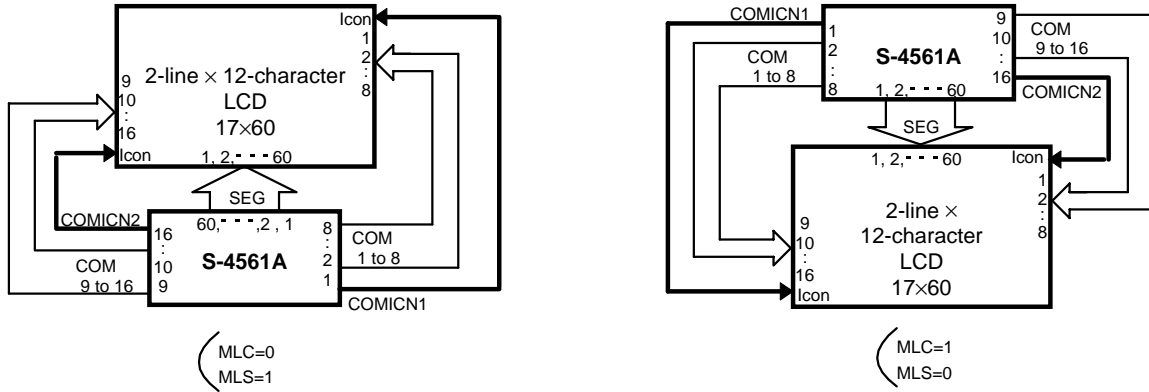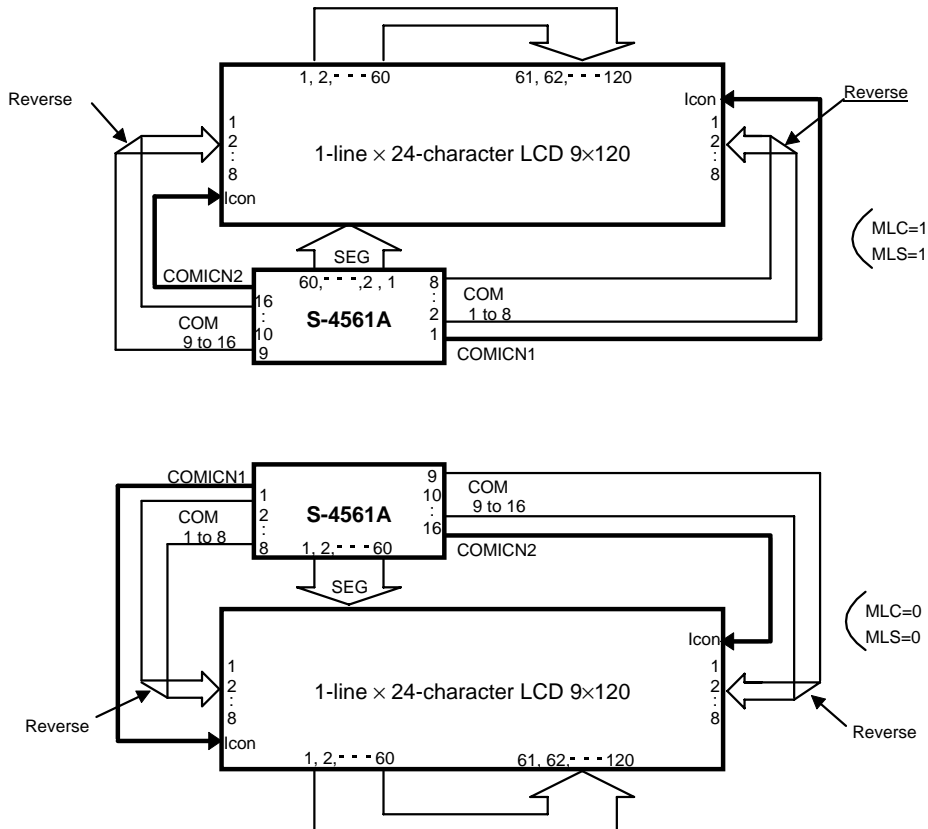

N=0: 2 -line x 12 -character LCD panel

Figure 14: 2-line x 12-character LCD panel

N=1: 1 -line $\times$ 24 -character LCD panel

Figure 15: 1-line x 24-character LCD panel

■ **Examples of LCD Drive Output Waveform**

Figure 16   Example of LCD Drive Output Waveform (1/5 bias)

■ **External Bias Resistor vs LCD Drive Waveform**

1. 1/4 or more bias

$R_{a2}=\alpha R_{a1}$
$0\leq\alpha$

Bias

$= \dfrac{R_a}{R_{a1}+R_{a1}+R_{a2}+R_{a1}+R_{a1}}$

$= \dfrac{1}{4+\alpha}$

2. 1/4 bias

3. 1/3 to 1/4 bias

$R_{C2}+R_{C3}=R_{C1}$
$R_{C2}=\beta R_{C1}\quad 0\leq\beta\leq 1$

Bias

$= \dfrac{R_{C1}}{R_{C1}+R_{C2}+R_{C3}+R_{C2}+R_{C1}}$

$= \dfrac{1}{3+\beta}$

4. 1/3 bias

5. 1/2 to 1/3 bias

$R_{e3}=\gamma(R_{e1}+R_{e2})$
$R_{e1}=R_{e3}$
$0\leq\gamma\leq 1$

Bias

$= \dfrac{R_{e1}+R_{e2}}{R_{e1}+R_{e2}+R_{e3}+R_{e2}+R_{e1}}$

$= \dfrac{1}{2+\gamma}$
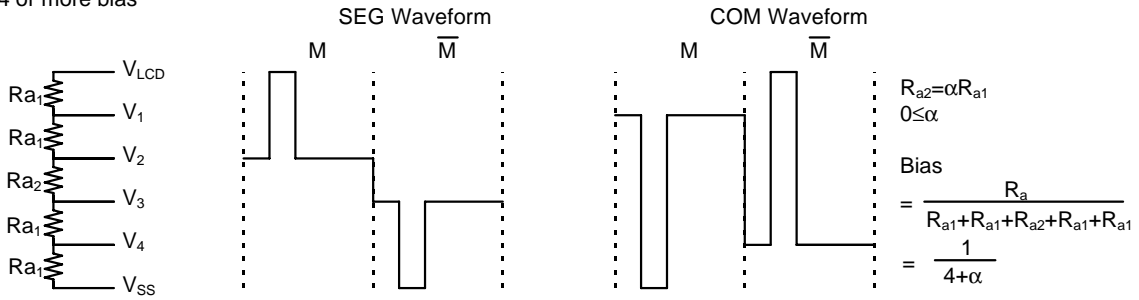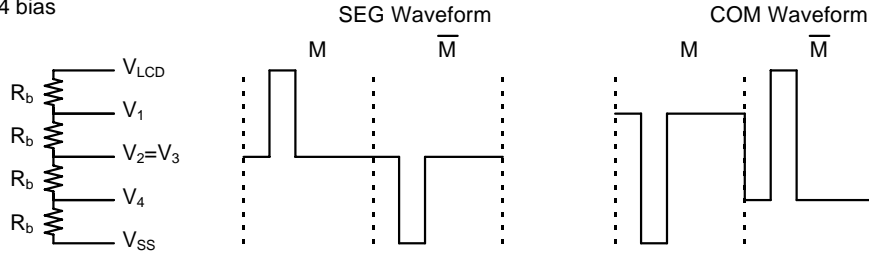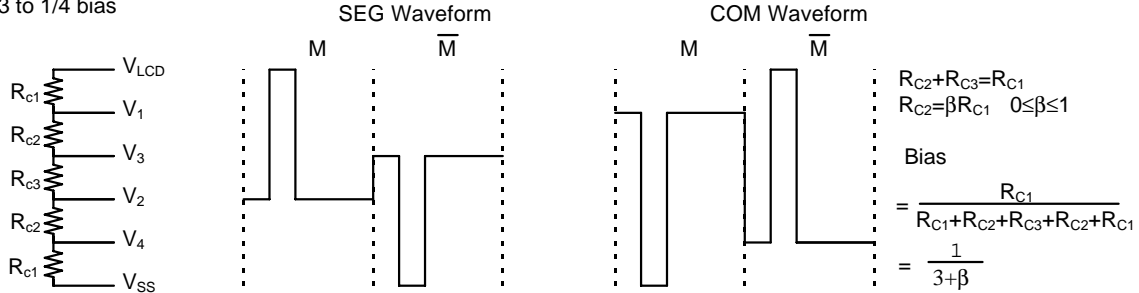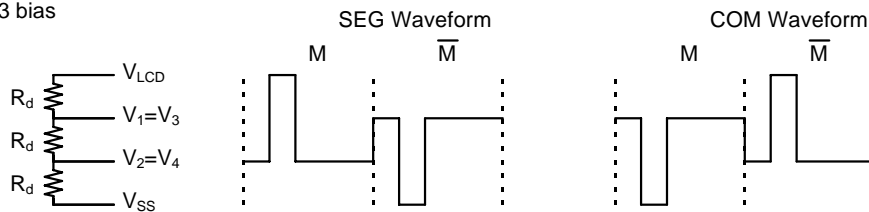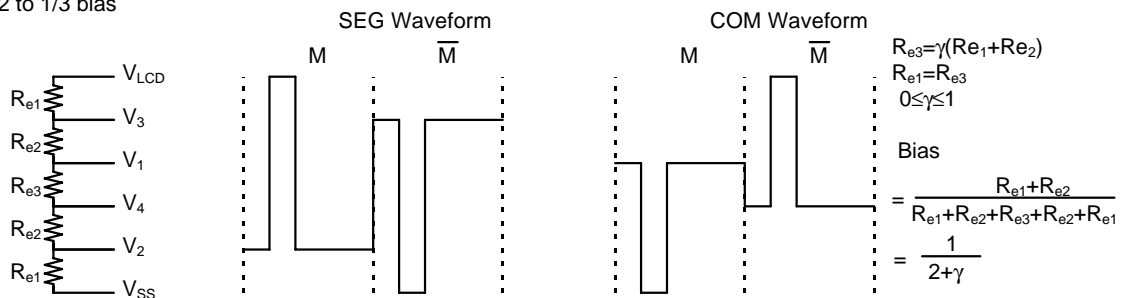
Figure 17 External Bias Resistor vs LCD Drive Waveform

■ Absolute Maximum Ratings

Table 27 Absolute Maximum Ratings

V_{DD}=0.0 V

Parameter		Symbol	Ratings	Unit
Supply voltage		V_{DD}	-0.4 to +7.0	V
LCD drive voltage 1		V_{LCD}	-0.4 to +8.0	V
LCD drive voltage 2		V_1, V_2, V_3, V_4	V_{LCD}-0.4	V
Input voltage		V_{IN}	-0.4 to V_{DD} +0.4	V
Output voltage		V_{OUT}	-0.4 to V_{DD} +0.4	V
Operating temperature range		T_{opr}	-30 to +85	°C
Storage temperature range	Chip	T_{stg}	-55 to +125	°C
	TCP		-55 to +100	

Remarks: • If your IC is used in the range exceeding the above absolute maximum ratings, IC's characteristics may drastically deteriorate and may lead to a breakdown of the device.
• Use this IC within the specified range of electrical characteristics. If not, the functions and reliability of the IC cannot be assured.
• When connecting a bias resistor externally, determine the LCD power supply voltage so that its state goes to $V_{LCD} \geq V_{DD}$ during display.
• Notice that isolation of the IC from light exposure is not taken iinto account for this IC design.

■ DC Characteristics

1. Electrical Characteristics

Table 28 Electrical Characteristics

(Unless otherwise specified: V_{SS}=0 V, V_{DD}=3.0±0.3 V, Ta=-30 to 85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage 1	V_{DD1}	Internal booster is used.	2.4	-	3.6	V	Note 1
Operating Voltage 2	V_{DD2}	External LCD power supply is used.	2.4	-	5.5	V	Note 1 Note 2
High-level Input Voltage	V_{IH}		$0.8 \times V_{DD}$	-	V_{DD}	V	Note 3
Low-level Input Voltage	V_{IL}		V_{SS}	-	$0.2 \times V_{DD}$	V	Note 3
High-level Output Voltage	V_{OH1}	I_{OH}=-0.5 mA	$0.8 \times V_{DD}$	-	-	V	Note 4
	V_{OH2}	I_{OH}=-50 µA	$0.8 \times V_{DD}$	-	-	V	OSC2
Low-level Output Voltage	V_{OL1}	I_{OL}=0.5 mA	-	-	$0.2 \times V_{DD}$	V	Note 4
	V_{OL2}	I_{OL}=50 µA	-	-	$0.2 \times V_{DD}$	V	OSC2
Pull-up Current	I_U	Ta=25°C, V_{DD}=3.0 V	-20	-10	-4	µA	RESX
Input Leak Current	I_{ILEAK}		-1.0	-	1.0	µA	Note 5
Output Current	I_{OLEAK}		-3.0	-	3.0	µA	Note 6
LCD Driver ON Resistor	R_{ON}	Ta=25°C, V_{LCD}=5.0 V 1/4-bias	-	3.0	5.0	kΩ	Note 7
Current Consumption During Standstill	I_S	Power Save	-	0.05	5.0	µA	Note 8
Operating Current	I_{DD1}	Internal booster is used: During LC display Rf=500 kΩ V_{OUT}=6.0 V V_{LCD}=5.0 V	-	70.0	105.0	µA	Note 9
	I_{DD2}	External LCD power supply is used: During LC display Rf=500 kΩ V_{LCD}=5.0 V	-	15.0	20.0	µA	Note 10
Oscillating Frequency	f_{OSC}	R_f=500 kΩ V_{DD}=3.0 V	27	34	41	kHz	
Reset Time	t_R		10	-	-	µs	Note 11
Reset Pulse Width	t_{RW}		20	-	-	µs	Note 12

2. LCD Power Supply Circuit Electrical Characteristics

2.1 When Using an Internal Booster: FNC1="H," FNC2="H"

Table 29   Electrical Characteristics

V_{SS}=0 V, V_{DD}=3.0±0.3 V, Ta=-30 to 85 °C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage 1	V_{DD1}	FNC1="H", FNC2="H"	2.4	-	3.6	V	Note 13
Boosting Output Voltage	V_{OUT}		4.8	-	7.2	V	
Voltage Regulator Output Voltage	V_{LCD1}		2.7	-	6.5	V	Note 14
LCD Power Supply Circuit Current Consumption 1	I_{LCD1}	V_{OUT}=6.0 V Double boosting V_{DD}=3.0 V V_{LCD}=5.0 V 1/4 bias Oscillating Frequency 34 kHz Display ON, Checker Display No Load of LCD Power Supply Circuit		55.0	85.0	μA	Note 15

2.2 When Using an External LCD Power Supply: FNC1="L," FNC2="L"

Table 30   Electrical Characteristics

V_{SS}=0 V, VDD=3.0±0.3V, Ta=-30 to 85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage 2	V_{DD2}	FNC1="L", FNC2="L"	2.4	-	5.5	V	Note 16
LCD Power Supply Circuit Operating Voltage 2	V_{LCD2}	FNC1="L", FNC2="L"	2.7	-	6.5	V	Note 17
LCD Power Supply Circuit Current Consumption 2	I_{LCD2}	V_{LCD2}=5.0 V 1/4-bias Oscillating Frequency 34 kHz Display ON, Checker Display No Load of LCD Power Supply Circuit		28.0	45.0	μA	Note 18

2.3 When Using an External Bias: FNC1="H," FNC2="L"

Table 31   Electrical Characteristics

V_{SS}=0 V, VDD=3.0±0.3 V, Ta=-30 to 85 °C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage Range 2	V_{DD2}	FNC1="H", FNC2="L"	2.4	-	5.5	V	Note 19
LCD Power Supply Circuit Voltage 3	V_{LCD3}	FNC1="H" FNC2="L"	2.7	-	6.5	V	Note 20
Bias Voltage	V_1, V_3		1.2	-	V_{LCD3} -0.4	V	Note 21
Input Voltage	V_2, V_4		0.4	-	V_{LCD3} -1.2		
LCD Power Supply Circuit Current Consumption 3	I_{LCD3}	V_{LCD3}=3.0V 1/3-bias Oscillating Frequency 34 kHz Display ON, Checker Display No Load of LCD Driver		10.0	15.0	μA	Note 22

2.4 Reference Voltage Circuit

Table 32　Reference Voltage

V_{SS}=0 V,　V_{DD}=3.0±0.3 V,　Ta=25 °C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Reference Voltage	V_{REF}	ΔV_{REF}=0.01% / °C	1.3	1.7	2.1	V	Note　23
		ΔV_{REF}=- 0.13% / °C	1.3	1.7	2.1		

3.　Reference

Table 33　Input Pin Capacity

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input Pin Capacity	C_{IN}	Ta=25 °C	-	5	8	pF	Note　4

Note 1　Sharp variation in the supply voltage or input signal voltage due to strange noises may lead to a malfunction of the IC. Supply stable supply voltage and input signal voltage.
If you change the level of the supply voltage intentionally, a malfunction may occur. NEVER change the level of the supply voltage.

Note 2　The maximum operating voltage of the logic is 5.5 V when an internal booster is not used.

Note 3　Pins RS, E, RWX, RESX, C86, P/SX, OSC1, FNC1, and FNC 2.

Pins D0 to D7 during display data write and command input.
Fully swing the levels VIH and VIL of the input signal within the range of power supply voltage so that the state is VIH=VDD, VIL=VSS. When the level of VIH and VIL is the middle level of the supply voltage, the through-current flowing through the input pin as well as the current consumption may be increased.

Note 4　Pins D0 to D7.

Note 5　Pins RS, E, RWX, RESX, C86, P/SX, FNC1, and FNC 2.

Note 6　Pins D0 to D7 during write and high-impedance.

Note 7　ON resistance between LCD drive output pins (SEG1 to SEG60, COM1 to COM16) and LCD drive bias voltage pins (V1, V2, V3, V4). Measure the current which flows after applying a 0.1-V difference between the LCD drive bias voltage pins (V1, V2, V3, V4) and LCD drive output pins in the external VLCD voltage input mode (FNC1, 2="HL").

Note 8　Power save state. When turning the input pin to "Floating," the through-current flows. Connect and fix the input pins to VSS or VDD.

Note 9　Shows the current consumption during display including CR oscillation.
It includes the current consumed by the booster, LCD supply voltage adjustment circuit, voltage regulator, LCD bias resistor when using the internal booster. The LCD drive output pin is no load. It does not include the current consumed by the LCD panel and wiring capacitor.   Measure it without access from the MPU.

Note 10　Shows the current consumption only for the logic during display including CR oscillation.
It does not include the current consumed by the LCD power supply systems, such as the booster, LCD supply voltage adjustment circuit, and voltage regulator, when using the external LCD power supply. The LCD drive output pin is no load. It does not include the current consumed by the LCD panel and wiring capacitor. Measure it without access from the MPU.

Note 11　Shows the wait time from when the reset ends at the rising edge of the RESX to when normal operation is possible.

Note 12　Specifies the minimum reset pulse width.

Note 13　Since the maximum output voltage of the booster is 7.2 V, the maximum operating voltage of the LCD power supply circuit including the logic and the booster is 3.6 V.

Note 14   Set output voltage VLCD of the voltage regulator so that VOUT - V LCD$\geq$0.2 V and the output voltage is 6.0 V at maximum.

Note 15   Shows the value of the current consumed by the booster, voltage regulator, voltage follower, internal bias resistor, and LCD driver. It does not include the value IRREG=V5/(R1+R2+R3) of the current flowing through external resistors R1, R2, and R3. Also, it does not include the value of the current consumed by the LCD panel. All of the current consumed during display are IDD1. Current consumed by the logic is IDD2. ILCD1 cannot be measured. ILCD1 - IDD2 is equivalent to ILCD1.

Note 16   Since the booster is not used, the maximum operating voltage of the logic is 5.5 V.

Note 17   Shows the operating voltage range of the voltage follower, internal bias resistor, and LCD driver.

Note 18   Shows the current consumed by the voltage follower, internal bias resistor, and LCD driver. It does not include the current consumed by the LCD panel. The current consumed during display is IDD2 + ILCD2. The current consumed by only the logic is ILCD2.

Note 19   Since the booster is not used, the maximum operating voltage of the logic is 5.5 V.

Note 20   Shows the operating voltage range of the voltage follower and LCD driver.

Note 21   V1, V2, V3 and V4 are limited by the voltage level within the input voltage range. Therefore, the bias ratio can be freely determined.

Note 22   Shows the current consumed by the voltage follower and LCD driver. It does not include the current consumed by the LCD panel. The current consumed during display is IDD2 + ILCD3. The current consumed by only the logic is ILCD2.

Note 23   Shows different characteristics depending upon the temperature coefficient selected by the corresponding command.

Note 24   When the frame frequency and the fluorescent lamp's frequency are the same, the display screen may flicker. Taking into consideration fluctuation in the IC and the oscillating resistor, as well as the temperature characteristics, determine the appropriate oscillating frequency.
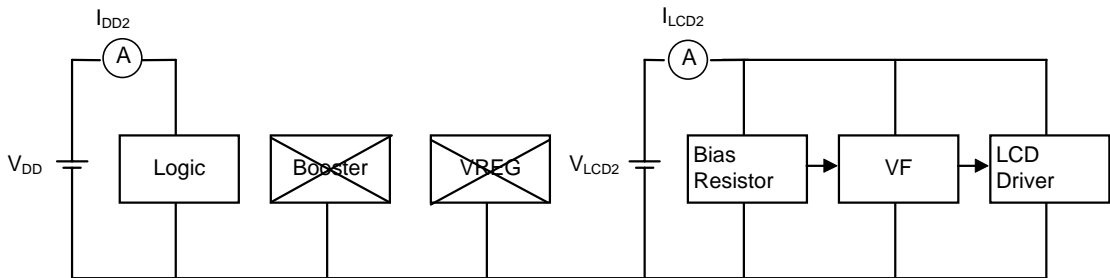
■ **Current Consumption Measurement Examples**

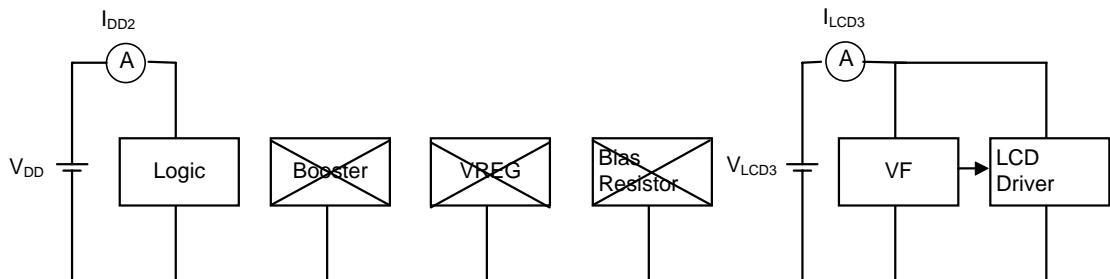1. Current Consumption of (FNC1, 2="H H") when using a booster:
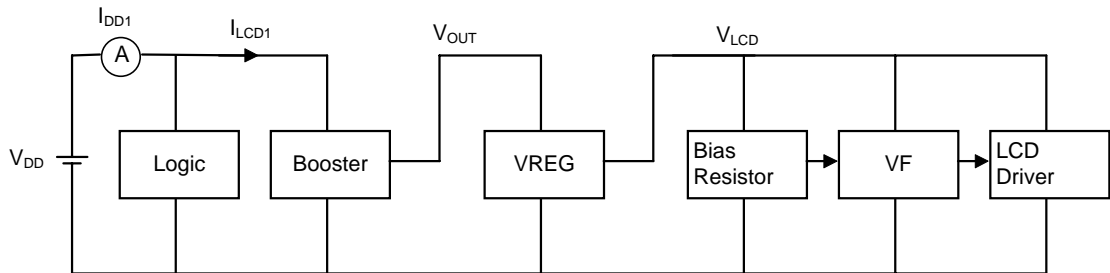
Remark: The current consumed by the LCD power supply circuit I_{LCD1} cannot be measured. It is equivalent to $I_{LCD1} = I_{DD1} - I_{DD2}$.

2. Current Consumption of (FNC1, 2="L L") when using an external power supply:

3. Current Consumption of (FNC1, 2="H L") when using an external bias resistor:

Remark: VREG: Voltage Regulator
VF: Voltage Follower

Figure 18 Current Consumption Measurement Examples

■ **Timing Characteristics**

1. Parallel Interface

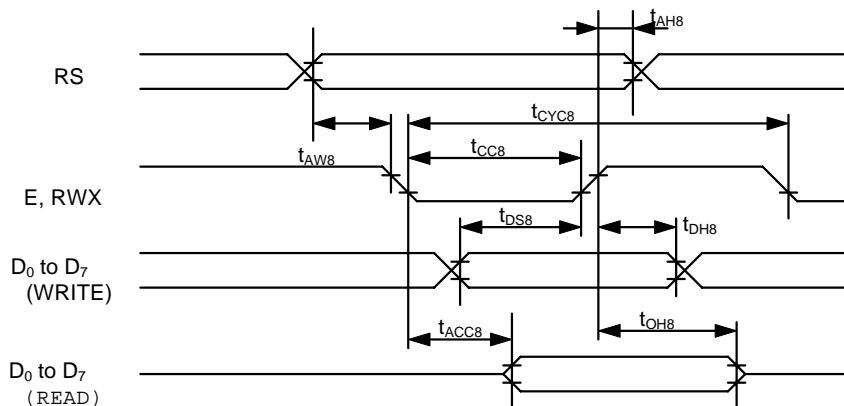**1.1 80-Family MPU Read/Write Timing Characteristics**

Figure 19   80-Family MPU Read/Write Timing Characteristics

Table 34 80-Family MPU Read/Write Timing Characteristics When VDD=3 V

(Ta=-30 to 85 °C, V_{DD}=3.0±0.3 V)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
RS	t_{AH8}	Address Hold Time		40	—	ns	
	t_{AW8}	Address Setup Time		40	—	ns	
E, RWX	t_{CYC8}	System Cycle Time		1000	—	ns	
	t_{CC8}	Control Pulse Width		200	—	ns	
D_0 to D_7	t_{DS8}	Data Setup Time		160	—	ns	
	t_{DH8}	Data Hold Time		40	—	ns	
	t_{ACC8}	Data Read Access Time	CL=15 pF		180	ns	
	t_{OH8}	Output Disable Time	CL=15 pF	10	120	ns	

Remarks: •   Rise/fall time of the input signal is 15 sec. or less.
   •   Timing is specified at 20% or 80% of the signal waveform.

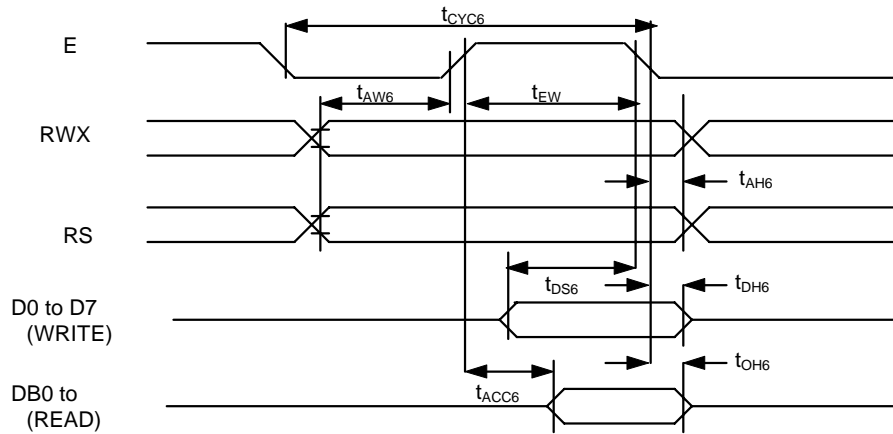### 1.2 68-Family MPU Read/Write Timing Characteristics

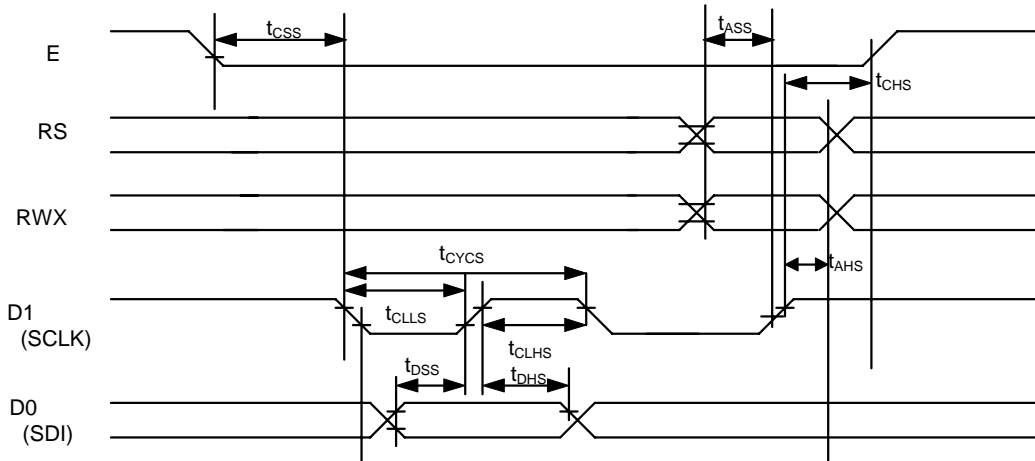**Figure 20 68-Family MPU Read/Write Timing**

Table 35 68-Family MPU Read/Write Timing Characteristics When VDD=3 V

(Ta=-30 to 85 °C, VDD=3.0±0.3 V)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
RS, RWX	t_{CYC6}	System Cycle Time		1000	—	ns	
	t_{AH6}	Address Hold Time		40	—	ns	
	t_{AW6}	Address Setup Time		40	—	ns	
D_0 to D_7	t_{DS6}	Data Setup Time		160	—	ns	
	t_{DH6}	Data Hold Time		40	—	ns	
	t_{ACC6}	Access Time	CL=15 pF		180	ns	
	t_{OH6}	Output Disable Time	CL=15 pF	10	120	ns	
E	t_{EW}	Enable Pulse Width	READ	200	—	ns	
			WRITE	160	—	ns	

Remarks: • Rise/fall time of the input signal is 15 sec. or less.
  • Timing is specified at 20% or 80% of the signal waveform.

2. Serial Interface

Figure 12 Serial Interface Read/Write Timing

**Table 36 Serial Interface Timing Characteristics When VDD=3V**

(Ta=-30 to 85 °C, V_{DD}=3.0±0.3 V)

Signal	Symbol	Designation	Conditions	Min.	Max.	Unit	Note
E	tCSS	Chip Select Setup Time		0		ns	
	tCHS	Chip Select Hold Time		50		ns	
RS, RWX	tASS	Address Setup Time		50		ns	
	tAHS	Address Hold Time		50		ns	
D0	tDSS	Data Setup Time		50		ns	
(SDI)	tDHS	Data Hold Time		50		ns	
D1	tCYCS	Clock Cycle Time		250		ns	
(SCLK)	tCLLS	Clock L Time		100		ns	
	tCLHS	Clock H Time		100		ns	

Remarks: • Rise/fall time of the input signal is 15 sec. or less.
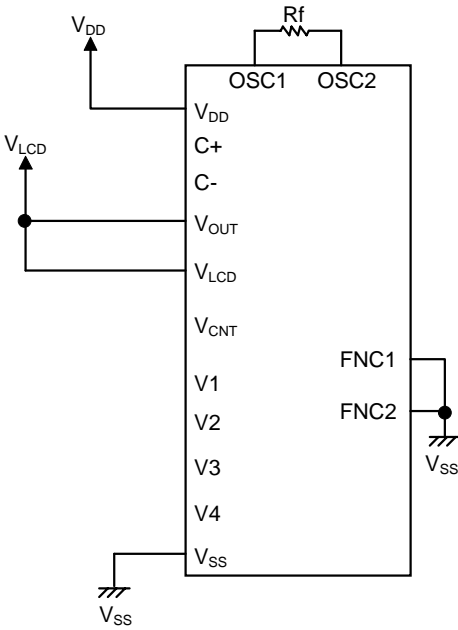   • Timing is specified at 20% or 80% of the signal waveform.

■ **Examples Application Circuits**

● When using an internal LCD power supply circuit (doubler):
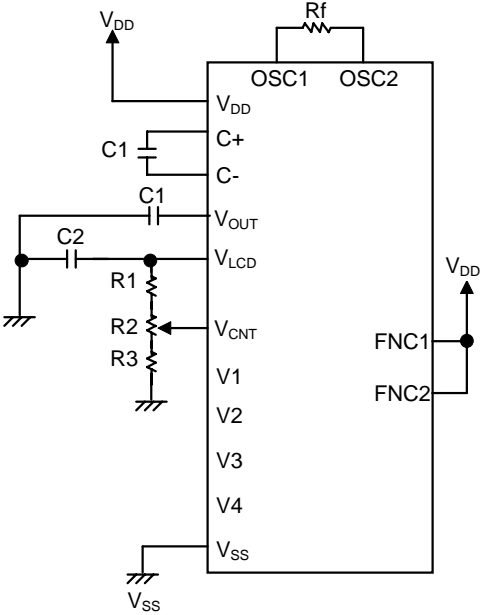
- Reference -
Rf=500 kΩ
C1= 0.47 μF
C2= 1 μF
R1+R2+R3 = 2MΩ

● When using external LCD power supply:
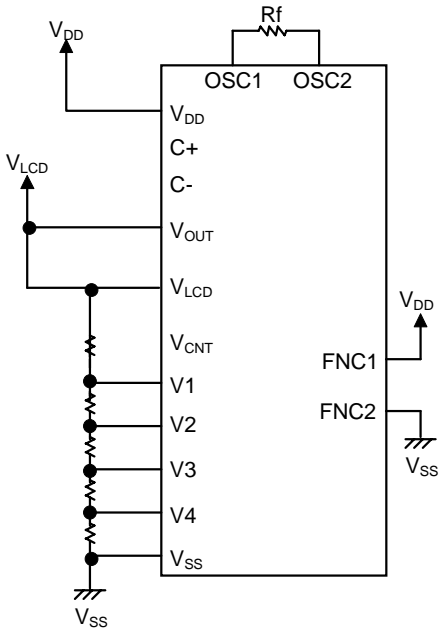
● When an external bias resistor is connected:

Figure 22 Examples Application Circuits

Chart 002: Relationship between Character Codes and Character Patterns

Upper / Lower	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	CG RAM (2)															
0010	CG RAM (3)															
0011	CG RAM (4)															
0100	CG RAM (5)															
0101	CG RAM (6)															
0110	CG RAM (7)															
0111	CG RAM (8)															
1000	CG RAM (1)															
1001	CG RAM (2)															
1010	CG RAM (3)															
1011	CG RAM (4)															
1100	CG RAM (5)															
1101	CG RAM (6)															
1110	CG RAM (7)															
1111	CG RAM (8)															

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