



STE30NK90Z

N-CHANNEL 900V - 0.21Ω - 28A ISOTOP
Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

| TYPE | V _{DSS} | R _{DS(on)} | I _D | P _w |
|------------|------------------|---------------------|----------------|----------------|
| STE30NK90Z | 900 V | < 0.26 Ω | 28 A | 500 W |

- TYPICAL R_{DS(on)} = 0.21 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR WELDING EQUIPMENT

Figure 1: Package

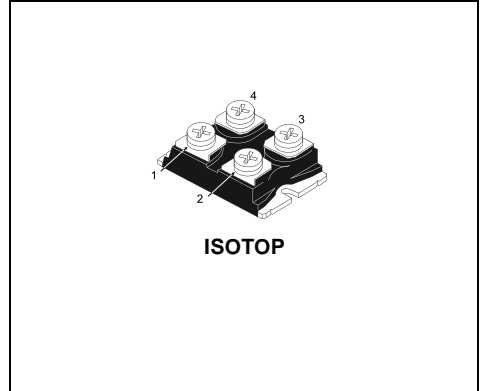


Figure 2: Internal Schematic Diagram

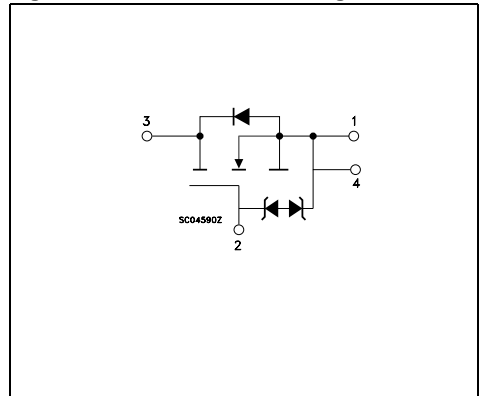


Table 2: Order Codes

| SALES TYPE | MARKING | PACKAGE | PACKAGING |
|------------|----------|---------|-----------|
| STE30NK90Z | E30NK90Z | ISOTOP | TUBE |

Table 3: Absolute Maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|--|-------------|---------------------|
| V_{DS} | Drain-source Voltage ($V_{GS} = 0$) | 900 | V |
| V_{DGR} | Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$) | 900 | V |
| V_{GS} | Gate- source Voltage | ± 30 | V |
| I_D | Drain Current (continuous) at $T_C = 25^\circ\text{C}$ | 28 | A |
| I_D | Drain Current (continuous) at $T_C = 100^\circ\text{C}$ | 18 | A |
| $I_{DM} (*)$ | Drain Current (pulsed) | 112 | A |
| P_{TOT} | Total Dissipation at $T_C = 25^\circ\text{C}$ | 500 | W |
| | Derating Factor | 4.3 | W/ $^\circ\text{C}$ |
| $V_{ESD(G-S)}$ | Gate source ESD(HBM-C=100pF, R=1.5K Ω) | 6.5 | KV |
| dv/dt (1) | Peak Diode Recovery voltage slope | 4.5 | V/ns |
| V_{ISO} | Insulation Withstand Voltage (AC-RMS) from All Four Terminals to External Heatsink | 2500 | V |
| T_j T_{stg} | Operating Junction Temperature Storage Temperature | - 65 to 150 | $^\circ\text{C}$ |

(*) Pulse width limited by safe operating area
 (1) $I_{SD} \leq 28\text{A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$.

Table 4: Thermal Data

| | | | |
|-----------|---|------|---------------------------|
| Rthj-case | Thermal Resistance Junction-case Max | 0.23 | $^\circ\text{C}/\text{W}$ |
| Rthj-amb | Thermal Resistance Junction-ambient Max | 40 | $^\circ\text{C}/\text{W}$ |

Table 5: Avalanche Characteristics

| Symbol | Parameter | Max Value | Unit |
|----------|--|-----------|------|
| I_{AR} | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max) | 13 | A |
| E_{AS} | Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 35\text{ V}$) | 500 | mJ |

Table 6: GATE-SOURCE ZENER DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|------------|-------------------------------|---|------|------|------|------|
| BV_{GSO} | Gate-Source Breakdown Voltage | $I_{GS} = \pm 1\text{ mA}$ (Open Drain) | 30 | | | V |

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)**Table 7: On/Off**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D = 1 \text{ mA}, V_{GS} = 0$ | 900 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current ($V_{GS} = 0$) | $V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$ | | | 10 100 | μA μA |
| I_{GSS} | Gate-body Leakage Current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{V}$ | | | ± 100 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 150 \mu\text{A}$ | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS} = 10\text{V}, I_D = 14 \text{ A}$ | | 0.21 | 0.26 | Ω |

Table 8: Dynamic

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|------|-----------------------|------|----------------------|
| $g_{fs} (1)$ | Forward Transconductance | $V_{DS} = 15 \text{ V}, I_D = 14 \text{ A}$ | | 26 | | S |
| C_{iss} C_{oss} C_{rss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | $V_{DS} = 25\text{V}, f = 1 \text{ MHz}, V_{GS} = 0$ | | 12000 852 166 | | pF pF pF |
| $C_{oss \text{ eq.}} (3)$ | Equivalent Output Capacitance | $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 720 \text{ V}$ | | 377 | | pF |
| $t_{d(on)}$ t_r $t_{d(off)}$ t_f | Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time | $V_{DD} = 450 \text{ V}, I_D = 13 \text{ A}$ $R_G = 4.7\Omega, V_{GS} = 10 \text{ V}$ (see Figure 17) | | 67 59 250 72 | | ns ns ns ns |
| Q_g Q_{gs} Q_{gd} | Total Gate Charge Gate-Source Charge Gate-Drain Charge | $V_{DD} = 720 \text{ V}, I_D = 26 \text{ A},$ $V_{GS} = 10\text{V}$ (see Figure 20) | | 350 51 190 | 490 | nC nC nC |

Table 9: Source Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|---|------|----------------------|-----------|-------------------------------------|
| I_{SD} $I_{SDM} (2)$ | Source-drain Current Source-drain Current (pulsed) | | | | 28 112 | A A |
| $V_{SD} (1)$ | Forward On Voltage | $I_{SD} = 28 \text{ A}, V_{GS} = 0$ | | | 2 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | $I_{SD} = 26 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}, T_j = 25^{\circ}C$ (see Figure 18) | | 1 18.9 36.6 | | μs μC A |
| t_{rr} Q_{rr} I_{RRM} | Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current | $I_{SD} = 26 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}, T_j = 150^{\circ}C$ (see Figure 18) | | 1.33 25.2 37.8 | | μs μC A |

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Figure 3: Safe Operating Area

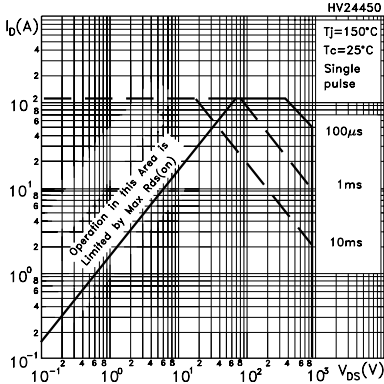


Figure 4: Output Characteristics

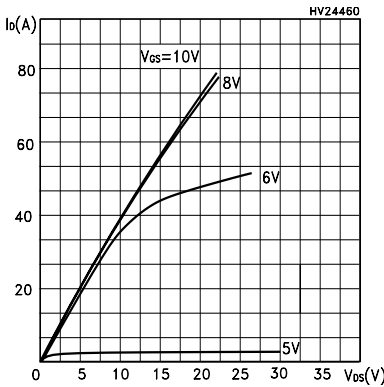


Figure 5: Transconductance

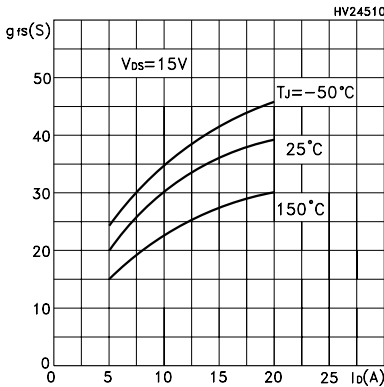


Figure 6: Thermal Impedance

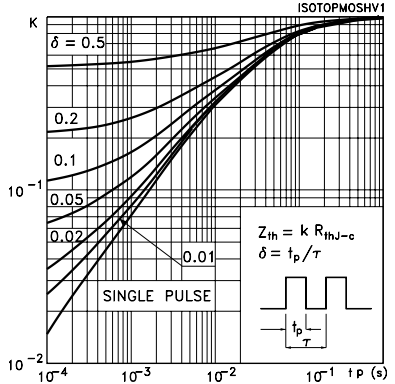


Figure 7: Transfer Characteristics

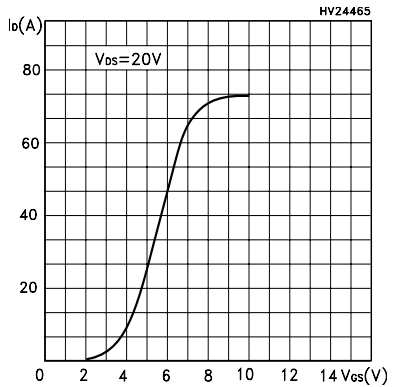


Figure 8: Static Drain-source On Resistance

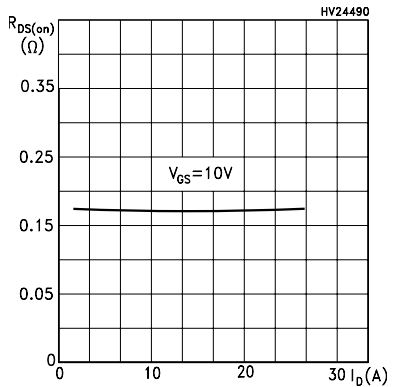


Figure 9: Gate Charge vs Gate-source Voltage

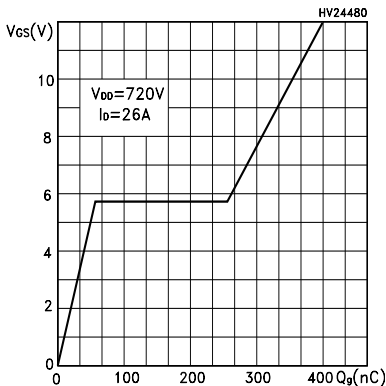


Figure 10: Normalized Gate Threshold Voltage vs Temperature

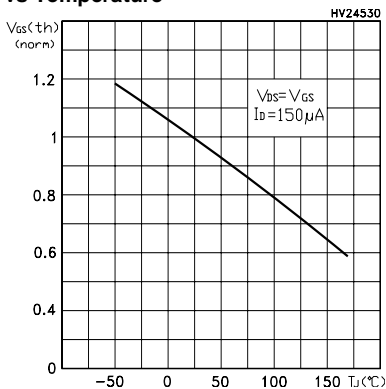


Figure 11: Source-Drain Diode Forward Characteristics

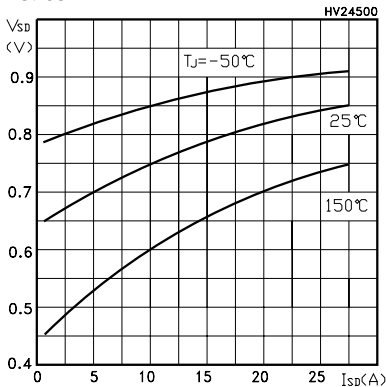


Figure 12: Capacitance Variations

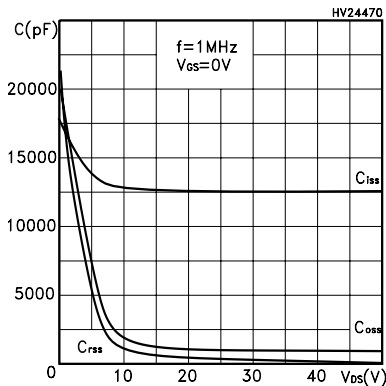


Figure 13: Normalized On Resistance vs Temperature

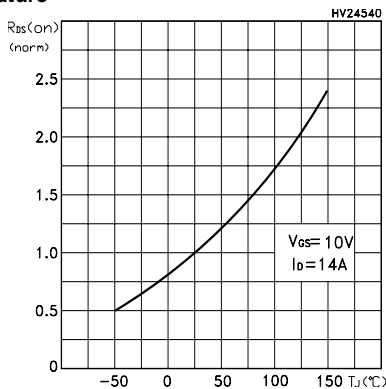


Figure 14: Normalized BVdss vs Temperature

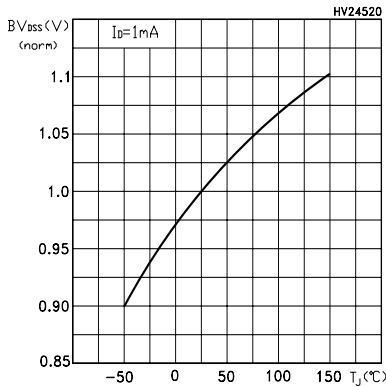


Figure 15: Avalanche Energy vs Starting Tj

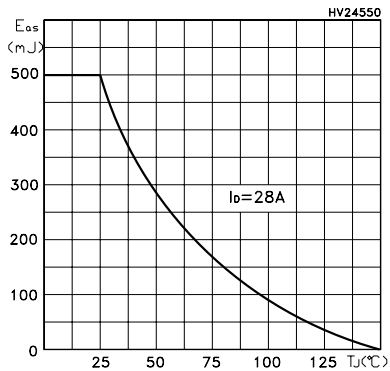


Figure 16: Unclamped Inductive Load Test Circuit

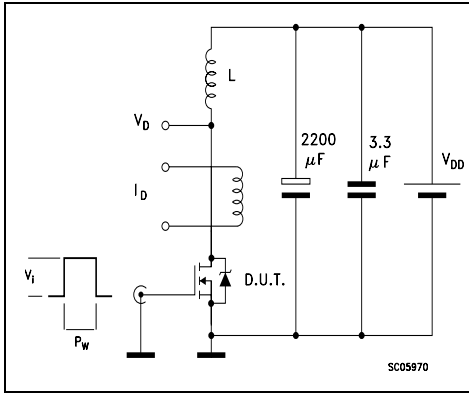


Figure 17: Switching Times Test Circuit For Resistive Load

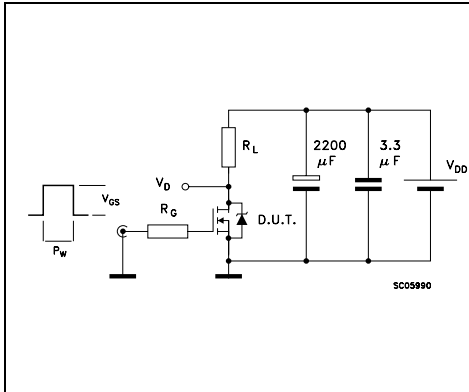


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

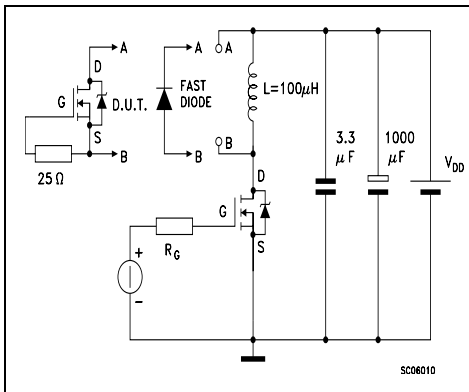


Figure 19: Unclamped Inductive Waferform

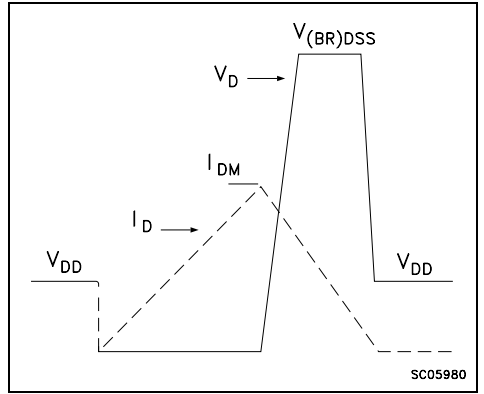
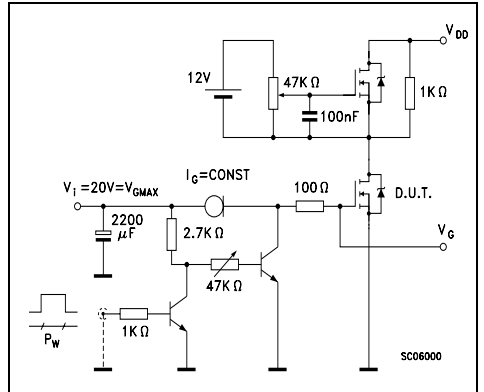


Figure 20: Gate Charge Test Circuit



ISOTOP MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-------|------|------|-------|------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 11.8 | | 12.2 | 0.466 | | 0.480 |
| B | 8.9 | | 9.1 | 0.350 | | 0.358 |
| C | 1.95 | | 2.05 | 0.076 | | 0.080 |
| D | 0.75 | | 0.85 | 0.029 | | 0.033 |
| E | 12.6 | | 12.8 | 0.496 | | 0.503 |
| F | 25.15 | | 25.5 | 0.990 | | 1.003 |
| G | 31.5 | | 31.7 | 1.240 | | 1.248 |
| H | 4 | | | 0.157 | | |
| J | 4.1 | | 4.3 | 0.161 | | 0.169 |
| K | 14.9 | | 15.1 | 0.586 | | 0.594 |
| L | 30.1 | | 30.3 | 1.185 | | 1.193 |
| M | 37.8 | | 38.2 | 1.488 | | 1.503 |
| N | 4 | | | 0.157 | | |
| O | 7.8 | | 8.2 | 0.307 | | 0.322 |

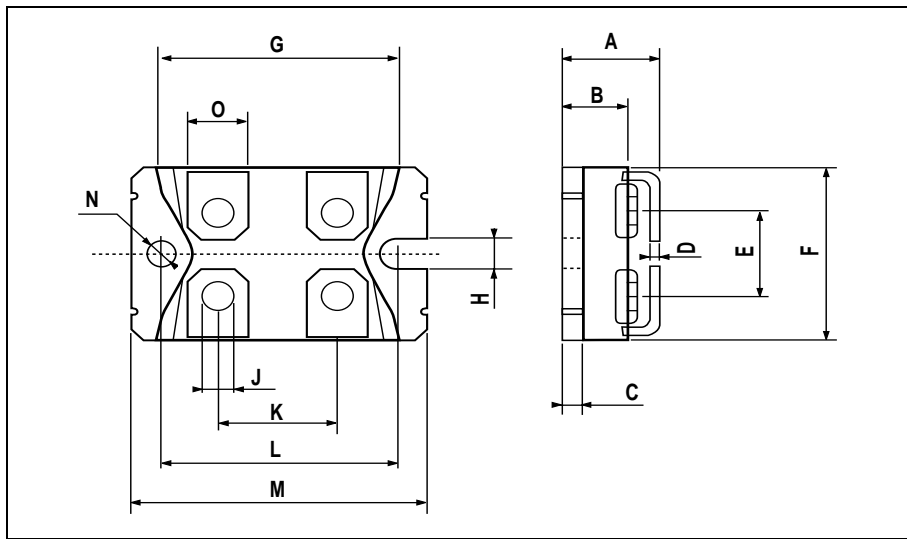


Table 10: Revision History

| Date | Revision | Description of Changes |
|-------------|-----------------|--|
| 12-May-2004 | 1 | First Release. |
| 15-Oct-2004 | 2 | New value inserted in table 3. (V_{ISO}) |
| 20-Jan-2005 | 3 | Final Datasheet |

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