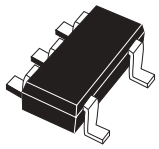
STM6717/6718/6719/6720
STM6777/6778/6779/6780

Dual/Triple Ultra-Low Voltage Supervisors with Push-Button Reset (with Delay Option)

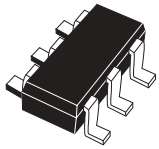
FEATURES SUMMARY

- PRIMARY SUPPLY (V_{CC1}) MONITOR. FIXED (FACTORY-PROGRAMMED) RESET THRESHOLDS: 4.63V TO 1.58V
- SECONDARY SUPPLY (V_{CC2}) MONITOR (STM6717/18/19/20/77/78). FIXED (FACTORY-PROGRAMMED) RESET THRESHOLDS: 3.08V TO 0.79V
- TERTIARY SUPPLY MONITOR (USING EXTERNALLY ADJUSTABLE RSTIN): 0.626V INTERNAL REFERENCE
- $\overline{RST}$ OUTPUTS (PUSH-PULL OR OPEN DRAIN); STATE GUARANTEED IF V_{CC1} OR $V_{CC2} \geq 0.8V$
- RESET DELAY TIME (t_{rec}) ON POWER-UP:
  - 210ms (typ)
- MANUAL RESET INPUT ($\overline{MR}$)
- OPTIONAL DELAYED MANUAL RESET INPUT (MRC) WITH EXTERNAL CAPACITOR (STM6777/78/79/80)
- LOW SUPPLY CURRENT - 11µA (TYP), $V_{CC1} = V_{CC2} = 3.6V$
- OPERATING TEMPERATURE: –40°C to 85°C (Industrial Grade)

Figure 1. Packages



SOT23-5 (WY)



SOT23-6 (WB)

Table 1. Device Options

Part Number	Monitored Voltages			Manual Reset Input ($\overline{MR}$)	Delayed $\overline{MR}$ Pin (MRC)	Reset Output ($\overline{RST}$)		Package
	V_{CC1}	V_{CC2}	RSTIN			Active-Low (Push-Pull)	Active-Low (Open Drain)	
STM6717	✔	✔		✔			✔	WY
STM6718	✔	✔		✔		✔		WY
STM6719	✔	✔	✔	✔			✔	WB
STM6720	✔	✔	✔	✔		✔		WB
STM6777	✔	✔		✔	✔		✔	WB
STM6778	✔	✔		✔	✔	✔		WB
STM6779	✔		✔	✔	✔		✔	WB
STM6780	✔		✔	✔	✔	✔		WB

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SUMMARY DESCRIPTION

The STM6717/18/19/20 and STM6777/78/79/80 Supervisors are a family of low voltage/low supply current processor (Micro or DSP) Supervisors, designed to monitor two (or three) system power supply voltages. They are targeted at applications such as Set-Top Boxes (STBs), portable, battery-powered systems, networking, and communication systems.

All device options have a push-button-type manual reset input ($\overline{MR}$). The STM6777/78/79/80 also includes an option which enables the user to delay the start of the Manual Reset process from 6µs (MRC pin left open) or more with external capacitor. The delay is implemented by connecting the appropriately sized capacitor between the MRC pin and V_{SS} (typical 4s delay with a 3.3µF capacitor, see Table 7., page 19).

Two of the three supplies monitored (V_{CC1} and V_{CC2}) have fixed (customer-selectable, factory-trimmed) thresholds (V_{RST1} and V_{RST2}). The third voltage is monitored using an externally adjustable RSTIN threshold (0.626V internal reference).

If any of the three monitored voltages drop below its factory-trimmed or adjustable thresholds, or if $\overline{MR}$ is asserted to logic low, a $\overline{RST}$ is asserted (driven low). Once asserted, $\overline{RST}$ is maintained at Low for a minimum delay period (t_{rec}) after ALL supplies rise above their respective thresholds and $\overline{MR}$ returns to High. These devices are guaranteed to be in the correct reset output logic state when V_{CC1} and/or V_{CC2} is greater than 0.8V.

These devices are available in a standard 5-pin or 6-pin SOT23 packages (see Table 1., page 1).

Figure 2. Logic Diagram (STM6717/18)

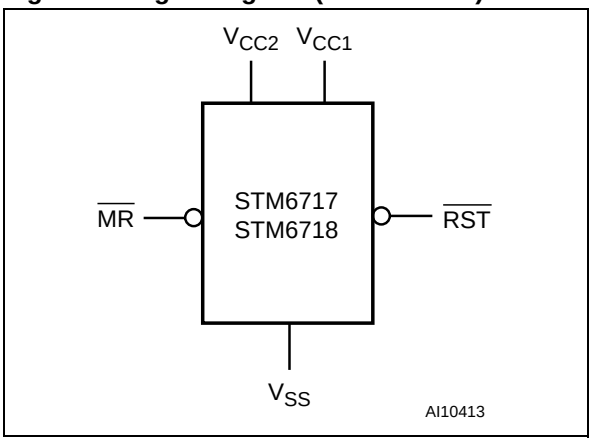


Figure 3. Logic Diagram (STM6719/20)

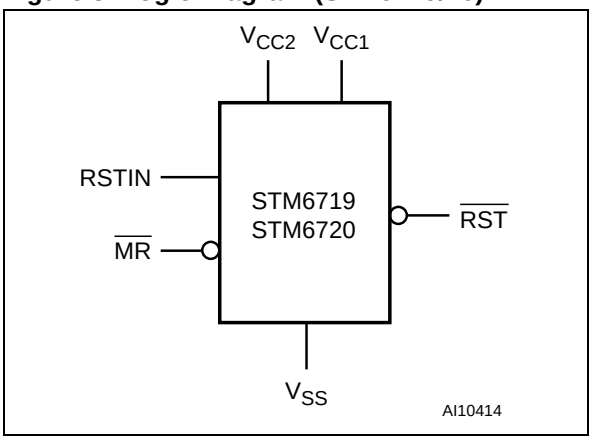


Figure 4. Logic Diagram (STM6777/78)

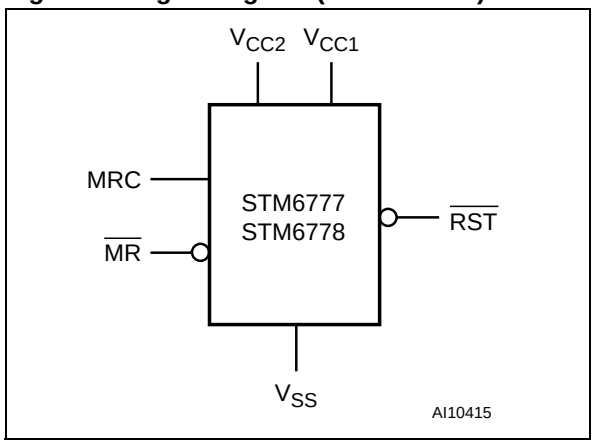


Figure 5. Logic Diagram (STM6779/80)

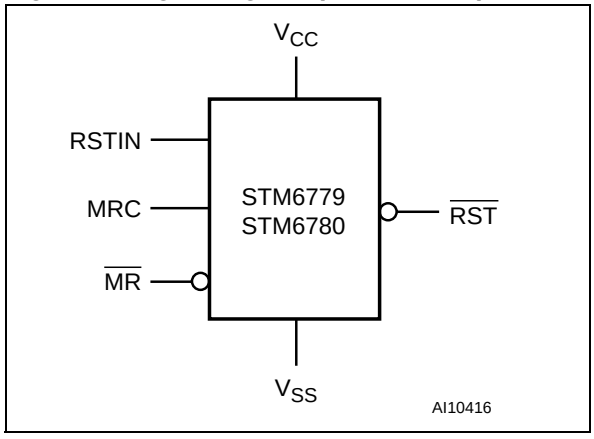


Table 2. Signal Names

$\overline{MR}$	Push-button Reset Input
MRC	Manual Reset Delay Input
$\overline{RST}$	Active-low Reset Output
V_{CC1}	Primary Supply Voltage Input
V_{CC2}	Secondary Supply Voltage Input
RSTIN	Adjustable Reset Comparator Input
V_{SS}	Ground

Figure 6. STM6717/18 SOT23-5 Connections

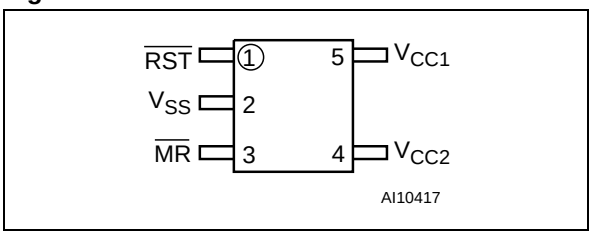


Figure 7. STM6719/20 SOT23-6 Connections

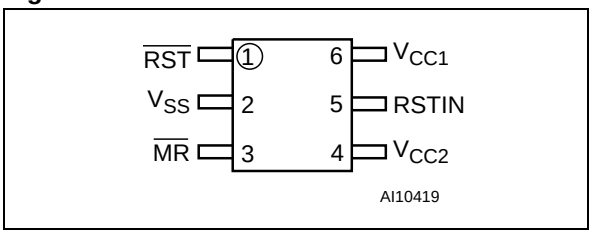


Figure 8. STM6777/78 SOT23-6 Connections

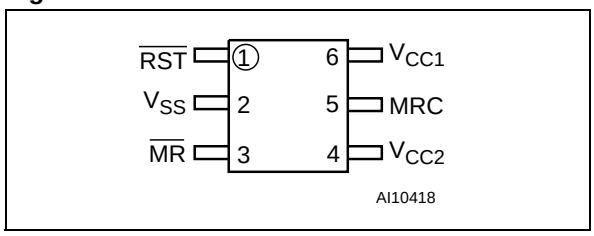
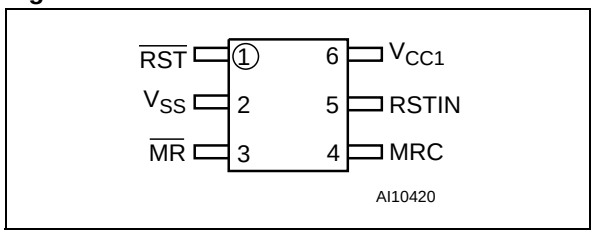


Figure 9. STM6779/80 SOT23-6 Connections



Pin Descriptions

Active-Low, Push-pull Reset Output ($\overline{RST}$) - STM6718/20/78/80. The $\overline{RST}$ pin is driven low and stays low whenever V_{CC1} or V_{CC2} or RSTIN falls below its factory-trimmed or adjustable reset threshold or when $\overline{MR}$ goes to logic low. It remains low for t_{rec} after ALL supply voltages being monitored rise above their reset thresholds and $\overline{MR}$ goes from low to high. (Push-pull outputs are referenced to V_{CC1}.)

Active-Low, Open Drain Reset Output ($\overline{RST}$) - STM6717/19/77/79. The $\overline{RST}$ pin is driven low and stays low whenever V_{CC1} or V_{CC2} or RSTIN falls below its factory-trimmed or adjustable reset threshold or when $\overline{MR}$ goes to logic low. It remains low for t_{rec} after ALL supply voltages being monitored rise above their reset thresholds and $\overline{MR}$ goes from low to high. Connect an external pull-up resistor to V_{CC1}. A 10kΩ pull-up resistor should be sufficient for most applications.

Push-Button Reset Input ($\overline{MR}$). When $\overline{MR}$ goes low the $\overline{RST}$ output is driven low. $\overline{RST}$ remains low as long as $\overline{MR}$ is low and for t_{rec} after $\overline{MR}$ returns to high. This active-low input has an internal 50kΩ pull-up resistor to V_{CC1}. It can be driven from a TTL or CMOS logic line, or with open drain/collector outputs, or connected to V_{SS} through a switch. If unused, leave this pin open or connect it to V_{CC1}. Connect a normally open momentary switch from $\overline{MR}$ to V_{SS}; external debounce circuitry is not required. (If $\overline{MR}$ is driven from long cables or if the device is used in noisy environments, connecting a 0.1µF capacitor from $\overline{MR}$ to V_{SS} provides additional noise immunity.

Manual Reset Delay Input (MRC) - STM6777/78/79/80). This pin is either left open or connected to V_{SS} via a capacitor. By selecting the appropriate capacitor, the manual reset process, initiated by pressing the push-button Manual Reset Input, can be delayed by any value from 6µs or more (see Table 7., page 19).

Primary Supply Voltage Monitoring Input (V_{CC1}). It also is the input for the primary reset threshold monitor. Available fixed (customer-selectable, factory-programmed) reset thresholds include 4.63V to 1.58V.

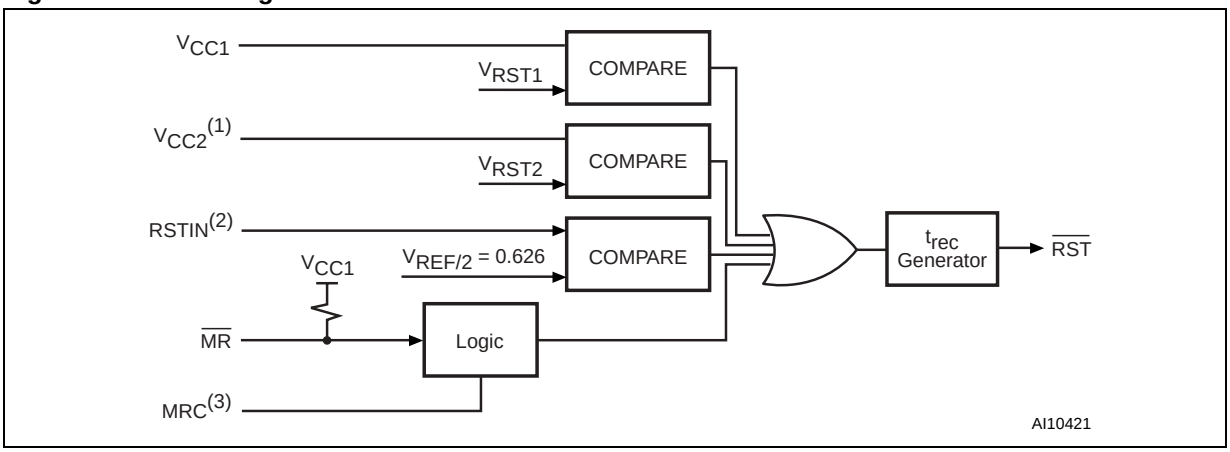
Secondary Supply Voltage Monitoring Input (V_{CC2}). This function is available on the STM6717/18/19/20/77/78. Fixed (customer-selectable, factory-programmed) reset thresholds include 3.08V to 0.79V.

Adjustable Reset Comparator Input (RSTIN; STM6719/20/79/80). This is a high impedance input. $\overline{RST}$ is driven low when the voltage at the RSTIN pin falls below 0.626V (internal reference voltage at this comparator). The monitored voltage reset threshold is set with an external resistor-divider network.

Table 3. Pin Functions

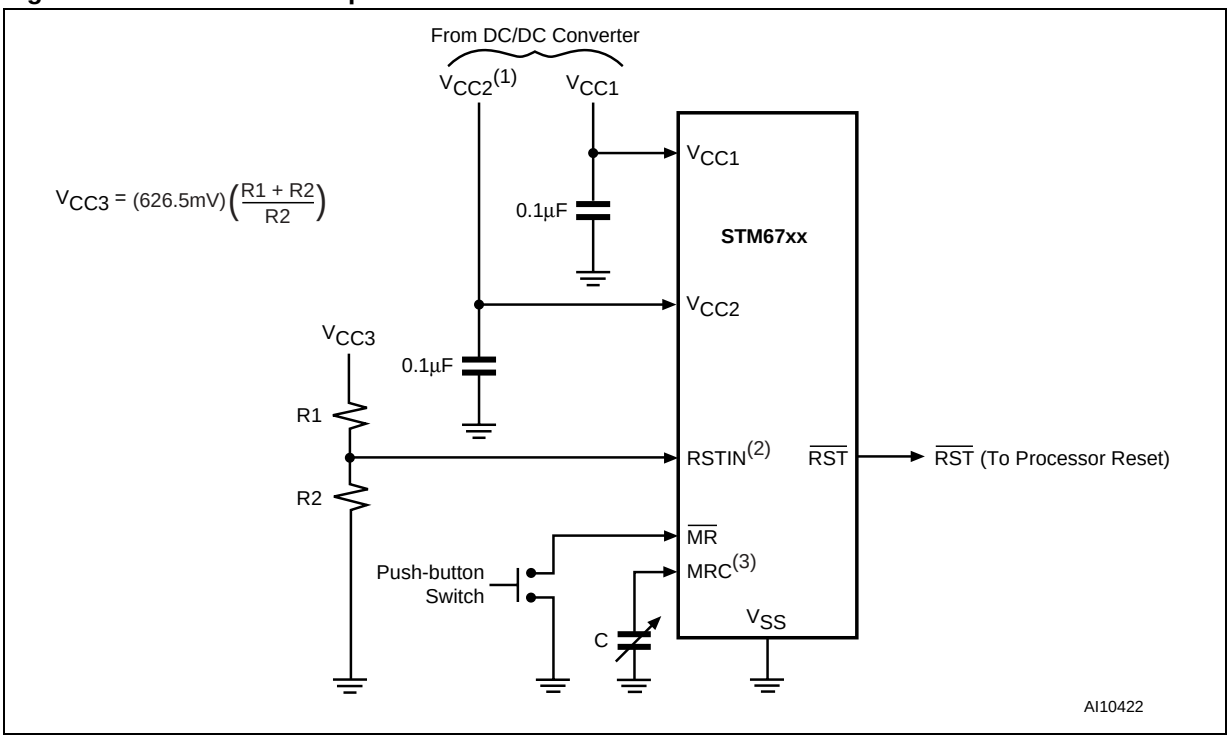
Pin				Name	Function
STM6717 STM6718	STM6719 STM6720	STM6777 STM6778	STM6779 STM6780		
1	1	1	1	$\overline{RST}$	Active-low Reset Output
3	3	3	3	$\overline{MR}$	Push-button Reset Input
–	–	5	4	MRC	Manual Reset Delay Input
5	6	6	6	V_{CC1}	Primary Supply Voltage Input
4	4	4	–	V_{CC2}	Secondary Supply Voltage Input
–	5	–	5	RSTIN	Adjustable Reset Comparator Input
2	2	2	2	V_{SS}	Ground

Figure 10. Block Diagram



Note: 1. V_{CC2} Input is available on STM6717/18/19/20/77/78.
2. RSTIN available only on STM6719/20/79/80.
3. MRC available only on STM6777/78/79/80.

Figure 11. Hardware Hookup



Note: 1. V_{CC2} is available only on STM6717/18/19/20/77/78.
2. RSTIN available only on STM6719/20/79/80.
3. MRC available only on STM6777/78/79/80.

OPERATION

Applications Information

1. Interfacing to Processors with Bi-directional Reset Pins

   Most processors with bi-directional reset pins can interface directly to the open drain $\overline{RST}$ outputs (STM6717/19/77/79). Systems simultaneously requiring a push-pull $\overline{RST}$ output and a bi-directional reset interface can be in logic contention. To prevent this contention, connect a 4.7kΩ resistor between $\overline{RST}$ and the processor's Reset I/O as shown in Figure 12.

2. Ensuring a Valid $\overline{RST}$ Output Down to V_{CC} = 0V

The STM67xx Supervisors are guaranteed to be in the correct $\overline{RST}$ output logic state when V_{CC1} and/or V_{CC2} is greater than 0.8V. In applications which require valid reset levels down to V_{CC} = 0, a pull-down resistor to active-low outputs (push-pull only, see Figure 13.) will ensure that the reset line is valid while the reset output can no longer sink or source current. This scheme does NOT work with the open drain outputs of the STM6717/19/77/79.

The resistor value used is not critical, but it must be large enough not to load the reset output when V_{CC} is above the reset threshold. For most applications, 100kΩ is adequate.

Figure 12. STM67xx Interface to Processor with Bi-directional Reset Pins

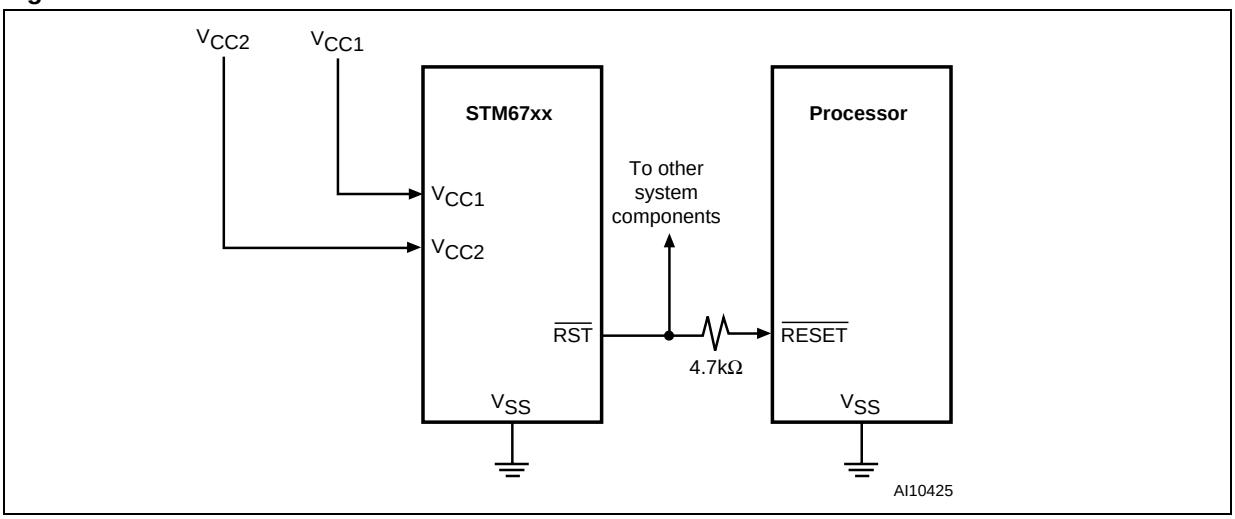
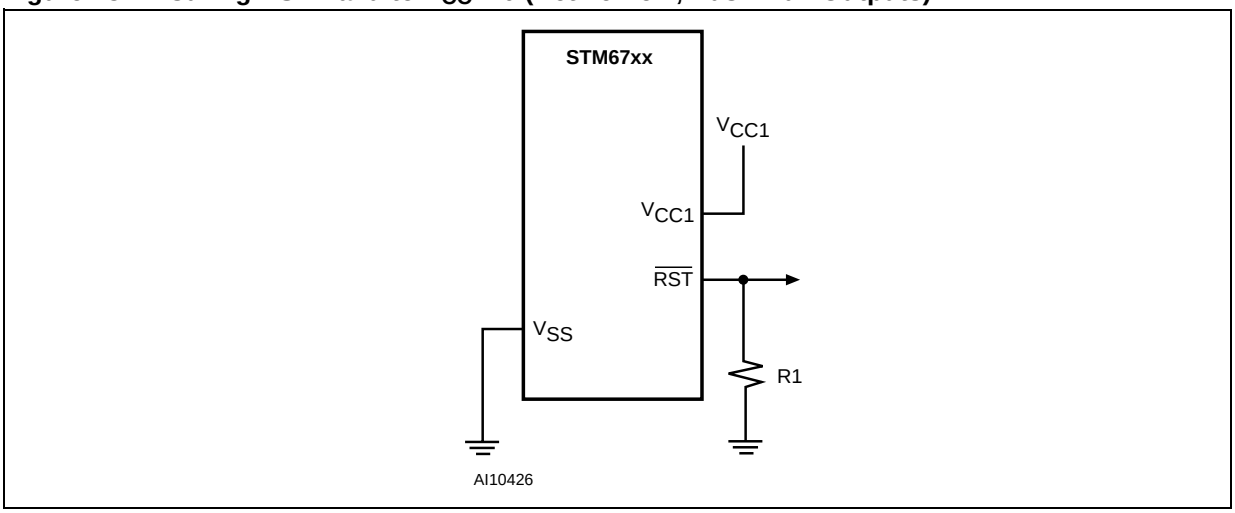


Figure 13. Ensuring $\overline{RST}$ Valid to V_{CC} = 0 (Active-Low, Push-Pull Outputs)



TYPICAL OPERATING CHARACTERISTICS

Note: Typical values are at T_A = 25°C unless otherwise noted.

Figure 14. Supply Current vs. Temperature (V_{CC1} = 5.5V; V_{CC2} = 3.6V)

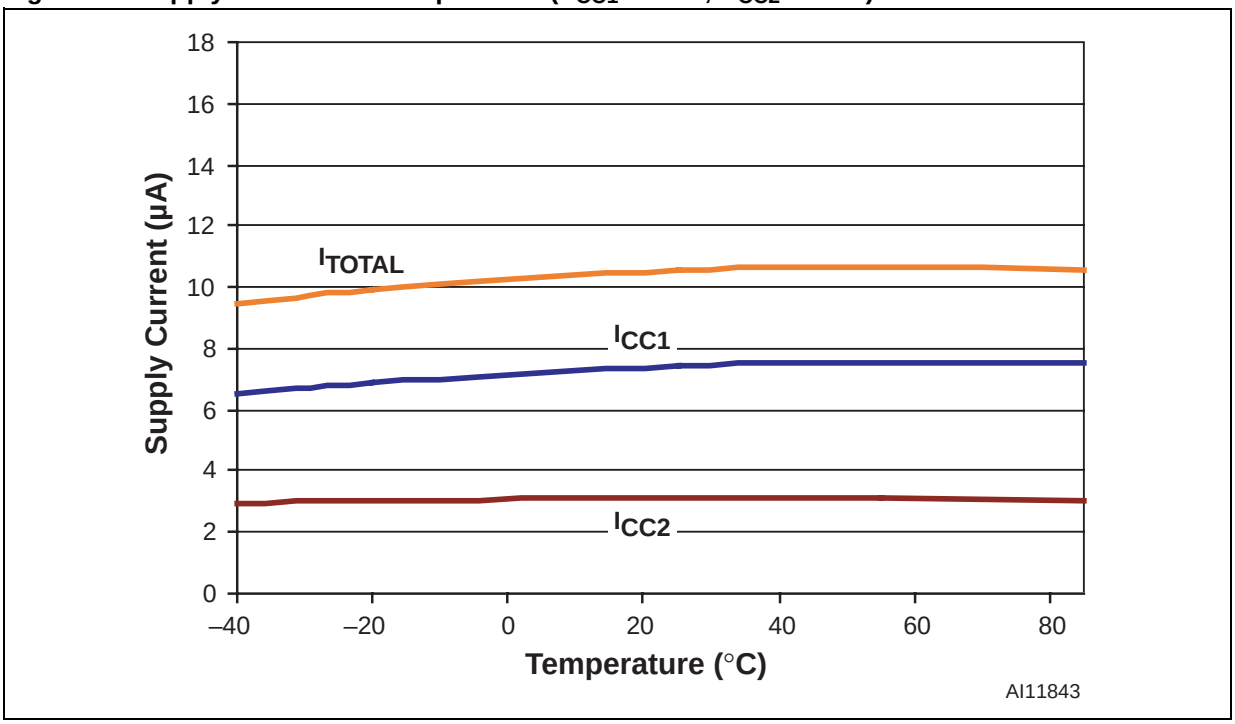


Figure 15. Supply Current vs. Temperature (V_{CC1} = 3.6V; V_{CC2} = 2.75V)

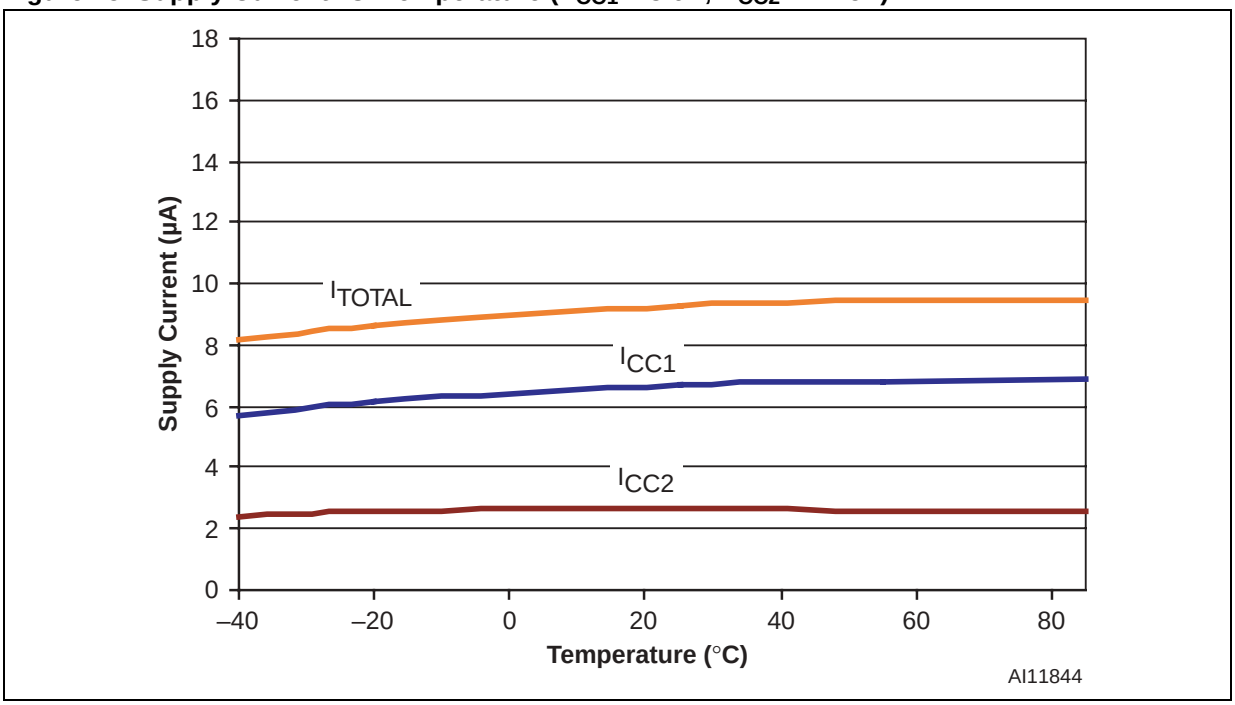


Figure 16. Supply Current vs. Temperature (V_{CC1} = 3.0V; V_{CC2} = 2.0V)

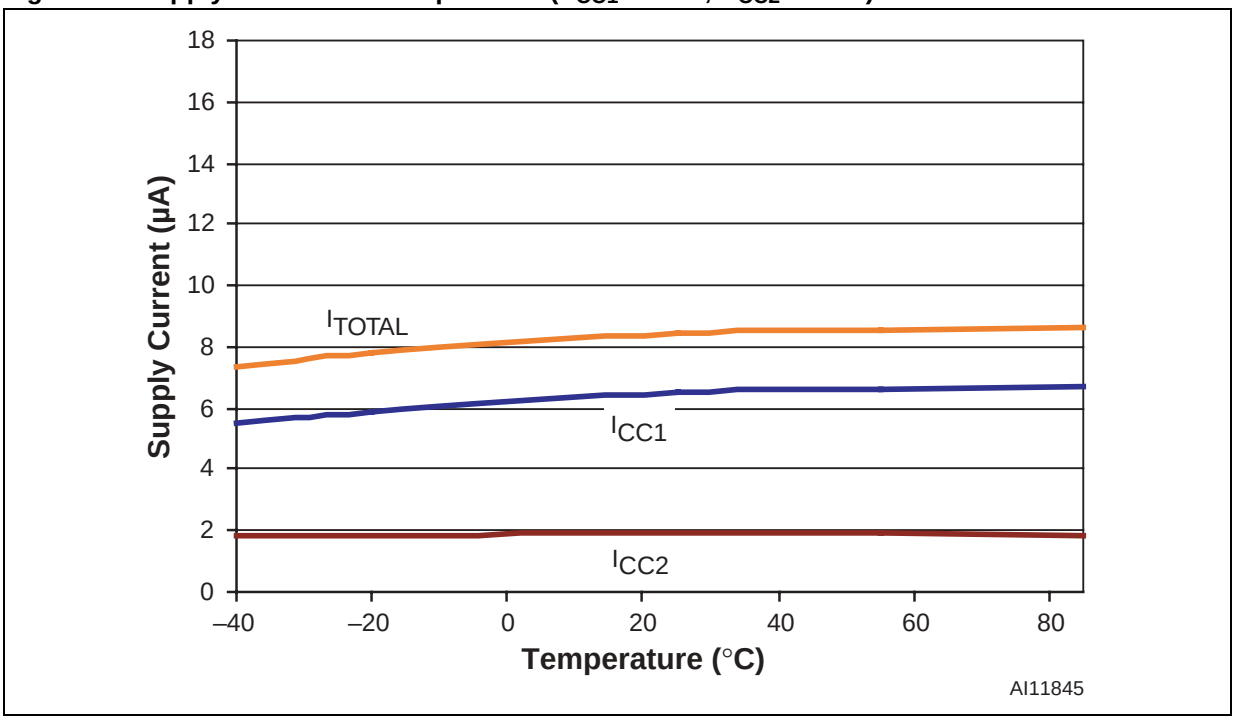


Figure 17. Supply Current vs. Temperature (V_{CC1} = 2.0V; V_{CC2} = 1.0V)

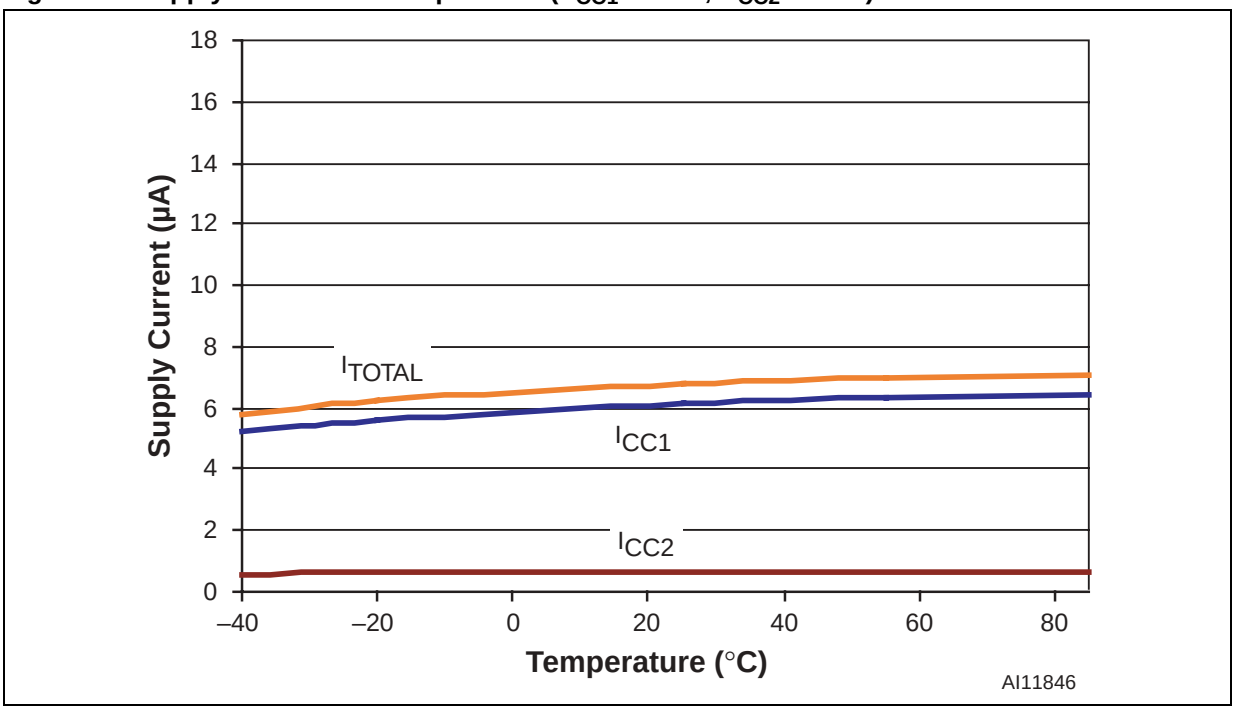


Figure 18. Normalized V_{CC} Reset Time-out Period vs. Temperature

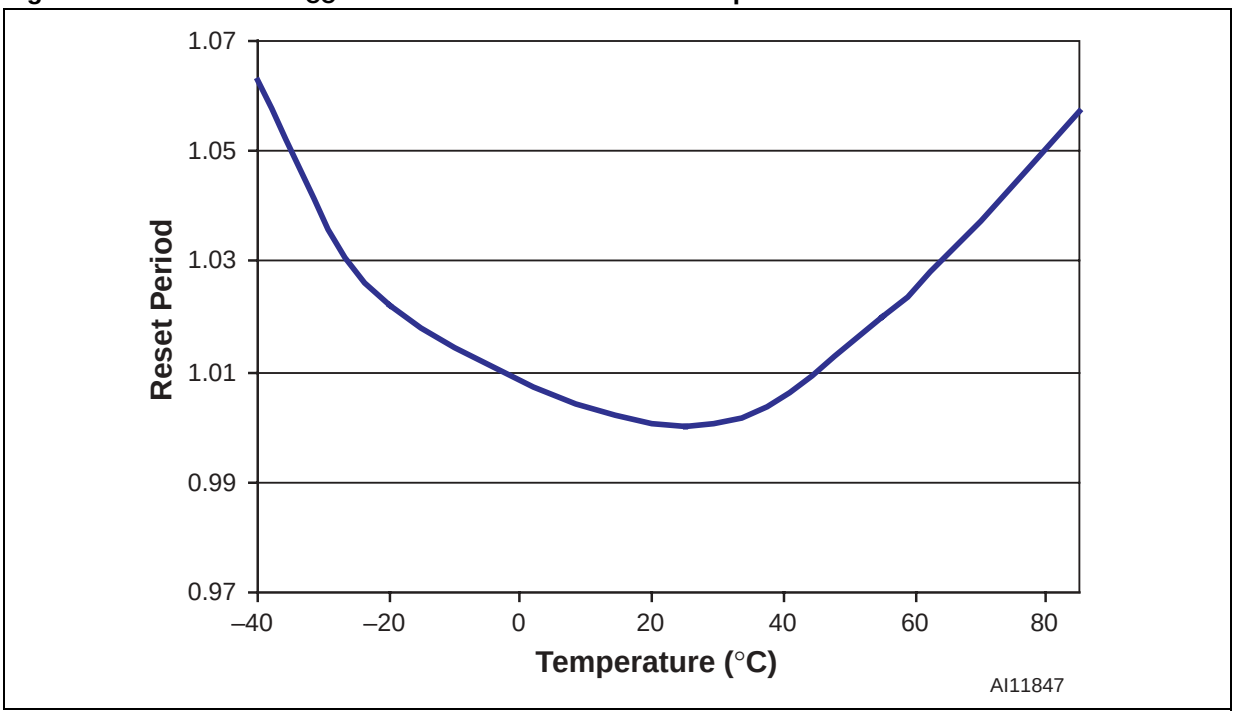


Figure 19. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

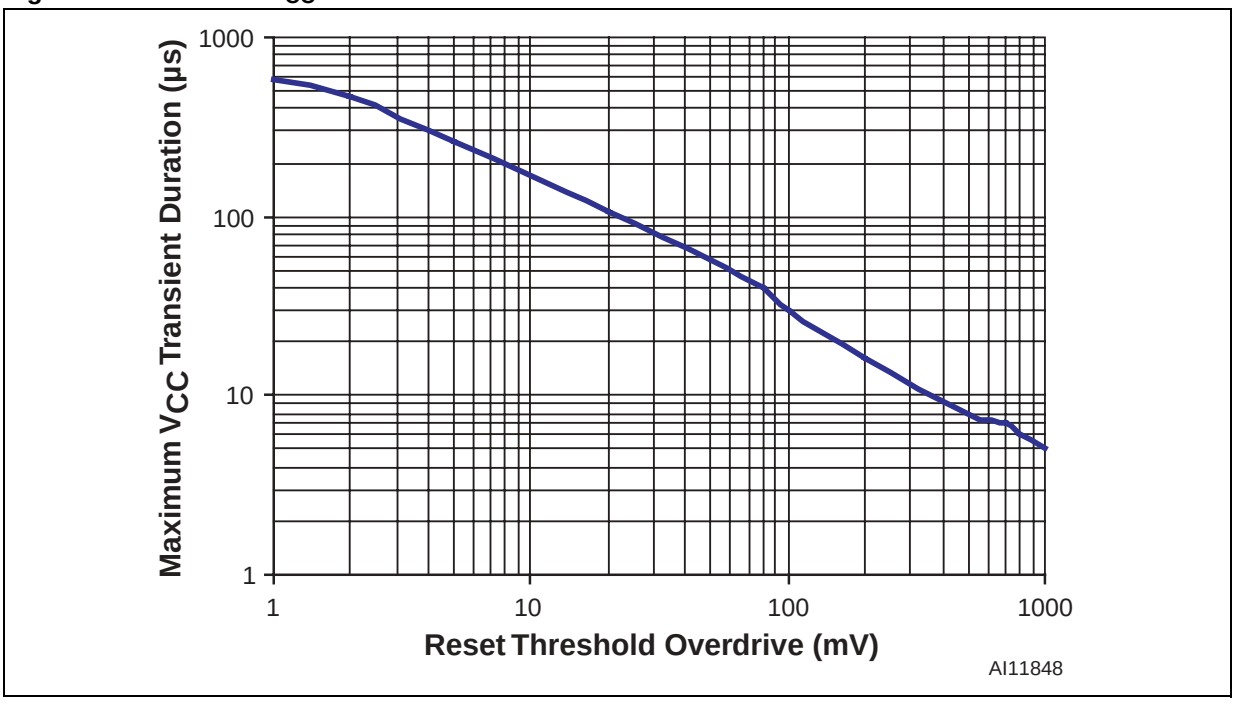


Figure 20. Normalized V_{RST1} Threshold vs. Temperature

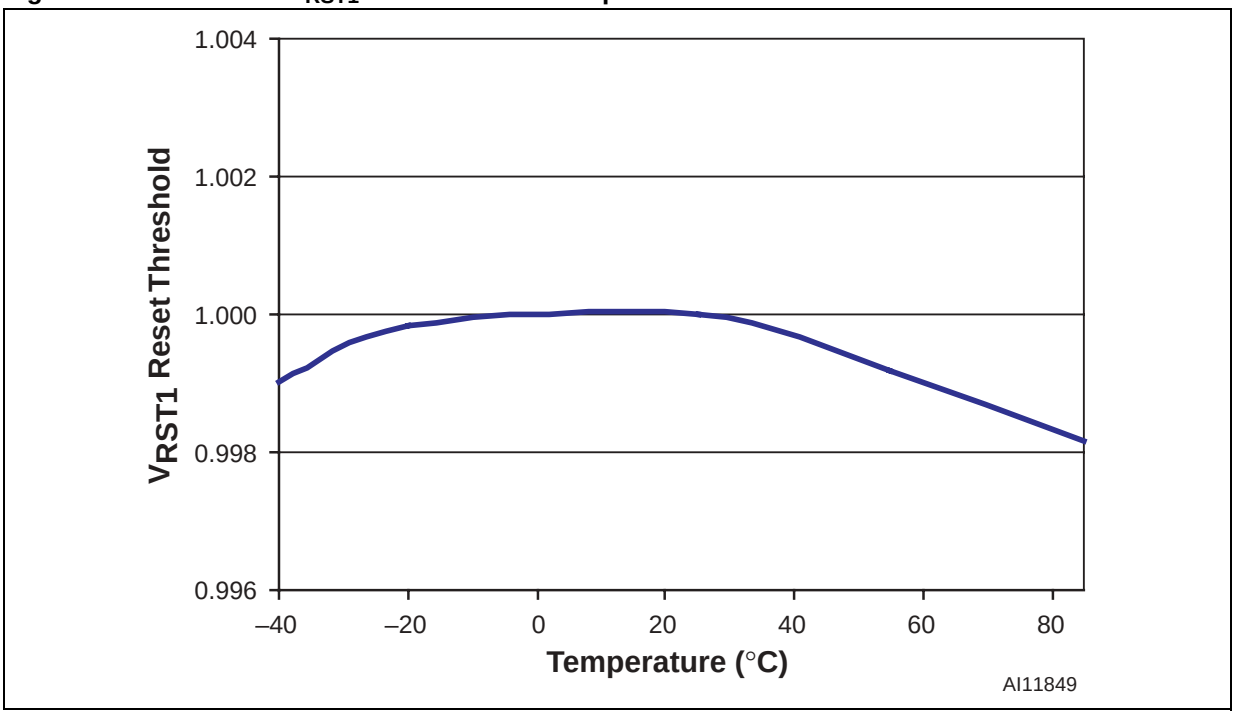


Figure 21. Normalized V_{RST2} Threshold vs. Temperature

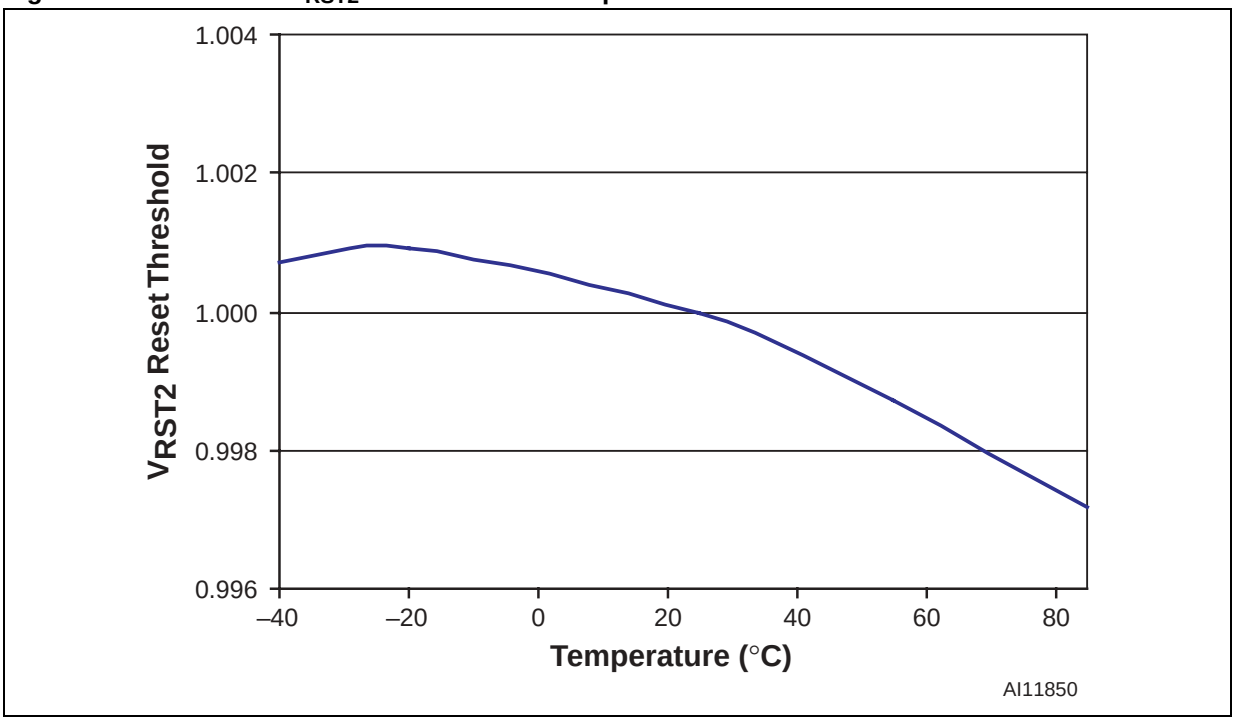


Figure 22. Reset Input Threshold vs. Temperature

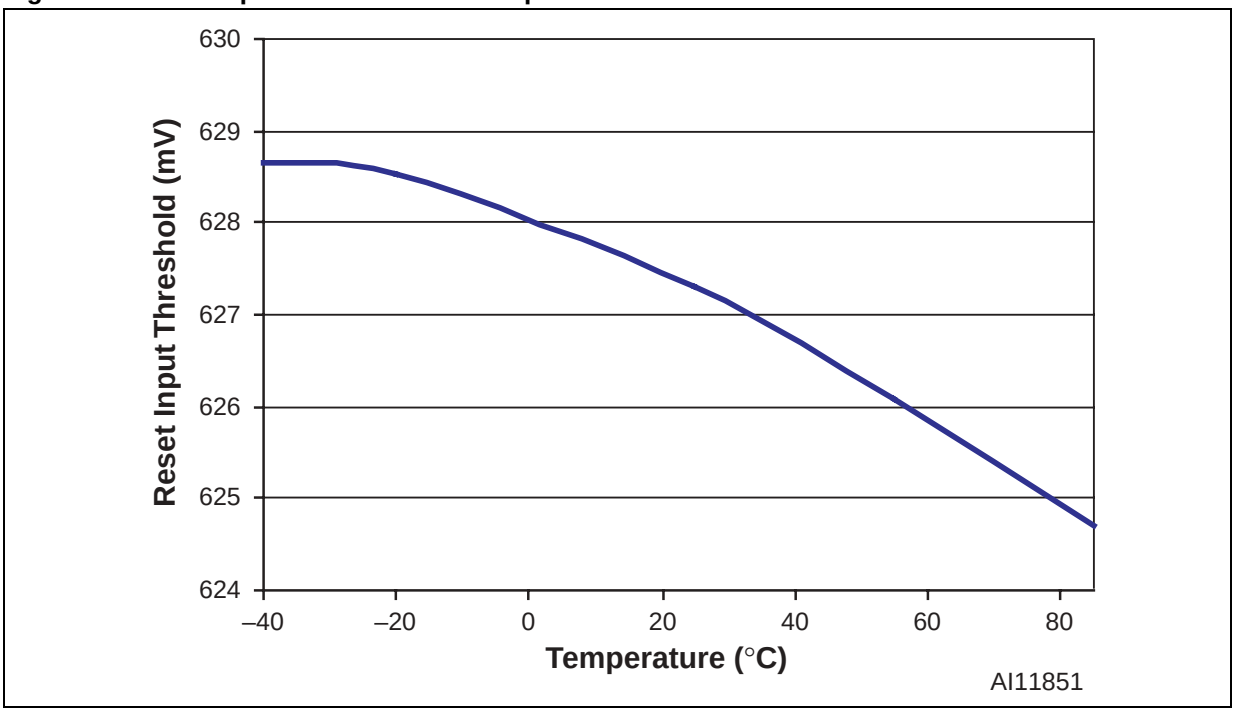


Figure 23. V_{CC1}-to-Reset Delay vs. Temperature

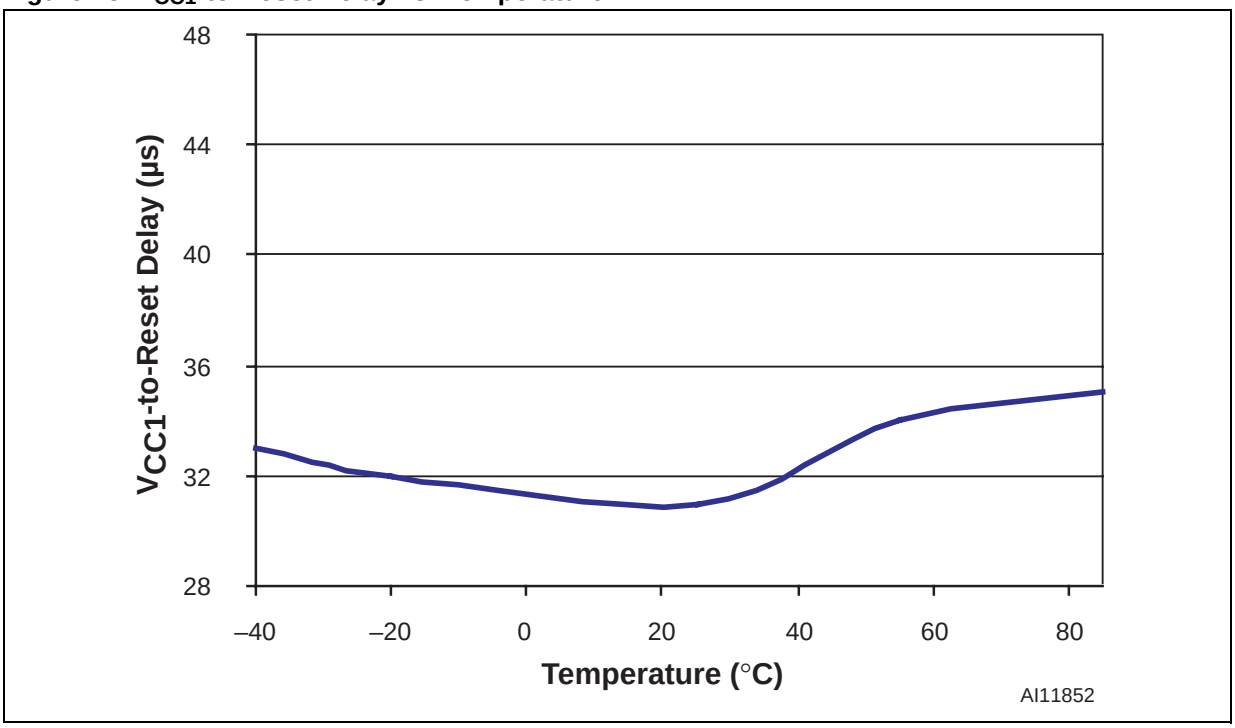


Figure 24. Reset Input-to-Reset Output Delay vs. Temperature

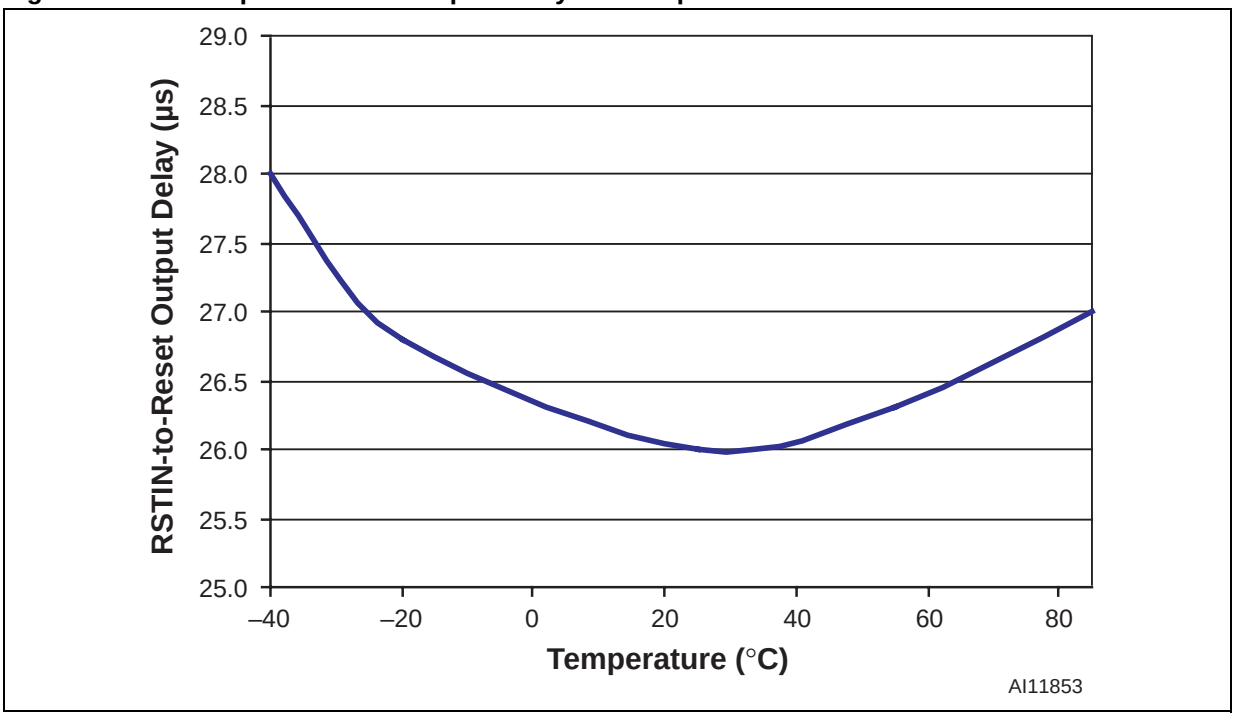
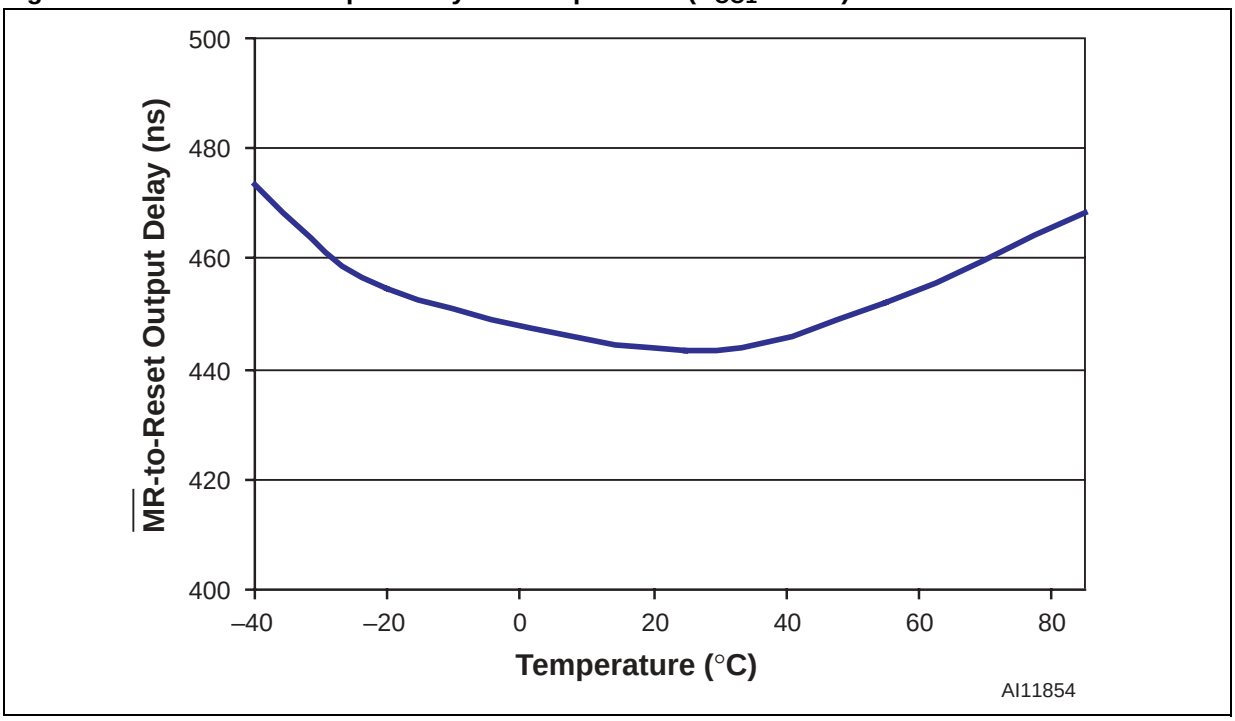


Figure 25. $\overline{MR}$-to-Reset Output Delay vs. Temperature (V_{CC1} = 3.6V)



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off)		–55 to 150	°C
T_{SLD}(1)	Lead Solder Temperature for 10 seconds		260	°C
V_{IO}	Input or Output Voltage		–0.3 to V_{CC1} + 0.3	V
			–0.3 to V_{CC2} + 0.3	V
V_{CC1}, V_{CC2}	Supply Voltage		–0.3 to 7.0	V
I_{IO}	Input or Output Current (all pins)		20	mA
P_D	Power Dissipation	SOT23-5	654	mW
		SOT23-6	675	mW

Note: 1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 5., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC Measurement Conditions

Parameter	STM67xx	Unit
V_{CC} Supply Voltage	0.8 to 5.5	V
Ambient Operating Temperature (T_A)	–40 to 85	°C
Input Rise and Fall Times	≤ 5	ns
Input Pulse Voltages	0.2 to 0.8V_{CC}	V
Input and Output Timing Ref. Voltages	0.3 to 0.7V_{CC}	V

Figure 26. AC Testing Input/Output Waveforms

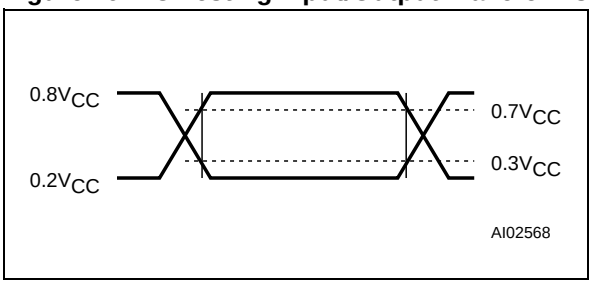


Figure 27. $\overline{MR}$ Timing Waveform (STM6717/18/19/20)

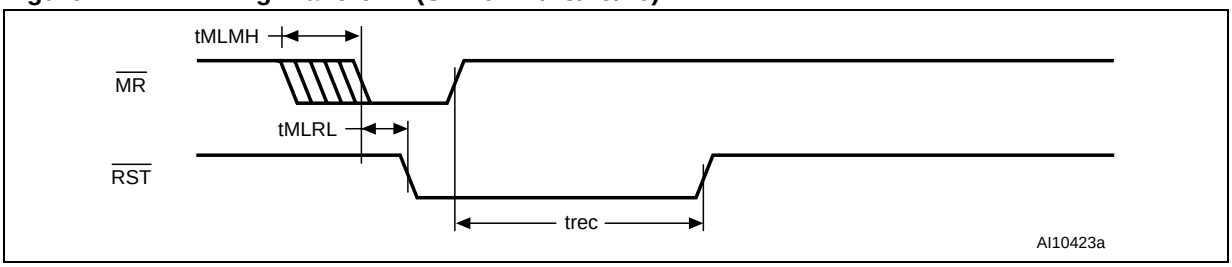
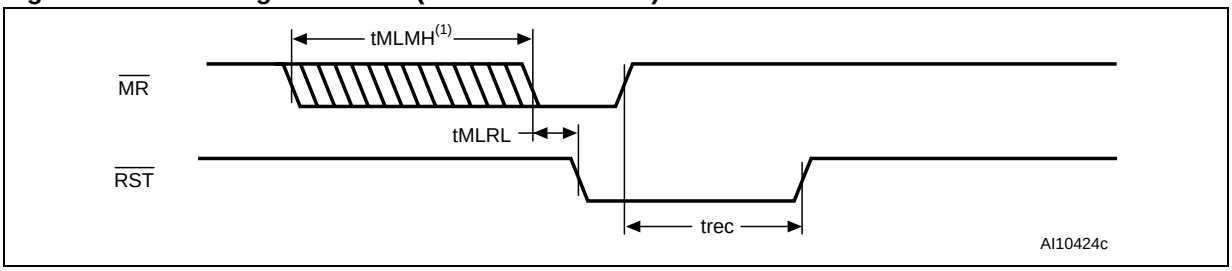


Figure 28. $\overline{MR}$ Timing Waveform (STM6777/78/79/80)



Note: 1. By connecting a certain capacitor between the MRC pin and V_{SS}, the $\overline{RST}$ can be delayed from 6µs or more (t_{MLMH}, see Table 7., page 19).

Table 6. DC and AC Characteristics

Sym	Alter-native	Description	Test Condition(1)	Min	Typ	Max	Unit
V_{CC}		Operating Voltage		0.8		5.5	V
I_{CC1}		V_{CC1} Supply Current	V_{CC1} < 5.5V, all I/O pins open		12	35	µA
			V_{CC1} < 3.6V, all I/O pins open		8	23	µA
I_{CC2}		V_{CC2} Supply Current	V_{CC2} < 3.6V, all I/O pins open		3	9	µA
			V_{CC2} < 2.75V, all I/O pins open		2.5	7	µA
I_{LI}(2)		Input Leakage Current	0V = V_{IN} = V_{CC}	–1		+1	µA
I_{LO}		Open Drain $\overline{RST}$ Output Leakage Current	V_{CC1} > V_{RST1}, V_{CC2} > V_{RST2}; $\overline{RST}$ not asserted			0.5	µA
V_{OL}		Output Low Voltage ($\overline{RST}$; Push-pull or Open Drain)	V_{CC1} or V_{CC2} ≥ 0.8V, I_{SINK} = 1µA, $\overline{RST}$ asserted			0.3	V
			V_{CC1} or V_{CC2} ≥ 1.0V, I_{SINK} = 50µA, $\overline{RST}$ asserted			0.3	V
			V_{CC1} or V_{CC2} ≥ 1.2V, I_{SINK} = 100µA, $\overline{RST}$ asserted			0.3	V
			V_{CC1} or V_{CC2} ≥ 2.7V, I_{SINK} = 1.2mA, $\overline{RST}$ asserted			0.3	V
			V_{CC1} or V_{CC2} ≥ 4.5V, I_{SINK} = 3.2mA, $\overline{RST}$ asserted			0.4	V
V_{OH}		Output High Voltage ($\overline{RST}$; Push-pull only)	V_{CC1} ≥ 1.8V, I_{SOURCE} = 200µA, $\overline{RST}$ not asserted	0.8V_{CC1}			V
			V_{CC1} ≥ 2.7V, I_{SOURCE} = 500µA, $\overline{RST}$ not asserted	0.8V_{CC1}			V
			V_{CC1} ≥ 4.5V, I_{SOURCE} = 800µA, $\overline{RST}$ not asserted	0.8V_{CC1}			V
t_R(3)		Push-pull RST Rise Time (STM6718/20/78/80)	Rise time measured from 10% to 90% of V_{CC}; C_L = 5pF, V_{CC} = 3.3V		5	25	ns
Reset Thresholds							
V_{RST1}(4)	V_{TH1}	V_{CC1} Reset Threshold	L (falling)	4.500	4.625	4.750	V
			M (falling)	4.250	4.375	4.500	V
			T (falling)	3.000	3.075	3.150	V
			S (falling)	2.850	2.925	3.000	V
			R (falling)	2.550	2.625	2.700	V
			Z (falling)	2.250	2.313	2.375	V
			Y (falling)	2.125	2.188	2.250	V
			W (falling)	1.620	1.665	1.710	V
			V (falling)	1.530	1.575	1.620	V

Sym	Alter-native	Description	Test Condition(1)	Min	Typ	Max	Unit
V_{RST2}(4)	V_{TH2}	V_{CC2} Reset Threshold	T (falling)	3.000	3.075	3.150	V
			S (falling)	2.850	2.925	3.000	V
			R (falling)	2.550	2.625	2.700	V
			Z (falling)	2.250	2.313	2.375	V
			Y (falling)	2.125	2.188	2.250	V
			W (falling)	1.620	1.665	1.710	V
			V (falling)	1.530	1.575	1.620	V
			I (falling)	1.350	1.388	1.425	V
			H (falling)	1.275	1.313	1.350	V
			G (falling)	1.080	1.110	1.140	V
			F (falling)	1.020	1.050	1.080	V
			K (falling)	0.895	0.925	0.955	V
			J (falling)	0.845	0.875	0.905	V
			E (falling)	0.810	0.833	0.855	V
			D (falling)	0.765	0.788	0.810	V
V_{HYST}		Reset Threshold Hysteresis	Referenced to V_{RST} typical		0.5		%
t_{RD}		V_{CC} to $\overline{RST}$ Delay	V_{CC1} = (V_{RST1} + 100mV) to (V_{RST} – 100mV)		20		µs
			V_{CC2} = (V_{RST2} + 75mV) to (V_{RST2} – 75mV)		20		µs
t_{rec}	t_{RP}	$\overline{RST}$ Time-out Period		140	210	280	ms
Adjustable Reset Comparator Input (STM6719/20/79/80)							
V_{RSTIN}		RSTIN Input Threshold		611	626.5	642	mV
I_{RSTIN}		RSTIN Input Current		–25		+25	nA
		RSTIN Hysteresis			3		mV
t_{RSTIND}		RSTIN to $\overline{RST}$ Output Delay	V_{RSTIN} to (V_{RSTIN} – 30mV)		22		µs

Sym	Alter-native	Description	Test Condition(1)	Min	Typ	Max	Unit
Manual (Push-button) Reset Input							
V_{IL}		$\overline{MR}$ Input Voltage				$0.3V_{CC1}$	V
V_{IH}				$0.7V_{CC1}$			V
t_{MLMH}	t_{MR}	$\overline{MR}$ Minimum Pulse Width (STM6717/18/19/20)		1			µs
		$\overline{MR}$ Minimum Pulse Width (STM6777/78/79/80)	MRC connected via capacitor to V_{SS}(5)		6		µs
t_{MLRL}	t_{MRD}	$\overline{MR}$ to $\overline{RST}$ Output Delay			200		ns
		$\overline{MR}$ Glitch Immunity (STM6717/18/19/20)			100		ns
		$\overline{MR}$ Pull-up Resistance		25	50	80	kΩ

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC1} = 0.8 to 5.5V and V_{CC2} = 0.8 to 3.6V (except where noted).
2. Input leakage for the MRC pin is not tested.
3. Guaranteed by design.
4. The leakage current measured on the $\overline{RST}$ pin is tested with the reset de-asserted (output high impedance).
5. Selecting the appropriate external capacitor (preferably less than 100pF) allows systems designers to vary the minimum delay from 6µs (MRC pin left open) or more (see Table 7.).

Table 7. t_{MLMH} Minimum Pulse Width

V_{CC1}	Capacitor Value(1)					
	100pF	**0.1µF**	**2.2µF**	**3.3µF**	**4.7µF**	**6.8µF**
1.6V	120µs	120ms	2.6s	4.0s	5.6s	8.2s
2.0V	122µs	122ms	2.7s	4.0s	5.8s	8.3s
3.0V	125µs	125ms	2.7s	4.1s	5.9s	8.5s
4.0V	128µs	129ms	2.8s	4.2s	6.0s	8.7s
5.0V	130µs	130ms	2.8s	4.3s	6.1s	8.8s

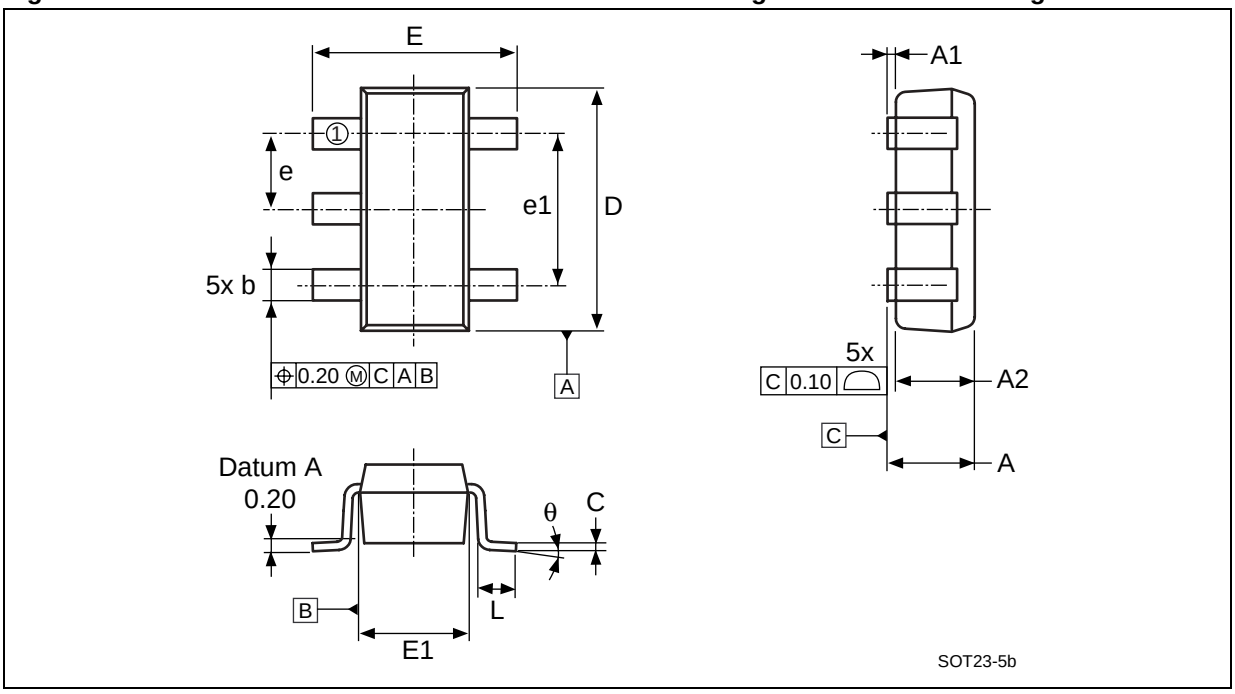
Note: 1. At 25°C (typical)

PACKAGE MECHANICAL

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 29. SOT23-5 – 5-lead Small Outline Transistor Package Mechanical Drawing



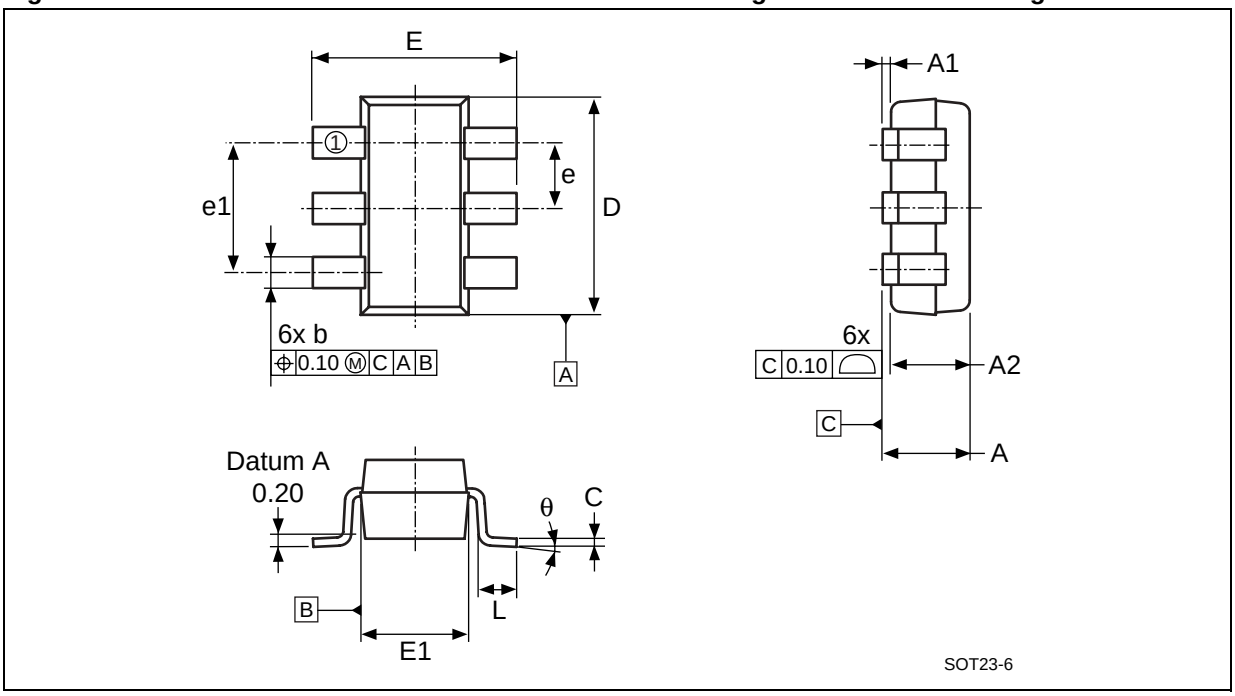
Note: Drawing is not to scale.

Table 8. SOT23-5 – 5-lead Small Outline Transistor Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.45	–	–	0.057
A1	–	–	0.15	–	–	0.006
A2	1.15	0.90	1.30	0.045	0.035	0.051
b	–	0.30	0.50	–	0.012	0.020
C	–	0.08	0.22	–	0.003	0.009
D	2.90	–	–	0.114	–	–
E	2.80	–	–	0.110	–	–
E1	1.60	–	–	0.063	–	–
e	0.95	–	–	0.037	–	–
e1	1.90	–	–	0.075	–	–
L	0.45	0.30	0.60	0.018	0.012	0.024
Θ	4°	0°	8°	4°	0°	8°
N	5			5		

Note: Dimensions per JEDEC SOT/SOP Product Outline MO-178C, variation AA

Figure 30. SOT23-6 – 6-lead Small Outline Transistor Package Mechanical Drawing



Note: Drawing is not to scale.

Table 9. SOT23-6 – 6-lead Small Outline Transistor Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.45	–	–	0.057
A1	–	–	0.15	–	–	0.006
A2	1.15	0.90	1.30	0.045	0.035	0.051
b	–	0.30	0.50	–	0.012	0.020
C	–	0.08	0.22	–	0.003	0.009
D	2.90	–	–	0.114	–	–
E	2.80	–	–	0.110	–	–
E1	1.60	–	–	0.063	–	–
e	0.95	–	–	0.037	–	–
e1	1.90	–	–	0.075	–	–
L	0.45	0.30	0.60	0.018	0.012	0.024
Θ	4°	0°	8°	4°	0°	8°
N	6			6		

Note: Dimensions per JEDEC SOT/SOP Product Outline MO-178C, variation AA

PART NUMBERING

Table 10. Ordering Information Scheme

Example: STM67xx LT WY 6 E

Device Type
STM67xx

Reset Thresholds (V_{RST1} and V_{RST2}) for V_{CC1} and V_{CC2}

STM6717/18/19/20/77/78 (V_{RST1} and V_{RST2})

Suffix	V_{RST1}	V_{RST2}
LT	4.625	3.075
MS	4.375	2.925
MR	4.375	2.625
TZ(1)	3.075	2.313
TW(1)	3.075	1.665
TI	3.075	1.388
TG(1)	3.075	1.110
TK	3.075	0.925
TE	3.075	0.833
SY(1)	2.925	2.188
SV(1)	2.925	1.575
SH	2.925	1.313
SF(1)	2.925	1.050
SJ	2.925	0.875
SD	2.925	0.788
YV	2.188	1.575
YH	2.188	1.313
YF	2.188	1.050
YJ	2.188	0.875
YD	2.188	0.788
VH	1.575	1.313
VF	1.575	1.050
VJ	1.575	0.875
VD	1.575	0.788

STM6779/80 (V_{RST1} only)

L–	4.625	–
T–	3.075	–
S–	2.925	–
Y–	2.188	–
V–	1.575	–
R–	2.625	–
Z–	2.313	–

Package
WY = SOT23-5
WB = SOT23-6

Temperature Range
6 = –40 to 85°C

Shipping Method
E = ECOPACK Package, Tubes
F = ECOPACK Package, Tape & Reel

Note: 1. These are standard versions and are typically held in stock. A non-standard version may require a higher minimum volumes, and/or longer delivery times. For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

REVISION HISTORY

Table 11. Document Revision History

Date	Version	Revision Details
18-October-04	1.0	First Draft
25-Oct-04	1.1	Descriptive text, sales types (Table 10)
14-Jan-05	1.2	Update characteristics, pin functions (Table 3)
09-Feb-05	1.3	Update characteristics (Figure 10; Table 3)
08-Apr-05	1.4	Update characteristics and mechanical dimensions; add table (Figure 10, 11, 28, 29, 30; Table 4, 6, 10, 8, 9)
28-Jul-05	1.5	Updated characteristics, reset delay (Figure 11, 28; Table 4, 6, 7, 10)
13-Sep-05	2.0	Add operating characteristics; update timings, document status, Lead-free text (Figure 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27, 28; Table 10)