

SN54BCT540, SN74BCT540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS012D – JULY 1988 – REVISED SEPTEMBER 1994

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State Outputs Drive Bus Lines or Buffer Memory-Address Registers
- P-N-P Inputs Reduce DC Loading
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK) and Flatpacs (W), and Plastic (N) and Ceramic (J) 300-mil DIPs

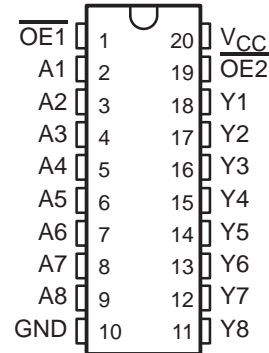
description

The SN54BCT540 and SN74BCT540A octal buffers and line drivers are ideal for driving bus lines or buffer memory-address registers. The devices feature inputs and outputs on opposite sides of the package that facilitate printed-circuit-board layout.

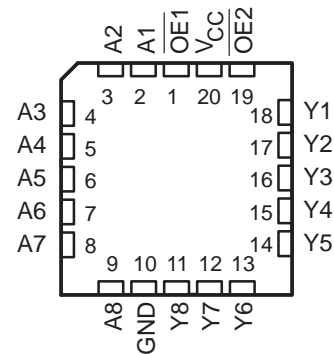
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

The SN54BCT540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT540A is characterized for operation from 0°C to 70°C .

SN54BCT540 . . . J OR W PACKAGE
SN74BCT540A . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT540 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

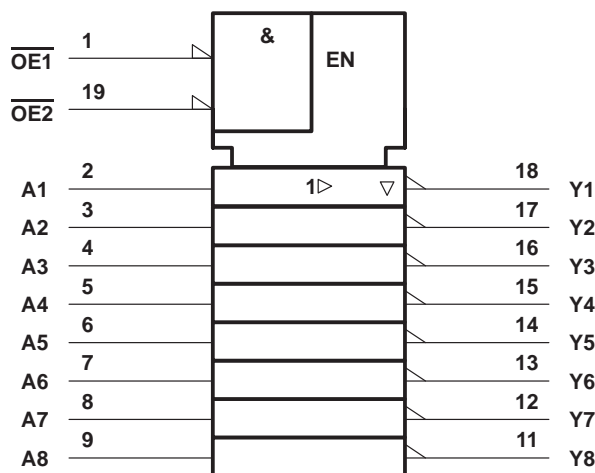
SN54BCT540, SN74BCT540A

OCTAL BUFFERS/DRIVERS

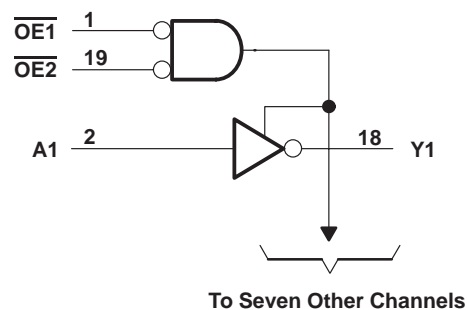
WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	- 0.5 V to 7 V
Input voltage range, V_I (see Note 1)	- 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O	- 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_{OH}	- 0.5 V to V_{CC}
Current into any output in the low state: SN54BCT540	96 mA
SN74BCT540A	128 mA
Operating free-air temperature range, T_A : SN54BCT540	- 55°C to 125°C
SN74BCT540A	0°C to 70°C
Storage temperature range	- 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

	SN54BCT540			SN74BCT540A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{IK} Input clamp current			-18			-18	mA
I_{OH} High-level output current			-12			-15	mA
I_{OL} Low-level output current			48			64	mA
T_A Operating free-air temperature	-55		125	0		70	°C

SN54BCT540, SN74BCT540A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT540			SN74BCT540A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 V$,	$I_I = -18 mA$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 V$	$I_{OH} = -3 mA$	2.4	3.3		2.4	3.3		V
		$I_{OH} = -12 mA$	2	3.2					
		$I_{OH} = -15 mA$				2	3.1		
V_{OL}	$V_{CC} = 4.5 V$	$I_{OL} = 48 mA$		0.38	0.55				V
		$I_{OL} = 64 mA$				0.42	0.55		
I_I	$V_{CC} = 5.5 V$,	$V_I = 7 V$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 V$,	$V_I = 2.7 V$			20			20	μA
I_{IL}	$V_{CC} = 5.5 V$,	$V_I = 0.5 V$			-0.6			-0.6	mA
I_{OZH}	$V_{CC} = 5.5 V$,	$V_O = 2.7 V$			50			50	μA
I_{OZL}	$V_{CC} = 5.5 V$,	$V_O = 0.5 V$			-50			-50	μA
$I_{OS}‡$	$V_{CC} = 5.5 V$,	$V_O = 0$	-100		-225	-100		-225	mA
I_{CCH}	$V_{CC} = 5.5 V$			20	30		20	30	mA
I_{CCL}	$V_{CC} = 5.5 V$			45	71		45	71	mA
I_{CCZ}	$V_{CC} = 5.5 V$			3	6		3	6	mA
C_i	$V_{CC} = 5 V$,	$V_I = 2.5 V$ or $0.5 V$		6			5		pF
C_o	$V_{CC} = 5 V$,	$V_O = 2.5 V$ or $0.5 V$		10			10		pF

† All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Figure 1)

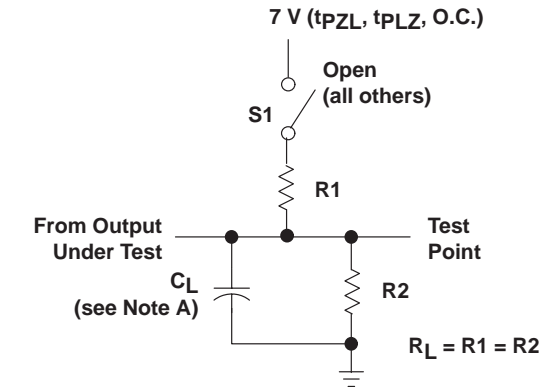
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5 V$, $C_L = 50 pF$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = 25^\circ C$			$V_{CC} = 4.5 V$ to $5.5 V$, $C_L = 50 pF$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = MIN$ to MAX §				UNIT
			'BCT540			SN54BCT540		SN74BCT540A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.5	4.1	5.8	1.9	7.2	2	6.9	ns
t_{PHL}			0.6	1.9	3.5	0.3	4.5	0.3	4	
t_{PZH}	\overline{OE}	Y	4	6.8	8.9	4.1	10.4	3.3	10.1	ns
t_{PZL}			5	8	10	5.3	11.8	4.3	11.3	
t_{PHZ}	OE	Y	3.5	5.7	7.8	2.7	9.4	2.7	9	ns
t_{PLZ}			3.8	5.5	7.4	3.5	8.9	3.5	8.5	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

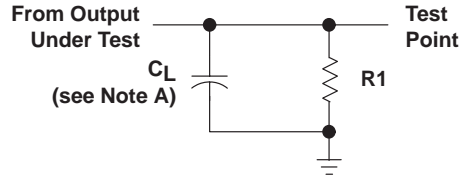
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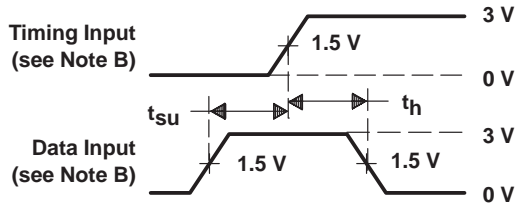
PARAMETER MEASUREMENT INFORMATION



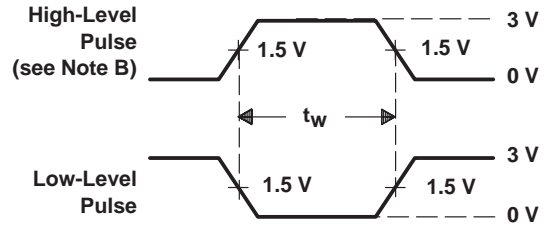
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



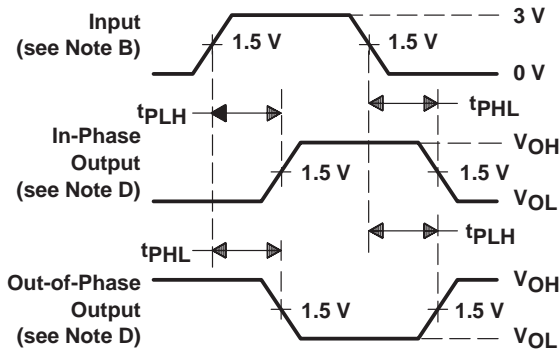
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



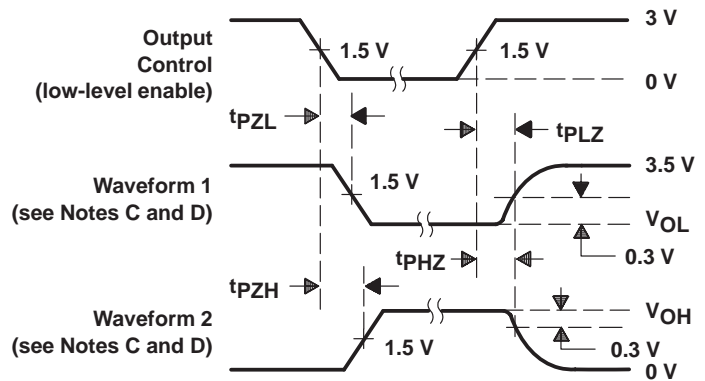
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuits and Voltage Waveforms

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