

SN54HC646, SN74HC646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCLS150B – DECEMBER 1982 – REVISED MAY 1997

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- High-Current 3-State Outputs Can Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (DW) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

The 'HC646 consist of bus-transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'HC646.

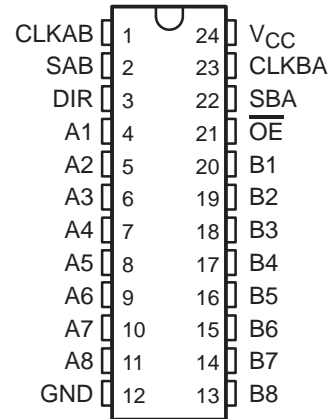
Output-enable (\overline{OE}) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either or both registers.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. DIR determines which bus receives data when \overline{OE} is active (low). In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

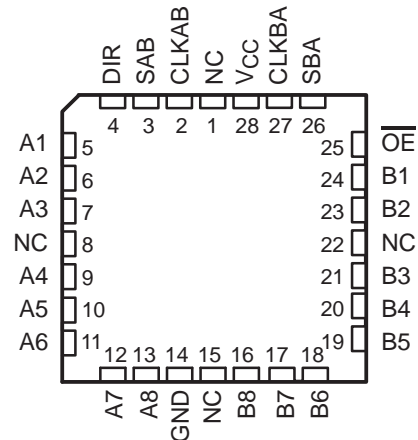
When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54HC646 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC646 is characterized for operation from -40°C to 85°C .

SN54HC646 . . . JT OR W PACKAGE
SN74HC646 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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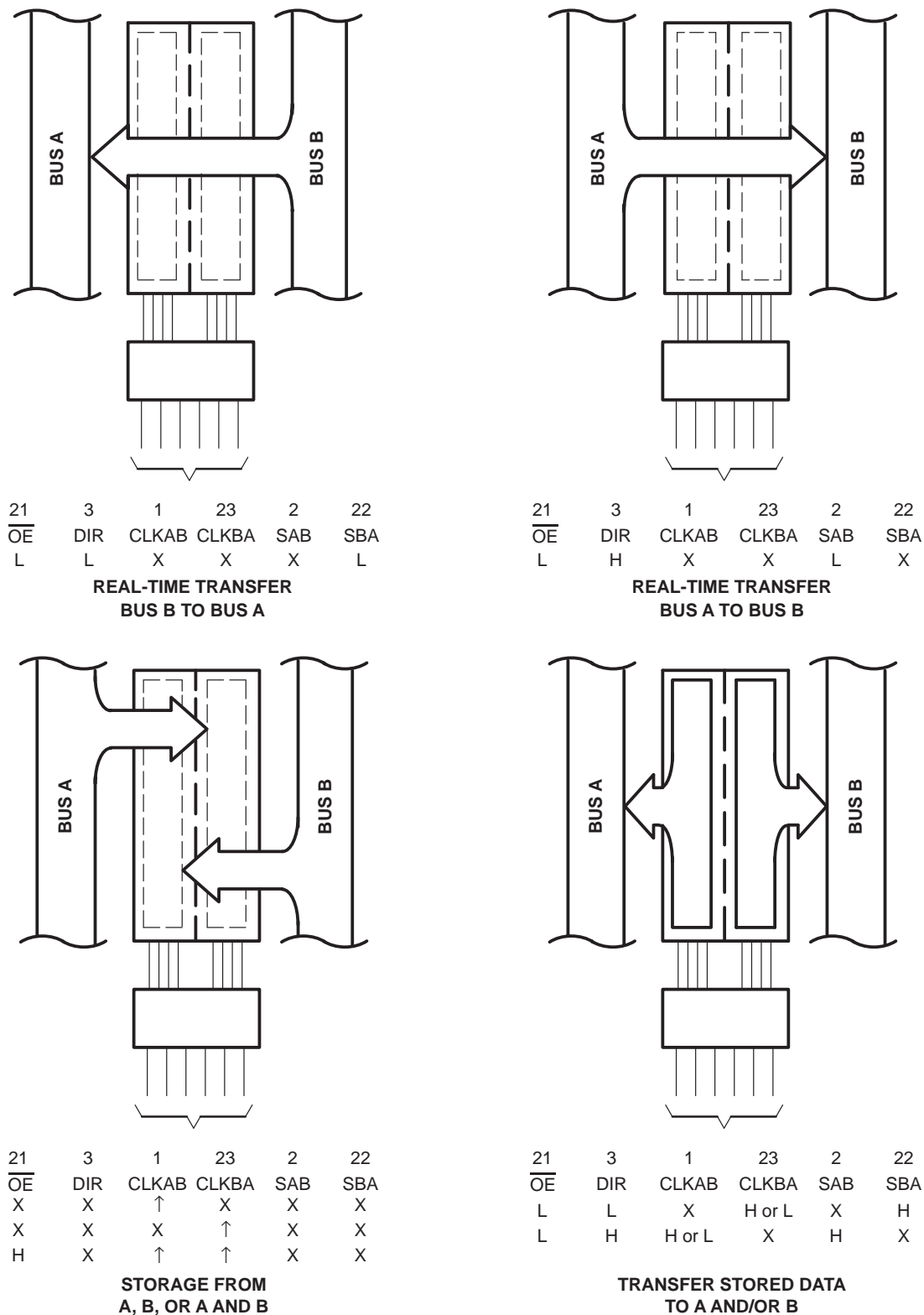
 **TEXAS
INSTRUMENTS**

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SN54HC646, SN74HC646 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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Pin numbers shown are for the DW, JT, NT, and W packages.

Figure 1. Bus-Management Functions

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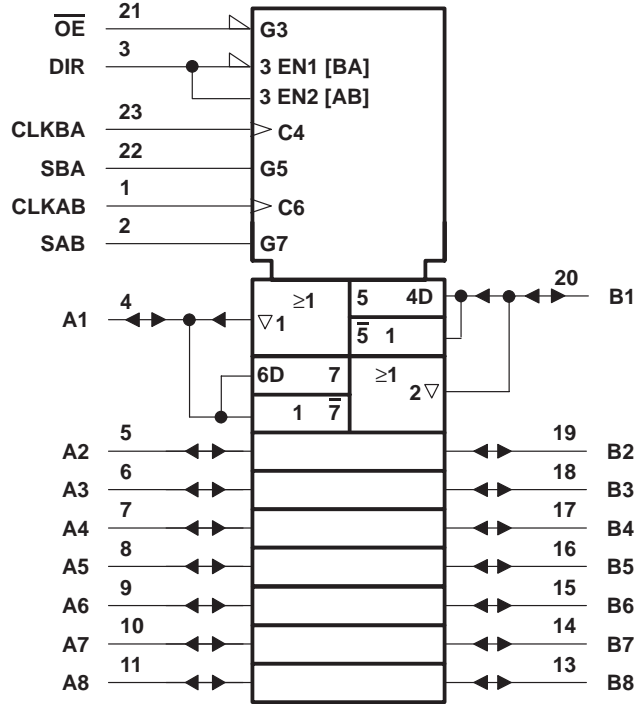
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FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|--------|-----|--------|--------|-----|-----|----------------|----------------|---------------------------|
| OE | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

† The data-output functions can be enabled or disabled by various signals at OE and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

logic symbol‡

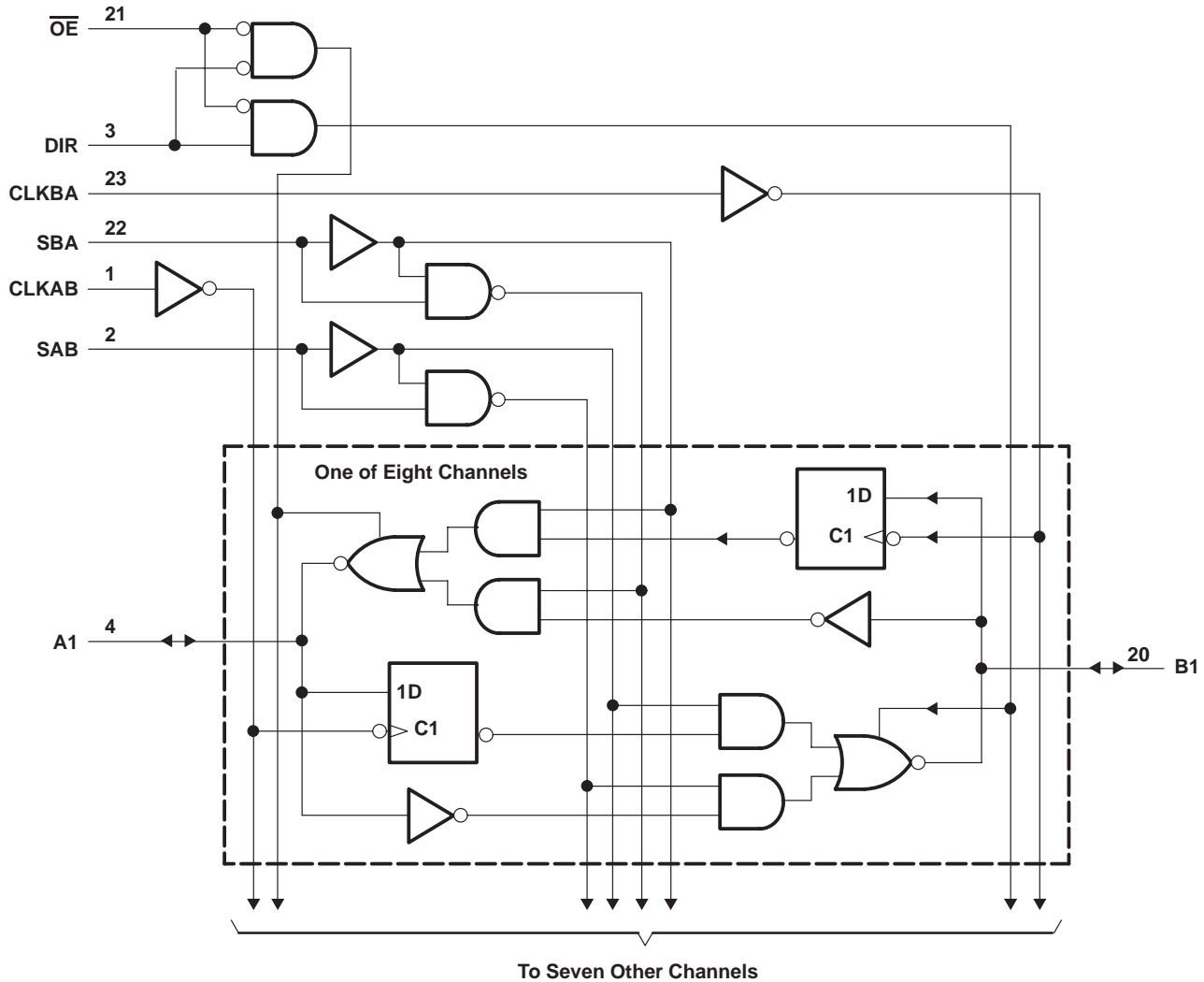


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, NT, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 35 mA |
| Continuous current through V_{CC} or GND | ± 70 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DW package | 81°C/W |
| NT package | 67°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



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recommended operating conditions

| | | SN54HC646 | | | SN74HC646 | | | UNIT |
|-----------------|---------------------------------------|-------------------------|-----|-----------------|-----------|-----|-----------------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | 1.5 | | V | |
| | | V _{CC} = 4.5 V | | 3.15 | 3.15 | | | |
| | | V _{CC} = 6 V | | 4.2 | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0 | 0.5 | 0 | 0.5 | V |
| | | V _{CC} = 4.5 V | | 0 | 1.35 | 0 | 1.35 | |
| | | V _{CC} = 6 V | | 0 | 1.8 | 0 | 1.8 | |
| V _I | Input voltage | 0 | | V _{CC} | 0 | | V _{CC} | V |
| V _O | Output voltage | 0 | | V _{CC} | 0 | | V _{CC} | V |
| t _t | Input transition (rise and fall) time | V _{CC} = 2 V | | 0 | 1000 | 0 | 1000 | ns |
| | | V _{CC} = 4.5 V | | 0 | 500 | 0 | 500 | |
| | | V _{CC} = 6 V | | 0 | 400 | 0 | 400 | |
| T _A | Operating free-air temperature | -55 | | 125 | -40 | | 85 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC646 | | SN74HC646 | | UNIT | |
|-----------------|-----------------|---|--------------------------|-----------------------|-------|-------|-----------|-------|-----------|-------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| V _{OH} | | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | | I _{OH} = -6 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | | | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | V | |
| | | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | | 0.1 |
| | | | | 6 V | | 0.001 | 0.1 | | 0.1 | | | 0.1 |
| | | | I _{OL} = 6 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | | 0.33 |
| | | | | 6 V | | 0.15 | 0.26 | | 0.4 | | | 0.33 |
| I _I | Control inputs | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA | |
| I _{OZ} | A or B | V _O = V _{CC} or 0 | 6 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA | |
| I _{CC} | | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 8 | | 160 | | 80 | μA | |
| C _i | Control inputs | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF | |

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | V _{CC} | T _A = 25°C | | SN54HC646 | | SN74HC646 | | UNIT |
|--|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} Clock frequency | 2 V | 0 | 6 | 0 | 4.3 | 0 | 5.5 | MHz |
| | 4.5 V | 0 | 31 | 0 | 22 | 0 | 27 | |
| | 6 V | 0 | 36 | 0 | 25 | 0 | 31 | |
| t _w Pulse duration, CLKBA or CLKAB high or low | 2 V | 80 | | 115 | | 95 | | ns |
| | 4.5 V | 16 | | 23 | | 19 | | |
| | 6 V | 14 | | 20 | | 16 | | |
| t _{su} Setup time, A before CLKAB↑ or B before CLKBA↑ | 2 V | 100 | | 150 | | 125 | | ns |
| | 4.5 V | 20 | | 30 | | 25 | | |
| | 6 V | 17 | | 26 | | 21 | | |
| t _h Hold time, A after CLKAB↑ or B after CLKBA↑ | 2 V | 5 | | 5 | | 5 | | ns |
| | 4.5 V | 5 | | 5 | | 5 | | |
| | 6 V | 5 | | 5 | | 5 | | |

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HC646 | | SN74HC646 | | UNIT |
|------------------|-----------------|-------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 2 V | 6 | 11 | | 4.4 | | 5.5 | MHz | |
| | | | 4.5 V | 31 | 54 | | 22 | | 27 | | |
| | | | 6 V | 36 | 64 | | 25 | | 31 | | |
| t _{pd} | CLKBA or CLKAB | A or B | 2 V | | 65 | 180 | | 270 | | 225 | ns |
| | | | 4.5 V | | 18 | 36 | | 54 | | 45 | |
| | | | 6 V | | 14 | 31 | | 46 | | 38 | |
| | A or B | B or A | 2 V | | 50 | 135 | | 205 | | 170 | |
| | | | 4.5 V | | 14 | 27 | | 41 | | 34 | |
| | | | 6 V | | 11 | 23 | | 35 | | 29 | |
| | SBA or SAB† | A or B | 2 V | | 70 | 190 | | 285 | | 240 | |
| | | | 4.5 V | | 20 | 38 | | 57 | | 48 | |
| | | | 6 V | | 16 | 32 | | 48 | | 41 | |
| t _{en} | \overline{OE} | A or B | 2 V | | 85 | 245 | | 370 | | 305 | ns |
| | | | 4.5 V | | 25 | 49 | | 74 | | 61 | |
| | | | 6 V | | 20 | 42 | | 63 | | 52 | |
| t _{dis} | \overline{OE} | A or B | 2 V | | 85 | 245 | | 370 | | 305 | ns |
| | | | 4.5 V | | 25 | 49 | | 74 | | 61 | |
| | | | 6 V | | 20 | 42 | | 63 | | 52 | |
| t _{en} | DIR | A or B | 2 V | | 80 | 245 | | 370 | | 305 | ns |
| | | | 4.5 V | | 25 | 49 | | 74 | | 61 | |
| | | | 6 V | | 20 | 42 | | 63 | | 52 | |
| t _{dis} | DIR | A or B | 2 V | | 80 | 245 | | 370 | | 305 | ns |
| | | | 4.5 V | | 25 | 49 | | 74 | | 61 | |
| | | | 6 V | | 20 | 42 | | 63 | | 52 | |
| t _t | | Any | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | 6 V | | 6 | 10 | | 15 | | 13 | |

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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switching characteristics over recommended operating free-air temperature range, $C_L = 150 \text{ pF}$
(unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC646 | | SN74HC646 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | CLKBA or CLKAB | A or B | 2 V | 90 | 265 | 400 | 330 | ns | | | |
| | | | 4.5 V | 24 | 53 | 80 | 66 | | | | |
| | | | 6 V | 20 | 46 | 68 | 57 | | | | |
| | A or B | B or A | 2 V | 70 | 220 | 335 | 280 | | | | |
| | | | 4.5 V | 20 | 44 | 67 | 56 | | | | |
| | | | 6 V | 15 | 38 | 57 | 49 | | | | |
| | SBA or SAB† | A or B | 2 V | 80 | 275 | 415 | 345 | | | | |
| | | | 4.5 V | 24 | 55 | 83 | 69 | | | | |
| | | | 6 V | 20 | 47 | 70 | 60 | | | | |
| t_{en} | \overline{OE} | A or B | 2 V | 113 | 330 | 500 | 410 | ns | | | |
| | | | 4.5 V | 33 | 66 | 100 | 82 | | | | |
| | | | 6 V | 27 | 57 | 85 | 71 | | | | |
| | DIR | A or B | 2 V | 113 | 330 | 500 | 410 | | | | |
| | | | 4.5 V | 33 | 66 | 100 | 82 | | | | |
| | | | 6 V | 27 | 57 | 85 | 71 | | | | |
| t_t | | Any | 2 V | 45 | 210 | 315 | 265 | ns | | | |
| | | | 4.5 V | 17 | 42 | 63 | 53 | | | | |
| | | | 6 V | 13 | 36 | 53 | 43 | | | | |

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics, $T_A = 25^\circ\text{C}$

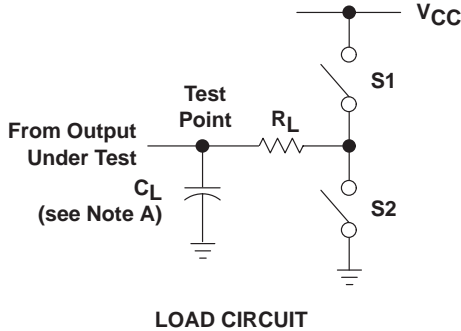
| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C_{pd} Power dissipation capacitance | No load | 50 | pF |

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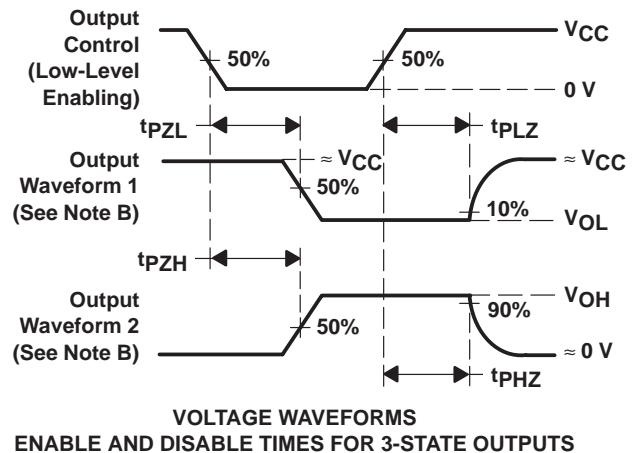
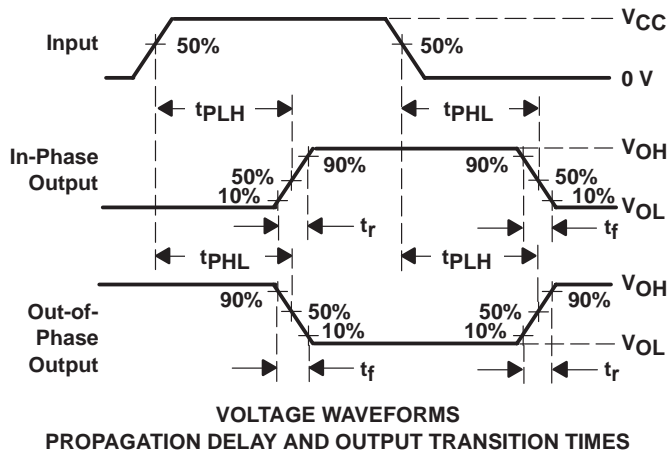
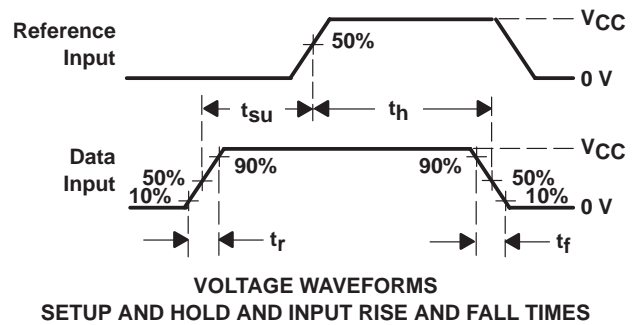
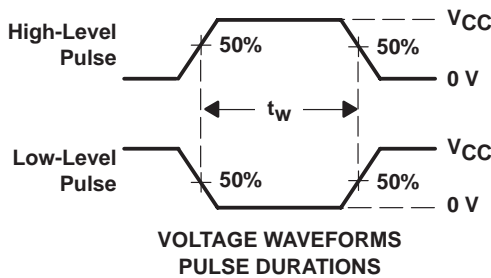


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PARAMETER MEASUREMENT INFORMATION



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | — | 50 pF or 150 pF | Open | Open |



- NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
G. t_{PZL} and t_{PZH} are the same as t_{en} .
H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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